Reduction of Die-Bonding Interface Thermal Resistance for High-Power LEDs Through Embedding Packaging Structure

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***Abstract*—Thermal management is a key issue for high-power light-emitting diodes (LEDs). In this study, a novel packaging structure was proposed to reduce the die-bonding interface thermal resistance and provided a new idea for LED heat-dissipation. The LED chip was embedded into a square groove at the lead-frame substrate. The gap between the edges of the LED chip and square groove was filled with boron nitride/silicone composite. So the heat generated from the chip could be dissipated from the side surfaces to the substrate. The experimental results show that the heat-dissipation ability of LEDs has been significantly improved by the new embedding packaging structure. The die-bonding interface thermal resistance can be reduced by more than 20%. The junction temperature rise can be reduced by 14%. Due to the fully embedding of LED chip in the square groove, the light intensity distribution is slightly shrunk and the light output power is slightly reduced by about 8%.**

***Index Terms*—Boron nitride (BN)/silicone, die-bonding interface, embedding packaging structure, light-emitting diodes (LEDs), thermal resistance.**

I. Introduction

Due to advantages over traditional light sources, such as high luminous efficiency, long life, high reliability and energy saving, high-power light-emitting diodes (LEDs) have been widely applied into our daily lives [1]–[3]. To achieve better light output performance and reduce cost, the power density of LED chip is developing to be higher [4], [5]. Then, the heat generated by the chip is greater that results in higher chip junction temperature, and it further causes lower luminous efficiency, poorer reliability, emission wavelength shifts, and shorter life time [6]–[8]. Therefore, the thermal management is a key issue for high-power LEDs.

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The current thermal management researches focus on reducing three parts of thermal resistances. First, outside cooling strategies are proposed to reduce the thermal resistance from device to atmosphere, such as the use of heat pipes [9], microchannel coolers [10], synthetic jets [11], microjet arrays [12], piezoelectric fans [13], thermoelectric cooling systems [14], and electrohydrodynamic solutions [15]. Second, some solutions are proposed to reduce the thermal resistance of packaging structure, mainly including new substrate materials and structures, such as metal core printed circuit board (MCPCB) [16], low temperature co-fired ceramic substrate [17], direct bonded copper substrate [18], direct plated ceramic substrate [19], silicon substrate [20], and metal matrix composite substrate [21]. Third, many researches focus on reducing die-bonding interface thermal resistance. Generally, the LED chip is attached onto the substrate by die-bonding material, mostly silver paste and most heat is dissipated through the die-bonding layer [22]. The die-bonding layer directly attaches the heat source, so the thermal resistance of die-bonding interface is becoming a more and more important research hotspot. The die-bonding interface thermal resistance is decomposed into one component representing the bulk thermal resistance and another component representing contact thermal resistance [4]. Many die-bonding materials, such as silver paste [23], carbon nanotube-embedded silver-paste [24], SAC305 solder [25], and Au/Sn-eutectic [26] have been studied. But due to the roughened lead-frame substrate, the contact between the substrate and die-bonding material is hard to be perfect [27]. Actually, there are many voids existing on the interface between the die-bonding layer and substrate [28]. Hence, the die-bonding interface thermal resistance is not reduced efficiently. More efficient approaches are still urgently in demand.

In this study, a new embedding packaging structure was proposed to reduce the die-bonding interface thermal resistance. Part of the heat generated from the chip could be dissipated from the side surfaces of LED chip to the substrate. The thermal and optical performance comparisons between the traditional packaging structure and proposed embedding packaging structure are conducted by experiment.

II. Principle

A new embedding packaging structure is proposed here to reduce the die-bonding interface thermal resistance. The LED chip is embedded into a square groove at the lead-frame substrate

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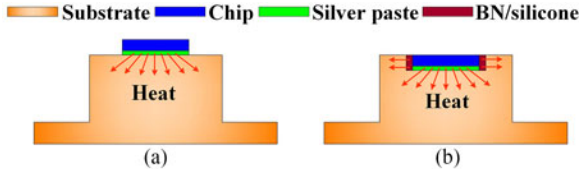

Fig. 1. Schematics of (a) traditional structure and (b) proposed embedding structure.

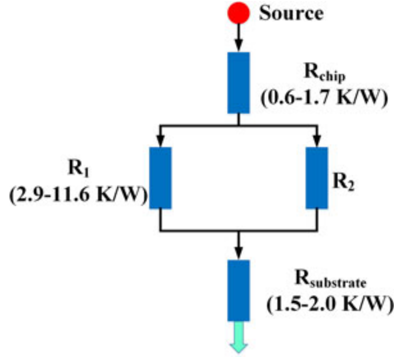

Fig. 2. Schematic of the thermal resistance model of proposed embedding structure.

and attached onto the substrate by silver paste. The gap between the edges of the LED chip and square groove is filled with boron nitride (BN)/silicone composite. The comparison between the traditional structure and proposed embedding structure is shown schematically in Fig. 1.

According to heat transfer theory, compared to traditional structure, the proposed structure provides one more heat transfer path through the BN/silicone composite to the substrate. This path is in parallel with the heat transfer path through silver paste. The thermal resistance model of the proposed structure can be simply schematized in Fig. 2. The common thermal resistance ranges of different materials in the thermal resistance model are presented in this figure.

According to the heat transfer theory [29], the following equation is established:

$$\frac{1}{R_p} = \frac{1}{R_1} + \frac{1}{R_2} \tag{1}$$

where R_p is the die-bonding thermal resistance of proposed structure, R_1 is the thermal resistance of silver paste, and R_2 is the thermal resistance of BN/silicone composite.

After calculating, the die-bonding thermal resistance of proposed structure is given as follows:

$$R_p = \frac{R_1 \cdot R_2}{R_1 + R_2} = \frac{R_1}{1 + \frac{R_1}{R_2}}. \tag{2}$$

The die-bonding thermal resistance of traditional structure is that of the silver paste, and it is shown as follows:

$$R_t = R_1. \tag{3}$$

So the thermal resistance of proposed structure is smaller than that of traditional structure. The heat-dissipation ability will be improved by the embedding packaging structure.

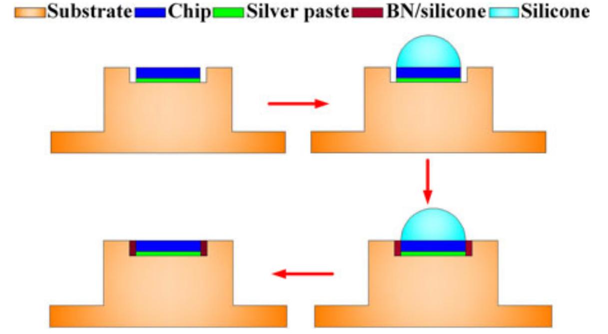

Fig. 3. Schematics of the fabricating processes of proposed embedding packaging structure.

From (2), it is obvious that when R_1 is constant, R_p will decrease with R_2 decreasing. So the thermal resistance of BN/silicone composite should be as smaller as possible. Similarly, R_p will be smaller for lower values of R_1; hence, lower resistance material should be selected as initial die bonding interface material.

Equation (2) can be changed to another form, as following:

$$\frac{R_p}{R_t} = \frac{1}{1 + \frac{R_1}{R_2}}. \tag{4}$$

From (4), it can be seen that when R_2 is constant, the ratio of R_p to R_t will be smaller with R_1 increasing. So the reductive percentage of the die-bonding thermal resistance by the proposed embedding structure is larger with R_1 increasing. The thermal enhancement effect of the proposed structure is more significant.

III. Experiments

LED devices with the traditional packaging structure and proposed embedding structure were fabricated to make a comparison. For the traditional structure, the LED chip was attached onto the Cu slug substrate by silver paste and the silver paste was cured at 120 °C for 30 min. The thermal conductivity value of silver paste is about 7.5 W/ mK. Then, the electrical connection between the chip and electrodes was completed by wire bonding. Finally, the LED package was attached onto a hexagonal MCPCB by heat-conducting silicone grease. For the proposed embedding packaging structure, the fabricating processes were relatively complicated and shown in Fig. 3.

First, at the center of the Cu substrate, a square groove was fabricated by precision machining. The LED chip was attached at the center of the square groove by silver paste and the silver paste was also cured at 120 °C for 30 min. Second, silicone was dispensed on the top surface of the LED chip to cover all the top surface area and the silicone was cured. Third, milled BN powder was filled into the gap between the edges of the LED chip and square groove. Then, the silicone of very small volume dipped by microprobe was dispensed to the gap filled with BN. It would fill the voids between BN particles by capillary action. Subsequently, the silicone was cured at 120 °C for 40 min. Fourth, the cured silicone on the top surface of LED chip was removed. The temporary silicone layer on top of the LED chip was added to avoid that there are residual BN particles

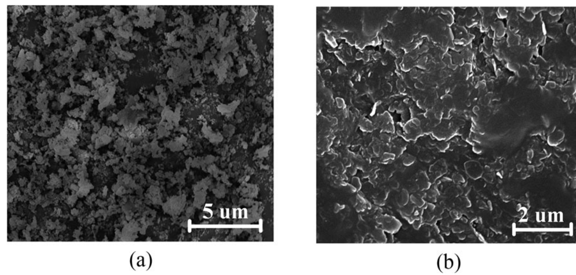

Fig. 4. SEM images of (a) milled BN powder and (b) BN/silicone composite.

or silicone on the LED top surface, which will affect the light output performance of LED chip. Finally, after the electrical connection between the chip and electrodes completed by wire bonding, the LED package was attached onto a hexagonal MCPCB by heat-conducting silicone grease.

The morphologies of BN powder and BN/silicone composite were studied using scanning electron microscope (SEM) (Nova NanoSEM 450, FEI, the Netherlands). The cross sections of samples were observed by digital microscope (VHX-600, KEYENCE, Japan). Different thermal resistance contributions were evaluated by using the thermal transient tester (T3Ster-Master, Mentor Graphics, USA). Light intensity distribution (LID) was obtained by LID curve tester (GO1900L, Everfine, China). The light output power (LOP) was measured by integrating sphere (HAAS-2000, Everfine, China).

The time of test system delay was set as 1 μs. Based on the thermal *R–C* network and structure function, the thermal resistance and thermal capacitance can be measured precisely. The measurement was made as follows. The first step was to obtain the *K* factor, which defines the relationship between junction temperature change and temperature sensitive parameter of forward voltage drop. The optical power was measured using the integrating sphere. Finally, the values of thermal resistance and thermal capacity were obtained from the transient temperature curve. The chip was charged by 350 mA for 60 s; the sensor current was 1 mA and the time was 100 s. The ambient temperature was maintained at 25 °C. The experimental result accuracies of temperature and thermal resistances were chosen to be 0.1 °C and 0.1 K/W, respectively.

IV. Results and Discussion

Hexagonal BN powder (Aladdin, Shanghai) was purchased with average particle size of 2 μm. The thermal conductivity value of Hexagonal BN powder is about 300 W/mK as shown in literatures [30], [31]. Ball milling process was carried out for 15 min. Fig. 4(a) is a SEM image showing the morphology of milled BN powder. It can be seen that the particle size is ranging from 2.5 μm to about 10 nm. The particle sizes are very nonuniform, and that is beneficial to high thermal conductivity of BN/silicone [32].

The milled BN powder was filled into the gap between the edges of the LED chip and square groove. After compaction by microprobe, the silicone was dispensed and filled the voids of BN powder. Fig. 4(b) shows the SEM image of BN/silicone composite. It can be seen that the milled BN particles are randomly dispersed in the composite and wrapped efficiently by silicone. The silicone is filled fully into the voids of BN particles. There are almost no air voids and the connection between BN particles is tight. The thermal conductivity was evaluated by thermal conductivity measurement apparatus (LW9389, Longwin, Taiwan). The measurement results show that the thermal conductivity of BN/silicone composite is about 4.4 W/mK.

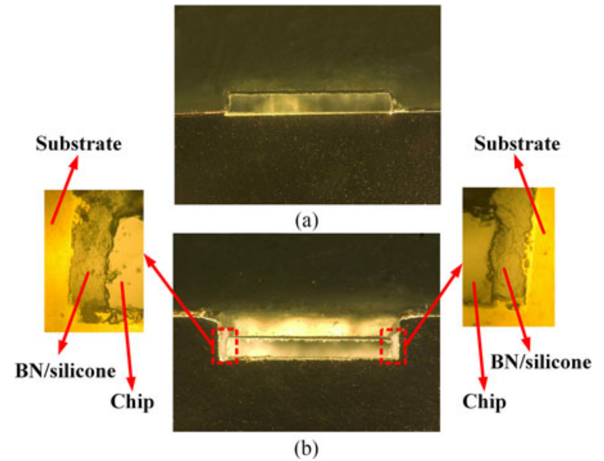

Fig. 5. Cross sections of (a) traditional structure and (b) proposed embedding structure.

The cross sections of traditional structure and proposed embedding structure are shown in Fig. 5. According to former thermal analysis, the thermal resistance of silver paste is larger with the die area decreasing. In order to minimize the overall die-bonding interface thermal resistance, a large size LED chip is chosen, and the die area is 50 × 50 mil. The height of LED chip is 150 μm. The LED chip is fully embedded into the square groove, which is at the center of the substrate. The smaller gap width between the edges of LED chip and square groove is beneficial to low thermal resistance of BN/silicone composite. However, if the gap width is too small, the filling process of BN/silicone composite is too hard to complete. Different gap widths are researched by changing the chip and square groove size, and it is found that both demands for thermal resistance and operability can be well satisfied when the gap width is around 50 μm. After measurement, the depth and width of the square groove are about 290 μm and 1.38 mm, respectively. The gap widths between the edges of the LED chip and square groove are ranging about from 50 to 60 μm. As shown in the insets of Fig. 5(b), the gap width between left side edges of the LED chip and square groove is about 60 μm and that in the right side is about 52 μm. It can be seen that the BN/silicone composite is tightly attached onto the edges of LED chip and substrate, and its height is a little larger than that of the chip. All of these ensure the efficient heat-dissipation path and low thermal resistance of BN/silicone composite.

Different structure functions, including cumulative structure functions and differential structure functions, are obtained by the transient thermal resistance measurements. The cumulative structure function is described that the cumulative thermal capacitance is the function of the cumulative thermal resistance. The differential structure function is defined as the derivative of the cumulative curve. The thermal resistance in the cumulative structure function is large in the relatively flat region, while the

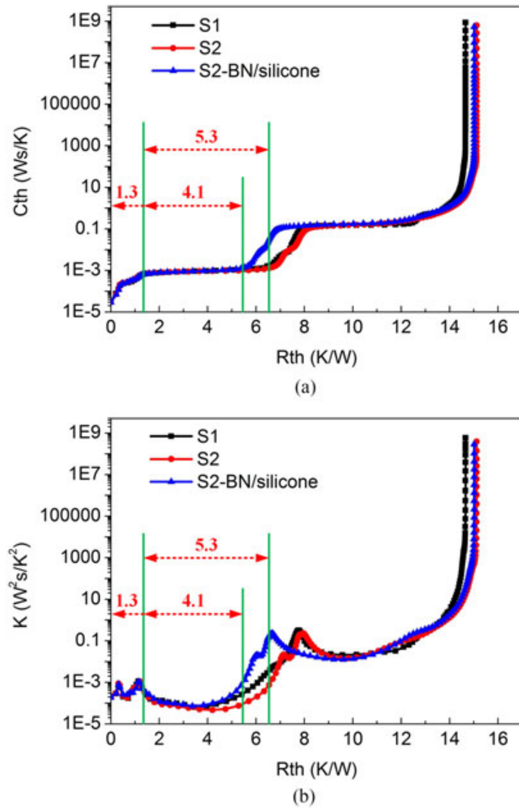

Fig. 6. Different structure functions of sample 1 of traditional structure and sample 2 of embedding structure before and after filling with BN/silicone composite. (a) Cumulative structure functions and (b) Differential structure functions ("S" represents "Sample").

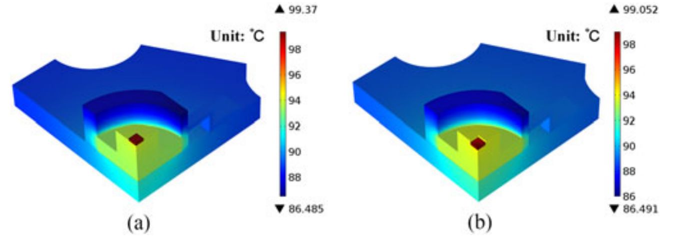

Fig. 7. Simulated temperature fields of LED models. (a) Traditional structure and (b) proposed embedding structure.

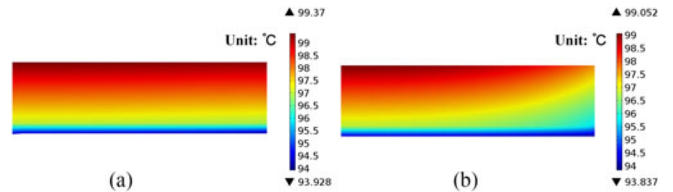

Fig. 8. Simulated temperature fields in cut plane of chip and die attach. (a) Traditional structure and (b) proposed embedding structure.

thermal capacitance is large in the steep region. In the differential structure function, the wave crests indicate that the region has a high thermal conductivity and the wave troughs indicate an area with low thermal conductivity. And the peaks typically point to the middle of any new region. Accordingly, the distance between the origin and the first peak yields the thermal resistance from the epitaxial layer to the middle region of the sapphire submount of the chip. The distance between the first and the third peaks represents the total thermal resistance of:

1) the die-bonding layer;
2) one-half of the sapphire submount; and
3) one-half of the Cu slug. For the traditional packaging structure, the thermal resistance of the die-bonding layer (silver paste) can ranges from 2.9 to 11.6 K/W [4], [24].

Sample 1 is fabricated with the traditional structure and sample 2 is fabricated with the proposed embedding structure. Before and after filling with BN/silicone composite, the structure functions are both shown in Fig. 6. In Fig. 6(a), it can be seen that the die-bonding interface thermal resistance of sample 2 without BN/silicone composite is very close to that of sample 1, both about 5.3 K/W. After filling with BN/silicone composite, the die-bonding interface thermal resistance of sample 2 is reduced to 4.1 K/W. The thermal resistances of the LED chips are all about 1.3 K/W. In Fig. 6(b), the first peaks are overlapped, so the distances of third peaks can also be considered as the differences of the die-bonding thermal resistances. The third peaks of sample 1 and sample 2 before filling with BN/silicone composite are very close. The distance of third peaks of sample 1 and sample 2 after filling with BN/silicone composite is $1.2\,\mathrm{K/W}$, consistent with the comparison results in Fig. 6(a). Consequently, compared to traditional packaging structure, the proposed embedding packaging structure can efficiently reduce the die-bonding interface thermal resistance by 22.6%.

In order to verify the thermal performance of the proposed structure further, thermal simulations were conducted. In simulations, only a quarter of the LED model was utilized to simulate the temperature field due to its symmetry, as shown in Fig. 7. The LED module was mounted on a hexagonal MCPCB for electrical connection and heat dissipation. Inside the LED module, a blue LED chip was mounted onto a lead-frame via silver paste. The ambient temperature was fixed at 25 °C. Forced convection was occurred at the bottom surface of the printed circuit board (PCB) with a heat transfer coefficient of 20 W/(m^2·K), and other surfaces were cooled by convection with a heat transfer coefficient of 5 W/(m^2·K). The material properties were the same as those in [33]. From the temperature fields shown here, it can be seen that the highest temperatures locate in the center of chips and the lowest temperatures locate in the plastic moulds. Most heat is transferred downwards by the Cu slug to the PCB.

Simulated temperature fields in the cut plane of chip and die attach are studied and shown in Fig. 8. It can be seen that both the highest and lowest temperatures are reduced by the proposed structure. The temperatures in side surfaces are reduced and the isothermal surfaces are warping up. It means part of heat is dissipated from the side surfaces. The mean temperatures of the chip top surface and bottom surface in the traditional structure are 99.29 °C and 96.96 °C, respectively, and those in the proposed structure are 98.37 °C and 96.27 °C, respectively. The mean temperature of the bottom surface of silver paste in the traditional structure is 94.24 °C, while that in the proposed structure is 94.10 °C. The heat flow generated from the chip is 0.68 W, which is the experimental result. According to the heat transfer theory, thermal resistance is defined as the temperature difference between the two sides of the bonding divided by the

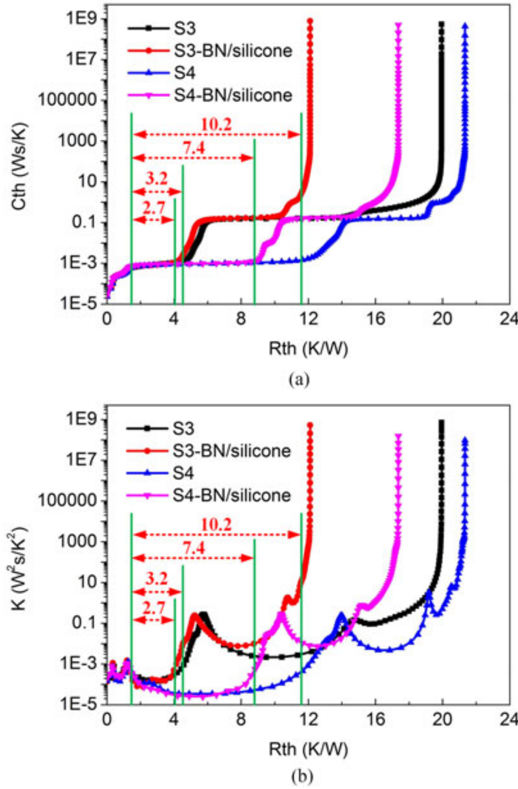

Fig. 9. Different structure functions of samples 3 and 4 of embedding structure before and after filling with BN/silicone composite. (a) Cumulative structure functions and (b) differential structure functions ("S" represents "Sample").

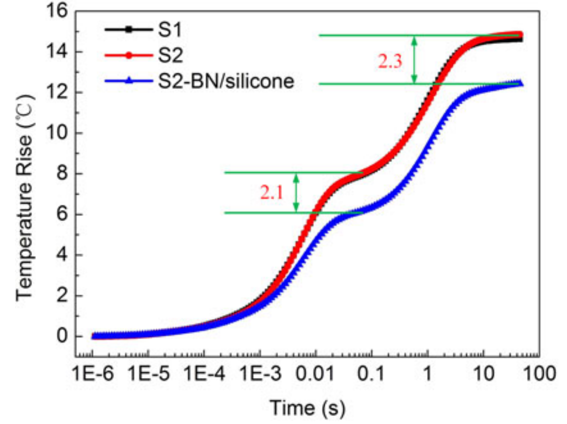

Fig. 10. Junction temperature rises of sample 1 of traditional structure and sample 2 of embedding structure before and after filling with BN/silicone composite ("S" represents "Sample").

heat flow [4]

$$R_{\mathrm{bond}} = \frac{T_1 - T_2}{q} \tag{5}$$

where T_1 and T_2 are the mean temperatures on the two sides of the layer and is the heat flow through this layer. After calculation, the simulated die-bonding thermal resistances in the traditional and proposed structures are 4.00 and $3.19\,\mathrm{K/W}$, respectively. Consequently, the die-bonding thermal resistance is reduced by 20.3%. It is close to the measurement results shown in Fig. 6. The simulated results and experimental results both demonstrate the efficient reduction of die-bonding interface thermal resistance by the proposed embedding structure.

To evaluate the regularity of the heat-dissipation ability improvement by the proposed embedding structure, samples 3 and 4 of the proposed embedding structure with different initial die-bonding interface thermal resistances are fabricated and measured. The results are shown in Fig. 9. In Fig. 9(a), before filling with BN/silicone composite, the die-bonding interface thermal resistances of samples 3 and 4 are about 3.2 and 10.2 K/W, respectively. After filling with BN/silicone composite, the die-bonding interface thermal resistances of samples 3 and 4 are reduced to about 2.7 and 7.4 K/W, respectively. In Fig. 9(b), the first peaks are overlapped, so the distances of third peaks can also be considered as the differences of the die-bonding thermal resistances. The distance of third peaks of sample 3 before and after filling with BN/silicone composite is 0.5 K/W, and that of sample 4 is 2.8 K/W, consistent with the comparison results in Fig. 9(a). As a result, the die-bonding interface thermal resistances of samples 3 and 4 are reduced by 15.6% and 27.5%, respectively. Thus, it can be concluded that the reductive percentage of the die-bonding interface thermal resistance by the proposed embedding structure is larger when the initial die-bonding interface thermal resistance, i.e., the thermal resistance of the silver paste is larger. The results are consistent with the aforesaid analysis of (4). Furthermore, the thermal resistance of lead-frame, including Cu slug, premolded, and ceramic packages, is 1.6 K/W, and the overall thermal resistances of samples 3 and 4 without BN/silicone composite are 6.1 and 13.1 K/W, as shown here. After filling with BN/silicone composite, they are reduced to 5.6 and 10.3 K/W, respectively. Consequently, the overall thermal resistances are reduced by about 8.2% and 21.4%, respectively.

Fig. 10 shows the junction temperature rises of samples 1 and 2 with the driving current of 350 mA. The bottom of the hexagonal MCPCB where the LED package mounts is at a constant temperature of 25 °C. Sample 1 is fabricated with the traditional structure and sample 2 is fabricated with the embedding structure. Their thermal resistances of the silver paste are both about 5.3 K/W as shown in Fig. 6. The temperature rise of sample 1 is 14.6 °C, and that of sample 2 before filling with BN/silicone composite is a little higher, 14.8 °C. But after filling with BN/silicone composite, the temperature rise of sample 2 is reduced to 12.5 °C. As a result, compared to traditional packaging structure, the proposed embedding packaging structure can reduce the junction temperature rise by 14.4%. Life-time estimation of high-power blue LED chips was conducted by extrapolation using exponential decay function and presented in the form of Arrhenius plot [34]. With this method, the L70 (30% degradation of light output to the initial value) lifetime of high-power LED chip with junction temperature of 75 °C is 44 356 h. After the junction temperature is reduced by 2.3 °C, 72.7 °C, the L70 lifetime is 47 611 h with the increase of 3255 h. The lifetime is increased by 7.3%, and as a result, the thermal reliability has been improved.

The effect of the proposed embedding structure on LEDs' optical performances is also measured. The LID curves of sample 1 of traditional structure and sample 2 of embedding structure before and after filling with BN/silicone composite are shown

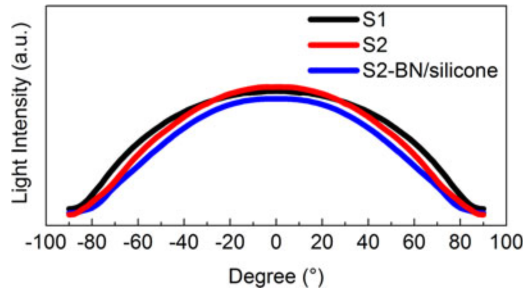

Fig. 11. LID curves of sample 1 of traditional structure, and sample 2 of embedding structure before and after filling with BN/silicone composite ("S" represents "Sample").

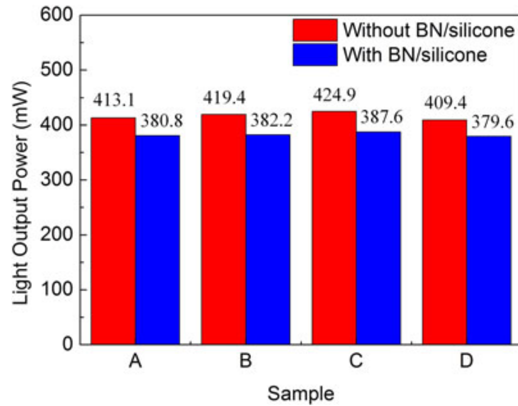

Fig. 12. LOP comparison of samples of embedding structure before and after filling with BN/silicone composite.

in Fig. 11. It can be seen that all the LID curves are Lambert distribution. The half light intensity angle (HLIA) of sample 1 is 134.3°. That of sample 2 before filling with BN/silicone composite is 124.2°. It is slightly smaller, about 122.1° after filling with BN/silicone composite. So compared to traditional structure, the proposed embedding structure reduces the HLIA by 9.1%. This is mainly due to the square groove in the substrate where the LED chip is fully embedded, as shown in Fig. 5.

Fig. 12 shows the LOP comparison results of samples of embedding structure before and after filling with BN/silicone composite. The LOPs are all reduced after filling with BN/silicone composite. Without BN/silicone composite, the LOPs are 413.1, 419.4, 424.9, and 409.4 mW, respectively. After filling with BN/silicone composite, they are correspondingly reduced to 380.8, 382.2, 387.6, and 379.6 mW. The LOPs are reduced by 7.8%, 8.9%, 8.8, and 7.3%, respectively. The average LOP reduction is 8.2%. This LOP loss is mainly due to the scattering of BN particles. Based on simple optical and thermal analysis, it can be obtained: the thermal conductivity of BN/silicone composite is larger with the BN concentration increasing, so the die-bonding thermal resistance is smaller and the thermal performance is better. On the other side, the scattering effect on light by BN particles is larger and the light output loss is larger. As this is the early stage of exploring principles, BN powder is filled as more as possible to obtain a high thermal conductivity, and it also brings about the undesired effects of light output loss.

In some specific applications, such as headlight and pico-projector, high power and high power density is required and a considerable amount of heat is generated [35], [36]. Therefore, it is of great importance to efficiently dissipate the heat from the chip. Furthermore, the viewing angle is required to be smaller to concentrate the light energy to a specific area. As shown in the research, the embedding packaging structure can provide better heat dissipation ability and smaller viewing angle. Thus, it can be a simple but effective industrial solution in these lighting applications.

V. Conclusion

In order to reduce the die-bonding interface thermal resistance, an embedding packaging structure is proposed. The heat dissipation method of utilizing chip side area as an additional heat transfer path is proposed and demonstrated for the first time. The experimental results show that the heat-dissipation ability of LEDs has been significantly improved by the proposed embedding packaging structure. Consequently, the die-bonding interface thermal resistance can be reduced by more than 20% and the reductive percentage is larger when the initial die-bonding interface thermal resistance is larger. The junction temperature rise can also be reduced by 14%. At the same time, the HLIA is reduced by about 9% and the LOP is slightly reduced by about 8%. Furthermore, the LOP loss can be significantly reduced. In our recent research, the vertical LED chip is adopted and the light output reduction is less than 2%. The cost may be slightly increased, but we believe that it could be well controlled after its wide application. The reliability of LEDs with high input current is improved, showing that the lifetime is longer and the optical performance stability is better. Thus, the proposed structure is believed to be promising in some LED applications with high input current.

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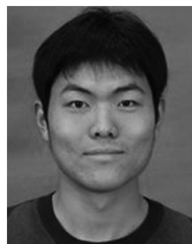

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