# Minimum-RMS-Current Operation of Asymmetric Dual Active Half-Bridge Converters With and Without ZVS

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***Abstract*—This paper presents a comprehensive steady-state analysis of asymmetrically operated dual active half-bridge (DAHB) dc–dc converters, i.e, DAHB converters operated with a non 0.5 duty-ratio. Such asymmetric operation presents an additional control handle, which may be used to optimize converter performance. The different possible modes of operation are introduced followed by detailed analysis of active power and rms current variation and zero-voltage-switching (ZVS) performance in each mode. Using this information, closed-form expressions corresponding to two control strategies are derived which minimise rms value of transformer current at a given power with and without ZVS operation. The accuracy of the theoretical predictions are verified using numerical optimisation approaches and also through MATLAB Simulink-based simulations. Finally, experimental results on a 625 W laboratory prototype are presented which validate the discussed ideas. Both simulation and experimental results indicate that the proposed strategies potentially offer significant efficiency advantages compared to simple square-wave control, especially under light-load conditions for converters operating with nonunity effective voltage conversion ratios.**

***Index Terms*—Bidirectional power flow, dual active half-bridge (DAHB), minimum rms current, zero-voltage-switching (ZVS).**

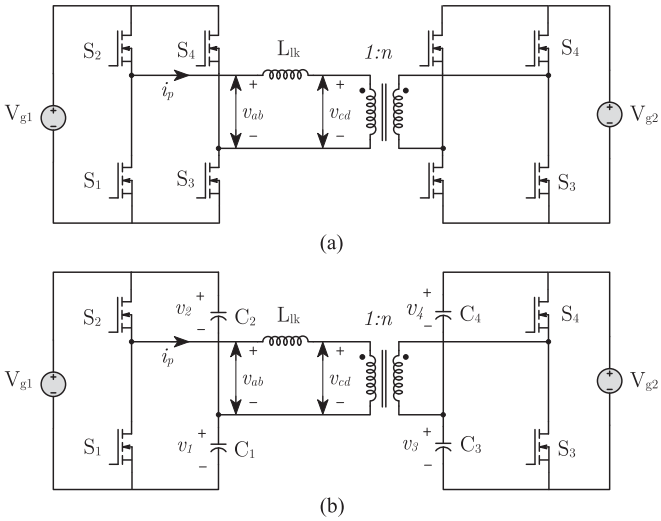


Fig. 1. The two forms of the DAB converter. (a) Full-Bridge. (b) Half-Bridge (DAHB).

## I. Introduction

DUAL-ACTIVE bridge (DAB) dc–dc converters [2] remain a popular choice for isolated bidirectional dc–dc power conversion applications like hybrid electric vehicles, uninterrupted power supplies, and battery chargers. These converters, having a voltage-fed full-bridge or half-bridge on either side of a high-frequency transformer, as shown in Fig. 1, do not have the voltage-spike problem associated with the current-fed dc–dc converter architecture [3]. Moreover, the MOSFETs have the possibility of undergoing natural zero-voltage switching (ZVS) operation in both directions of power-flow.

At low power levels (below 750 W), dual active half-bridge (DAHB) converters are generally preferred to their full-bridge counterparts because of their benefits of low device count and reduced size [4]. Another added advantage of DAHB converters is absence of dc component of transformer magnetizing current in steady state due to the presence of the half-bridge capacitors. In contrast, full-bridge DAB converters may operate with a nonzero dc component of magnetizing current in a steady state due to application of unequal volt-seconds during a switching cycle on either side of the transformer [5]. Such operation may arise due to several reasons, such as unmatched device transition times, device voltage drop, gate drive delays, and pulsating loads, and increases core loss and chance of transformer saturation. Hence closed-loop control is necessary to prevent dc flux buildup in the full-bridge DAB converter [5], [6]. In view of these advantages, half-bridge converters operating on the DAB principle have found use in a variety of bidirectional power-flow applications in the low power regime [7]–[20].

The simplest way to regulate power flow in DAHB converters, as in DAB converters, is to drive the primary and secondary side bridges with a duty-ratio of 0.5 and vary the phase overlap between the resulting square waves to vary the active power output. This control strategy, referred to as simple phase-shift control (*SPC*) in this paper, results in high-circulating current [34] in the circuit, which leads to increased conduction losses and higher current rating of the devices. Another critical limitation is that ZVS operation over the entire power range is possible only when the effective voltage conversion ratio is unity [2].

Manuscript received February 9, 2016; revised July 18, 2016; accepted September 6, 2016. Date of publication September 27, 2016; date of current version February 27, 2017. This paper was presented in part at the *IEEE Energy Conversion Congress and Exposition*, Pittsburgh, PA, USA, Sep. 2014 [1]. Recommended for publication by Associate Editor R. Ayyanar.

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Digital Object Identifier 10.1109/TPEL.2016.2613874

Many modulation strategies have been proposed in contemporary literature to overcome these problems, with the majority of such approaches in the realm of dual-active full-bridge converters [21]–[35]. These schemes attempt to enhance converter performance by utilizing, in the most generic case, the duty-ratios of the primary and secondary bridges as additional control handles along with the phase shift. Though the fundamental harmonic approximation (FHA) based strategy discussed in [28] and [26] can be adopted for DAHB converters as well, it is only accurate for converters with a resonant tank network operating at a switching frequency close to the tank resonant frequency. In this paper, nonresonant DAHB converters are considered, and hence adopting the FHA instead of an exact analysis would lead to gross errors in active power and rms current computation. The exact approach discussed in [29] and [31] cannot be directly extended to DAHB converters because of the fundamentally different nature of the transformer voltage waveforms of the two converters (rectangular in DAHB versus quasisquare wave in DAB), which leads to different operating modes.

Researchers have also proposed use of asymmetric duty-ratio control to minimise rms current and improve ZVS performance of the boost-integrated/ current-fed DAHB converter [7] by rendering a trapezoidal or flat-topped profile to the transformer current waveform [9], [10], [17], [18]. However, as established in a subsequent section of this paper, such flat-topped operation is not possible, in general, for the voltage-fed DAHB converter, which is the focus of this paper.

Recognizing that a voltage-fed DAHB converter operating with SPC has a higher transformer rms current than a DAB converter or a current-fed DAHB converter at the same power, it is clear that rms current minimization in voltage-fed DAHB converters is of critical importance to ensure good operating efficiencies. As a consequence, this paper takes up the hitherto unstudied problem of asymmetric operation of voltage-fed DAHB converters with the objective of mitigating the issue of reactive power flow. Specifically, a two-degree of freedom based control approach is adopted, wherein both bridges are assumed to be driven at the same (non 0.5) duty-ratio.

The remaining part of the paper is organized as follows. In Section II, the different modes possible for generic (non 0.5 duty-ratio) operation are systematically identified followed by analysis of active power output and rms current variation in each mode in Section III. ZVS conditions for all devices are developed in detail in Section IV. Finally, in Section V, information gleaned from the presented analysis is used to propose a modulation strategy which minimizes transformer rms current for a given output power. This proposed control scheme is referred to as optimal phase-shift control (*OPC*). It is shown that OPC operation leads to loss of ZVS operation at low powers. Since at higher switching frequencies, ZVS operation is often considered mandatory, a second modulation strategy, referred to as optimal phase-shift control with ZVS (*OPCZ*), is also developed which additionally takes ZVS operation into account while minimising rms current. All analytical predictions are validated through simulation and experimental results presented in Sections VI and VII, respectively.

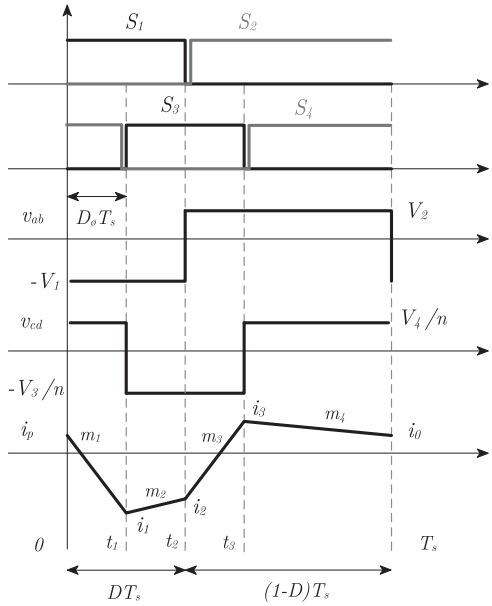


Fig. 2. Generic waveforms of transformer voltage and current.

TABLE I
AVERAGE CAPACITOR VOLTAGES

| $V_1$ | $V_2$ | $V_3$ | $V_4$ |
|---|---|---|---|
| $V_{g1}.(1-D)$ | $V_{g1}.D$ | $V_{g2}.(1-D)$ | $V_{g2}.D$ |

## II. GENERIC ANALYSIS

Without loss of generality, the primary-side half-bridge ($S_1$, $S_2$) is assumed to be interfaced with the low-voltage dc port ($V_{g1}$), whereas the secondary-side half-bridge ($S_3$, $S_4$) is assumed to be interfaced with the high-voltage dc port ($V_{g2}$). In a practical application, $V_{g2}$ could represent the voltage of the high-voltage dc bus feeding the PWM inverter of a two-stage PV microinverter or a hybrid electric vehicle, while $V_{g1}$ could denote the voltage of the low-voltage battery port.

Steady-state waveforms of primary voltage $v_{\rm ab}$, reflected secondary voltage $v_{\rm cd}$, and primary current $i_p$, for a general case are shown in Fig. 2. Each bridge is driven with a duty-ratio $D$ (corresponding to the low-side devices) and the respective gate-pulses of the primary and secondary side are phase shifted by $D_\phi T_s$. $V_1, V_2, V_3$, and $V_4$ denote average voltages across capacitors $C_1, C_2, C_3$, and $C_4$ which can be determined from flux balance of the inductors $L_{\rm lk}$ and $L_m$ (the magnetizing inductance). Expressions for the same are noted in Table I.

From Fig. 2, it can be seen that the primary current waveform is piecewise linear having four sections with slopes $m_1,\ m_2,\ m_3,\ m_4$ and initial values $i_0,\ i_1,\ i_2,\ i_3$. From Fig. 2, it can be seen that the primary current waveform is piecewise linear having four sections with slopes $m_1,\ m_2,\ m_3,\ m_4$ and initial values $i_0,\ i_1,\ i_2,\ i_3$. From charge balance of $C_1$ and $C_2$, it follows that the average value of this current over one switching period is zero. Using this, the following generic expressions

TABLE II
POSSIBLE MODES OF OPERATION

| Mode I | Mode II | Mode III |
|---|---|---|
| $D < 0.5$<br>$D_\phi < D$ | $D < 0.5$<br>$D < D_\phi < 1-D$ | $D < 0.5$<br>$1-D < D_\phi$ |
| **Mode IV** | **Mode V** | **Mode VI** |
| $D > 0.5$<br>$D_\phi < 1-D$ | $D > 0.5$<br>$1-D < D_\phi < D$ | $D > 0.5$<br>$D < D_\phi$ |

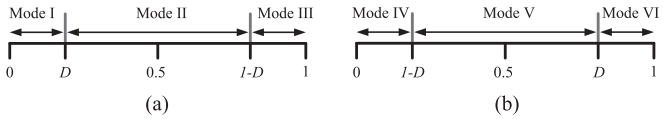


Fig. 3. Range of $D_\phi$ for different operation modes (a) $D < 0.5$. (b) $D > 0.5$.

for $i_0,\ i_1,\ i_2,\ i_3$ can be derived:

$$i_0 = -\frac{1}{2T_s}\big[m_1 t_1(T_s - t_1 + t_3) + m_2(t_2 - t_1) \times (T_s + t_3 - t_1 - t_2) + m_3(t_3 - t_2)(T_s - t_2)\big] \quad (1)$$

$$i_1 = \frac{1}{2T_s}\big[m_1 t_1(T_s + t_1 - t_3) - m_2(t_2 - t_1) \times (T_s + t_3 - t_1 - t_2) - m_3(t_3 - t_2)(T_s - t_2)\big] \quad (2)$$

$$i_2 = \frac{1}{2T_s}\big[m_1 t_1(T_s + t_1 - t_3) + m_2(t_2 - t_1) \times (T_s - t_3 + t_1 + t_2) - m_3(t_3 - t_2)(T_s - t_2)\big] \quad (3)$$

$$i_3 = \frac{1}{2T_s}\big[m_1 t_1(T_s + t_1 - t_3) + m_2(t_2 - t_1) \times (T_s - t_3 + t_1 + t_2) + m_3(t_3 - t_2)(T_s + t_2)\big]. \quad (4)$$

Depending on the relative values of $D$ and $D_\phi$, six modes of operation are possible. Conditions for operation in each such mode is listed in Table II. Fig. 3 gives a pictorial representation of the same.

Transformer primary and (reflected) secondary voltage and primary current waveforms for each mode are shown in Fig. 4. The modes differ from one another in the way that the active power output varies with variation in $D$ and $D_\phi$. Modes I and IV have similar relative waveforms of $v_{\rm ab}$ and $v_{\rm cd}$. Thus they have the same expression for power output. The same is true for modes III and VI. Expressions for $t_1, t_2, t_3$ and $m_1, m_2, m_3$ for the different modes are noted in Table III.

A special case of asymmetric operation occurs when the transformer current waveform has a trapezoidal shape [9]. Such flat-topped profile of the current is possible only when the positive and negative levels of the primary and secondary voltage match each other, i.e, if

$$V_1 = \frac{V_3}{n},\ V_2 = \frac{V_4}{n}$$
$$\Rightarrow V_{g1}.(1-D) = \frac{V_{g2}.(1-D)}{n},\ V_{g1}.D = \frac{V_{g2}.D}{n}$$
$$\Rightarrow n.V_{g1} = V_{g2}. \quad (5)$$

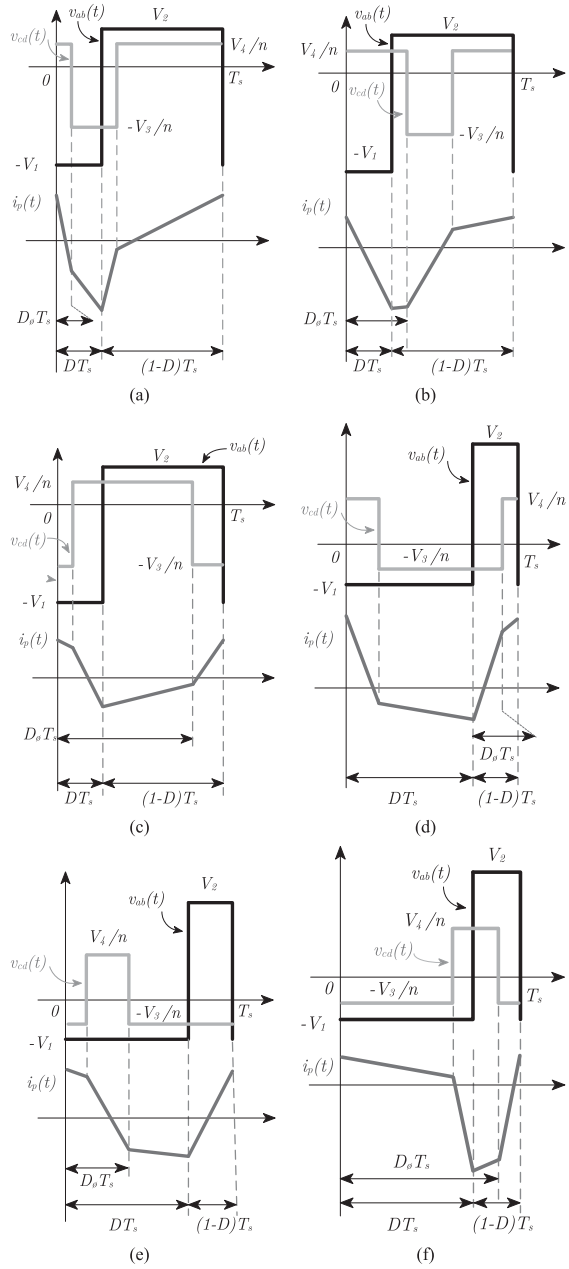


Fig. 4. Primary, (reflected) secondary voltages and primary current for the six modes (for $M = V_{g2}/(nV_{g1}) < 1$). (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI.

From (5), it can be concluded that flat-topped modulation is not possible if either $V_{g1}$ and $V_{g2}$ deviate from their nominal values, i.e, the effective voltage conversion ratio ($M = V_{g2}/nV_{g1}$) deviates from unity.

## III. ACTIVE POWER OUTPUT AND TRANSFORMER RMS CURRENT

### A. Active Power

The average active power over a switching time-period is given by

$$P = \frac{1}{T_s}\int_0^{T_s} v_{\rm ab}(t) i_p(t)\, dt. \quad (6)$$

TABLE III
EXPRESSIONS OF $t_1, t_2, t_3$ AND $m_1, m_2, m_3$ FOR THE DIFFERENT MODES

| | $t_1/T_s$ | $t_2/T_s$ | $t_3/T_s$ | $m_1.L_{\rm lk}$ | $m_2.L_{\rm lk}$ | $m_3.L_{\rm lk}$ |
|---|---|---|---|---|---|---|
| Mode I, IV | $D_\phi$ | $D$ | $D_\phi + D$ | $-V_1 - V_4/n$ | $-V_1 + V_3/n$ | $V_2 + V_3/n$ |
| Mode II | $D$ | $D_\phi$ | $D_\phi + D$ | $-V_1 - V_4/n$ | $V_2 - V_4/n$ | $V_2 + V_3/n$ |
| Mode III, VI | $D_\phi - 1 + D$ | $D$ | $D_\phi$ | $-V_1 + V_3/n$ | $-V_1 - V_4/n$ | $V_2 - V_4/n$ |
| Mode V | $D_\phi - 1 + D$ | $D_\phi$ | $D$ | $-V_1 + V_3/n$ | $-V_1 - V_4/n$ | $-V_1 + V_3/n$ |

TABLE IV
ACTIVE POWER OUTPUT IN DIFFERENT MODES

| Mode I, IV | Mode II |
|---|---|
| $CD_\phi\,[2DD' - D_\phi]$ | $CD^2(1-2D_\phi)$ |
| **Mode III, VI** | **Mode V** |
| $C(D_\phi - 1)\,[2DD' + D_\phi - 1]$ | $C(1-D)^2(1-2D_\phi)$ |

TABLE V
CONDITIONS FOR MAXIMUM POWER OUTPUT

| $D_{\rm max}$ | $D_{\phi\,\rm max}$ | $P_{\rm max}$ | Mode |
|---|---|---|---|
| 1/2 | $D.(1-D) = 1/4$ | $C/16$ | I |

For modes I and IV, this can be expressed as

$$P = \frac{1}{T_s}\left[-V_1.\left(\frac{1}{2}(i_0+i_1)t_1 + \frac{1}{2}(i_1+i_2)(t_2-t_1)\right) + V_2.\left(\frac{1}{2}(i_2+i_3)(t_3-t_2) + \frac{1}{2}(i_3+i_0)(T_s-t_3)\right)\right]. \tag{7}$$

Using the expressions for $i_o,\ i_1,\ i_2,\ i_3$ given in (1) through (4) and those listed in Table III, (7) can be simplified to yield

$$P = \frac{D_\phi}{2f_s}\left[m_1(D_\phi + D^2 - D) + m_2(D - D_\phi) + m_3 D(1-D)\right](V_1 + V_2). \tag{8}$$

Using the expressions of Table I, this can be simplified as

$$P = CD_\phi\,[2DD' - D_\phi] \tag{9}$$

where $C = V_{g1}V_{g2}/(2nL_{\rm lk}f_s)$, $D' = (1-D)$. Adopting a similar approach, expressions for power output in other modes can be also derived, which are listed in Table IV.

Conditions for maximum power output across all modes are listed in Table V, from which it can be seen that maximum power is obtained for SPC in mode I. Fig. 5 shows the contour plots of output power versus $D$ and $D_\phi$ for the parameter values specified in Table VI. Unless otherwise mentioned, all simulation results and representative curves shown in the paper correspond to the specifications of Table VI. Fig. 6 shows variation of active power in the different modes. It can be observed that the power flow is symmetrical about $D = 0.5$ (e.g, $P_{|D=0.3} = P_{|D=0.7}$, for same $D_\phi$) and inverse-symmetrical about $D_\phi = 0.5$ (e.g, for same $D$, $P_{|D_\phi=0.3} = -P_{|D_\phi=0.7}$). It can also be observed that for a given

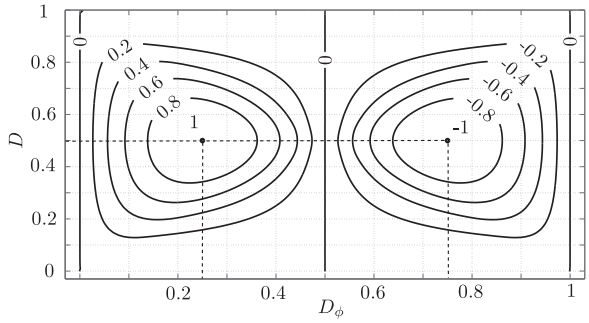


Fig. 5. Contour plots showing variation of active power (normalised to the maximum power) with $D$, $D_\phi$.

TABLE VI
PARAMETER VALUES FOR SIMULATION AND ALL PLOTS

| $V_{g1}$ | $V_{g2}$ | $L_{\rm lk}$ | $n$ | $f_s$ |
|---|---|---|---|---|
| 50 V | 200 V | 5 $\mu$H | 2 | 50 KHz |

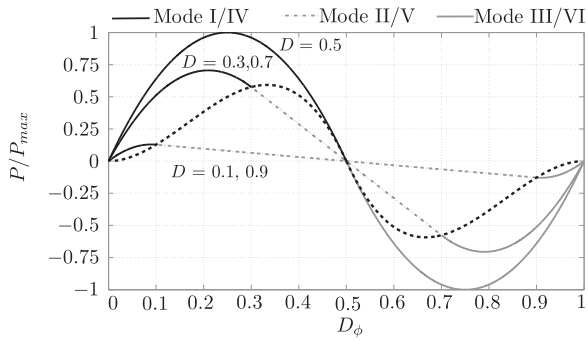


Fig. 6. Illustrating variation of normalised power in different modes.

value of $D$, maximum forward/reverse power in mode II (or V), occurs at the boundary of modes I/III (or IV/VI) and II (or V). The trajectory of this maximum power (shown by the dotted black line in Fig. 6) is given by

$$P_{m2(\max)(D)} = CD^2(1-2D) \tag{10}$$

from which the global maxima in mode II can be obtained as $P_{m2(\max)} = C/27$. For any power below this limit, one solution each in mode I and II exists for a given value of $D$. For $P > P_{m2(\max)}$, both solutions are in mode I.

TABLE VII
EXPRESSIONS FOR $i^2_{p(\mathrm{RMS})}$ IN DIFFERENT MODES

| | |
|---|---|
| Mode I, IV | $K[a(DD')^2 + bD_\phi^2(3DD' - D_\phi)]$ |
| Mode II | $K[a(DD')^2 + bD^2(3D_\phi D'_\phi - D)]$ |
| Mode III/VI | $K[a(DD')^2 + b(D'_\phi)^2(3DD' - D'_\phi)]$ |
| Mode V | $K[a(DD')^2 + b(D')^2(3D_\phi D'_\phi - D')]$ |

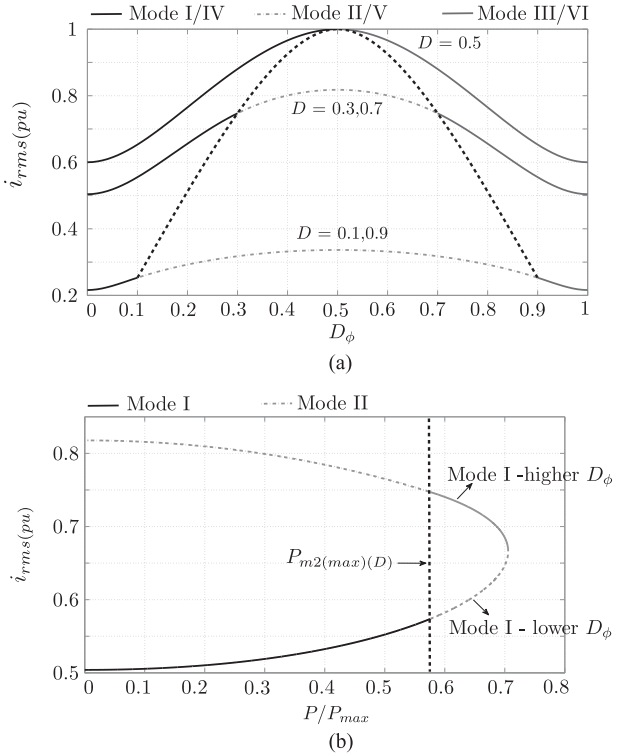


Fig. 7. Illustrating variation of (normalised) rms transformer current. For a given $D$, rms current increases monotonically in modes I/IV and II/V as $D_\phi$ approaches 0.5. (a) Variation of rms current in different modes. (b) Variation of rms current versus power for a given $D\,(=0.3)$.

### B. Transformer RMS Current

For the generic transformer current ($i_p$) waveform of Fig. 2, the rms value is given by

$$\begin{aligned} i^2_{p(\mathrm{rms})} = \; & (1/3)[(i_0^2 + i_1^2 + i_0.i_1).t_1 + (i_1^2 + i_2^2 + i_1.i_2) \\ & .(t_2 - t_1) + (i_2^2 + i_3^2 + i_2.i_3).(t_3 - t_2) \\ & + (i_3^2 + i_0^2 + i_3.i_0).(1 - t_3)]. \end{aligned} \tag{11}$$

As with active power output, the above expression may be simplified in different modes of operation using (1)–(4) and Table III. The resulting expressions are listed in Table VII, where $K = V_{g1}^2/(12L_{\mathrm{lk}}^2 {f_s}^2)$, $D' = 1 - D$, $D'_\phi = 1 - D_\phi$, $M = V_{g2}/nV_{g1}$, $a = (1 - M)^2$ and $b = 4M$. Variation of the normalised rms current with $D$ and $D_\phi$ are plotted in Fig. 7(a) and (b) respectively. It can be observed from Fig. 7(a) that for a given value of $D$, the rms current increases across the modes as $D_\phi$ approaches 0.5. Also, for a given value of $D_\phi$, the rms current is symmetrical about $D = 0.5$ and increases as $D$ approaches 0.5. The peak rms current is obtained at $D = 0.5$ and $D_\phi = 0.5$. Two further key observations can be made from Fig. 7(b), which shows the variation of rms current with power in modes I and II for a given value of $D$. For $P < P_{m\,2(\mathrm{max})(D)}$, solutions in both mode I and II are possible. However, the mode I solution clearly has a lower rms current throughout this power range. Second, for $P > P_{m\,2(\mathrm{max})(D)}$, of the two solutions possible in mode I, the solution corresponding to lower $D_\phi$ results in lower rms current.

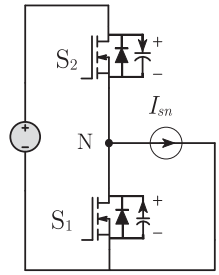


Fig. 8. Switching power-pole. For ZVS of $S_1$, just before its turn-on, $I_{\mathrm{sn}}$ should be directed away from $N$.

TABLE VIII
CONDITIONS FOR ZVS TURN-ON OF SWITCHES IN DIFFERENT MODES

| | $S_1$ | $S_2$ | $S_3$ | $S_4$ |
|---|---|---|---|---|
| Mode I, IV | $i_0 > 0$ | $i_2 < 0$ | $i_1 < 0$ | $i_3 > 0$ |
| Mode II | $i_0 > 0$ | $i_1 < 0$ | $i_2 < 0$ | $i_3 > 0$ |
| Mode III, VI | $i_0 > 0$ | $i_2 < 0$ | $i_3 < 0$ | $i_1 > 0$ |
| Mode V | $i_0 > 0$ | $i_3 < 0$ | $i_2 < 0$ | $i_1 > 0$ |

TABLE IX
SIMPLIFIED CONDITIONS FOR ZVS TURN-ON OF $S_1$ AND $S_2$ IN DIFFERENT MODES

| | Mode I, IV | Mode II |
|---|---|---|
| $S_1$ | $2MD_\phi > (M-1)D'$ | $2MD_\phi > (M-1)D'$ |
| $S_2$ | $2MD_\phi > (M-1)D$ | $2MD_\phi < M(1+D) + D'$ |
| | **Mode III, VI** | **Mode V** |
| $S_1$ | $2M(1-D_\phi) > (M-1)D$ | $2M(1-D_\phi) > (M-1)D$ |
| $S_2$ | $2MD_\phi < M(1+D) + D'$ | $2MD_\phi > (M-1)D$ |

## IV. ZVS CONDITIONS

Fig. 8 depicts a voltage-stiff complementary switching power-pole. The basic (necessary) condition for the low-side device $S_1$ to achieve ZVS turn-on is that, just prior to its turn-on, a net inductor current ($I_{\mathrm{sn}}$) should be present at the switch-node ($N$) and directed away from it so as to discharge its parasitic output capacitor. Following similar logic it can be concluded that, for ZVS turn-on of the top-side device $S_2$, $I_{\mathrm{sn}}$ should be directed towards the switch-node to ensure discharge of its output capacitor. This basic idea, in conjunction with the information of switching transition-instants, obtainable from Fig. 4, can be used to deduce the conditions for ZVS turn-on of each switch in different modes. These conditions are listed in Table VIII.

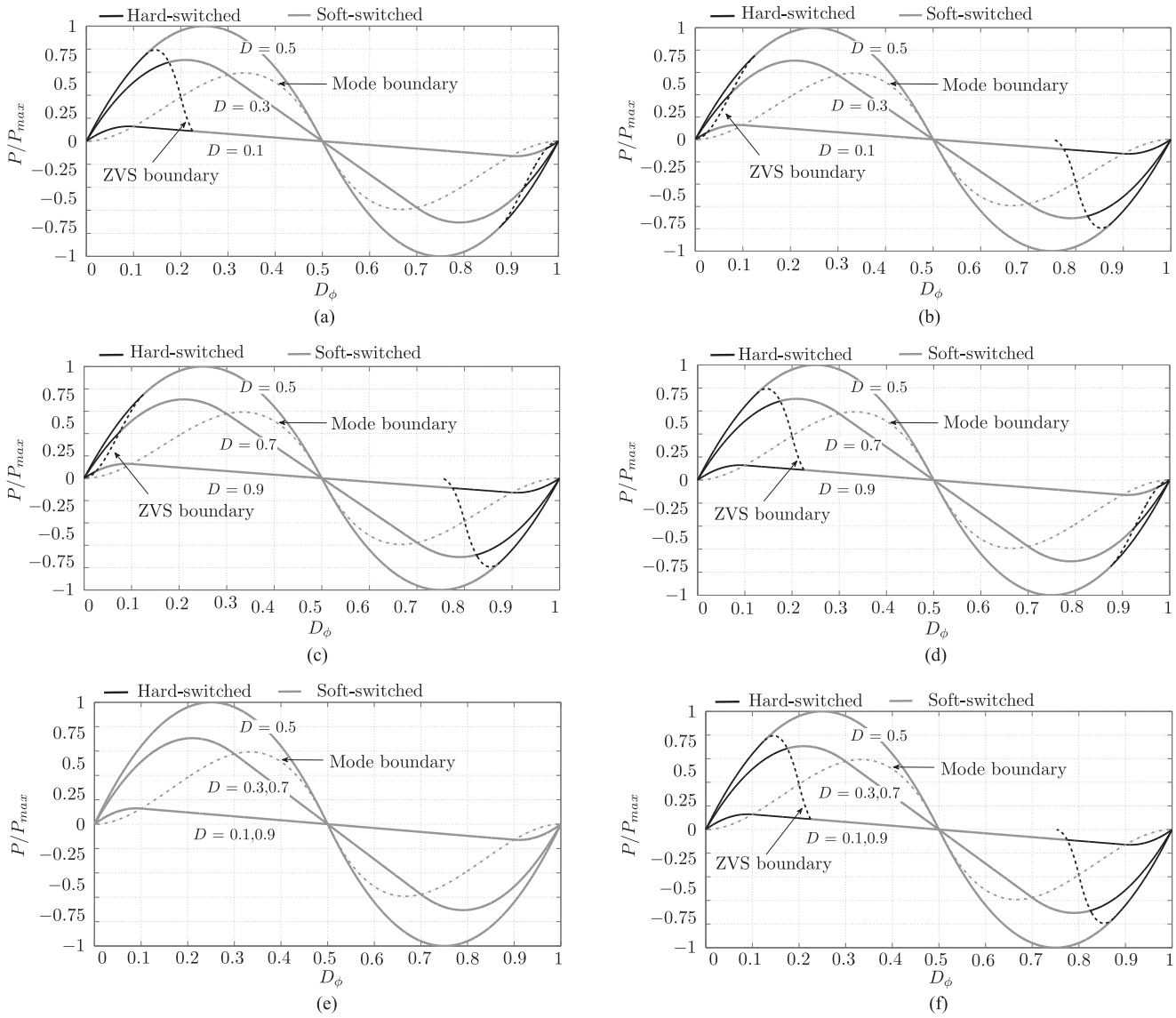


Fig. 9. Illustrating ZVS range of the topology. On the HV-side, both devices ($S_3$, $S_4$) get ZVS irrespective of the direction of power-flow and the value of $D$. For the LV-side devices, for forward powering with $D < 0.5$, ZVS of the low-side device ($S_1$) ensures ZVS of the high-side device ($S_2$). The opposite is true for reverse powering. (a) Bottom device ($S_1$) on LV-side for $D < 0.5$. (b) Top device ($S_2$) on LV-side for $D < 0.5$. (c) Bottom device ($S_1$) on LV-side for $D > 0.5$. (d) Top device ($S_2$) on LV-side for $D > 0.5$. (e) Both HV-side devices ($S_3$, $S_4$) $\forall$ $D$. (f) For all devices $\forall$ $D$.

Using (1) through (4) and the expressions listed in Table III, simplified necessary conditions for ZVS of switches $S_1$ and $S_2$ can be obtained. These are listed in Table IX, where $M = V_{g2}/nV_{g1}$ and $D' = 1 - D$.

Using these conditions and the boundary conditions defining the modes given in Table II, the following key conclusions can be drawn. First, it can be shown that, for $M < 1$, the listed conditions are satisfied in all modes. This implies that in both directions of power-flow, the high-voltage side devices, always undergo ZVS. Further it can be shown that, for positive power-flow and $M > 1$, conditions for $S_2$ hold if those of $S_1$ hold for $D < 0.5$; while for $D > 0.5$, conditions for $S_1$ hold if those of $S_2$ hold. It can also be shown that, this criticality of the low- and high-side devices vis-a-vis ZVS occurrence, are reversed for reverse power-flow. From the foregoing arguments, it also follows that, for $M = 1$ (flat-topped modulation), all four devices undergo ZVS. However, this is not really an advantage since, as discussed in Section II, any deviation of the voltage-ratio from its nominal value results in loss of flat-topped modulation. All the aforementioned assertions can be verified using Fig. 9, which identifies the hard- and soft-switched zones of operation of the switches on the power-flow curve.

## V. Minimum RMS Current Solution

This section discusses details of the mathematical optimization techniques used to derive closed form expressions of optimal values of the control variables for the OPC and OPCZ algorithms.

### A. Optimal Solution Without ZVS (OPC)

The problem of minimizing rms current at a given power (without ZVS consideration) can be formally stated as

$$\begin{aligned} &\min \quad i_{p(\text{rms})}(D, D_\phi) \\ &\text{s.t } P\ (D, D_\phi) = \ P_{\text{ref}}. \end{aligned} \tag{12}$$

As discussed in Section III-B, for a given value of $D$, rms current is minimized for a lower value of $D_\phi$. Thus, rms current values in modes I, IV are lesser than in the other modes and hence the active power output expression for these modes are considered for the equality constraint. Similarly for the objective function, the expression for rms current in modes I and IV are considered. Thus, the optimization problem can be restated as

$$\begin{aligned} \min \quad & a(DD')^2 + bD_\phi^2(3DD' - D_\phi) \\ \text{s.t} \quad & P_{\text{ref}} = CD_\phi\,[2DD' - D_\phi] \end{aligned} \tag{13}$$

which can be handled using standard Lagrangian formulation to arrive at the following solution for $M \neq 1$

$$D_\phi^3 + (a/3b)(D_\phi^2 - P_{\text{ref}}/C) = \ 0 \tag{14}$$

$$D^2 - D + (3b/2a)D_\phi^2 + D_\phi = \ 0. \tag{15}$$

Taking into consideration the fact that the solution of the above problem must be real, it can be shown that at all powers for $M = 1$ and above a certain limiting power ($P_{\text{lim}}$) for $M \neq 1$, the optimal solution is given by

$$D_\phi = \left(1 - \sqrt{1 - 16\,(P_{\text{ref}}/C)}\right)/4,\ D = 0.5. \tag{16}$$

For the $M \neq 1$ case, the critical value of $D_\phi$, corresponding to $P = P_{\text{lim}}$ may be obtained by simultaneously solving (14) and the power equality constraint (13) with $D = 0.5$ to yield

$$D_{\phi\ \text{lim}} = -(a/3b) + \sqrt{(a/3b)^2 + (1/2)(a/3b)} \tag{17}$$

from which an expression for $P_{\text{lim}}$ (in terms of $a$ and $b$) can be obtained using (13) and setting $D = 0.5$.

### B. Optimal Solution with ZVS (OPCZ)

When it is necessary to ensure ZVS operation of all devices while minimizing rms current of the transformer, the constrained optimization problem takes the form

$$\begin{aligned} &\min \quad i_{p(\text{rms})}(D, D_\phi) \\ &\text{s.t } P\ (D, D_\phi) = \ P_{\text{ref}} \\ &\quad z_j\ (D, D_\phi) > \ 0;\ j = 1,\ 2,\ 3,\ 4 \end{aligned} \tag{18}$$

where (18) represents the inequalities corresponding to ZVS operation. For the purpose of finding the optimal solution, operation below $D = 0.5$ is only considered as this simplifies the analysis without loss of generality since both active power output and rms current expressions are symmetric about $D = 0.5$.

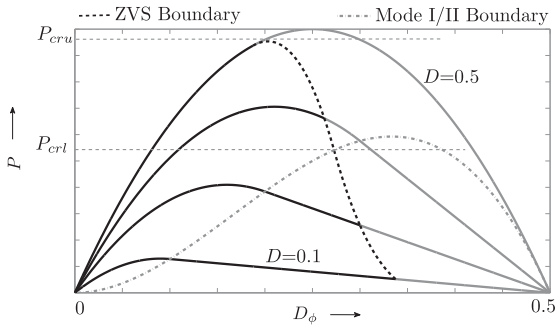


Fig. 10. Illustrating the position of the two critical power limits $P_{cr(u)}$ and $P_{cr(l)}$ on the complete power-scale of the converter.

For further simplification, forward power transfer is only considered. This implies operation in either Mode I or II and hence as discussed in Section IV, ZVS of the bottom device on the LV side ($S_1$) ensures ZVS of all devices of the converter. Thus in accordance with Table IX, the ZVS criterion of (18) can be represented by the single inequality

$$2MD_\phi > (M-1)D'. \tag{19}$$

The approach adopted for solving the optimization problem of (18) involves dividing the power-range of the converter into three operating zones—low, medium, and high. The two critical power limits $P_{\text{crl}}$ and $P_{\text{cru}}$ separating these three zones are depicted in Fig. 10, which also shows the ZVS boundary and boundary between modes I and II.

*1) Zone 1 (Low Power - $P < P_{\text{crl}}$):* Careful observation of Fig. 10 reveals that below a certain power, operation in Mode I is always hard-switched. This power (referred to as $P_{cr(l)}$) can be found by identifying the particular value of $D$ for which the whole of Mode I is just hard-switched. This is obtained by solving the ZVS boundary constraint (19) with the Mode I/II boundary equation, i.e, $D_\phi = D$. This yields

$$D_{cr(l)} = \ (M-1)/(3M-1) \tag{20}$$

$$P_{cr(l)} = \ C(1-M)^2(1+M)/(3M-1)^3. \tag{21}$$

Below this power, operation in Mode II is mandatory to ensure ZVS. Also, below this power the ZVS constraint is always active, i.e, the optimal solution satisfying only (12) is different from that satisfying both (12) and (18). Thus, in order to satisfy the complementary slackness conditions of the Karush-Kuhn-Tucker (KKT) equations [36], [37], the optimal solution must lie on the ZVS boundary and can be found by solving the ZVS boundary constraint with the power-flow equation in Mode II, i.e, by solving the following equations:

$$2MD_\phi = \ (M-1)D' \tag{22}$$

$$P = \ CD^2(1 - 2D_\phi). \tag{23}$$

*2) Zone 2 (Medium Power - $P_{\text{crl}} < P < P_{\text{cru}}$):* For operation above $P_{cr(l)}$, in general, feasible solutions exist in both Mode I and II, provided the power is less than the maximum

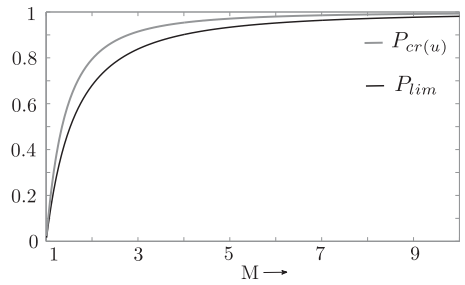


Fig. 11. Comparison of $P_{cr(u)}$ and $P_{\rm lim}$ (normalised with respect to the maximum power). Note that $P_{cr(u)} > P_{\rm lim}$ always.

possible power in Mode II, $P_{m2(\max)}$, which is $C/27$. However, as detailed in Section III, a solution in Mode II always has a higher rms value of current than the corresponding solution in Mode I for the same $D$. Thus, for minimizing rms current above $P_{cr(l)}$, the converter is to be operated in Mode I. Further, it can be observed from Fig. 10 that above a certain power in Mode I (referred to as $P_{cr(u)}$), the ZVS condition is always satisfied. This power level is equal to the maximum value of power in Mode I corresponding to ZVS boundary operation and is given by

$$D_{cr(u)} = (3M-1)/(6M) \tag{24}$$

$$P_{cr(u)} = C[(M-1)/2M][(3M+1)/6M]^3. \tag{25}$$

Operation below $P_{cr(u)}$ implies the ZVS constraints are active and like before the optimal solutions can then be obtained by simultaneously solving the ZVS boundary condition and the power equation of Mode I, i.e,

$$2MD_\phi = (M-1)D' \tag{26}$$

$$P = CD_\phi(2DD' - D_\phi). \tag{27}$$

*3) Zone 3 (High Power - $P > P_{\rm cru}$):* For operation above $P_{cr(u)}$, the ZVS constraint is no longer binding and hence the optimization problem has an equality constraint only. The problem in this power range thus reduces to the same one discussed in Section V-A. Fig. 11 shows the plot of $P_{cr(u)}$ and $P_{\rm lim}$ for different values of $M$, from which it is seen that $P_{cr(u)} > P_{\rm lim}$ always. This implies that the solution of the equality-constraint minimization problem for $P > P_{cr(u)}$ will be $D = 0.5$. The conclusions of the foregoing discussion can be used to develop the complete algorithm for operating the DAHB under ZVS while minimizing the transformer rms current. This is represented in the flowchart of Fig. 12.

Theoretically predicted trajectories of the control variables $(D, D_\phi)$ for the two optimisation strategies are shown in Fig. 13. These plots correspond to the system specifications listed in Table VI, for which $P_{\rm lim} = 0.68$ p.u and $P_{\rm cru} = 0.79$ p.u. From Fig. 13(a), it can be observed that for powers below $P_{\rm lim}$, the minimum current trajectory (MCT) for OPC operation follows a curved path, which is governed by (15). Above $P = P_{\rm lim}$, the MCT coincides with the $D = 0.5$ line (SPC). More interestingly, most of the MCT below $P = P_{\rm lim}$ corresponds to

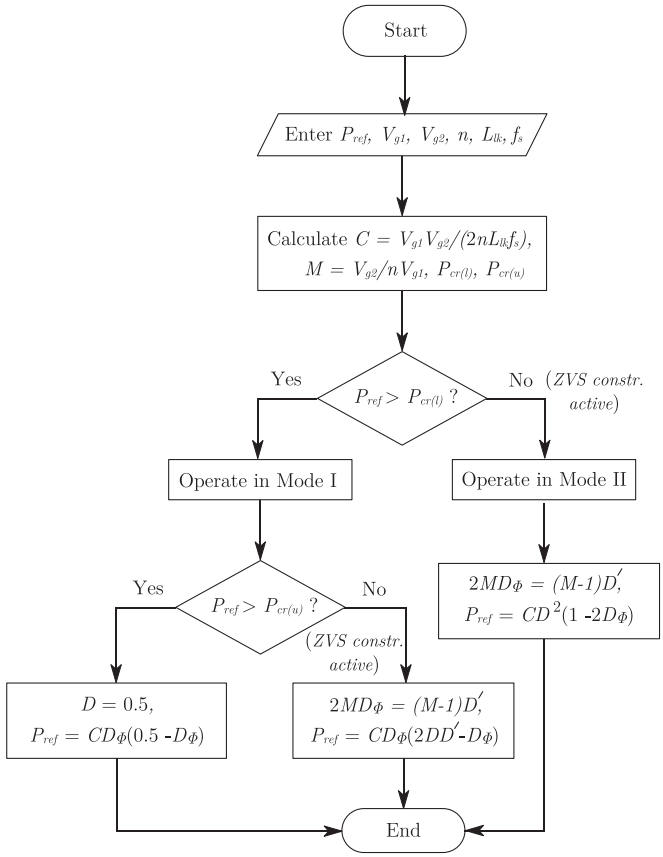


Fig. 12. Algorithm for minimum transformer rms current operation while ensuring ZVS for positive power flow.

hard-switched operation. For OPCZ control, the MCT for zones 1 and 2 coincide with the ZVS boundary, as Fig. 13(b) illustrates, while above $P = P_{\rm cru}$, the MCT follows the SPC trajectory.

### C. Closed-Loop Implementation

The simplest way of operating the converter with closed-loop optimal control is to calculate offline the optimal values of $D$ and $D_\phi$ (under different operating conditions) and store these data points in the truth-table of a digital controller [29]. An alternative closed-loop implementation strategy, similar to the one discussed in [31], utilizes knowledge of the relationship among the control variables under optimal operating condition. Block diagrams of the implementation strategies for the two schemes are shown in Figs. 14 and 15. The phase-shift $D_\phi$ is adjusted by a PI controller to deliver the desired amount of power $P_{\rm ref}$. For the OPC scheme, using (15), the reference value of $D$ can be expressed in terms of $D_\phi$ as

$$D = \frac{1-\sqrt{1-4\alpha}}{2} \tag{28}$$

where $\alpha = D_\phi((3b/2a)D_\phi + 1)$. Similarly, for OPCZ, reference value of $D$ can be calculated from (26). The duty-ratio $D$ is then adjusted by another slower control loop to match this reference and ensure optimal current operation under steady state.

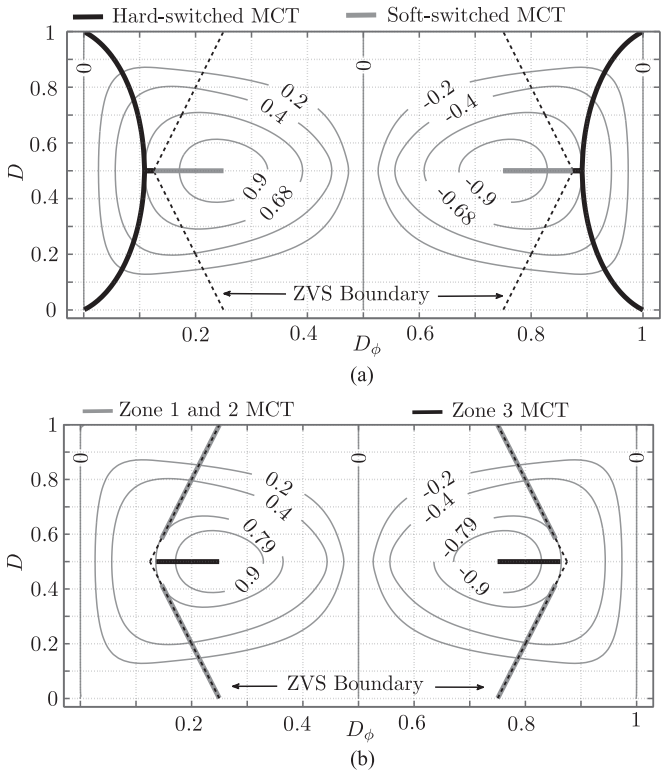


Fig. 13. Minimum current trajectories (MCT) on the $D$-$D_\phi$ plane for the OPC and OPCZ strategies. The normalised constant power contours are shown by the light grey curves. The soft-switched region is on the inner side of the ZVS boundaries. (a) OPC. The trajectory follows $D = 0.5$ for $P$ greater than $P_{\rm lim}$ ($= 0.68$) and is hard-switched at lower powers. (b) OPCZ. The trajectory lies on the ZVS boundary for $P < P_{\rm cru}$ ($= 0.79$) and on the $D = 0.5$ line for $P > P_{\rm cru}$.

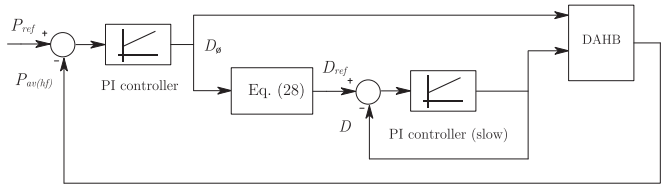


Fig. 14. Closed-loop implementation strategy of OPC control below $P = P_{\rm lim}$. Above $P = P_{\rm lim}$, SPC is adopted.

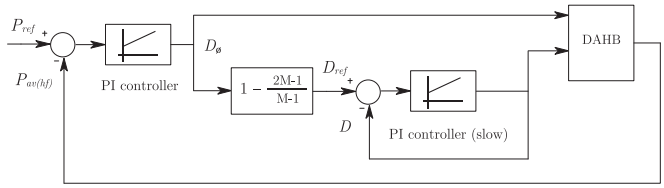


Fig. 15. Closed-loop implementation strategy of OPCZ control below $P = P_{\rm cru}$. Above $P = P_{\rm cru}$, SPC is adopted.

### D. Validation of the Proposed Algorithms

In order to verify the theoretical predictions of Sections V-A and V-B, two numerical optimization approaches have been used. The first of these approaches is a brute-force method, which numerically finds the optimal values of $D$ and $D_\phi$ for any given power, by performing an extensive search over the entire decision space. A second approach directly uses the MATLAB function "fmincon," commonly used for finding numerical solutions of constrained optimization problems. Both techniques lead to exactly identical solutions of the control variables and also show excellent match with the mathematically predicted trajectories, as Fig. 16 illustrates. For instance, for the system specifications of Table VI, the power limits for OPCZ operation are calculated as $P_{cr(l)} = 240$ W and $P_{cr(u)} = 493$ W. As Fig. 16(b) illustrates below 240 W, $D_\phi > D$, indicating that the optimal solution with ZVS lies in Mode II. Similarly, between 169 and 493 W, the OPCZ trajectory lies in Mode I ($D_\phi < D$) and above 493 W, the optimal solution corresponds to operation with $D = 0.5$.

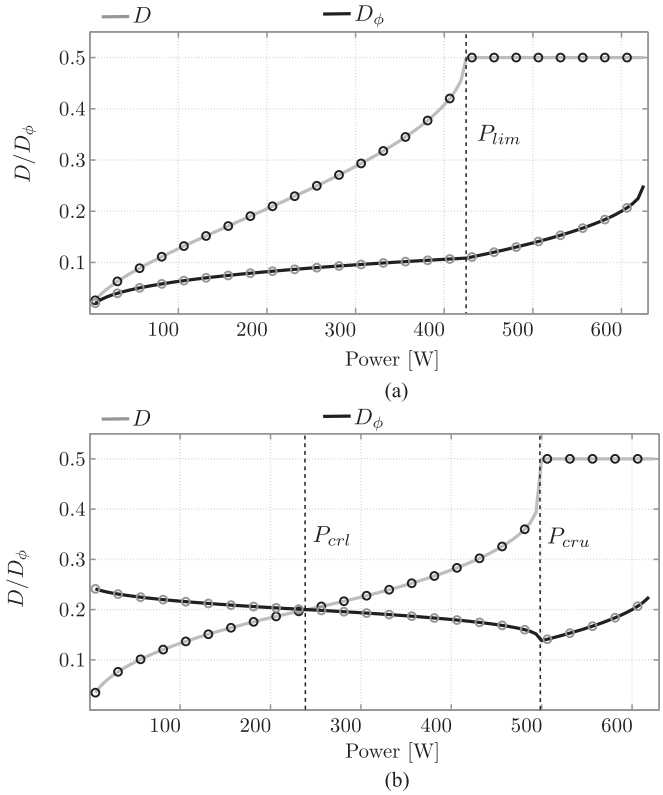


Fig. 16. Trajectories followed by the control variables for the two optimization schemes. The solid curves correspond to theoretical prediction. Numerical solutions computed at discrete power levels are marked by "o." (a) Optimal phase-shift control without ZVS. (b) OPCZ.

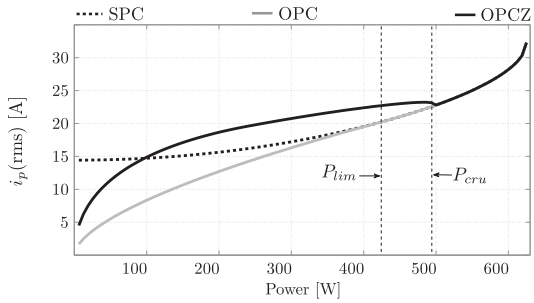


Fig. 17. Comparison of rms currents of the three control strategies obtained from simulation.

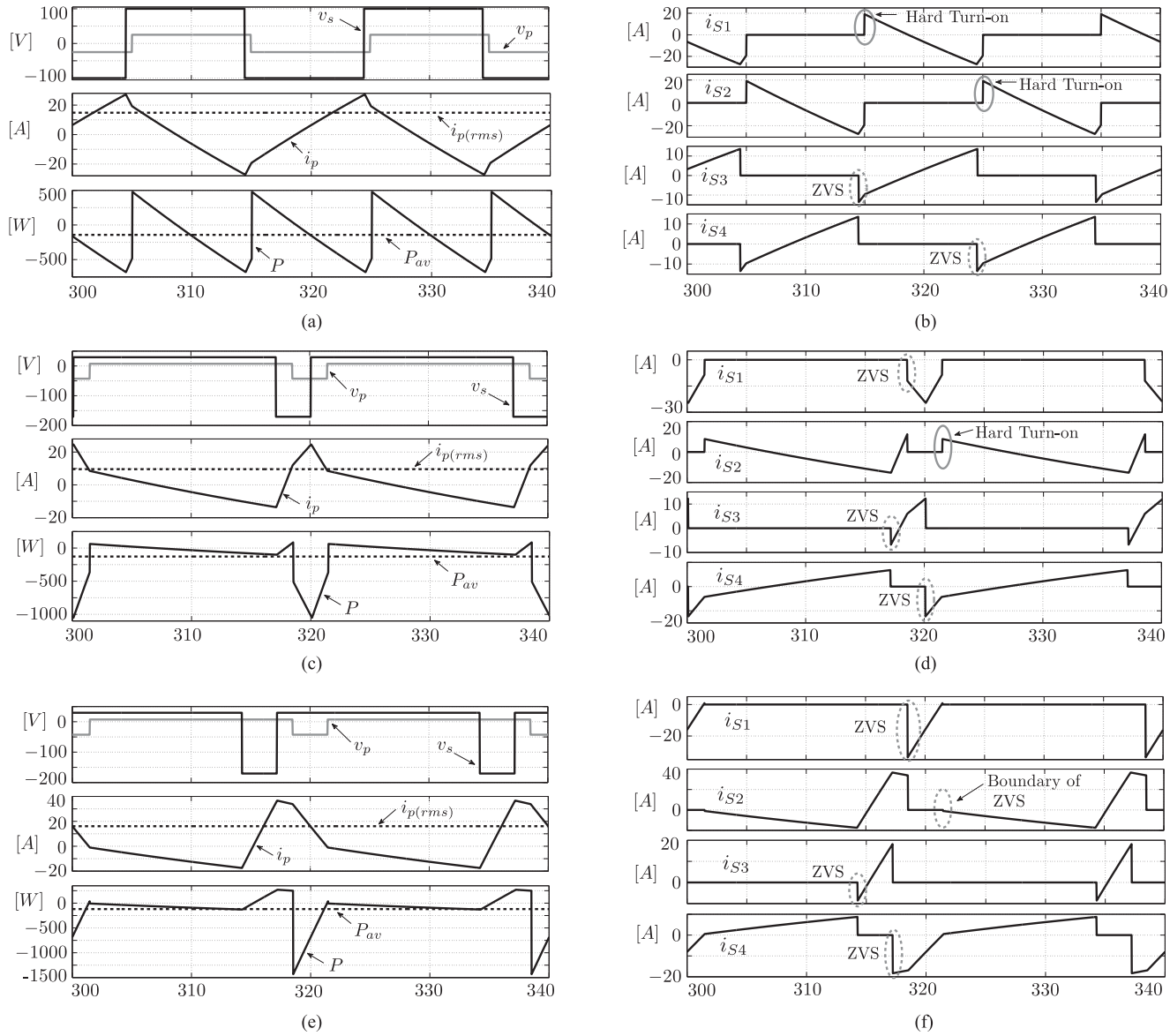


Fig. 18. Simulation results comparing the three modulation strategies at 127 W power (zone 1 operation). Time scale : 10 $\mu$s/div. The rms current of the OPC strategy is the least but it cannot ensure ZVS operation of one of the LV devices. The OPCZ algorithm achieves ZVS turn-on of all devices at the cost of increased RMS current. (a) SPC: $D = 0.5$, $D_\phi = 0.026$; $i_{p(\text{rms})} = 14.88$ A. (b) SPC: Hard turn-on of $S_1$ and $S_2$ (both LV side switches). (c) OPC: $D = 0.1469$, $D_\phi = 0.0687$ (Mode I); $i_{p(\text{rms})} = 9.54$ A. (d) OPC: Hard turn-on of $S_2$ (top switch on LV side). (e) OPCZ: $D = 0.1476$, $D_\phi = 0.213$ (Mode II); $i_{p(\text{rms})} = 16.1$ A. (f) OPCZ: ZVS turn-on of all devices.

## VI. Simulation Results

A simulation model of the circuit with parameter values mentioned in Table VI has been developed in MATLAB Simulink. Key waveforms for operation with each strategy at a power level of 127 W (20% of the maximum power) are shown in Fig. 18. Since the value of $P_{cr(l)}$ for the operating condition is around 240 W, the chosen power reference of 127 W corresponds to operation in zone 1. As Fig. 18(a) and (b) illustrate, the OPC strategy reduces rms current in comparison to SPC by about 5 A. However, as can be observed from Fig. 18(b) and (d), both strategies miss ZVS. While for SPC both LV side switches fail to undergo ZVS, for OPC the top device on the LV side (as predicted from theory for power flow from LV side to HV side) undergoes hard turn-on. Occurrence of hard-switching of $S_1$ and of $S_2$ for SPC and $S_2$ for OPC can be inferred by observing that the switch current waveforms abruptly jump to a positive value at turn-on. In contrast, as Fig. 18(f) shows, for the OPCZ scheme, both LV side devices achieve ZVS since the switch currents go in the negative direction after the switches start conduction. This indicates that the output capacitances of the switches are discharged after which their body-diode starts conduction, when the devices can be turned on with ZVS. Though the OPCZ strategy ensures ZVS of both devices, it results in considerably higher rms current (16.1 A) compared to OPC, as can be seen from Fig. 18(e). It can be noticed that, as predicted by analysis, operation for the OPC and OPCZ schemes are in modes I and II,

TABLE X
COMPONENTS USED IN THE HARDWARE PROTOTYPE

| Component | Specification | Part no. |
|---|---|---|
| $S_1 - S_2$ | 200 V, 10.7 mΩ | IPP110N20NAXK |
| $S_3 - S_4$ | 550 V, 140 mΩ | IPW5OR140CP |
| $C_1, C_2, C_3, C_4$ | 20 $\mu$F, 500 V | MKP1848C62050JP4 |

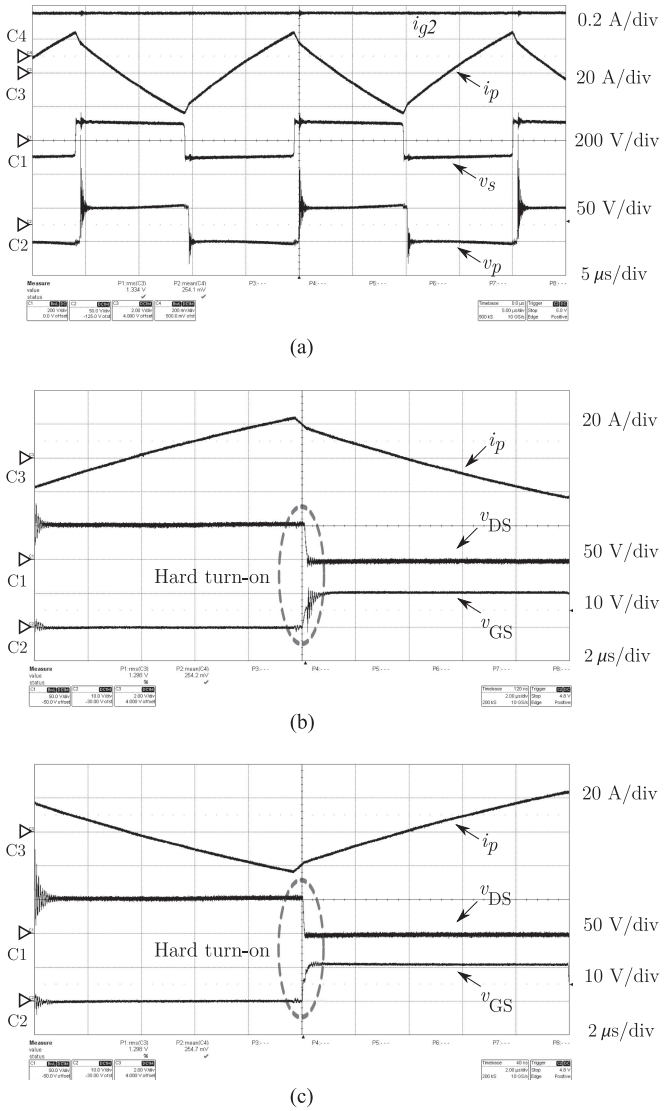


Fig. 19. Experimental waveforms for SPC at 127 W. $D = 0.5$, $D_\phi = 0.026$ and $i_{p(\text{rms})} = 13.3$ A. (a) SPC : Transformer voltages ($v_p$, $v_s$), primary current ($i_p$) and LV side output current ($i_{g2} = 2.54$ A). (b) SPC : Hard turn-on of $S_2$ (top switch on LV side). (c) SPC : Hard turn-on of $S_1$ (bottom switch on LV side).

respectively. Furthermore, as Fig. 18(f) shows, operation with OPCZ lies on the ZVS boundary, as indicated by the current through the ZVS-critical device $S_2$ gradually starting from zero at its turn-on.

A comparison of the rms current values of the three control strategies is shown in Fig. 17, obtained by performing simulations at different points across the power range of the converter is carried out to obtain. Clearly, the OPC strategy

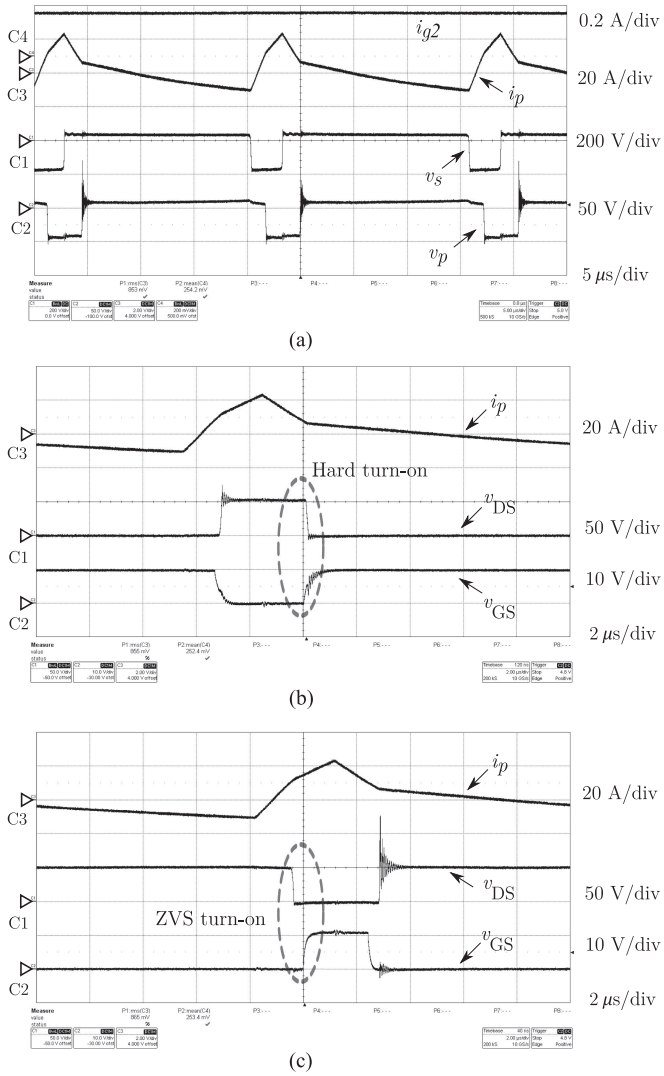


Fig. 20. Experimental waveforms for OPC at 127 W. $D = 0.147$, $D_\phi = 0.0687$ and $i_{p(\text{rms})} = 8.5$ A. (a) OPC : Transformer voltages ($v_p$, $v_s$), primary current ($i_p$) and LV side output current ($i_{g2} = 2.54$ A). (b) OPC : Hard turn-on of $S_2$ (top switch on LV side). (c) OPC : ZVS turn-on of $S_1$ (bottom switch on LV side).

provides advantage of operation with reduced rms current compared to SPC and OPCZ. Since this reduction is much more pronounced at low loads, the OPC strategy significantly improves the light-load efficiency of the converter compared to SPC control.

## VII. EXPERIMENTAL RESULTS

A 625 W prototype of the converter, with specifications listed in Table X, has been built and tested to verify the discussed ideas experimentally. A 60-V dc electronic load (Prodigit make) is operated in constant-voltage mode to mimic the low-voltage dc port ($V_{g1}$) while the main power is drawn from a 300 V power supply. PWM logic signals for the MOSFETs are generated using a Xilinx Spartan 3-based FPGA control card (XC3S200). The operating voltages and switching frequency of the converter are same as mentioned in Table VI, i.e, 200 V on the HV side, 50 V on the LV side, and $f_s = 50$ KHz. The transformer's turns-ratio

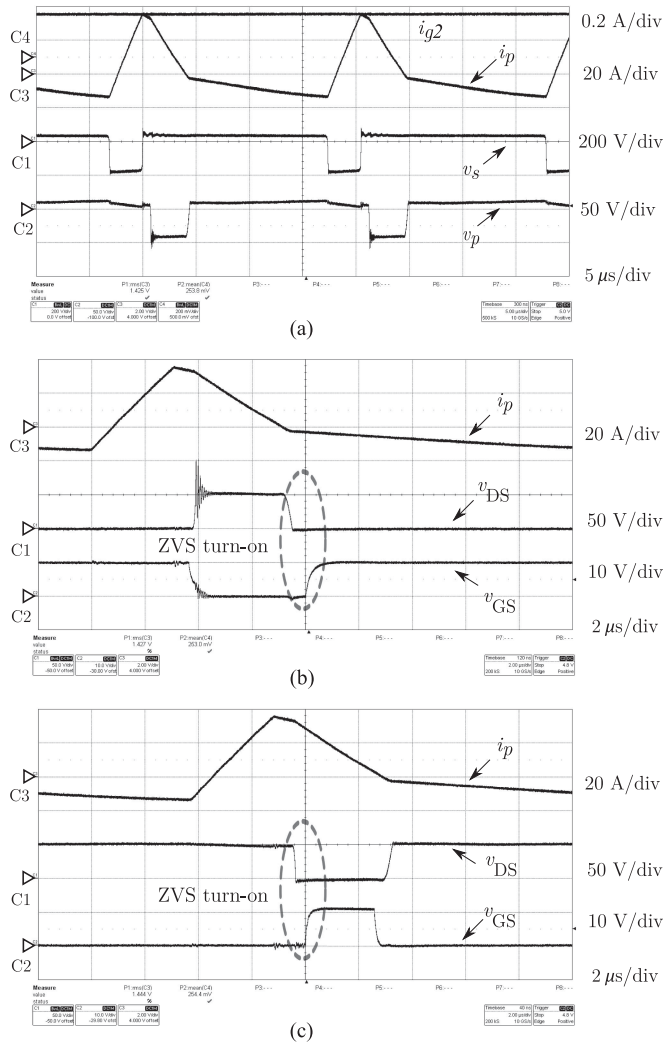


Fig. 21. Experimental waveforms for OPCZ at 127 W. $D = 0.148$, $D_\phi = 0.2131$ and $i_{p\,(\mathrm{rms})} = 14.2$ A. (a) OPCZ : Transformer voltages ($v_p$ , $v_s$), primary current ($i_p$) and LV side output current ($i_{g2} = 2.54$ A). (b) OPCZ : ZVS turn-on of $S_2$ (top switch on LV side). (c) OPCZ : ZVS turn-on of $S_1$ (bottom switch on LV side).

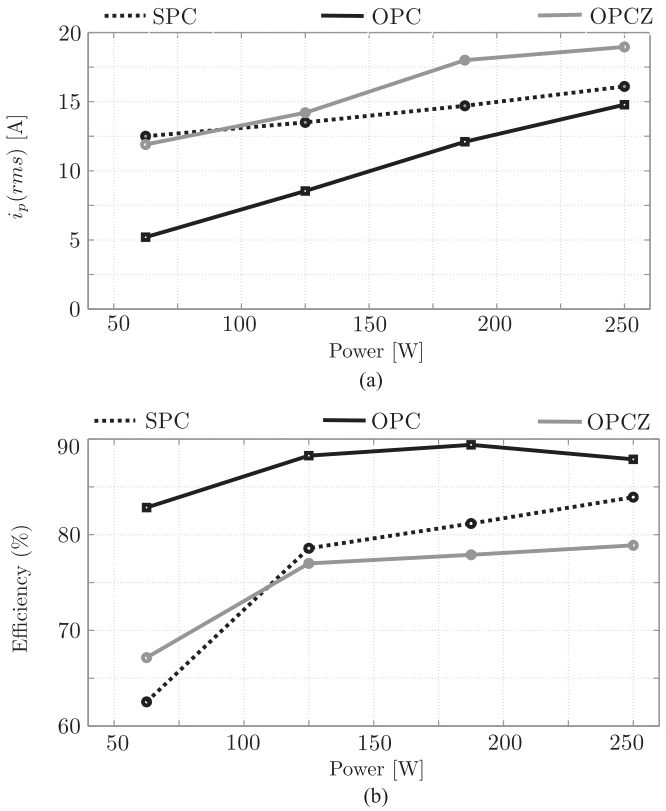


Fig. 22. Comparison of experimentally measured rms current and efficiency of the three schemes under light-load conditions. (a) RMS current. (b) Efficiency.

is 2:1. An external inductance of 20 $\mu$H put in series with the transformer secondary (HV side) serves as the effective leakage inductance since the transformer's inherent leakage inductance is measured to be very small (about 1 $\mu$H). The leakage inductor and transformer windings are constructed with several parallel thin wires (32 AWG) to reduce skin and proximity effects. The resistances of the windings at 50 KHz are measured to be 25 m$\Omega$ for the leakage inductor and 40 m$\Omega$ on LV side for the transformer.

Experimental results comparing the three modulation strategies at the same operating condition as the simulation results of Fig. 18 are shown in Figs. 19–21. As can be observed, values of the experimentally obtained rms current for the three schemes show reasonably good match with those obtained from simulation. Switching waveforms across each device are also shown, which agree with the hard-switching/ZVS predictions of analysis and simulation.

A high-frequency ringing can be observed for the OPCZ case on the gate and drain waveforms of the top device ($S_2$) at its turn-off transition. The source of this ringing is the energy trapped in the parasitic inductance of the switching leg, which resonates with the MOSFETs' output capacitances [38]. As the top device switches OFF at higher current compared to the bottom device, this ringing is much more pronounced at its turn-off transition. It is possible to mitigate this ringing by slowing down the turn-off of $S_2$ by increasing the corresponding gate-resistance. However, such arbitrary slowing down of the turn-off transition would lead to loss of fidelity of the duty-ratios and hence deviation from optimal operating condition.

Experimentally obtained rms current and efficiency figures for the three schemes are depicted in Fig. 22. Since the advantages offered by the optimal schemes are more pronounced under light-load conditions, results till 40% of maximum power are compared. It can be observed that the rms current values closely match with the simulation results of Fig. 17. The OPC scheme is found to offer the best efficiency at all powers, while except very low powers (below 10%), the OPCZ strategy has efficiency poorer than SPC.

In order to understand this better, a detailed loss breakdown of the three schemes at 127 W power is shown in Fig. 23, from which two key observations can be made. First, the increased conduction loss of the OPCZ scheme can be identified as the root cause behind its low efficiency. Second, it can be noted that

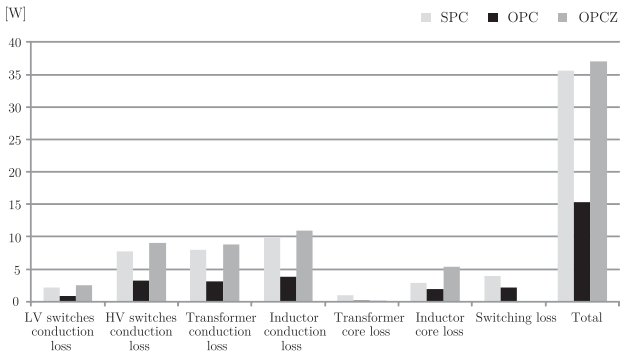


Fig. 23. Breakdown of losses incurred for the three schemes at 125 W.

the switching losses of SPC and OPC schemes are much lower compared to their conduction losses.

In summary, the benefit of attaining ZVS of both LV switches in the OPCZ scheme is offset by its increased conduction losses. However, as discussed in [31], in a different design, where the conduction losses and switching losses are close to each other, the benefit of the OPCZ scheme would be more clearly accentuated. Such design changes include selection of better high-frequency winding (such as Litz wire), operation at higher voltages (resulting in reduced transformer rms currents at the same power) or higher switching frequency operation.

## VIII. Conclusion

A comprehensive analysis of the steady-state behaviour of DAHB converters operated using a two degree of freedom based control is presented in this paper. Based on knowledge derived from the analysis, two control strategies are developed which minimise transformer rms current at a given power with and without ZVS. It is theoretically proven that for converters operating with unity effective voltage conversion ratios ($M$), simple square wave control (SPC) results in the least rms current throughout the power range while also ensuring ZVS operation. The same is also shown to be true at higher powers (above $P_{\mathrm{cru}}$) even for converters with nonunity $M$. However, in converters with $M \neq 1$, SPC results in considerably more rms current and loss of ZVS operation at low powers. Under such light-load conditions for converters with nonunity value of $M$, the proposed OPC strategy results in considerable reduction of rms current, though it still misses ZVS. The OPCZ strategy can ensure ZVS of all devices, albeit with higher rms current. Thus the proposed optimisation strategies potentially offer significant efficiency improvements over simple square-wave control. The theoretical framework is verified using numerical optimisation techniques, MATLAB Simulink-based simulations and finally through experimental tests on a 625 W laboratory prototype operating with $M = 2$. A natural extension of the work is to adopt a three degree of freedom based control approach, where the duty-ratios of the bridges are different, in order to further improve converter performance.

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