Generation of the Large DC Gain Step-Up Nonisolated Converters in Conjunction With Renewable Energy Sources Starting From a Proposed Geometric Structure

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***Abstract*—A very simple geometric structure whose branches can be filled by inductors, capacitors, diodes, short-circuits, or open-circuits is proposed. It serves for generating large dc gain-purposed switching cells by making different choices of the type of component on each branch. The switching cells are integrated in basic converters. It is shown that almost all the high dc gain nonisolated converters based on switched-capacitor-inductor cells proposed in the last years, regardless of their complexity, can be derived through this method. From the same geometric structure, new high dc gain boosting converters can be derived in a systematic manner. The available and the new converters in each class as defined by the number of reactive components are compared in terms of their performance: dc gain, semiconductor elements count, voltage and current stress on transistors and diodes, character of the input current, easiness of the transistor driving, and easiness of the control as determined by common/uncommon line-load ground, power stage efficiency. This comparison allows us to choose the optimal solution for each specific application in conjunction with the green sources of energy, multisource microgrids, electric vehicles, data and communications systems, and so on. The geometric structure is generalized in different ways, allowing for the development of ultrahigh dc gain converters. One of the proposed generalized ultrahigh dc gain converters is fully analyzed and built in the laboratory, with the experimental results verifying the theoretical analysis.**

***Index Terms*—High step-up dc gain converters, switched-capacitor cell, switched-inductor cell, large dc gain converter systematic derivation, switched-capacitor-inductor cell.**

I. Motivation

THE last decade saw a rapid development of the environment-friendly sources of energy with the purpose to reduce the world dependency on the classical polluting and depletable resources of energy. However, the renewable power generation units are variable in nature: the output of a solar cell varies with the insolation, of a wind cell with the weather and of a fuel cell with the age or chemistry conditions. For being useful as front-end of the electrical grid, the voltage generated by the renewable sources has to be stabilized, as the customers are highly dependent on uninterruptible, high quality power supply. The voltage supplied by the green energy sources is also too low to be used as such. Even in grid connected applications, multiple series–parallel PV arrays for increasing the voltage are not always chosen due to safety issues, parasitic capacitance effects, and module mismatch. And, in local microgrids, isolated solar cells are preferred. The implication is that each cell has to be followed by a converter that is able to step-up the voltage by several times. It is highly desirable for the power electronics circuit to absorb a nonpulsating current in order to prolong the life of the clean source of energy.

In hybrid electric vehicles, low voltages of 14 or 42 V from batteries or fuel cells have to be raised to hundreds of volts. Data and telecommunications applications use a 400 V dc distribution system, converters able to raise the standard backing battery 48 V to 400 V to being necessary.

The simplest answer for a voltage step-up circuit is the boost converter. However, it would have to operate with an extreme large duty-cycle to get a larger dc gain. The increased voltage stress on its switches would seriously affect the efficiency, and in any case, a boost converter cannot provide a very steep voltage gain [1]. Any transformer-based or coupled-inductor based solution would affect the efficiency and size of the converter (the switch voltage stress is increased by ringing between the parasitic capacitance of the switch and the leakage inductance at switch turn-off, requiring snubbers) [2]. Cascade of converters has to be avoided in order to maintain a high efficiency.

The switched-capacitor converters present a theoretical unlimited dc gain, which can be increased by increasing the number of the capacitors. So, they would be the ideal solution for very large dc gain converters. However, the input current is very pulsating, rendering them less suitable for the use in conjunction with the green energy cells. [3]–[12].

More recently, another idea became predominant: defining step-up noncontrolled switched-capacitor-inductor structures and integrating them in a classical boost/modified boost stage

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for getting hybrid very high dc gain converters [13]. A quite large number of papers have been published in the last years containing different proposals of hybrid nonisolated large dc gain converters [14]–[42].

In this work, the term "large/high dc gain" converter will be used for all those converters with a dc gain up to that of the quadratic stage (for a typical nominal duty-cycle of 0.75, the ideal dc gain of a large/high gain converter would be up to 16). For higher dc gain converters, obtained from example by using a generalized structure, the term "ultrahigh" dc gain converters will be used.

The purpose of this paper is to present a way of developing such converters starting from a generic geometric structure. This approach does not only allow for the re-discovery of almost all the published solutions, but permits the proposal of new topologies. It also gives the possibility of generalizing each structure, from a simple one containing just three reactive elements (including the inductor and capacitor of the classical boost stage) to a complex one with *n* reactive elements for getting ultrahigh dc gains. Due to space limitations, cells containing coupled-inductors are not included in this work.

The generic structure of the noncontrolled inductor-capacitor switched cell is proposed in Section II. Then, different geometric possibilities for generalizing it are discussed. Sections III, IV, and V analyze hybrid large dc gain converters containing three, four, and five reactive elements, respectively. Available and new converters that have been generated in each class will be compared in terms of their performances (dc gain, diodes and transistors count, voltage and current stresses on switches, character of the input current, easiness of transistor driving, easiness of control as determined by common/uncommon line-load ground, etc.). In order to compare in a fair way the dc gain of different converters, one has to consider only the converters in the same class as defined by the number of their reactive elements: it is normal that each additional inductor or capacitor increases the dc gain. This is why, the converters have been classified in three-, four-, and five-reactive components based converters. Section VI comprises a number of rules for deriving the switched cells such that to avoid fault cases or for optimizing the performances. Then, a number of examples follow to show the application of these rules. Generalized structures will make the subject of Section VII. One of the proposed generalized converters will be analyzed and designed in detail, with experimental results and comparison with available solutions in Section VIII, and finally Section IX conclude.

II. Proposed Generic Geometrical Structure and Its Generalization

In Fig. 1, the very simple geometric structure which can generate all the noncontrolled switched-capacitor-inductor cells is proposed. It contains seven branches. On a branch a single component (inductor, capacitor, or diode) can be placed. Some of the branches can be short-circuits and others open-circuits. Depending on the number of the reactive elements used in this structure, one gets different classes of high dc gain converters when the passive switched-capacitor-inductor cell is placed within a boost converter. Sometimes, the boost inductor or boost output capacitor or output diode can become redundant because their role is taken by elements within the switched-capacitor-inductor cell. In such a case, the redundant element can be removed. The switched-capacitor-inductor cell comprises as particular cases the switched-capacitor (only capacitors and diodes) and switched-inductor (only inductors and diodes) cells.

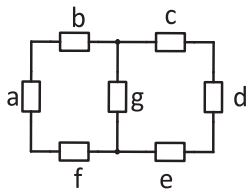

Fig. 1. Basic generic geometrical structure for getting passive switched-capacitor-inductor cells.

The basic structure can be generalized in different ways. For getting ultrahigh dc gain-purposed switched-capacitor-inductor cells, the generalization ways shown in Fig. 2(a)–(d) have been found as most adequate. By connecting basic switched-capacitor-inductor cells of the same type according to these generalized geometric structures, and inserting the obtained circuit in a boost converter, the ultrahigh dc gain converters are obtained. Another possibility is to combine different types of basic switched-capacitor-inductor cells in the same generalized geometric structure.

1) *The first generalization way [see* Fig. 2*(a)]:* One starts by combining two cells [see Fig. 2(a_1)]: branch 2b of the second cell is superimposed on branch 1b of the first cell. The third cell is then added (note that such a generalization method is suitable for cells where branches c, d, and e are open-circuits; or, a similar way of generalization if a, b, and f are open-circuits) as in Fig. 2(a_2) by superimposing branch 3g of the third cell on branch 2g of the second cell. Branches 3a, 3b, 3f take the place of the open-circuits 2c, 2d, and 2e. The fourth cell is added in the same way as we added the second cell, i.e., by superimposing branch 4b on 3b, like in Fig. 2(a_3). The fifth cell is added as the third cell was added, and so on.
2) *Second way of generalization [see* Fig. 2*(b)]:* One proceeds by superimposing branch 2e of the second cell on branch 1b of the first cell (this generalization way is suitable for the switching cells where on branches b and e there are placed the same type of elements, i.e., inductors, or capacitors, or diodes, or short-circuits, or open-circuits; or, a similar way of generalization if on f and c are placed elements of the same type)—Fig. 2(b_1). The third cell comes with 3e superimposed on 2b—Fig. 2 (b_2), the fourth cell comes with 4e superimposed on 3b, and so on.
3) *The third generalization way [see* Fig. 2*(c)]*: To get it, branch 2e of the second cell is superimposed on branches 1b, 1c (this way of generalization is suitable for switching cells in which branch e is an open-circuit. Or, a similar generalization, if c is an open-circuit, or b is an open circuit, or f is an open circuit)—Fig. 2(c_1), the

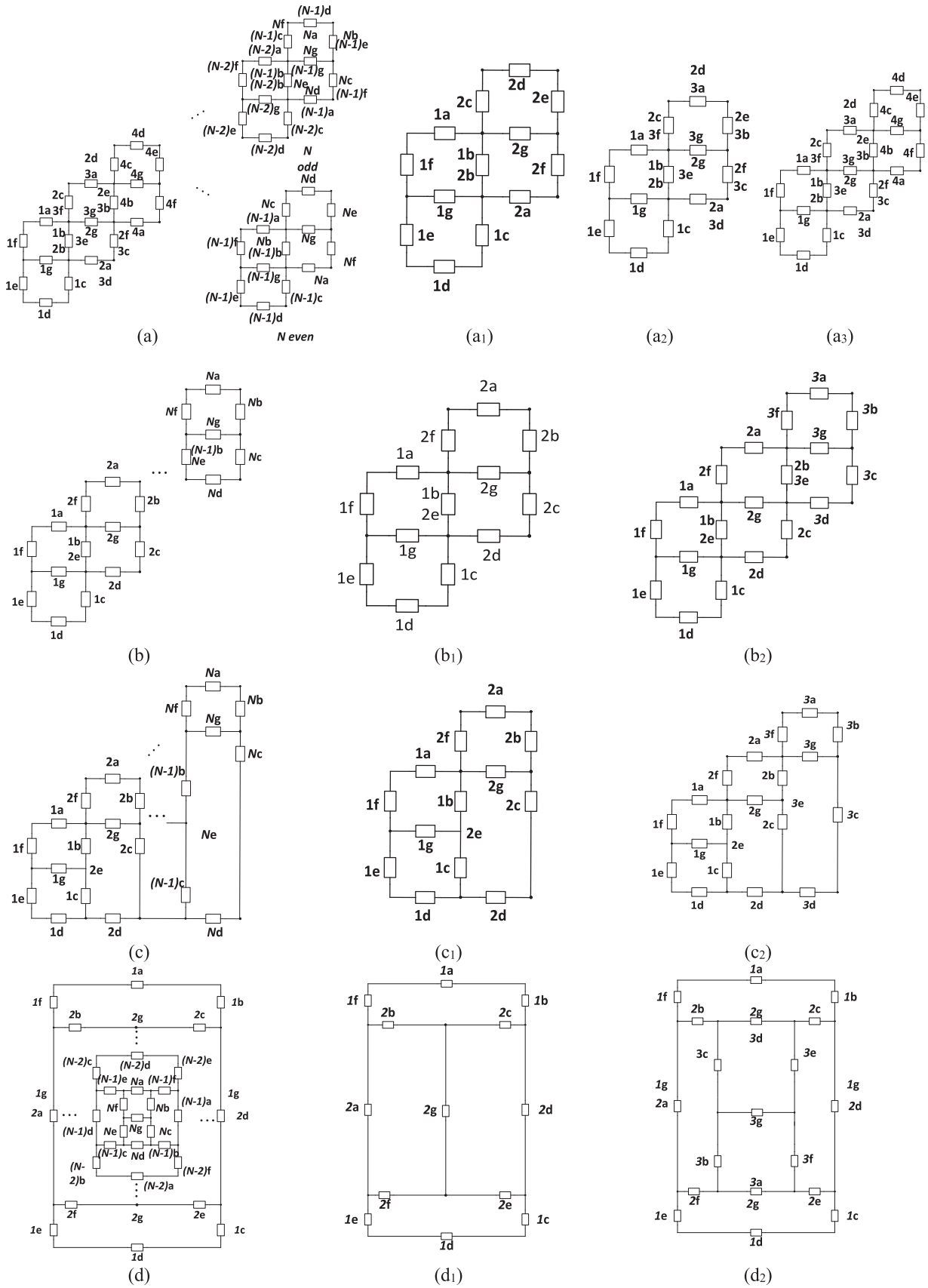

Fig. 2. Possible generalizations of the basic structure for getting ultrahigh dc gain-purposed switched-capacitor-inductor cells. (a) First generalization way and (a_1)–(a_3) its first steps; (b) second generalization way and (b_1) and (b_2) its first steps; (c) third generalization way and (c_1) and (c_2) its first steps; (d) fourth generalization way and (d_1) and (d_2) its first steps.

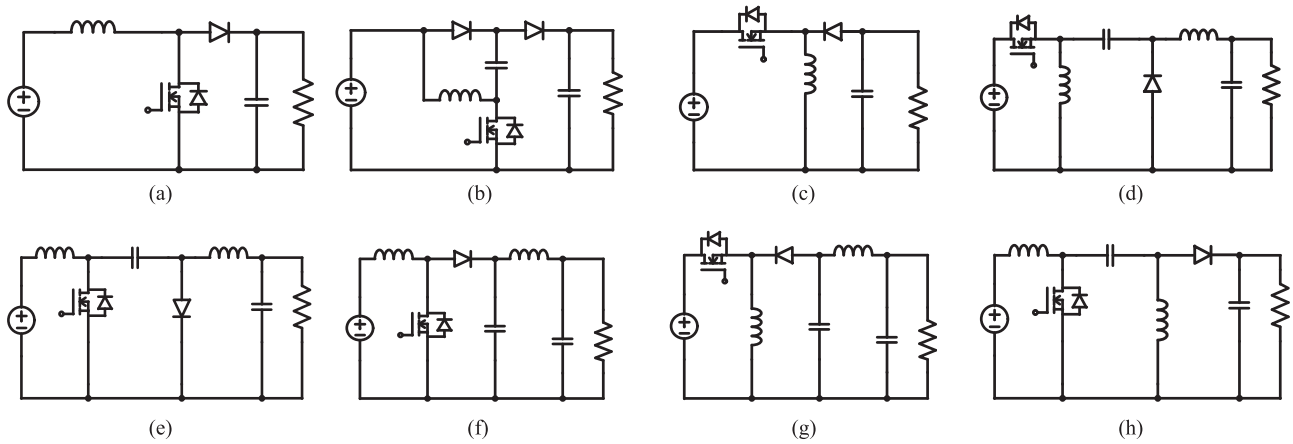

Fig. 3. Basic converters used for inserting passive switching cells. (a) Boost converter. (b) Modified-boost converter [14], [15]. (c) Buck-boost converter. (d) Zeta converter. (e) Cuk converter. (f) Boost converter with current sink load. (g) Buck-boost converter with current sink load. (h) SEPIC converter.

TABLE I
DC GAINS OF THE BASIC CONVERTERS OF FIG. 3

	(a)	(b)	(c)	(d)	(e)	(f)	(g)	(h)
DC gain	$\frac{1}{1-D}$	$\frac{2-D}{1-D}$	$\frac{-D}{1-D}$	$\frac{D}{1-D}$	$\frac{-D}{1-D}$	$\frac{1}{1-D}$	$\frac{-D}{1-D}$	$\frac{D}{1-D}$

third cell comes with 3e superimposed on 2b, 2c, and so on—Fig. 2(c_2).

4) *The fourth generalization way:* Fig. 2(d) is obtained as follows: branch 1g of the first cell is replaced by all second cell—Fig. 2d_1 (this way of generalization is suitable for all the switching cells with branch g as an open circuit). Then branch 2g is replaced by all third cell [see Fig. 2(d_2)], and so on.

It will be seen in the following sections that each of the large dc gain-purposed switching cells belongs to at least one of the categories considered above.

III. THREE REACTIVE ELEMENTS BASED HIGH DC GAIN CONVERTERS

The basic converters used by different authors for inserting the switching cells in order to get large dc gain converters are presented in Fig. 3. Table I provides their dc gains. The converter in Fig. 3(b) was at the origin a boost converter, in which a capacitor and a diode were added by the proposers [14], [15], such that to charge the inductor and capacitor in parallel in the on-switching stage, and to discharge them in series, together with the line, to the load in the off-switching stage. The resulting converter provided a larger dc gain than the original boost one, as seen in Table I. An output inductor was added in the converters presented in Fig. 3(f) and (g) by the proposer [16] just to get a nonpulsating output current, without influencing the dc gain. In order to assure a discharging path for the output inductor current in the off-switching stage, a flying capacitor was added in Fig. 3(f) and (g).

After placing two reactive elements (one capacitor and one inductor, two capacitors or two inductors) and diodes on the branches (a)–(g) in Fig. 1 in different ways, and selecting some of the branches as short- or open-circuits, the obtained switched-cells are inserted in either the converter shown in Fig. 3(a) or in Fig. 3(c) in order to get the high dc gain converters containing three reactive elements of Fig. 4(a)–(f). For example, the circuit in Fig. 4(a) was obtained by placing the inductors on branches (b) and (e), the diodes on branches (c), (g), and (f), and replacing branches (a) and (d) by short-circuits. The circuit in Fig. 4(c) is the known hybrid switched-capacitor boost converter. The converters in Fig. 4(a), (b), (e), and (f) have been proposed by previous authors, the converters in Fig. 4(c) and (d) are newly derived directly from the geometrical structure. Rules for placing the components on the branches of Fig. 1 in order to avoid fault topologies or for optimizing the results will be given in Section VI.

When inserting a passive switching cell in one of these basic converters, some of the original components (the input inductor or the rectifier diode or a capacitor) become redundant, their role being taken by elements of the switching cell [13]. This possibility of eliminating the redundant components helps in reducing the complexity of the converter.

Of course, many more possibilities exist by making other choices for the way of filling the branches (a)–(g) of the generic structure by respecting the rules of Section VI.

The six converters of Fig. 4 are compared in Table II in terms of their dc gain, number of diodes, voltage and current stress on the transistor and diodes, position of the active switch, existence of line-load common ground, character of the input current, and theoretical and experimental efficiencies. Of course, in order to compare in a fair way the dc gain, one has to consider only the converters in the same class as defined by the number of their reactive elements: it is normal that each additional inductor or capacitor increases the dc gain. This is why, here, the comparison is made only among converters with three reactive components. In order to fairly compare the efficiency of these converters, each one was implemented in the laboratory for the same input voltage $V_{\rm in} = 20$ V, output voltage $V_o = 100$ V, output power $P_o = 30$ W, and operated with the same switching frequency $f_s = 100$ kHz.

Graphics of the theoretical voltage gain versus duty-cycle, switches voltage stress and switches current stress versus

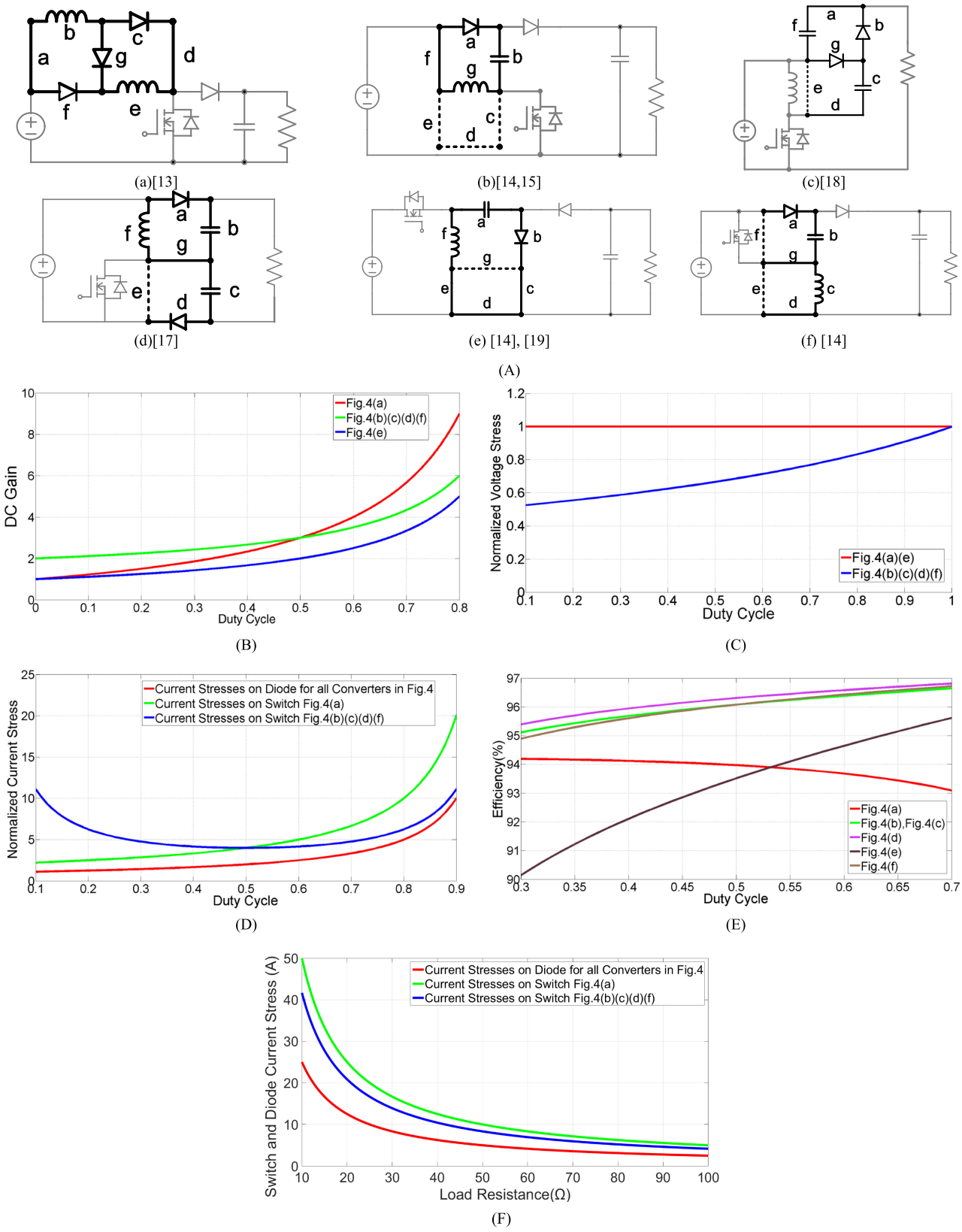

Fig. 4. Three reactive elements based high gain dc converters. (A) Panels (a–d) are derived from basic converter of Fig. 3(a) with the boost inductor replaced by the inductor(s) of the switching cell in (a, b), and the boost output diode–capacitor replaced by the diode and capacitor of the switching cell in (c, d); Panels (e) and (f) are derived from basic converter of Fig. 3(c) with the buck-boost inductor replaced by the inductor of the switching cell. (B) Theoretical dc gain versus duty-cycle. (C) Normalized theoretical voltage stresses (voltage stress over V_o) on switches versus duty-cycle. (D) Normalized theoretical current stresses (current stress over I_o) on switches versus duty-cycle. (E) Efficiency versus duty-cycle. (F) Theoretical current stresses on switches versus load.

TABLE II
COMPARISON OF THE THREE REACTIVE ELEMENTS HIGH DC GAIN CONVERTERS

	Derived from Fig. 3(a)				Derived from Fig. 3(c)	
	Fig. 4(a)	Fig. 4(b)	Fig. 4(c)	Fig. 4(d)	Fig. 4(e)	Fig. 4(f)
DC gain	$\frac{1+D}{1-D}$	$\frac{2-D}{1-D}$	$\frac{2-D}{1-D}$	$\frac{2-D}{1-D}$	$\frac{-1}{1-D}$	$\frac{2-D}{1-D}$
Voltage stress on diodes	V_o	$\frac{V_o}{2-D}$	$\frac{V_o}{2-D}$	$\frac{V_o}{2-D}$	V_o	$\frac{V_o}{2-D}$
Current stress on diodes	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$
Voltage stress on switch	V_o	$\frac{V_o}{2-D}$	$\frac{V_o}{2-D}$	$\frac{V_o}{2-D}$	V_o	$\frac{V_o}{2-D}$
Current stress on switch	$\frac{2I_o}{1-D}$	$\frac{I_o}{D(1-D)}$	$\frac{I_o}{D(1-D)}$	$\frac{I_o}{D(1-D)}$	$\frac{I_o}{D(1-D)}$	$\frac{I_o}{D(1-D)}$
Number of diodes	4	2	2	2	2	2
High/low side gate driver	Low	Low	Low	Low	High	Low
Common ground	Yes	Yes	Yes	No	Yes	Yes
Input current	Nonpulsating	Pulsating	Pulsating	Pulsating	Pulsating	Pulsating
Theoretical efficiency/	94.18%	95.40%	95.40%	95.54%	93.82%	95.47%
Experimental efficiency**	92.9%	94.1%	94.1%	94.3%	92.5%	94.1%

**The efficiency refers to the power stage only. As the purpose was just to compare the converters, all of them have been built under the same conditions, with discrete elements. No optimization was tried. An implementation on PCB board will give a better number for the efficiency of all the converters, but the differences between them will remain the same.

duty-cycle, efficiency versus duty-cycle, switches current stress versus load (the diode with the highest average current stress is considered) are provided in Fig. 4(B)–(F).These graphics can be helpful to the designer in choosing an optimized topology as function of his needs (range of the load in his application, for example), and an optimized nominal duty-cycle by taking into account the dc gain, and voltage and current stresses.

The highest dc gain is obtained by the converter in Fig. 4(a): for a nominal duty-cycle D of 0.75, it is able to ideally step-up the voltage by seven times (compared with a boost converter which would ideally step-up the line by four times for the same nominal duty-cycle). The price is the need for four diodes (two diodes in the other four solutions which would step-up the voltage only by five times for $D = 0.75$) and a larger voltage stress on the transistor and diodes, what decreases its efficiency with about 1%. It is possible to see that an "optimum" converter according to all the criteria does not exist. For each specific criterion, a certain converter can be the best.

IV. FOUR REACTIVE ELEMENTS BASED HIGH DC GAIN CONVERTERS

By "populating" the branches of Fig. 1 with two reactive elements (one capacitor and one inductor, or two capacitors) and 1–4 diodes in different ways, replacing the remaining branches by open-circuits or short-circuits, and inserting the obtained switched-cells in the basic converters of Fig. 2, the high dc gain converters in Fig. 5(a)–(r) are obtained. The solutions in Fig. 5(f)–(h), (j), (k), and (n) have been obtained by inserting a total of three reactive elements on the branches of the generic structure. When inserting the switched cell in a boost or buck-boost converter, the inductor contained in the switched cell made redundant the input inductor of the classical converter. As a result, these solutions have been included in the same class of converters with four reactive components. The converters in Fig. 5(a), (b), and (d)–(r) have been proposed by previous authors, whereas the converter in Fig. 5(c) is newly derived directly from the geometrical structure of Fig. 1.

As said in Section III, many more solutions can be found by making other choices for the branches of the generic structure, by respecting the rules of Section VI, opening the way to many researches looking for viable converters.

All these converters are compared in Table III by looking to the same features as discussed in Section III. The efficiencies of the power stages have been measured in the laboratory under the same conditions as for the converters in Section III. The same graphics as in Section III are given for facilitating a better comparison of the converters when the performances over the duty cycle variation and load variation can be seen.

Among the 18 converters proposed in this class, the "champions" relative to the dc gain are the quadratic converters or their equivalent, see Fig. 5(a), (g), and (h). However, they present the largest voltage stress on the transistor and diodes, resulting in a lower efficiency.

By weighting the dc gain and the voltage stress, the converters in Fig. 5(b)–(e) and (i) appear as the successful solutions for a duty-cycle $D = 0.75$: ideal dc gain of eight times (i.e., the double of the ideal dc gain of a classical boost converter), voltage stress equal to half of the output voltage (compared with the voltage stress on semiconductors equal to the output voltage in boost and quadratic boost). All these solutions make use of three diodes and feature a nonpulsating input current and an advantageous position of the switch, rendering its driving easier. However, only the circuits in Fig. 5(b), (c), and (i) present a line-load common ground, and the circuit in Fig. 5(e) inverses the load voltage polarity. Again, one can see that it is not possible to speak about an optimum converter from the point of view of all the criteria; each designer has to tradeoff the performances according to his application.

V. FIVE REACTIVE ELEMENTS BASED HIGH DC GAIN CONVERTERS

By placing on the branches of Fig. 1 three reactive elements (two capacitors and one inductor, or three capacitors) and 1–3 diodes in different ways, replacing the remaining

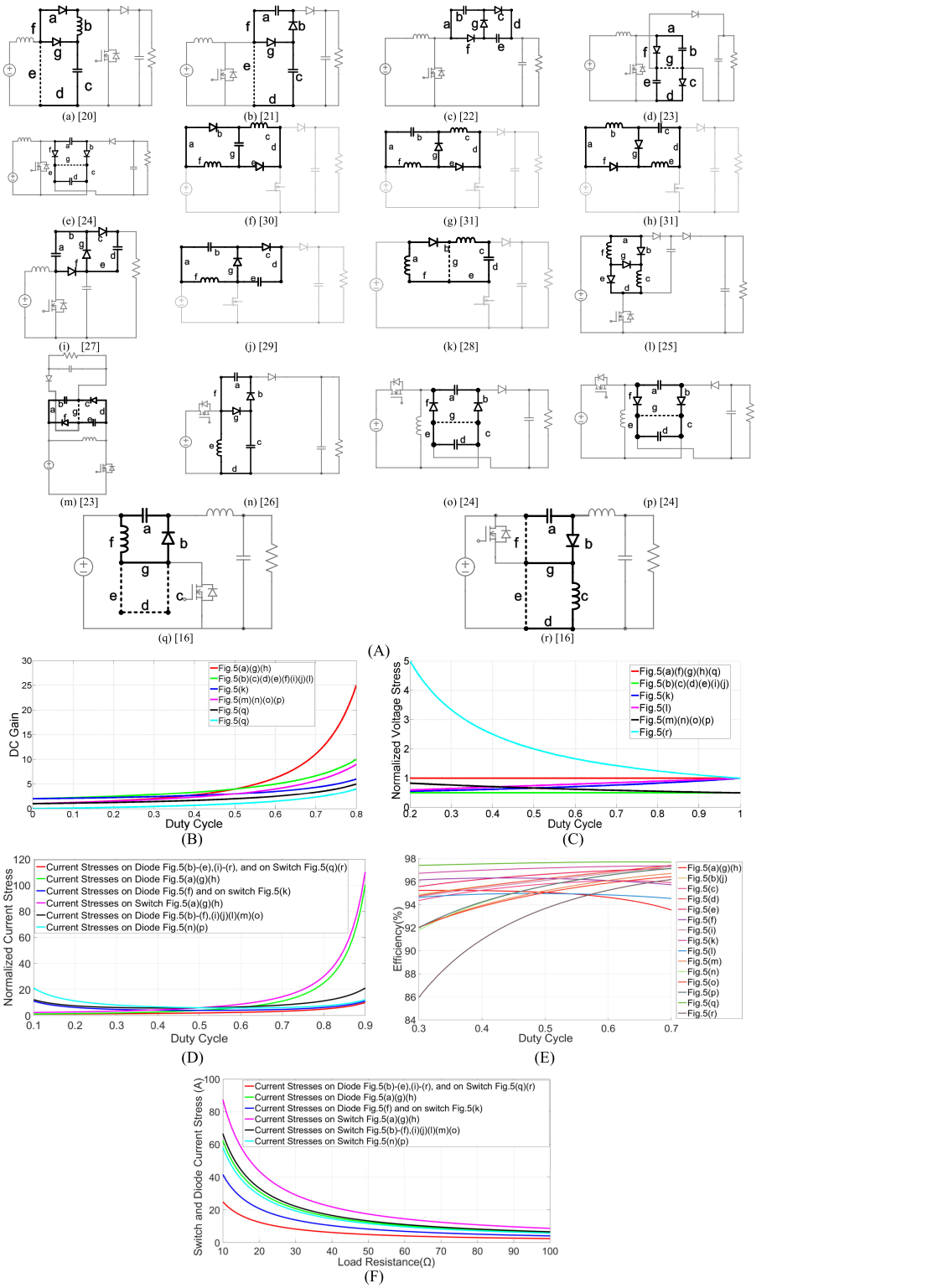

Fig. 5 Four reactive elements based high gain dc converters. (A) Panels (a)–(k) are derived from basic converter of Fig. 3(a), with the boost inductor replaced by the inductors of the switching cell in panels (f–h, (j), and (k), and the boost output diode replaced by the diode of the switching cell in (c, i). Panel (a) can also be seen as derived from Fig. 3(h) with the SEPIC inner inductor and capacitor replaced by the elements of the switched cell. Panel (l) is derived from the basic converter of Fig. 3(b). Panels (m)–(p) are derived from basic converter of Fig. 3(c) with the buck-boost inductor replaced by the inductor of the switching cell in (n). Panel (q) is derived from basic converter of Fig. 3(f) with the boost inductor, diode, and flying capacitor replaced by the elements of the switching cell. Panel (r) is derived from basic converter of Fig. 3(g) with the buck-boost input inductor, output diode, and flying capacitor replaced by elements of the switching cell. (B) Theoretical dc gain versus duty-cycle. (C) Normalized theoretical voltage stresses (voltage stress over V_o) on switches versus duty-cycle. (D) Normalized theoretical current stresses (current stress over I_o) on switches versus duty-cycle. (E) Efficiency versus duty-cycle. (F) Theoretical current stresses on switches versus load.

TABLE III
COMPARISON OF THE FOUR REACTIVE ELEMENTS HIGH DC GAIN CONVERTERS

	Derived from Fig. 3(a)								
	Fig. 5(a)	Fig. 5(b)	Fig. 5(c)	Fig. 5(d)	Fig. 5(e)	Fig. 5(f)	Fig. 5(g)	Fig. 5(h)	Fig. 5(i)
DC gain	$\frac{1}{(1-D)^2}$	$\frac{2}{1-D}$	$\frac{2}{1-D}$	$\frac{2}{1-D}$	$-\frac{2}{1-D}$	$\frac{2}{1-D}$	$\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	$\frac{2}{1-D}$
Voltage stress on diodes	V_o	$\frac{V_o}{2}$	$\frac{V_o}{2}$	$\frac{V_o}{2}$	$\frac{V_o}{2}$	V_o	V_o	V_o	$\frac{V_o}{2}$
Current stress on diodes	$\frac{I_o}{(1-D)^2}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{D(1-D)}$	$\frac{I_o}{(1-D)^2}$	$\frac{I_o}{(1-D)^2}$	$\frac{I_o}{1-D}$
Voltage stress on switch	V_o	$\frac{V_o}{2}$	$\frac{V_o}{2}$	$\frac{V_o}{2}$	$\frac{V_o}{2}$	V_o	V_o	V_o	$\frac{V_o}{2}$
Current stress on switch	$\frac{(2-D)I_o}{(1-D)^2}$	$\frac{(1+D)I_o}{D(1-D)}$	$\frac{(1+D)I_o}{D(1-D)}$	$\frac{(1+D)I_o}{D(1-D)}$	$\frac{(1+D)I_o}{D(1-D)}$	$\frac{(1+D)I_o}{D(1-D)}$	$\frac{(2-D)I_o}{(1-D)^2}$	$\frac{(2-D)I_o}{(1-D)^2}$	$\frac{(1+D)I_o}{D(1-D)}$
Number of diodes	3	3	3	3	3	3	3	3	3
High/low side gate driver	Low	Low	Low	Low	Low	Low	Low	Low	Low
Common ground	Yes	Yes	Yes	No	No	Yes	Yes	Yes	Yes
Input current	Nonpulsating	Nonpulsating	Nonpulsating	Nonpulsating	Nonpulsating	Pulsating	Nonpulsating	Nonpulsating	Nonpulsating
Theoretical efficiency/ experimental efficiency**	91.71% 90.3%	94.89% 93.5%	93.20% 91.9%	94.89% 93.6%	94.89% 93.6%	93.39% 92.0%	91.71% 90.4%	91.71% 90.3%	94.69% 93.3%

	Derived from Fig. 3(a)		Derived from Fig. 3(b)	Derived from Fig. 3(c)				Derived from Fig. 3(f)	Derived from Fig. 3(g)
	Fig. 5(j)	Fig. 5(k)	Fig. 5(l)	Fig. 5(m)	Fig. 5(n)	Fig. 5(o)	Fig. 5(p)	Fig. 5(q)	Fig. 5(r)
DC gain	$\frac{2}{1-D}$	$\frac{2-D}{1-D}$	$\frac{2}{1-D}$	$-\frac{1+D}{1-D}$	$\frac{2-D}{1-D}$	$\frac{1+D}{1-D}$	$-\frac{1+D}{1-D}$	$\frac{1}{1-D}$	$\frac{-D}{1-D}$
Voltage stress on diodes	$\frac{V_o}{2}$	$\frac{V_o}{2-D}$	$V_o - V_{in}$	$\frac{V_o}{1+D}$	$\frac{V_o}{2-D}$	$\frac{V_o}{1+D}$	$\frac{V_o}{1+D}$	V_o	$V_{in} + V_o$
Current stress on diodes	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$
Voltage stress on switch	$\frac{V_o}{2}$	$\frac{V_o}{2-D}$	$V_o - V_{in}$	$\frac{V_o}{1+D}$	$\frac{V_o}{2-D}$	$\frac{V_o}{1+D}$	$\frac{V_o}{1+D}$	V_o	$V_{in} + V_o$
Current stress on switch	$\frac{(1+D)I_o}{D(1-D)}$	$\frac{I_o}{D(1-D)}$	$\frac{(1+D)I_o}{D(1-D)}$	$\frac{(1+D)I_o}{D(1-D)}$	$\frac{(2-D)I_o}{D(1-D)}$	$\frac{(1+D)I_o}{D(1-D)}$	$\frac{(2-D)I_o}{D(1-D)}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$
Number of diodes	3	2	5	3	3	3	3	1	1
High/low side gate driver	Low	Low	Low	Low	Low	High	High	Low	High
Common ground	Yes	Yes	Yes	No	No	No	No	Yes	Yes
Input current	Pulsating	Nonpulsating	Pulsating	Pulsating	Pulsating	Pulsating	Pulsating	Nonpulsating	Nonpulsating
Theoretical efficiency/ experimental efficiency**	94.89% 93.6%	95.40% 94.1%	91.61% 90.2%	93.63% 92.3%	93.92% 92.6%	93.63% 92.3%	94.85% 93.5%	95.42% 94.2%	93.71% 92.4%

**The efficiency refers to the power stage only. As the purpose was just to compare the converters, all of them have been built under the same conditions, with discrete elements. No optimization was tried. An implementation on PCB board will give a better number for the efficiency of all the converters, but the differences between them will remain the same.

branches by open- or short-circuits, and inserting the obtained switched-cells in basic converters, the high dc gain converters in Fig. 6(a)–(i) are obtained. The switched cells in Fig. 6(d), (g), and (h) contain only two capacitors; however, the basic converter contains three reactive elements, which also gives a final structure of five reactive components. The converters in Fig. 6(a)–(c) and (e)–(i) have been proposed by other authors. The solution in Fig. 6(d) is newly derived from the generic geometrical structure.

All these converters are compared in Table IV in the same terms as in the previous sections.

The "winners" in this class of converters appear to be the solutions in Fig. 6(c) and (d): an ideal dc gain of nine times for $D = 0.75$ (i.e., the double minus one unity of the gain in converters with three reactive elements) with the lowest voltage stress on the semiconductors. However, these converters present a pulsating input current. It can be seen [solutions in Fig. 6(e) and (f)] how a high voltage stress on the transistor and diodes affects the efficiency. It can be noticed that the converters derived from Cuk, SEPIC, and ZETA basic converters do not have the highest dc gain in their class, due to the fact that despite having two extra reactive elements compared with the boost and buck-boost stages, the Cuk, SEPIC, and ZETA basic converters feature the same dc gain as a basic buck-boost stage.

VI. RULES FOR DERIVING VIABLE SWITCHED CELLS

A number of criteria have to be followed when placing the components on the branches of the geometric structure in the precedent sections.

A. Rules for Avoiding Fault Topologies (Circuits That Do Not Work)

1) Diodes have to assure the flowing of the inductor currents at the switching from a topology to another one. The capacitor voltages have to be continuous at the switching moments, meaning that loops of capacitors at different charging levels are forbidden.
2) If it is planned
   a) to charge a capacitor when a diode in its path conducts, the positive end of the capacitor has to be connected to the cathode of the diode [see Fig. 7(a)].
   b) to discharge the capacitor through the diode, the diode anode has to be connected to the positive end of the capacitor [see Fig. 7(b)].

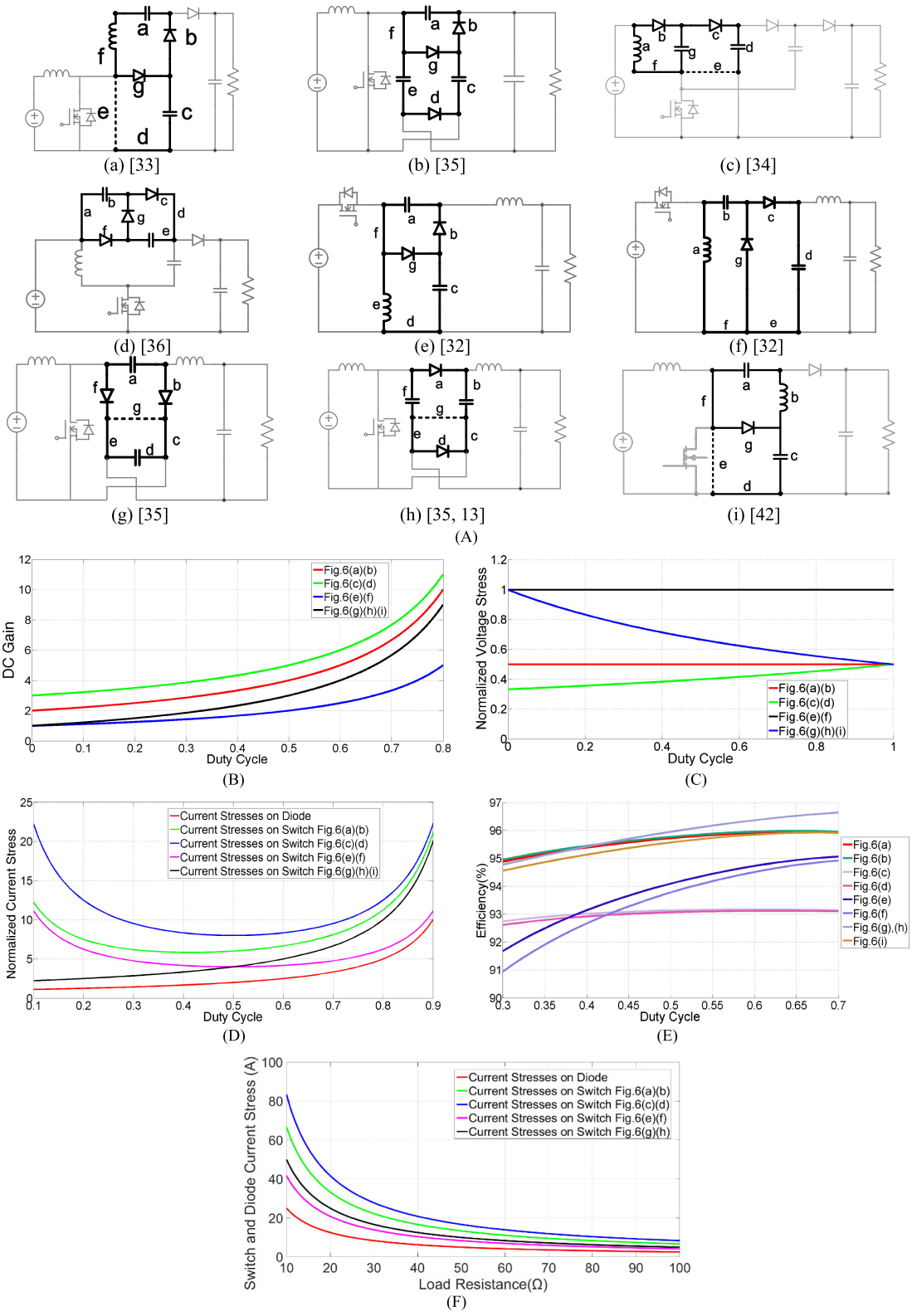

Fig. 6. Five reactive elements based high gain dc converters. (A) Panels (a) and (b) are derived from basic converter of Fig. 3(a). Panels (c) and (d) are derived from the basic converter of Fig. 3(b). Panels (e) and (f) are derived from basic converter of Fig. 3(d) with the ZETA inductor, flying capacitor, and diode replaced by the elements of the switching cell. Panels (g) and (h) are derived from the basic converter of Fig. 3(e) with the Cuk flying capacitor and diode replaced by the capacitor and diode of the switching cell. Panel (i) is derived from Fig. 3(h) with the SEPIC inner inductor and capacitor replaced by their homologues of the switched cell. (B) Theoretical dc gain versus duty-cycle. (C) Normalized theoretical voltage stresses (voltage stress over V_o) on switches versus duty-cycle. (D) Normalized theoretical current stresses (current stress over I_o) on switches versus duty-cycle. (E) Efficiency versus duty-cycle. (F) Theoretical current stresses on switches versus load.

TABLE IV
COMPARISON OF THE FIVE REACTIVE ELEMENTS HIGH DC GAIN CONVERTERS

	Derived from Fig. 3(a)		Derived from Fig. 3(b)		Derived from Fig. 3(d)		Derived from Fig. 3(e)		Derived from Fig. 3(h)
	Fig. 6(a)	Fig. 6(b)	Fig. 6(c)	Fig. 6(d)	Fig. 6(e)	Fig. 6(f)	Fig. 6(g)	Fig. 6(h)	Fig. 6(i)
DC gain	$\frac{2}{1-D}$	$\frac{2}{1-D}$	$\frac{3-D}{1-D}$	$\frac{3-D}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$-\frac{1+D}{1-D}$	$\frac{1+D}{1-D}$	$\frac{1+D}{1-D}$
Voltage stress on diodes	$\frac{V_o}{2}$	$\frac{V_o}{2}$	$\frac{V_o}{3-D}$	$\frac{V_o}{3-D}$	V_o	V_o	$\frac{V_o}{1+D}$	$\frac{V_o}{1+D}$	$\frac{V_o}{1+D}$
Current stress on diodes	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$
Voltage stress on switch	$\frac{V_o}{2}$	$\frac{V_o}{2}$	$\frac{V_o}{3-D}$	$\frac{V_o}{3-D}$	V_o	V_o	$\frac{V_o}{1+D}$	$\frac{V_o}{1+D}$	$\frac{V_o}{1+D}$
Current stress on switch	$\frac{(1+D)I_o}{D(1-D)}$	$\frac{(1+D)I_o}{D(1-D)}$	$\frac{2I_o}{D(1-D)}$	$\frac{2I_o}{D(1-D)}$	$\frac{I_o}{D(1-D)}$	$\frac{I_o}{D(1-D)}$	$\frac{2I_o}{1-D}$	$\frac{2I_o}{1-D}$	$\frac{2I_o}{1-D}$
Number of diodes	3	3	4	4	2	2	2	2	2
High/low side gate driver	Low	Low	Low	Low	High	High	Low	Low	Low
Common ground	Yes	No	Yes	Yes	Yes	Yes	No	No	Yes
Input current	Nonpulsating	Nonpulsating	Pulsating	Pulsating	Pulsating	Pulsating	Nonpulsating	Nonpulsating	Nonpulsating
Theoretical Efficiency/	94.87%	94.93%	94.42%	94.31%	94.03%	93.89%	94.95%	94.95%	94.89%
Experimental Efficiency**	93.6%	93.6%	93.1%	93.0%	92.7%	92.6%	93.7%	93.7%	93.5%

**The efficiency refers to the power stage only. As the purpose was just to compare the converters, all of them have been built under the same conditions, with discrete elements. No optimization was tried. An implementation on PCB board will give a better number for the efficiency of all the converters, but the differences between them will remain the same.

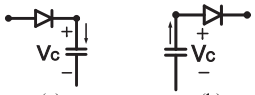

Fig. 7. (a) Rule 2 for placing a diode and a capacitor to be charged. (b) Rule 2 for placing a diode and a capacitor to be discharged.

3) In order to get a step-up dc gain, the inductor has to be connected to the switch (if more inductors are in the switching cells, they have to be connected to the switch through diodes). Thus, in the on-switching stage, the inductor(s) will be charged, as typical in a classical boost converter.
4) When placing the diodes, their direction has to coincide with that of the inductor current.
5) If a diode is in conduction in both switching stages, it can be replaced with a short-circuit. After filling the branches with reactive elements and diodes, the remaining branches are filled with short-circuits if there is a need to have paths for the inductor currents or for the capacitors charging and discharging, and by open-circuits if no current has to flow through them.
6) In the basic switching cell with seven branches, no more than five reactive elements can be placed; an additional one will lead to contradicting one of the above rules.
7) In any switching cell, the total number of reactive elements cannot differ with more than one unity from the total number of diodes; otherwise, the diodes would have to satisfy opposite requirements regarding their direction.
8) The reactive elements can be placed on different branches in an aleatory manner (for example, all switching cells in Fig. 5(f)–(h) and (k) contain two inductors and one capacitor). However, the placing of the diodes has then to take place such that to respect the rules 1–4.
9) No more than three inductors are needed in a basic switching cell. No more than three capacitors are needed in a switching cell. A higher dc gain can be obtained by generalizing the switching cells according to the methods exposed in Section II.

B. Rules for Optimization of the Derived Converters

As pointed out previously, an "optimum" converter according to all the criteria does not exist. For each specific criterion, a certain converter can be the best.

1) If it is required to obtain the highest possible dc gain with the given number of reactive elements, the components have to be placed so that all the reactive elements are charged in parallel from the source in the on-switching stage and discharged in series to the load in the off-switching stage [for example, the converters in Figs. 4(a) and (e) and 5(c), (d), (f)–(h), (m), (o), and (p)].
2) If the requirement is a lower switch voltage stress, a capacitor will be placed in the switching cell such that to form a loop with the switch, rectifier diode and output capacitor/load [for example, Figs. 4(b)–(d) and (f), 5(b), (c), (e), and (i)–(l), and 6(a)–(d), (g), and (h)].

1) Examples of Applying the Above Rules

Example 1:

1) Two inductors are used to form the switching cell.
2) The two inductors have to be charged in parallel (on-stage) and discharged in series (off-stage) to assure a step-up dc gain. The inductors are placed according to rule A8. The inductor currents directions are determined [see Fig. 8(a)].
3) Diodes are placed on branches f and c according to the currents directions to assure the currents flow in the on-stage (rule A4) [see Fig. 8(b)]. A diode should be placed on branch g to assure the flow of the discharging inductor currents in the off-stage (rule A1). Short circuits are placed on branches a and d to assure the flow of the currents in both stages [see Fig. 8(c)].
4) The equivalent switching topologies are shown in Fig. 8(d) and (e).

The switching cell derived in such a way was used in the converters in Figs. 4(a) and 5(l). Its dual, containing two capacitors, obtained in a similar manner by respecting the previous rules about the position of the diodes in relation with the capacitors (rule A2), was used for getting the converters in

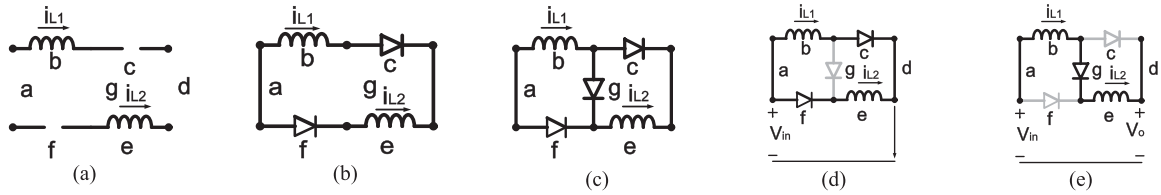

Fig. 8. Design example 1.

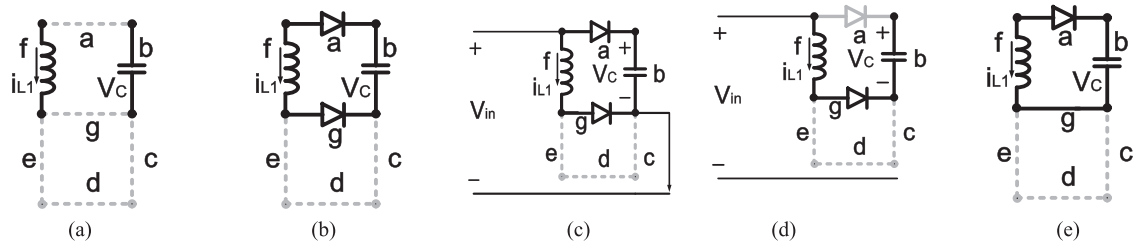

Fig. 9. Design example 2.

Figs. 5(c) and 6(d).The above structure can be easily generalized by following one of the presented generalization methods in Section II.

Example 2:

1) One inductor and one capacitor are used to form the switching cell.
2) To get a step-up function, both the inductor and capacitor have to be charged in the on-stage in parallel and discharged in series in the off-stage (rule B1).
3) The inductor and the capacitor are placed on branches f and b, respectively (rule A8). The inductor current direction is determined [see Fig. 9(a)]. Diodes have to be placed on branches a and g to respect the previous rules related to the place of a diode in relation with an inductor (A1 and A4), respectively in relation with a capacitor (A2) [see Fig. 9(b)].
4) The switching diagrams are shown in Fig. 9(c) and (d). The diode on branch g remains on in two switching stages; it can be replaced by a short circuit, according to rule A5. As the flow of the inductor current and the charging/discharging path of the capacitor were assured, the remaining branches c–e have no role to play, so they can be replaced by open-circuits. Thus, the final version of the cell is shown in Fig. 9(e).

This switching cell was used in the converters shown in Figs. 4(b) and 5(q). It can be easily generalized as explained in Section II.

Example 3:

1) Two inductors and one capacitor are used to construct the switching cell.
2) The two inductors are charged in the on-stage. The capacitor *C* is used to charge one of the inductors, for example, L_2 in order to achieve a higher dc gain. The inductors are placed on branches c and f, the capacitor on branch b (rule A8). The inductors currents direction and the polarity of the capacitor are determined [see Fig. 10(a)].
3) To charge L_1, a diode has to be placed on branch *e* with the orientation dictated by the inductor current i_{L1} (rule A4). To charge *C* from L_1, a diode has to be placed on branch g with the anode connected to the plus of the capacitor voltage (according to rule A2). The flow of the inductor currents in both stages is allowed by placing short-circuits on branches a and d [see Fig. 10(b)].
4) The switching topologies are shown in Fig. 10(c) and (d).

The obtained switching cell was used to obtain the converters in Fig. 5(g) and (h).By using a dual derivation procedure, similar cells with two capacitors and one inductor can be obtained, as those used for deriving the converters in Figs. 4(c) and 5(j).

By using the general rules, all the switching cells presented in Figs. 4–6 can be derived.

The purpose of the next example is to show how a new converter, which was not previously derived, can be obtained by following the stated rules.

Example 4:

1) One inductor and three capacitors are used to construct the switching cell.
2) The inductor and capacitor *C*1 are charged in the on-stage; capacitors *C*2 and *C*3 are charged in the off-stage.
3) The inductor is placed on branch a and the capacitors are placed on branches g, f, and d (rule A8). The current of the inductor and the polarity of the capacitors are decided [see Fig. 11(a)]. According to rules A1, A2, and A4, diodes are placed on branches b, c, and e, respectively. As all the branches have been "populated" by elements, no branch can become open- or short-circuit [see Fig. 11(b)].
4) The new cell is inserted in a boost converter; the boost inductor is rendered redundant by the switching cell inductor [see Fig. 11(c)]. The switching stages are shown in Fig. 11(d) and (e).

The dc gain is obtained as

$$M = \frac{3 - D}{1 - D}.$$

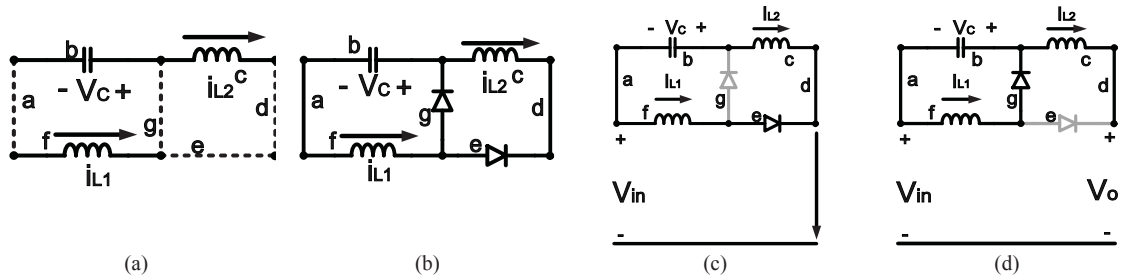

Fig. 10. Design example 3.

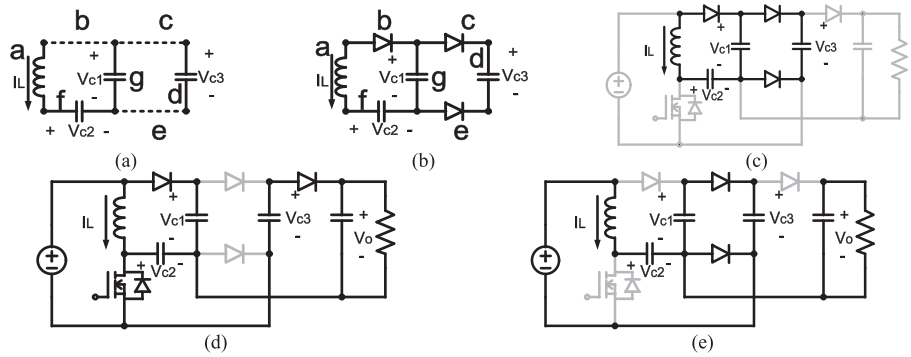

Fig. 11. Design example 4.

VII. Generalized Ultrahigh DC Gain Converters

Based on the generalized geometric structures of Fig. 2, a few of the switched cells presented in Figs. 4 and 5 are generalized, and then inserted in a classical boost converter as shown in Fig. 12. Fig. 12(a) is based on the generalization type (a) explained in Section II. It is suitable for any basic switching cell in which either the set of branches (c), (d), and (e) or the set (a), (b), and (f) are open-circuits. The detailed steps to get the generalized switching cell are shown in Fig. 12(a1)–(a4). Fig. 12(b) and (c) is obtained by following the generalization type (b) described in Section II. It is suitable for any switching cell in which either branches (b) and (e) or branches (c) and (f) contain the same type of component. The generalization process is explained in Fig. 12(c1)–(c3). Fig. 12(d) and (e) is based on the generalization way (c) proposed in Section II. It is suitable for those switching cells in which branch (e) is an open-circuit. The steps for getting the generalized structure are shown in Fig. 12(d_1) and (d_2). The generalized structure in Fig. 12(g) is an application of the generalization type (d) shown in Section II. It is suitable for the switching cells containing an open-circuit as branch (g). The step-by-step derivation of the generalized cell is shown in Fig. 12(g_1)–(g_3). Table V consolidates the results of these generalizations. It shows which switched cell was used in the generalized structure, which geometry among those developed in Fig. 2 served as the template for generalization, the final ultrahigh dc gain converter obtained in such a way and its dc gain. In the table, *n* gives the number of individual switched cells comprised in the final circuit.

Fig. 12(l) presents a special way of generalization: two switched cells [see Fig. 5(b) and (c)] are used alternatively in the geometric structure of Fig. 2(b). Such a solution combines the advantages of each one of the two switched cells relative to the other one: if the switched cell in Fig. 5(b) is used alone in the generalized structure [as in Fig. 12(e)], the voltage on the capacitors on branches (c) of the switched cells will increase from a cell to the next one. If the switched cell in Fig. 5(c) is used alone in the generalized structure [as in Fig. 12(f)], a very large output capacitor would be required. The mixed solution mitigates among the two disadvantages. In the formula of the dc gain, *m* represents the number of cells of the first type [see Fig. 5(b)] and *n* the number of cells of the second type [see Fig. 5(c)]. Future researches may find many other advantageous combinations of switched cells in a generalized structure.

VIII. Experimental Results

An ultrahigh dc gain converter [see Fig. 12(l)] was built in the laboratory[1] by using two switched cells, one of the type defined in Fig. 5(b) and one of the type defined in Fig. 5(c) ($m = n = 1$). The circuit in Fig. 13 was implemented under the following conditions: $V_{\rm in} = 30$ - - 60 V (nominal 30 V), $f_s = 200$ kHz, $P_{\rm out} = 10$ - - 150 W (nominal 75 W). It was operated with D = 0.56. The expected output voltage according to the theoretical result of Table V is $V_o = \frac{m+n+1}{1-D} V_{\rm in} = 204.5$ V. The expected voltages on the capacitors are $V_{\rm C1} = V_{\rm C2} = V_{\rm C3} = \frac{V_o}{m+n+1} = 68.1$ V, $V_{\rm C4} = \frac{(m+n)V_o}{m+n+1} = 136.3$ V. The expected voltage stress on the transistor and diodes is $\frac{V_o}{m+n+1} = 68.1$ V.

The derived converter was designed following the procedure from [1]. The active switch was designed according to the requirements: maximum voltage across it $\frac{V_o}{3} = 68.1$ V; maximum

1.The prototype was built on PCB.

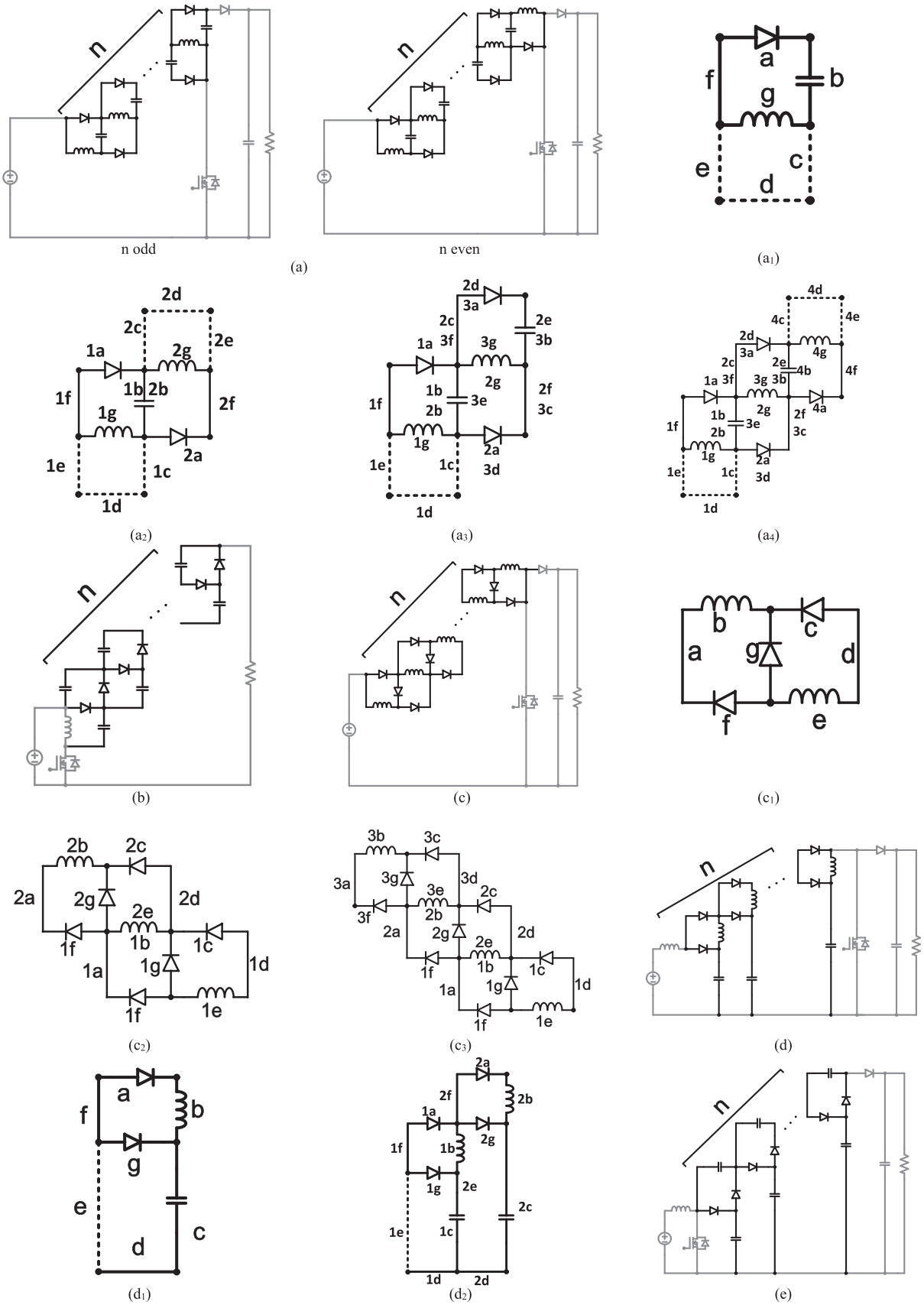

Fig. 12 Generalized ultrahigh dc gain converters and (a_1)–(a_4), (c_1)–(c_3), (d_1)–(d_2), (g_1)–(g_3) step-by-step derivation of the generalized structures.

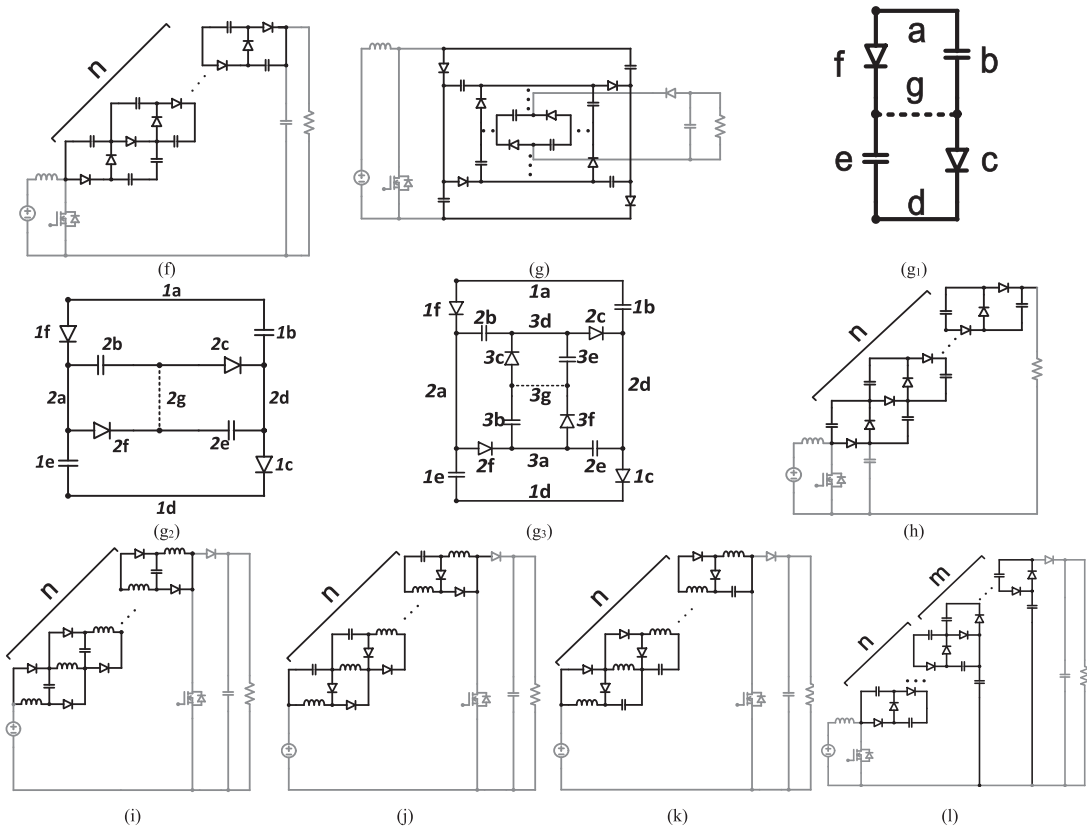

Fig. 12 continued

TABLE V
GENERALIZED ULTRAHIGH DC GAIN CONVERTERS

Basic switched cell used in the generalization	Generalized geometric structure	Generalized ultrahigh DC gain converter	DC gain
Fig. 4(b)	Fig. 2(a)	Fig. 12(a)	$\frac{n+2}{2(1-D)}, n$ even $\frac{n+3-2D}{2(1-D)}, n$ odd
Fig. 4(c)	Fig. 2(b)	Fig. 12(b)	$\frac{n+1-D}{1-D}$
Fig. 4(a)	Fig. 2(b)	Fig. 12(c)	$\frac{1+n\,D}{1-D}$
Fig. 5(a)	Fig. 2(c)	Fig. 12(d)	$\frac{1}{(1-D)^{n+1}}$
Fig. 5(b)	Fig. 2(c)	Fig. 12(e)	$\frac{n+1}{1-D}$
Fig. 5(c)	Fig. 2(b)	Fig. 12(f)	$\frac{n+1}{1-D}$
Fig. 5(d)	Fig. 2(d)	Fig. 12(g)	$\frac{n+1}{1-D}$
Fig. 5(i)	Fig. 2(b)	Fig. 12(h)	$\frac{n+1}{1-D}$
Fig. 5(f)	Fig. 2(b)	Fig. 12(i)	$\frac{n+1}{1-D}$
Fig. 5(g)	Fig. 2(b)	Fig. 12(j)	$\frac{1}{(1-D)^{n+1}}$
Fig. 5(h)	Fig. 2(b)	Fig. 12(k)	$\frac{1}{(1-D)^{n+1}}$
Fig. 5(b) and (c)	Fig. 2(b)	Fig. 12(l)	$\frac{n+m+1}{1-D}$

current through it 4.06 A; and rms current 2.85 A. The switching frequency was set at 200 kHz. As a consequence, the IRF640N MOSFET with 200 V rating voltage and 18 A drain current is chosen. The diode D_o was designed taking into account the voltage stress across it $\frac{V_o}{3} = 68.1$ V and current of 0.917 A. The diode NTSV20U100CTG with 100 V reverse voltage, 20 A forward current, and 0.485 V forward voltage is chosen.

The inductor is chosen as L = 220 μH, $f_s = 200$ kHz according to the inequality $L \geq \frac{DT_s V_{\text{in}}}{\Delta I_L} = 168\ \mu$H.

The output capacitor was designed according to the conditions:

1) ripple in the output voltage less than 0.05%

$$C_o \geq \frac{DT_s V_o}{R\Delta V_o} = 1.12\,\mu\text{F}$$

2) load transient specification

$$C_o \geq \frac{\Delta I_o}{2\pi f_{\text{BW}} \Delta V_{\text{o,trans}}} = 159\,\mu\text{F}$$

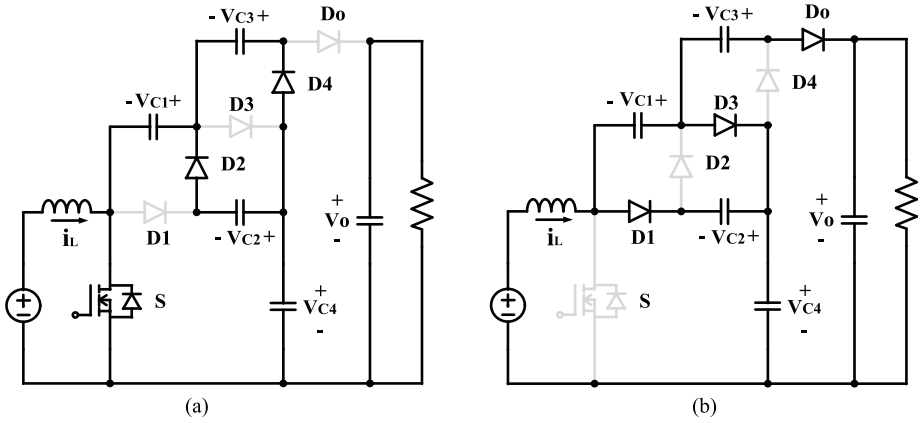

Fig. 13. Circuit diagram of the generalized mixed-cells converter built in the laboratory. (a) Switching topology ON; (b) switching topology OFF.

where ΔI_o and $\Delta V_{o,\mathrm{trans}}$ are the changes of the load current and output voltage respectively during the transient response, and f_{BW} is the control loop unity-gain bandwidth of the controlled converter

3) rms capacitor current

$$I_{C\mathrm{orms}} = \sqrt{{I_o}^2 D + (I_{\mathrm{Do}} - I_o)^2 (1-D)} = 0.414\,\mathrm{A}.$$

A Nichicon-type 220-μF capacitor with 11-mΩ equivalent series resistance (ESR) is chosen. The final output voltage ripple requirement is then fulfilled

$$\Delta V_{\mathrm{co}} + I_{D\mathrm{omax}} r_{\mathrm{Co}} = 0.01\,\mathrm{V} < 0.005\,V_o.$$

The flying capacitors are designed from the conditions

$$C_1 \geq \frac{I_{C1_{\mathrm{in}}} DT_s}{\Delta V_{\mathrm{C1}}} = 10.7\,\mu\mathrm{F}$$

$$C_2 = C_3 \geq \frac{I_{C2_{\mathrm{in}}} DT_s}{\Delta V_{\mathrm{C3}}} = 5.38\,\mu\mathrm{F}$$

$$C_4 \geq \frac{I_{C4_{\mathrm{in}}} (1-D) T_s}{\Delta V_{\mathrm{C4}}} = 5.38\,\mu\mathrm{F}.$$

Nichicon-type 47 μF capacitors are chosen.

The prototype is built by using the components: $C_1 = 47\,\mu$F, $C_2 = 47\,\mu$F, $C_3 = 47\,\mu$F, $C_4 = 47\,\mu$F, $C_{\mathrm{out}} = 220\,\mu$F, and $L = 220\,\mu$H, and the switch and diodes are of type IRFI640 and NTSV20U100CT respectively. The steady-state experimental waveforms are shown in Fig. 14, under the conditions: $V_{\mathrm{in}} = 30\,\mathrm{V}$, $f_s = 200\,\mathrm{kHz}$, $P_{\mathrm{out}} = 75\,\mathrm{W}$, and $D = 0.56$ .The experimental output voltage is 200.38 V and the experimental voltage stress on the semiconductors is 66.79 V. The results are very close to the theoretical ones. Fig. 15(a) shows the measured efficiency at different load values and Fig. 15(b) at different duty-cycle values. The nominal efficiency is 93.37%.

Fig. 16 shows the transient response of the converter for a change in the input voltage from 30 to 60 V. The output voltage overshoot is 1.96 V, i.e., approximately 1% of the steady-state value, the transient time being 27.4 ms.

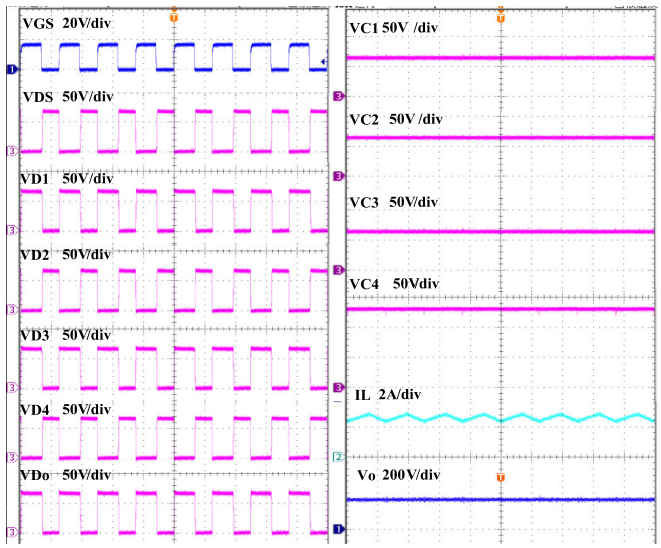

Fig. 14. Steady-state experimental waveforms for the prototype shown in Fig. 13, $V_{\mathrm{GS}}, V_{\mathrm{DS}}, V_{D1}, V_{D2}, V_{D3}, V_{D3}, V_{D4}, V_{\mathrm{Do}}, V_{C1}, V_{C2}, V_{C3}, V_{C4}$, I_L, V_o 4 μs/div.

The power losses are calculated following the equations from [1]; with ID1 $-$ 4, 0 denoting the average currents through the diodes and V_D the forward voltage of a diode in conduction, the losses due to the parasitic resistances of the inductor (r_L), capacitors ($r_{C1-4,0}$) and switch ($R_{\mathrm{DS_on}}$), and the switching loss, with $V_{\mathrm{DS\_off}}$ denoting the off-state value of the drain-source voltage, I_{DS} the on-current through the switch, t_r the transient time taken by the turn-on process, t_f the transient time taken by the turn-off process are expressed as follows:

$$\begin{aligned} P_{\mathrm{loss}} = {} & P_{D1\mathrm{loss}} + P_{D2\mathrm{loss}} + P_{D3\mathrm{loss}} + P_{D4\mathrm{loss}} + P_{D\mathrm{oloss}} \\ & + P_{\mathrm{switch\_loss}} + P_{rL\_\mathrm{loss}} + P_{rc1\_\mathrm{loss}} + P_{rc2\_\mathrm{loss}} \\ & + P_{rc3\_\mathrm{loss}} + P_{rc4\_\mathrm{loss}} + P_{rco\_\mathrm{loss}} + P_{\mathrm{switch\_on}} \\ & + P_{\mathrm{switch\_off}} + P_{\mathrm{controller}} \end{aligned}$$

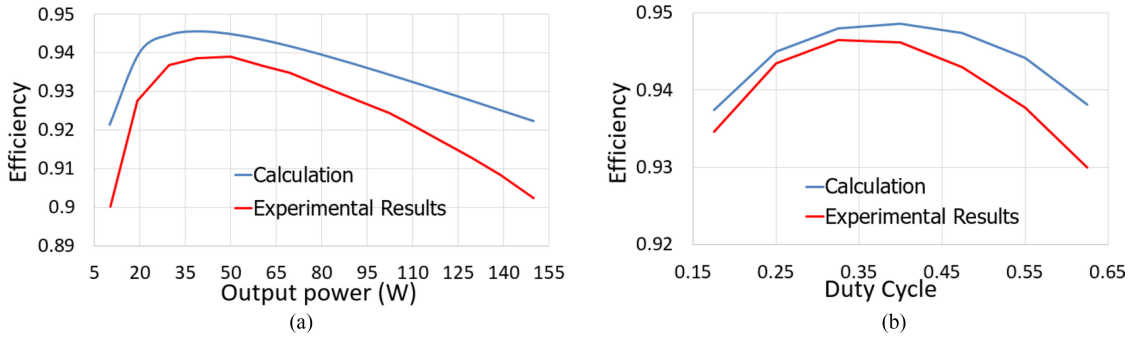

Fig. 15. (a) Experimental and theoretical efficiency of the prototype shown in Fig. 13 under different load values ($D = 0.56$); and (b) versus duty-cycle ($P_o = 60$ W, $V_o = 200$ V).

$$
\begin{aligned}
P_{D1\text{loss}} &= I_{D1} V_D (1-D) \\
P_{D2\text{loss}} &= I_{D2} V_D D \\
P_{D3\text{loss}} &= I_{D3} V_D (1-D) \\
P_{D4\text{loss}} &= I_{D4} V_D D \\
P_{Do\text{loss}} &= I_{Do} V_D (1-D) \\
P_{\text{Switch\_loss}} &= I_{DS}^2 R_{DS\_on} D \\
P_{rL\_\text{loss}} &= I_L^2 r_L \\
P_{rC1\_\text{loss}} &= I_{C1\_in}^2 r_C D + I_{C1\_out}^2 r_C (1-D) \\
P_{rC2\_\text{loss}} &= I_{C2\_in}^2 r_C D + I_{C2\_out}^2 r_C (1-D) \\
P_{rC3\_\text{loss}} &= I_{C3\_in}^2 r_C D + I_{C3\_out}^2 r_C (1-D) \\
P_{rC4\_\text{loss}} &= I_{C4\_in}^2 r_C D + I_{C4\_out}^2 r_C (1-D) \\
P_{rCo\_\text{loss}} &= I_{Co\_in}^2 r_{Co} D + I_{Co\_out}^2 r_{Co} (1-D) \\
P_{rCo\_\text{loss}} &= I_{Co\_in}^2 r_{Co} D + I_{Co\_out}^2 r_{Co} (1-D) \\
P_{\text{switch\_on}} &= \frac{V_{DS\_off} I_{DS} t_r f_s}{2} \\
P_{\text{switch\_off}} &= \frac{V_{DS\_off} I_{DS} t_f f_s}{2}.
\end{aligned}
$$

Calculating the average values of the currents through the diodes from ampere-second balance equations on the capacitors, and performing a few algebraic steps, it was obtained unnumberd equation shown as bottom page.

The theoretical efficiency was calculated for the values of the parameters of the components used in the design $V_D = 0.485$ V, $r_L = 0.06\ \Omega$, $r_{Co} = 0.11\ \Omega$, $r_{C1-4} = 0.15\ \Omega$, $R_{DS\_on} = 0.1\ \Omega$, $t_r = 29$ ns, $t_f = 28.5$ ns, for $V_o = 200$ V, D = 0.56, $f_s = 200$ kHz. The estimated efficiency is presented versus the variation of the load in Fig. 15(a) and versus duty-cycle in Fig. 15(b). The experimental and calculated curves are quite close. In the theoretical calculation of the efficiency, a constant value of 0.5 W for the power consumption in the controller was added. Thus the experimental results match the theoretical one even at very low load.

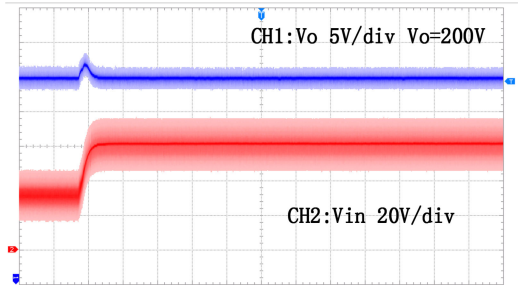

Fig. 16. Transient response of the prototype shown in Fig. 13 for a change in the input voltage from 30 to 60 V at 75 W load, 50 ms/div.

The new converter is compared with available converters containing the same number of reactive elements in Table VI.

It is possible to see again that it does not exist an an "optimum" converter according to all the criteria does not exist. For each specific criterion, a certain converter can be the best. For example, the third converter in the above table provides the highest dc gain, but at the cost of the highest voltage stress on the transistor and rectifier diode (three times higher than that in the proposed converter). The fourth and fifth converters in the table contain two active switches, requiring more drivers, resulting in a higher cost.

IX. Conclusion

It was shown that almost all the available hybrid nonisolated step-up large dc gain converters obtained by integrating a switched inductor-capacitor-diode cell into a basic power stage (boost, buck-boost, Cuk, SEPIC, and ZETA) can be derived from the same geometric structure by replacing its branches by capacitors, inductors, diodes, open-circuits, and short-circuits in different ways.

$$
\eta = \frac{P_o}{P_o + P_{\text{loss}}} = \frac{V_o}{V_o + 5V_D + \frac{V_o(2+D)^2 R_{DS\_on}}{D(1-D)^2 R} + \frac{9V_o r_L}{(1-D)^2 R} + \frac{(10+D^2)V_o r_C}{D(1-D)R} + \frac{V_o(2+D)(t_r+t_r)f_s}{2D(1-D)}}
$$

TABLE VI
COMPARISON OF THE PROPOSED CONVERTER WITH SIX REACTIVE ELEMENTS CONVERTERS

Converters	Proposed converter	[38]	[39]	[40]	[41]
Number of inductors	1	2	3	1	0
Number of capacitors	5	4	3	5	6
Number of diodes	5	3	5	6	6
Number of active switches	1	1	1	2	2
DC gain	$\frac{3}{1-D}$	$-\frac{1+D}{1-D}$	$\frac{1}{(1-D)^3}$	$\frac{4}{1-D}$	4
Voltage stress on diodes	$\frac{V_o}{3}$	$\frac{V_o}{1+D}$	V_o	$\frac{V_o}{2}$	$\frac{V_o}{4}$
Current stress on diodes	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{(1-D)^3}$	$\frac{I_o}{1-D}$	$\frac{I_o}{D}$
Voltage stress on switch	$\frac{V_o}{3}$	$\frac{V_o}{1+D}$	V_o	$\frac{V_o}{2}$	$\frac{V_o}{4}$
Current stress on switch	$\frac{(2+D)I_o}{D(1-D)}$	$\frac{(1+D)I_o}{D(1-D)}$	$\frac{3+D^2-3D}{(1-D)^3}I_o$	$\frac{(3+D)I_o}{D(1-D)}$	$\frac{3I_o}{D}$
Line-to-load common ground	Common ground	Common ground	Common ground	Common ground	Not common ground
Input current	Nonpulsating	Nonpulsating	Nonpulsating	Pulsating	Pulsating

The classification of the switched-cells according to their generation allowed for a comparison of the performances of the converters belonging to each class as defined by the number of the reactive elements they contained. By weighting the dc gain and the voltage stress on the transistor and diodes, it was noticed that in each class there are several "champions". The efficiencies of these "winners" are close one to the other. As each of these circuits can have some other distinct advantages (like as nonpulsating input current, advantageous position of the switch rendering easy its driving, common line-to-load ground), the choice of using each one of these solutions is dependent on the type of the application.

A huge number of new hybrid large dc gain converters can be developed starting from the same generic geometric cell by placing the reactive elements, diodes, open-circuits and short-circuits in other ways. A few such examples of new switched cells inserted in boost converters have been given. However, this methodology opens the way for many further researches which will be able to generate new viable hybrid converters presenting features adequate to each application where a very large dc gain is necessary.

The generic geometric structure was generalized in a few ways, allowing for the derivation of ultrahigh dc gain switched cells. In addition, it was shown how the advantages of different basic switched cells can be explored together by populating the generalized structure with different types of switched-cells. An example was given, together with the theoretical and experimental results. Again, the method opens the way to many further researches for getting more ultrahigh dc gain converters, with different performances, as may be required in different applications in the future.

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