# Extending the Linear Modulation Range to the Full Base Speed Using a Single DC-Link Multilevel Inverter With Capacitor-Fed H-Bridges for IM Drives

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***Abstract*—In this paper, a new space vector pulse width modulation method to extend the linear modulation range of a cascaded five level inverter topology with a single dc supply is presented. Using this method, the inverter can be controlled linearly and the peak phase fundamental output voltage of the inverter can be increased from 0.577 to $0.637V_{dc}$ without increasing the dc bus voltage and without exceeding the induction motor voltage rating. This new technique makes use of cascaded inverter pole voltage redundancy and property of the space vector structure for its operation. Using this, the induction motor drive can be operated till the full speed range (0–50 Hz) with the elimination of lower order harmonics in the phase voltage and phase current. The five-level topology presented in this paper is realized by cascading a two-level inverter and two full bridge modules with floating capacitors. The inverter topology and its operation for extending the modulation range is analyzed extensively. Simulation and experimental results for both steady-state and dynamic operating conditions are presented in this paper.**

***Index Terms*—Induction motor drive, multilevel inverter, overmodulation, pulse width modulation (PWM), voltage source inverter.**

## I. Introduction

MULTILEVEL inverters play a major role in the modern-day medium- and high-power energy conversion processes. The attractive features of multilevel inverters compared to a two-level inverter are reduced switching frequency, reduced switching loss, improved voltage and current THD, reduced *dv*/*dt*, etc. Because of these reasons, multilevel inverters find application in motor drives, power quality, renewable energy, electric vehicles, etc. [1]–[3].

Neutral point clamped (NPC) inverter [4], [5], flying capacitor (FC) inverter [6], and cascaded H-Bridge (CHB) inverter [7] are the commonly used multilevel inverter topologies for research and industrial fields. The active NPC inverter is another interesting topology realized by cascading NPC and FC inverters [8]. Cascaded multilevel inverter topologies [9], [10] and modular multilevel inverter topologies [11], [12] are other popular areas of research. Various multilevel inverter topologies for the open-end winding induction motor are presented in [13] and [14].

In [15] and [16], the operation of a two level inverter in the overmodulation region ($0.577$–$0.637V_{dc}$) is presented. An overmodulation operation of a multilevel inverter with a hexagonal space vector structure is discussed in [17] and [18]. In all inverters with a hexagonal space vector structure, fifth and seventh harmonics will be present in the motor phase voltage during the overmodulation operation. In [19] and [20], a cascaded inverter topology to extend the linear modulation range is presented. But this topology also results in lower order harmonics in the inverter output voltage. In [20] and [21], a cascaded inverter topology with nearly sinusoidal currents for HVdc applications is presented using CHBs. The pulse width modulation (PWM) scheme in [20] has large spikes at the output phase voltages and it can create problem with motor winding insulations when used for variable speed drives. For HVdc applications these spikes can be removed using small filters. In these topologies, the H-bridges are used for harmonic suppression and the proposed PWM scheme [20] results in lower order harmonics in the inverter output voltage. In [21], a cascaded inverter topology with asymmetric square wave modulation is presented for HVdc applications with nearly sinusoidal output voltage. But in this scheme, each phase uses 15 CHBs for harmonic suppression. This scheme needs to be further studied for a variable speed drive applications by extracting the correct modulating wave for the H-bridges, under steady-state and transient conditions. Also the large number of H-bridges can be justified for HVdc applications, but may not be justified for medium-voltage variable speed drive applications. In [13], an inverter topology with a 12-sided space vector structure is presented which eliminates fifth and seventh harmonics over the entire modulation range. In [14], an inverter topology with a 18-sided space vector structure is presented to eliminate 5th, 7th, 11th, and 13th harmonics from motor phase voltage. But these topologies require multiple dc power supplies for operation. In [22], the operation of an inverter with a single dc supply and elimination of lower order harmonics (fifth and seventh) for the entire modulation range is presented. But for all these topologies mentioned earlier, the

Manuscript received April 26, 2016; revised July 1, 2016; accepted September 3, 2016. Date of publication September 16, 2016; date of current version February 27, 2017. Recommended for publication by Associate Editor A. Nami.

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Digital Object Identifier 10.1109/TPEL.2016.2610458

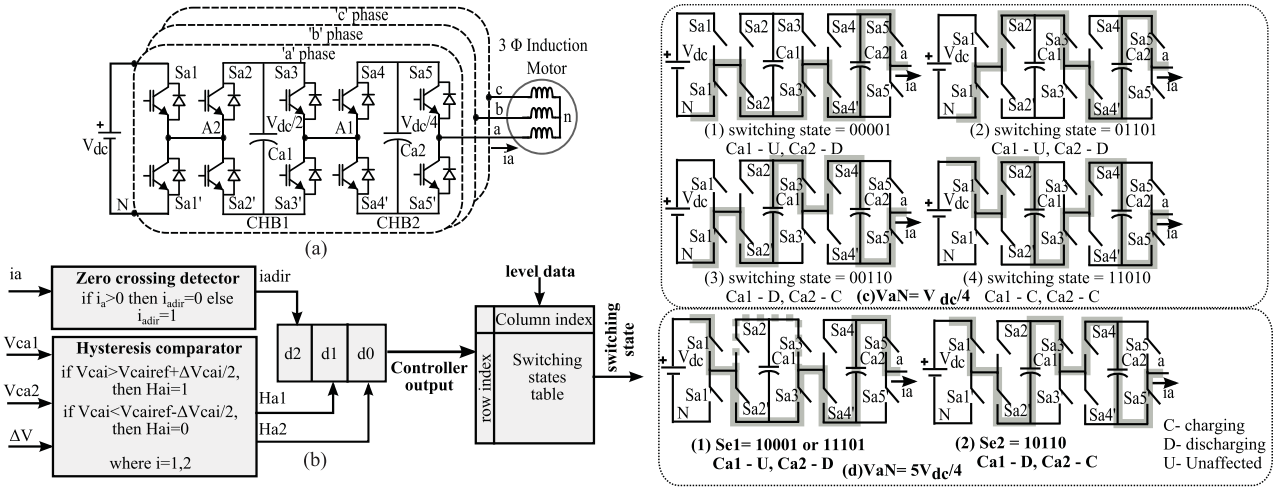


Fig. 1. (a) Power circuit topology with single dc supply (INV-1) used for the proposed linear overmodulation operation. (b) and (c) Switching state and current path for the redundant pole voltage levels of $V_{\rm dc}/4$ and $5V_{\rm dc}/4$ for "a" phase. (d) Capacitor voltage controller using a hysteresis comparator.

inverter control is not linear in the overmodulation region. In [23], increasing the number of levels and thereby increasing the modulation range of an FC inverter using the space vector redundancy is presented.

A multilevel inverter scheme with minimum number of CHBs is presented in this paper. In the work presented in this paper, the constraints addressed are as follows:

1) To use a multilevel inverter topology with low number of CHBs and with a single dc supply enabling simpler regeneration operation of the induction motor drive.
2) Eliminate the lower order harmonics (5th, 7th, 11th, and 13th) and also with a nearly sinusoidal inverter output voltage, using linear space vector pulse width modulation (SVPWM) control, to the full base speed range where the maximum phase peak fundamental is $0.637V_{\rm dc}$ (as in the case of conventional schemes operated in six-step mode).
3) Linear control from zero speed to full speed range, that is, 0 to $0.637V_{\rm dc}$ at full load condition and transient operations irrespective of the induction motor power factor (PF).
4) Never exceed the rated machine phase voltage ($2V_{\rm dc}/3$), implying that the maximum voltage space vector amplitude along any phase axis will be $V_{\rm dc}$ same as in the case of a conventional hexagonal space vector structure.
5) It also ensures that the capacitor voltage control is achieved over a sampling period using switching state redundancies, irrespective of load PF.

A five-level inverter topology with a single dc supply is used and its operation to extend the linear modulation range without increasing the dc bus voltage is analyzed based on the above-mentioned constraints in this paper. The voltage balancing of floating capacitors of the inverter is done using the inverter pole voltage redundancies. The inverter topology and the SVPWM method to extend the linear modulation range are explained in detail in the following sections.

## II. Inverter Topology

The cascaded multilevel inverter topology with a single dc supply used in this paper is shown in Fig. 1(a). The inverter topology is realized by cascading a two-level inverter with two CHB cells with a floating capacitor. The topology consists of five pairs of complementary switches (32 switching states for each phase). In each phase, switches Sx1, Sx2, Sx3, Sx4, Sx5 and Sx1$'$, Sx2$'$, Sx3$'$, Sx4$'$, Sx5$'$ (x = a, b, and c) are operated in a complementary manner (Sx1 = 1 implies Sx1 is ON and Sx1$'$ is OFF). For the first CHB module (CHB1), the floating capacitor voltage is $V_{\rm dc}/2$ and for the second CHB module (CHB2) the floating capacitor voltage is $V_{\rm dc}/4$. Considering "a" phase, the two-level inverter generates the voltages 0 and $V_{\rm dc}$ at "A2" with respect to negative dc bus "N." CHB1 generates voltage levels $+V_{\rm dc}/2$, 0, and $-V_{\rm dc}/2$ at "A1" with respect to "A2." CHB2 generates voltage levels $+V_{\rm dc}/4$, 0, and $-V_{\rm dc}/4$ at "a" with respect to "A1." The combination of two-level inverter, CHB1 and CHB2 can generate 11 voltage levels $-3V_{\rm dc}/4$, $-2V_{\rm dc}/4$, $-V_{\rm dc}/4$, 0, $V_{\rm dc}/4$, $2V_{\rm dc}/4$, $3V_{\rm dc}/4$, $V_{\rm dc}$, $5V_{\rm dc}/4$, $6V_{\rm dc}/4$, and $7V_{\rm dc}/4$.

The inverter pole voltage levels 0, $V_{\rm dc}/4$, $2V_{\rm dc}/4$, $3V_{\rm dc}/4$, and $V_{\rm dc}$ can be realized in multiple ways, which can be utilized for maintaining the capacitor voltage over a switching cycle. For pole voltage levels 0 and $V_{\rm dc}$, the capacitor charge is unaffected because all the capacitors are bypassed. There are four redundant switching states for the pole voltage levels $V_{\rm dc}/4$, $2V_{\rm dc}/4$, and $3V_{\rm dc}/4$. For these pole voltage levels, the capacitor charging can be controlled irrespective of the modulation index, load current direction, and PF. The pole voltage levels $-V_{\rm dc}/4$ and $5V_{\rm dc}/4$ can be realized in three ways. For these pole voltages, CHB2 floating capacitor (Cx2) charge can be controlled irrespective of the load current PF, but the CHB1 floating capacitor (Cx1) discharges or charges depending on the load current (PF). For the inverter pole voltage levels $-3V_{\rm dc}/4$, $-2V_{\rm dc}/4$, $6V_{\rm dc}/4$, and $7V_{\rm dc}/4$, both CHB1 and CHB2 floating capacitor (Cx1 and Cx2) charging or discharging depends on the load current (PF). The switch transitions and current paths for the redundant switching states of pole voltage levels $V_{\rm dc}/4$ and $5V_{\rm dc}/4$ for "a" phase are shown in Fig. 1(b) and (c). The inverter pole voltages, switching state redundancies, and effect on capacitor charge for a given current direction are shown in Table I for "a" phase. A hysteresis controller is used for capacitor voltage balancing for "a"

TABLE I
INVERTER SWITCHING STATES AND EFFECT ON CAPACITOR CHARGING FOR PHASE "A"

| Pole Voltage ($V_{\rm an}$) Levels | Status of switches | | | | | Capacitor charging status $i_a$ +ve | |
|---|---|---|---|---|---|---|---|
| | Sa1 | Sa2 | Sa3 | Sa4 | Sa5 | Ca1 | Ca2 |
| $-V_{\rm dc}/4$ | 0 | 0 | 0 | 1 | 0 | U | C |
| | 0 | 1 | 0 | 0 | 1 | C | D |
| | 0 | 1 | 1 | 1 | 0 | U | C |
| $V_{\rm dc}/4$ | 0 | 0 | 0 | 0 | 1 | U | D |
| | 0 | 0 | 1 | 1 | 0 | D | C |
| | 0 | 1 | 1 | 0 | 1 | U | D |
| | 1 | 1 | 0 | 1 | 0 | C | C |
| $2V_{\rm dc}/4$ | 0 | 0 | 1 | 0 | 0 | D | U |
| | 0 | 0 | 1 | 1 | 1 | D | U |
| | 1 | 1 | 0 | 0 | 0 | C | U |
| | 1 | 1 | 0 | 1 | 1 | C | U |
| $3V_{\rm dc}/4$ | 0 | 0 | 1 | 0 | 1 | D | D |
| | 1 | 0 | 0 | 1 | 0 | U | C |
| | 1 | 1 | 0 | 0 | 1 | C | D |
| | 1 | 1 | 1 | 1 | 0 | U | C |
| $5V_{\rm dc}/4$ | 1 | 0 | 0 | 0 | 1 | U | D |
| | 1 | 0 | 1 | 1 | 0 | D | C |
| | 1 | 1 | 1 | 0 | 1 | U | D |

Note: "U" denotes capacitor charge is unaffected; "C" denotes capacitor is charging; "D" denotes capacitor is discharging. Current ($i_a$) flow from inverter pole "a" to machine neutral "n" is taken as positive.

TABLE II
SWITCHING STATE SELECTION BASED ON CAPACITOR VOLTAGE AND CURRENT DIRECTION FOR PHASE "A"

| | | | Switching state selected (Sa1,Sa2,Sa3,Sa4,Sa5) | | | |
|---|---|---|---|---|---|---|
| $i_{adir}$ | $H_{a1}$ | $H_{a2}$ | $V_{\rm dc}/4$ | $2V_{\rm dc}/4$ | $3V_{\rm dc}/4$ | $5V_{\rm dc}/4$ |
| 0 | 0 | 0 | 1,1,0,1,0 | 1,1,0,0,0 | 1,1,1,1,0 | 1,0,0,0,1 |
| 0 | 0 | 1 | 0,0,0,0,1 | 0,0,1,1,1 | 1,1,0,0,1 | 1,0,0,0,1 |
| 0 | 1 | 0 | 0,0,1,1,0 | 0,0,1,1,1 | 1,1,1,1,0 | 0,1,0,0,1 |
| 0 | 1 | 1 | 0,0,0,0,1 | 0,0,1,1,1 | 0,0,1,0,1 | 0,1,0,0,1 |

Note: If $i_a$ is flowing from inverter pole "a" to motor neutral "n" as shown in Fig. 1, $i_{adir} = 0$ else $i_{adir} = 1$.

phase [see Fig. 1(d)], where $H_{ai}$ is the *i*th hysteresis controller output, $V_{\rm cai}$ is the *i*th capacitor voltage, $V^*_{\rm cai}$ is the *i*th capacitor voltage reference, $\triangle V_{\rm cai}$ is the *i*th capacitor voltage ripple, and $i = 1$ and 2. Similarly, hysteresis controllers for the other phases can be defined. Using the hysteresis controller output and current direction, a switching state can be selected from the switching state table (Table II) for charging or discharging of the capacitor.

## III. FIVE LEVEL INVERTER SPACE VECTOR STRUCTURE WITH EXTENDED SPACE VECTOR LOCATIONS

The capacitor voltage can be controlled over a switching cycle for the pole voltage levels $V_{\rm dc}/4$, $2V_{\rm dc}/4$, and $3V_{\rm dc}/4$ and all the capacitors are bypassed for the pole voltage levels 0 and $V_{\rm dc}$ of the inverter topology presented. All the three phases together generates 125 ($5^3$) pole voltage combinations. These 125 pole voltage combinations are mapped to 61 space vector locations

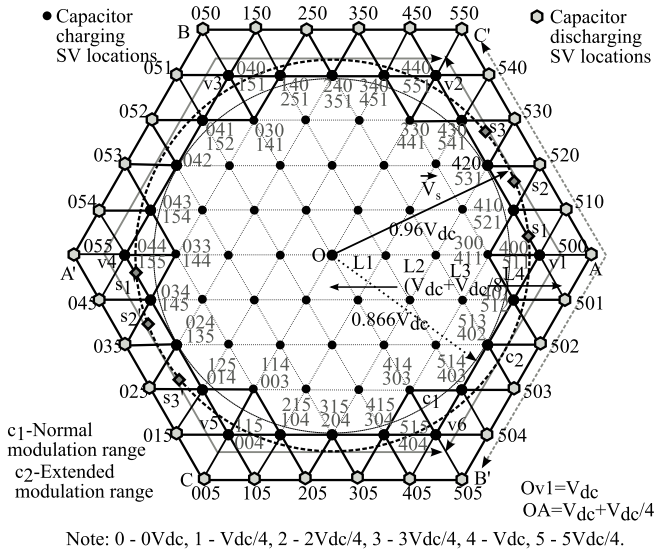


Fig. 2. Five-level space vector structure with extended space vector locations (marked as lightly shaded dots).

as shown by dark dots in Fig. 2. Four concentric hexagons are formed by grouping these 61 space vector locations. The maximum peak of the fundamental output voltage possible with this space vector structure is $0.577V_{\rm dc}$ in the linear modulation range. For getting fundamental voltage more than $0.577V_{\rm dc}$, the inverter needs to be operated in the overmodulation region. This will introduce lower order harmonics in the motor phase voltage and hence in the phase current. Various overmodulation operation algorithms are presented in [17] and [18]. By applying voltage vectors v1–v6 one by one (see Fig. 2) for an equal duration, the maximum peak fundamental voltage possible is $0.637V_{\rm dc}$ (also called the six-step operation and modulation index $m = 1$ for $0.637V_{\rm dc}$ peak fundamental output voltage), and results in substantial amount of fifth- and seventh-order harmonics in the motor phase voltage.

For increasing the peak phase fundamental voltage from 0.577 to $0.637V_{\rm dc}$ with linear control, a six-level space vector structure is formed by including the pole voltage levels $-V_{\rm dc}/4$ and $5V_{\rm dc}/4$. These new 30 space vector locations are shown as lightly shaded dots in Fig. 2. By using these space vector locations, the magnitude of longest vector in the space vector structure shown in Fig. 2 is $V_{\rm dc} + V_{\rm dc}/4$ compared to $V_{\rm dc}$ in the conventional five-level case. When $5V_{\rm dc}/4$ or $-V_{\rm dc}/4$ pole voltage level is used for any phase, the CHB2 floating capacitor can be controlled over a switching cycle and the capacitor charging of CHB1 depends on the load current magnitude and duration of CHB1 switching.

## IV. INVERTER OPERATION WITH EXTENDED SPACE VECTOR LOCATIONS AND CAPACITOR BALANCING

For the inverter topology shown in Fig. 1(a), up to $0.577V_{\rm dc}$, all the capacitors can be controlled over a sampling period. From Table I, observe that there are four redundant switching states for the pole voltage levels $V_{\rm dc}/4$, $2V_{\rm dc}/4$, and $3V_{\rm dc}/4$. For these pole voltage levels, the capacitor charging

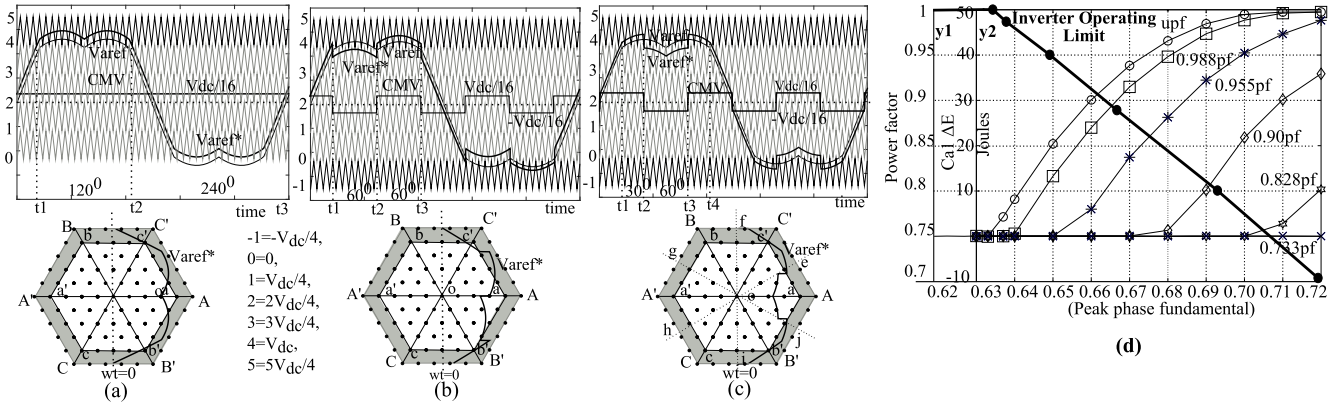


Fig. 3. (a)–(c) Carrier-based SVPWM method for extending the linear modulation range of a cascaded multilevel inverter. (d) Inverter operation (simulated) for various modulation indices and load PFs. The *y*1-axis shows the load PF, the *y*2-axis shows change in capacitor energy after 50 fundamental cycles, and the *x*-axis shows the peak phase fundamental voltage as fraction of $V_{\rm dc}$. The *y*1-axis shows the operating limit (dark line) of the inverter for various load PFs.

can be controlled irrespective of the modulation index, load current direction, and PF. For examining the inverter operation above $0.577V_{\rm dc}$, consider the inverter is operating with a peak phase fundamental voltage of $0.637V_{\rm dc}$ and the inverter current is at full load and unity PF (only phase "a" is considered for analysis, same analysis can be applied for "b" and "c" phases).

### A. SVPWM Method 1

Fig. 3(a) shows the "a" phase reference signal (Varef) for the operation of inverter with $0.637V_{\rm dc}$ peak output voltage. In this method, a $5V_{\rm dc}/4$ pole voltage level is used for inverter operation. A constant common mode voltage (CMV) of $V_{\rm dc}/16$ ($0.637V_{\rm dc} - 0.577V_{\rm dc} \cong V_{\rm dc}/16$) is added to the reference signal to make the reference signal reside within the level shifted carriers. This new reference signal is shown as Varef*. In Fig. 3(a), from time *t*1 to *t*2 (120° duration), the "a" phase reference signal is realized by switched averaging $5V_{\rm dc}/4$ and $V_{\rm dc}$. When $5V_{\rm dc}/4$ is switched and the pole voltage redundancy Se2 [see Fig. 1(d)] is used, capacitor Ca1 discharges and Ca2 charges. If pole voltage redundancy Se1 is used, capacitor Ca1 is bypassed and Ca2 discharges for positive direction of current. The time duration for which the inverter pole remains at $5V_{\rm dc}/4$ will be less than 60° of the fundamental for $0.637V_{\rm dc}$ peak output voltage operation. Now by switching Se1 and Se2 alternatively, the duration for which the capacitor Ca1 discharges continuously will be less than 30° of the reference wave. As shown in Fig. 3(a), from *t*2 to *t*3 the reference voltage is traversing through levels $3V_{\rm dc}/4$, $2V_{\rm dc}/4$, and $V_{\rm dc}/4$. All the capacitor voltage can be controlled for these levels. The charge lost by Ca1 during *t*1–*t*2 can be regained during the time period *t*2–*t*3.

By analyzing the space vector structure shown in Fig. 3(a), "a" phase capacitors Ca1 and Ca2 can be completely controlled for the region C′BA′CB′. Similar analysis can be done for "b" and "c" phase capacitors. For "b" phase, Cb1 always discharges for the region C′BA′ and Cb1 and Cb2 can be completely controlled for the region A′CB′AC′. For "c" phase Cc1 always discharges for the region A′CB′ and Cc1 and Cc2 can be completely controlled for the region B′AC′BA′.

### B. SVPWM Method 2

Fig. 3(b) shows the "a" phase reference signal (Varef) for the operation of inverter with $0.637V_{\rm dc}$ peak output voltage. In this method, pole voltage levels $5V_{\rm dc}/4$ and $-V_{\rm dc}/4$ are used for inverter operation in the extended modulation operation. From Table I, observe that for positive direction of current, the capacitor charging status for $5V_{\rm dc}/4$ and $-V_{\rm dc}/4$ is complementary to each other. This property is used in this SVPWM method to balance the capacitors more quickly than method 1. In this method, a CMV wave of peak-to-peak magnitude $V_{\rm dc}/8$ as shown in Fig. 3(b) is added to the reference voltage Varef to get Varef*. In Fig. 3(b), observe that from time *t*1 to *t*2 (60°) the "a " phase reference voltage is in between the levels $3V_{\rm dc}/4$ and $V_{\rm dc}$. During this region capacitor voltage can be controlled over a sampling period. Again from time *t*2 to *t*3 (60°), the reference voltage is in between $V_{\rm dc}$ and $5V_{\rm dc}/4$. So the capacitor Ca1 continuously discharges for positive direction of current if the switching state Se2 [see Fig. 1(d)] is used. With PWM operation and by using the redundancies Se1 and Se2, the capacitor Ca1 discharge duration can be estimated as less than 15° of the fundamental for $0.637V_{\rm dc}$ peak output voltage operation. Similar analysis can be done for the negative half cycle of the reference voltage. The method of generation of CMV is shown in Table III.

By analysing the space vector structure shown in Fig. 3(b), "a" phase capacitors Ca1 and Ca2 can be completely controlled for the region B′b′aA. In the region Aac′C′, Ca1 discharges if pole voltage redundancy Se2 is used and Ca2 can be controlled. Similar analysis can be done for "b" and "c" phase capacitors. For "b" phase, Cb1 always discharges for the region Bba′A′ and B′b′aA. Cb1 and Cb2 can be completely controlled for the region Bbc′C′ and B′b′cC. For "c" phase Cc1 always discharges for the region B′b′cC and Bbc′C′. Cc1 and Cc2 can be completely controlled for the region Cca′A′ and C′c′aA.

### C. SVPWM Method 3

This method also uses pole voltage levels $5V_{\rm dc}/4$ and $-V_{\rm dc}/4$ for inverter operation. From Table I, observe that for positive direction of current, the capacitor charging status for $5V_{\rm dc}/4$

TABLE III
CMV SELECTION TABLE

| Conditions | | SVPWM CMV | | |
|---|---|---|---|---|
| | | 1 | 2 | 3 |
| Varef > Vbref > Vcref | Vbref < 0 | $V$ | $V$ | $V$ |
| | Vbref ≥ 0 | $V$ | $V$ | $-V$ |
| Vbref > Varef > Vcref | Varef ≥ 0 | $V$ | $-V$ | $-V$ |
| | Varef < 0 | $V$ | $-V$ | $V$ |
| Vbref > Vcref > Varef | Vcref < 0 | $V$ | $V$ | $V$ |
| | Vcref ≥ 0 | $V$ | $V$ | $-V$ |
| Vcref > Vbref > Varef | Vbref ≥ 0 | $V$ | $-V$ | $-V$ |
| | Vbref < 0 | $V$ | $-V$ | $V$ |
| Vcref > Varef > Vbref | Varef < 0 | $V$ | $V$ | $V$ |
| | Varef ≥ 0 | $V$ | $V$ | $-V$ |
| Varef > Vcref > Vbref | Vcref ≥ 0 | $V$ | $-V$ | $-V$ |
| | Vcref < 0 | $V$ | $-V$ | $V$ |

Note: $V = V_{\rm dc}/16$

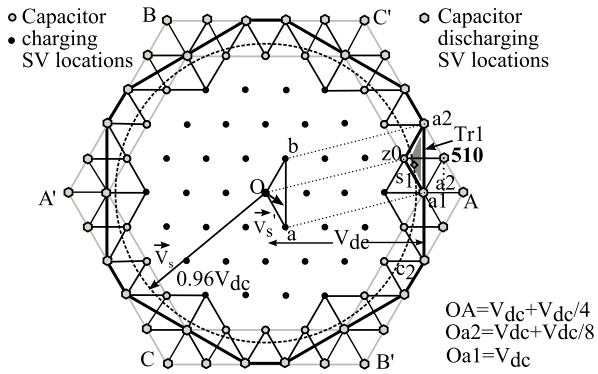


Fig. 4. Space vector structure formed (shown by the dark line) from the five-level space vector structure and extended vectors for overmodulation operation without exceeding the motor phase voltage rating.

and $-V_{\rm dc}/4$ is complementary to each other. In this method, a CMV wave of peak-to-peak magnitude $V_{\rm dc}/8$, as shown in Fig. 3(c), is added to the reference voltage Varef to get Varef*. By using this method, the capacitor discharge duration of (60°) is split into (30°) duration of the fundamental for $0.637V_{\rm dc}$ peak output voltage operation. In Fig. 3(c), observe that, from time *t*1 to *t*2 (30°), the "a" phase reference voltage is in between the levels $5V_{\rm dc}/4$ and $V_{\rm dc}$. During this region, capacitor Ca1 discharges if pole voltage redundancy Se2 is used. From time *t*2 to *t*3 (60°) the reference voltage is in between $V_{\rm dc}$ and $3V_{\rm dc}/4$. Both the capacitors Ca1 and Ca2 can be completely controlled over a sampling period during this region. Again from *t*3 to *t*4, reference voltage is in between the levels $5V_{\rm dc}/4$ and $V_{\rm dc}$ and Ca1 discharges if pole voltage redundancy Se2 is used. With PWM operation and by using the pole voltage redundancies Se1 and Se2 alternatively, the capacitor Ca1 discharge duration can be estimated as less than 7.5° of the reference signal (Varef) for $0.637V_{\rm dc}$ peak output voltage operation. So by using this method, the capacitor size reduces substantially. The method of generation of CMV is shown in Table III. By analysing the space vector structure shown in Fig. 3(c), "a" phase capacitors Ca1 and Ca2 can be completely controlled over the region eOjA. Similar analysis can be done for "b" and "c" phase capacitors.

The description above conveyed that the capacitor Cx1 charge balancing of each phase depends on the modulation index and load current PF for all the SVPWM methods discussed. The capacitor charge of Ca1 over a fundamental cycle is proportional to the time period for which the CHB1 of "a" phase is operated. The operating time period of CHB1 is obtained from the level-shifted carrier-based SVPWM algorithm presented and the switching function from the charge controller. The capacitor Ca1 charge "Qa1" over a fundamental cycle is given by

$$\mathrm{Qa1} = \sum_{n=1}^{N} (\mathrm{Sa1} - \mathrm{Sa2})(I_m \sin(\mathrm{wt} - \phi))\mathrm{Tga(nT)} \quad (1)$$

$$\mathrm{Vca1f} = \frac{\mathrm{Qa1}}{C} + \mathrm{Vca1in} \quad (2)$$

$$\mathrm{Eca1} = \frac{1}{2} C(\mathrm{Vca1in}^2 - \mathrm{Vca1f}^2) \quad (3)$$

where Tga(nT) is the "a" phase reference voltage (measure of modulation index), $(\mathrm{Sa1} - \mathrm{Sa2})$ is the CHB1 switching function, $I_m$ is the peak value of load current, $\phi$ is the load PF, Vca1in is the initial voltage of capacitor Ca1 at the start of fundamental, Vca1f is the voltage of capacitor Ca1 at the end of fundamental cycle, $N$ is the number of samples per cycle, and *C* is the capacitance value of Ca1. The expression given in (1) is simulated in MATLAB-Simulink for various modulation index and PF (peak load current is taken as a full load motor current and is kept constant) to find the operating limit and Fig. 3(d) shows the results (SVPWM method 3 is used for the implementation and is considered for analysis). Using (1), capacitor energy can be calculated for every sampling instant. The change in capacitor energy for 50 fundamental cycles for various modulation indexes and PFs is indicated by *y*2-axis of Fig. 3(d). From Fig. 3(d) (*y*1-axis), it can be seen that inverter can be operated up to $0.633V_{\rm dc}$ for unity PF operation and $0.637V_{\rm dc}$ for a PF of 0.988 lagging or leading. Normally, the full load PF of the induction motor is nearly 0.9 lag and the inverter can be used for full speed range operation of induction motor ($0.637V_{\rm dc}$) without going into the overmodulation operation. The advantage of this inverter operation is the linear control of the inverter, lower order harmonics elimination, torque ripple reduction, and faster response. Furthermore, the inverter can generate fundamental voltage output of $0.66V_{\rm dc}$ for a PF of 0.9 lag/lead and $0.72V_{\rm dc}$ for a PF of 0.73 lag/lead [see Fig. 3(d)]. This means that the inverter will remain in the linear modulation range during the event of small short-term dc-link voltage sags also. The simulation results of various SVPWM schemes with motor phase voltage, capacitor voltages Vca1 and Vca2, phase current (*ia*) at 0.99 PF lag, and phase voltage frequency spectrum for the inverter operation at $0.637V_{\rm dc}$ are shown in Fig. 6. Observe that for the same capacitance value for Ca1 and for SVPWM scheme 3, the capacitor voltage ripple is lower compared to the other schemes.

For the inverter operation with the space vector diagram shown in Fig. 4, switching of the vector 510 results in exceeding the machine phase voltage by 12.5%. This can be avoided by modifying the space vector structure as shown in Fig. 4 (dark line). The PWM timing is obtained by using a special

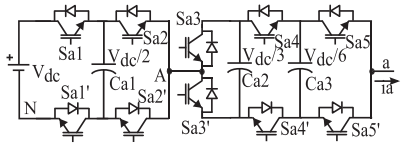


Fig. 5. Phase "a" of a seven level inverter topology (INV-2) with a single dc supply with reduced switch count and reduced switch voltage rating for extending the linear modulation range.

triangle search algorithm along with the conventional SVPWM algorithm.

The proposed SVPWM technique can also be used for extending the modulation range of a seven-level inverter topology, as shown in Fig. 5 [24]. The advantage of this topology is reduced number of switches for seven-level operation and reduced switch voltage rating. From the numerical simulations, this inverter topology can generate fundamental voltage output up to $0.625V_{\rm dc}$ at unity PF operation and $0.637V_{\rm dc}$ at 0.93 PF lag/lead. The proposed extended modulation technique can also be applied to the inverter topologies presented in [25] and [26]. The cascaded inverter topologies INV-1 [see Fig. 1(a)] and INV-2 (see Fig. 5) are compared with other conventional inverter topologies on the basis of peak fundamental output voltage with linear operation, capacitor requirement, switch requirement, and power supply requirement, as shown in Table IV.

## V. Experimental Results

A three-phase, 400 V, 3 kW, 50 Hz induction motor with an open loop V/f control scheme is implemented in hardware for testing the five level inverter topology. A DSP (TMS320F28335) is used as main controller and an FPGA (Xilinx SPARTAN-3 XC3S200) is used as the PWM signal generator with a dead time of 2.5 $\mu$s. A level-shifted carrier-based PWM algorithm [27] is implemented for lower modulation index operation. At higher modulation indixes, a special triangle search algorithm is used along with the carrier-based SVPWM to avoid exceeding the motor voltage rating. From the SVPWM algorithm, information about the pole voltage levels to be switched can be obtained for each phase. The capacitor voltage controller selects a switching state (from Table II) by processing the level data and hysteresis controller outputs. The switching state information of all the three phases and PWM signals are send to the FPGA module. The FPGA module processes these signals and add a dead time of 2.5 $\mu$s for the complementary switches on the leading edge or trailing edge based on the current direction.

The capacitor sizing of Cx2 is done by using the relation $C = I_p T_s/\Delta V_c$, where $C$ is the capacitance value of Ca2, Cb2, and Cc2, $I_p$ is the peak load current, $\Delta V_c$ is the peak to peak voltage ripple, and $T_s$ is the inverter switching time. In order to design capacitance values, a worst case switching frequency of 900 Hz is selected. For 2% peak-to-peak voltage ripple, capacitance value of 2200$\mu$ F is selected for Cx2 (x = a, b, and c) of all the three phase capacitors for conducting the experiment. For sizing the capacitor Cx1, it is required to find the total time period for which the capacitor is discharging. For $0.637V_{\rm dc}$, fundamental output voltage with SVPWM method 3, inverter pole "a" goes to level 5 during the 30° region B′jO [see Fig. 3(c)]. The total time period for which the inverter pole is at level 5 can be approximated as 15° of the fundamental cycle for $0.637V_{\rm dc}$ operation. Again, considering the interleaved capacitor switching, the duration for which the capacitor Ca1 discharges continuously can be approximated as 7.5° of fundamental cycle. From the simulation results, for $0.637V_{\rm dc}$ peak phase fundamental output voltage operation, the time duration for which the capacitor Ca1 is discharged continuously is found to be 0.3 ms. From this information, capacitor sizing of Cx1 can be obtained as 1500 $\mu$ F for a voltage ripple of 2% and peak load current of 10 A. For conducting the experiment, capacitance value of 2200 $\mu$ F is selected for Cx1.

The induction motor is run at frequencies of 10 Hz [modulation index ($m$) = 0.2] with reference voltage vector tracing the region inside L1 (see Fig. 2), 20 Hz ($m$ = 0.4) with reference voltage vector tracing the region L2, and 45 Hz ($m$ = 0.866, $0.577V_{\rm dc}$) with reference voltage vector tracing the region L4 at no load. The experimental result for 45 Hz ($0.577V_{\rm dc}$) operation showing the motor phase voltage ($V_{\rm an}$), inverter pole voltage ($V_{\rm an}$), CHB1 capacitor voltage (Vca1), and CHB1 capacitor voltage ripple ($\Delta$Vca1) along with the phase current ($i_a$) for phase "a" is shown in Fig. 10(a).Fig. 7 shows the motor phase voltage ($V_{\rm an}$), inverter pole voltage ($V_{\rm an}$), CHB1 capacitor voltage ripple ($\Delta$Vca1), and CHB2 capacitor voltage ripple ($\Delta$Vca2) along with the phase current ($i_a$) for phase "a" for $0.637V_{\rm dc}$ operation of the inverter for all the three SVPWM technique discussed in Section IV. Fig. 9(a) shows the $0.637V_{\rm dc}$ operation of the inverter without exceeding the machine voltage rating with SVPWM method 3.Fig. 9(a) shows the motor phase voltage ($V_{\rm an}$), CHB1 and CHB2 capacitor voltage, CHB1 and CHB2 capacitor voltage ripple, and phase current ($i_a$) for $0.637V_{\rm dc}$ operation. Observe that all the capacitor voltages are within the designed limits. Fig. 9(b) shows the inverter pole voltage ($V_{\rm an}$), two-level inverter pole voltage ($V_{A2N}$), CHB1 pole voltage ($V_{A1A2}$), and CHB2 pole voltage ($V_{aA1}$) for $0.637V_{\rm dc}$ operation with SVPWM method 3. It can be observed that the higher voltage inverter switches less for this mode of operation. In Fig. 8(a), the six-step operation of the five-level inverter with a dc-link voltage of 300 V is shown. The inverter pole voltage ($V_{\rm an}$), motor $\alpha$-axis voltage ($V_\alpha$), motor $\beta$-axis voltage ($V_\beta$), and motor phase current ( $i_a$) are shown in Fig. 8(a). The plot of $V_\alpha$ and $V_\beta$ (which is a hexagon) is also shown in Fig. 8(a). It can be seen that lower order harmonics are present in motor phase current. In Fig. 8(c), the inverter pole voltage ($V_{\rm an}$), motor $\alpha$-axis voltage ($V_\alpha$), motor $\beta$-axis voltage ($V_\beta$), and motor phase current ($i_a$) are shown for proposed operation of inverter with SVPWM method 3. The plot of $V_\alpha$ and $V_\beta$ is also shown in Fig. 8(c). The average of the ($V_\alpha$ and $V_\beta$) plot traces a circle. This means that for the same fundamental voltage as that of the six-step operation, the proposed inverter operation results in elimination of lower order harmonics. The motor phase voltage harmonic spectrum for conventional six-step operation ($0.637V_{\rm dc}$) and for new method (SVPWM-3) is shown in Fig. 8(b) and (d). It can be seen that with the same fundamental voltage, the lower order harmonics are eliminated with the new method (SVPWM-3) .

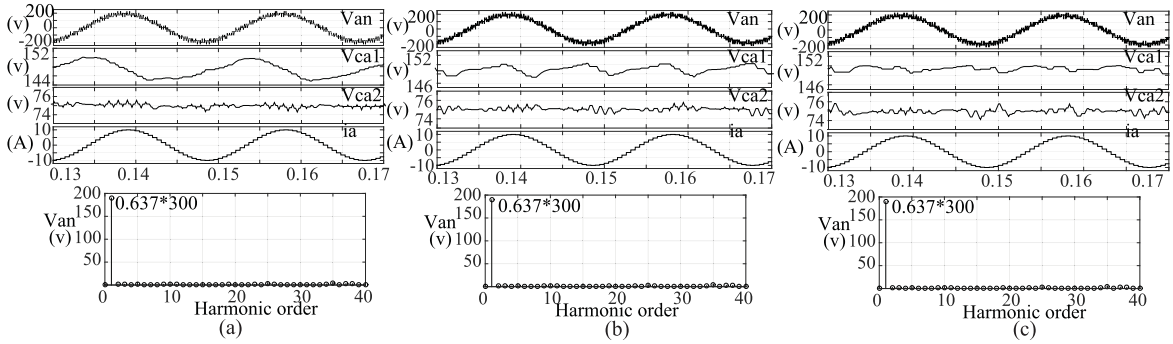


Fig. 6. Simulation results showing the motor phase voltage ($V_{\rm an}$), reference signal (Tga), $V_{\rm dc}/2$ capacitor voltage ripple ($\Delta$Vca1), $V_{\rm dc}/4$ capacitor voltage ripple ($\Delta$Vca2), load current ($i_a$), and motor phase voltage ($V_{\rm an}$) frequency spectrum at 0.988 PF lag for phase "a" for $0.637V_{\rm dc}$ operation. (a) SVPWM scheme 1, (b) SVPWM scheme 2, (c) SVPWM scheme 3.

TABLE IV
CASCADED INVERTER TOPOLOGY INV-1 AND INV-2 IS COMPARED WITH OTHER INVERTER TOPOLOGIES

| Inverter topology | Levels | End of linear modulation range | Linear control | Capacitors | | IGBT | | | | | Clamping diodes | | Power supply | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $\frac{V_{\rm dc}}{4}$ | $\frac{V_{\rm dc}}{6}$ | $V_{\rm dc}$ | $\frac{V_{\rm dc}}{2}$ | $\frac{V_{\rm dc}}{3}$ | $\frac{V_{\rm dc}}{4}$ | $\frac{V_{\rm dc}}{6}$ | $\frac{V_{\rm dc}}{4}$ | $\frac{V_{\rm dc}}{6}$ | $V_{\rm dc}$ | $\frac{V_{\rm dc}}{6}$ | $\frac{V_{\rm dc}}{4}$ |
| INV-1 | 5 +1 | $0.637V_{\rm dc}$ | up to $0.637V_{\rm dc}$ | 9 | 0 | 6 | 12 | 0 | 12 | 0 | 0 | 0 | 1 | 0 | 0 |
| NPC | 5 | $0.577V_{\rm dc}$ | up to $0.577V_{\rm dc}$ | 4 | 0 | 0 | 0 | 0 | 24 | 0 | 36 | 0 | 1 | 0 | 0 |
| FC | 5 | $0.577V_{\rm dc}$ | up to $0.577V_{\rm dc}$ | 18 | 0 | 0 | 0 | 0 | 24 | 0 | 0 | 0 | 1 | 0 | 0 |
| CHB | 5 | $0.577V_{\rm dc}$ | up to $0.577V_{\rm dc}$ | 0 | 0 | 0 | 0 | 0 | 0 | 36 | 0 | 0 | 0 | 0 | 6 |
| INV-2 | 7 + 1 | $0.637V_{\rm dc}$ | up to $0.637V_{\rm dc}$ | 0 | 18 | 0 | 12 | 6 | 0 | 12 | 0 | 0 | 1 | 0 | 0 |
| NPC | 7 | $0.577V_{\rm dc}$ | up to $0.577V_{\rm dc}$ | 0 | 6 | 0 | 0 | 0 | 0 | 36 | 0 | 90 | 1 | 0 | 0 |

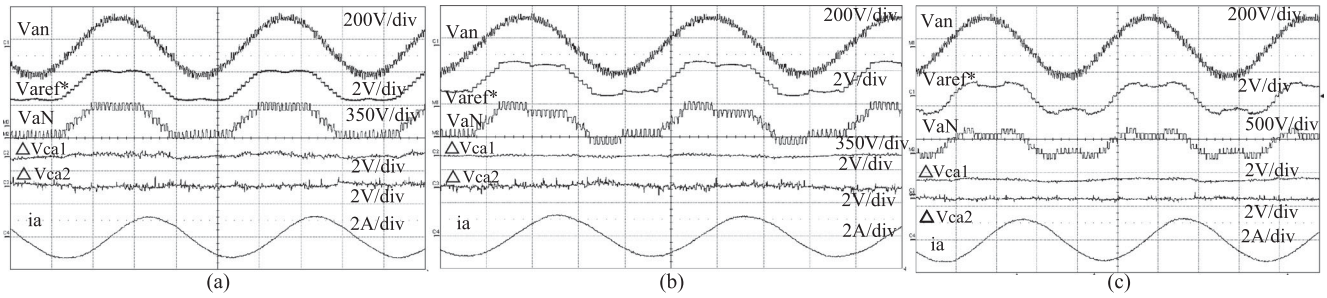


Fig. 7. Motor phase voltage ($V_{\rm an}$), "a" phase reference voltage (Varef$^*$), inverter pole voltage ($V_{\rm an}$), $V_{\rm dc}/2$ capacitor voltage ripple ($\Delta$Vca1), $V_{\rm dc}/4$ capacitor voltage ($\Delta$Vca2), and phase current ($i_a$) for phase "a" for full modulation index ($V_{\rm an} = 0.637V_{\rm dc}$). (a) 50 Hz operation with SVPWM method 1 and modulation index of 1. (b) 50 Hz operation with SVPWM method 2 and modulation index of 1. (c) 50 Hz operation with SVPWM method 3 and modulation index of 1. Time scale: 5 ms/div.

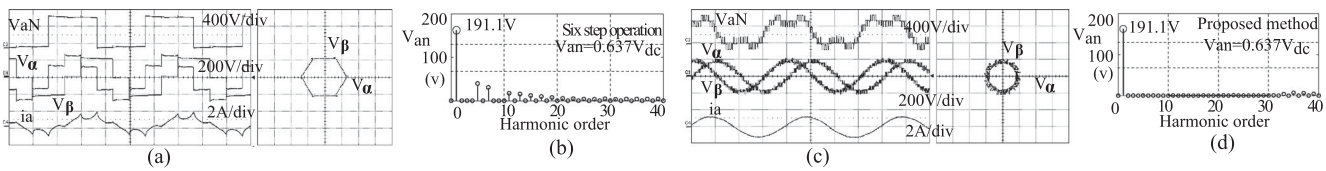


Fig. 8. (a) Inverter pole voltage ($V_{\rm an}$), motor $\alpha$-axis voltage ($V_\alpha$), motor $\beta$-axis voltage ($V_\beta$), and motor phase current ($i_a$) and ($V_\alpha$, $V_\beta$) plot for six-step operation ($0.637V_{\rm dc}$) of a five-level inverter. (c) Inverter pole voltage ($V_{\rm AN}$), motor $\alpha$-axis voltage ($V_\alpha$), motor $\beta$-axis voltage ($V_\beta$), and motor phase current ($i_a$) and ($V_\alpha$, $V_\beta$) plot for the new method of operation ($0.637V_{\rm dc}$) of the inverter. (b) and (d) Frequency spectrum of motor phase voltage for six-step operation and new method.

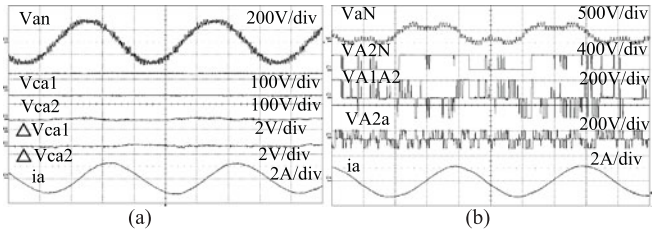


Fig. 9. (a) Motor phase voltage ($V_{\rm an}$), inverter pole voltage ($V_{\rm an}$), CHB1—$V_{\rm dc}/2$ capacitor voltage (Vca1), CHB2—$V_{\rm dc}/4$ capacitor voltage (Vca2), CHB1—$V_{\rm dc}/2$ capacitor voltage ripple ($\Delta$Vca1), and CHB2—$V_{\rm dc}/4$ capacitor voltage ripple ($\Delta$Vca2) along with phase current ($i_a$) for phase "a" for $0.637V_{\rm dc}$ operation with SVPWM method 3 and without exceeding the machine phase voltage rating. Time scale: 5 ms/div. (b) Inverter pole voltage ($V_{\rm an}$), two-level inverter pole voltage ($V_{A2N}$), CHB1 pole voltage ($V_{A1A2}$), and CHB2 pole voltage ($V_{aA1}$) for $0.637V_{\rm dc}$ operation with SVPWM method 3. Time scale: 5 ms/div.

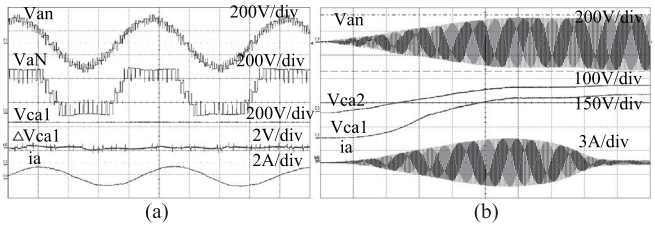


Fig. 10. (a) Motor phase voltage ($V_{\rm an}$), inverter pole voltage ($V_{\rm an}$), $V_{\rm dc}/2$ capacitor voltage (Vca1), $V_{\rm dc}/2$ capacitor voltage ripple ($\Delta$Vca1), and phase current ($i_a$) for phase "a" for 45 Hz with modulation index 0.866 ($0.577V_{\rm dc}$). Time scale: 5 ms/div. (b) Experimental results showing charging of capacitor voltages to the reference voltage for phase "a" when the inverter is switched ON for modulation index corresponding to $0.637V_{\rm dc}$ fundamental output voltage. Wave forms shown are motor phase voltage ($V_{\rm an}$), $V_{\rm dc}/2$ capacitor voltage (Vca1), $V_{\rm dc}/4$ capacitor voltage (Vca2), and phase current ($i_a$). Time scale: 0.5 s/div.

The proposed method has to give satisfactory results for dynamic conditions also. First of all, the inverter should automatically charge the capacitors to its reference voltage independent of the modulation index. This feature is tested by turning on the inverter with all the capacitors in the discharged state for $0.637V_{\rm dc}$ operation with SVPWM method 3.Fig. 10(b) shows that the inverter automatically charges the capacitors to its reference value within a few cycles. Also during startup, induction motor rotor speed is nearly zero (slip is very high) for a few cycles of fundamental voltage. Motor draws higher than rated current (0.5–0.6 PF) during this operation. Fig. 10(b) shows that both the capacitors are continuously charging for the start-up operation and this indicates that the inverter can be operated without any capacitor precharging circuit at any load condition for $0.637V_{\rm dc}$. Fig. 11(a) shows the motor phase voltage ($V_{\rm an}$), CHB1 capacitor voltage (Vca1), CHB2 capacitor voltage (Vca2) along with the machine current ($i_a$) for an acceleration of the motor from 40 to 50 Hz in 1 s with SVPWM method 3. It can be seen that the capacitor voltages are tightly controlled and are within the hysteresis band for this operation. The effectiveness of the capacitor voltage balancing algorithm for the full modulation index operation ($0.637V_{\rm dc}$) with SVPWM method 3 is tested by disabling the voltage balancing algorithm at time $T_d$ and then reenabling at $T_e$. Fig. 11(b) shows that the capacitor voltages start deviating from the reference at $T_d$ and then coming back to the reference after several fundamental cycles when the balancing algorithm is reenabled at $T_e$.

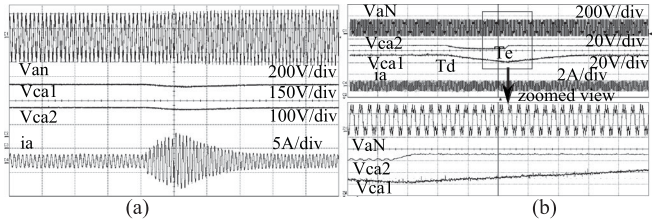


Fig. 11. (a) Experimental results showing quick acceleration of motor from 40 to 50 Hz. Wave forms shown are motor phase voltage ($V_{\rm an}$), $V_{\rm dc}/2$ capacitor voltage (Vca1), $V_{\rm dc}/4$ capacitor voltage (Vca2), and phase current ($i_a$). Time scale: 0.2 s/div, (b) Experimental results show the stability of capacitor voltage balancing algorithm. Capacitor voltage balancing algorithm is disabled at time $T_d$ and again reenabled at $T_e$. Wave forms shown are inverter pole voltage ($V_{\rm an}$), $V_{\rm dc}/2$ capacitor voltage (Vca1), $V_{\rm dc}/4$ capacitor voltage (Vca2), and phase current ($i_a$). Time scale: 0.5 s/div.

## VI. Conclusion

In this paper, SVPWM methods to extend the linear modulation range to the full base speed of the induction motor using a five-level cascaded inverter topology with a single dc supply without exceeding the motor phase voltage is presented. Using the method presented in this paper, the inverter can be controlled linearly in the conventional overmodulation region ($0.577$–$0.637V_{\rm dc}$). By using this technique, induction motor drives can be operated to the full speed range without increasing the dc-link voltage and without having any lower order harmonics (5th, 7th, 11th, and 13th) in the phase current and the induction motor electromagnetic torque pulsation also gets reduced. The inverter can also be operated in the linear modulation range during short-term voltage sags in the dc link.

The overmodulation operation of the cascaded inverter topology with a single dc supply is analyzed extensively and simulation and steady state experimental results are presented in this paper. The dynamic experimental results showing the stable operation of the inverter in the overmodulation region is presented to validate the new technique. The capacitor balancing technique presented can be applied to other cascaded multilevel inverter topologies with at least two floating capacitors (capacitor voltage needs to be summable to dc bus voltage).

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