Efficient Substrate Noise Coupling Verification and Failure Analysis Methodology for Smart Power ICs in Automotive Applications

Yasser Moursy, Hao Zou, Raouf Khalil, Ramy Iskander, Pierre Tisserand, Dieu-My Ton, Giuseppe Pasetti, and Marie-Minerve Louërat

***Abstract*—This paper presents a methodology to analyze the substrate noise coupling and reduce their effects in smart power integrated circuits. This methodology considers the propagation of minority carriers in the substrate. Hence, it models the lateral bipolar junction transistors that are layout dependent and are not modeled in conventional substrate extraction tools. It allows the designer to simulate substrate currents and check their effects on circuits functionality. The proposed methodology employs a dedicated tool for substrate network generation referred to as AUTOMICS. We applied the methodology on two test cases. The first case is a dc–dc buck converter chip fabricated with a 0.35 μm high-voltage-CMOS technology. The dc coupling current between the switches and the bandgap circuit is simulated and verified with measurements. The second test case is an automotive industrial chip that has a latch-up failure due to substrate coupling. In transient simulations, the failure has been reproduced as in measurements. This highlights the stronghold of the methodology since it can be used to prevent this type of failures before fabrication. The proposed methodology can reduce the number of redesigns in the automotive industry. Hence, it shortens the time-to-market, improves the robustness of the design, and reduces the cost.**

***Index Terms*—DC–DC power conversion, failure analysis, power FET switches, semiconductor device modeling, semiconductor device noise.**

I. Introduction

NOWADAYS, the electronic systems are extensively employed in the automotive industry. These emerging technologies are mainly deployed to offer safer and more comfortable environment for the automobile driver. The trend in the automotive technology is to enhance the vehicle connectivity to the internet as a part of Internet of Things and to reduce the CO_2 emission. Furthermore, the reliability and durability are the main two features for the automotive electronic applications.

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Smart power ICs are employed in the automotive industry since they incorporate the high-voltage (HV) and low-voltage (LV) circuits on the same die [1]. This feature allows us to miniaturize the electronic systems and implement more functionality in the vehicles. However, the substrate noise coupling in the smart power ICs becomes a severe issue. Failures due to the substrate noise coupling are still reported in tests after fabrication. Most of these failures are caused by the minority carriers propagation since their behavior cannot be predicted by the current commercial tools. Therefore, we need to investigate the minority carriers propagation in the substrate and their modeling techniques to validate the capability of simulation for such complicated behavior.

In smart power ICs, the HV circuits commonly drive inductive loads. The presence of such loads stimulates parasitic components and injects minority carriers in the substrate. The noise due to minority carriers injection is a function of the operating voltages and currents. This noise becomes nonnegligible and can cause significant effects, such as latch-up. Therefore, techniques were investigated to study the substrate coupling due to the minority carriers propagation. In [2], the noise in smart power ICs was addressed and a TCAD-guided design methodology for substrate current investigation was proposed. Addressing more complex structure with this methodology could be impractical as it takes excessively long time. In [3], the PN junction and resistor models were modified by additional terminal to take into account the minority carrier concentrations and gradients at the boundaries. These enhanced models can be used to create a substrate network which considers the minority carriers propagation in the substrate. A manually extracted three-dimensional substrate parasitic network was simulated and the dc coupling between HV devices was shown [4]. However, the substrate network was extracted manually that would be tedious for large circuit analyses and the injected current levels in the substrate were considerably low.

The enhanced models were modified in [5] to simulate high levels of injected currents. The capacitive components in the PN junction were modeled in [6]. These components are essential in transient simulations. In order to emulate the large difference in doping concentrations, a model, which is referred to as homojunction model, was developed. The doping concentration discontinuity affects the minority carriers propagation [7]. Therefore, the substrate can be modeled using three enhanced

components, which are the enhanced diode, enhanced resistor, and enhanced homojunction models that are simulated in SPICE environment.

The main objective of this paper is to propose analysis and verification methodology for substrate noise coupling effects in HV applications. It can be used to analyze failures that occur due to minority carriers coupling. Since this methodology is able to detect the failures in simulation environment, it can be used to prevent these failures before fabrication. Hence, it reduces the time-to-market and reduces the product cost. It relies on automatically extracting the substrate parasitic components from the layout. The tool used for the extraction and constructing the equivalent substrate network is called AUTOMICS.

This paper is organized as follows. Section II discusses the AUTOMICS substrate extraction framework. In Section III, the proposed methodology for substrate noise analysis is explained. The substrate coupling in a dc–dc buck converter test case is elaborated in Section IV. DC simulation results for the substrate parasitic currents in dc–dc buck converter circuit are compared with measurements. Section V shows an industrial test case (AUTOCHIP1). Transient simulations are performed to reproduce a failure that occurs due to minority carriers coupling. Finally, the conclusions are drawn in Section VI.

II. AUTOMICS: Pragmatic Substrate Parasitic Extraction Framework

One of the keys to alleviate failures after fabrication is to model the lateral NPN parasitic transistors. These parasitic components are layout dependent and their parameters cannot be extracted automatically by the current extraction tools. They inherently model the minority carriers propagation in the substrate. The enhanced diodes, resistors, and homojunction models allow modeling these parasitic components [8]. AUTOMICS is a parasitic extraction tool that is capable of modeling the substrate including the minority carriers propagation. This tool uses the enhanced components to construct the substrate equivalent network. It is developed using the "openAccess" open source application programming interface. The extraction procedure has the following two steps:

1) geometrical features extraction using AUTOMICS tool;
2) technological parameters calibration.

AUTOMICS tool flow starts with the geometrical features extraction of the parasitic components in the layout. The inputs and outputs of the tool are depicted in Fig. 1. The main flow of the tool can be divided into three main stages [8], [9]: preprocessing stage, extraction stage, and postprocessing stage. The input is the layout of the design. A reduction mechanism is used to filter out the layers that do not contribute in the substrate parasitic coupling such as metal and poly-silicon layers. This reduction is essential to simplify the extracted netlist meanwhile keeping the most relevant information for the parasitic coupling analysis [10]. An adaptive meshing strategy is used to reduce the number of the components [11]. The meshing in the vertical direction can significantly affect the results as shown in [12] and [13]. Hence, fine meshing is used along the substrate depth. A netlist describing the extracted parasitic components connections is generated.

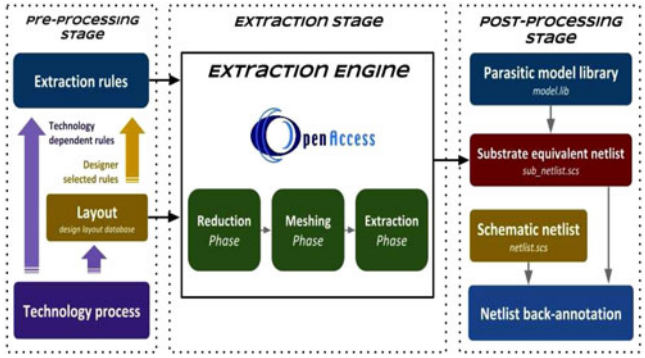

Fig. 1. AUTOMICS substrate parasitic extraction flow [8].

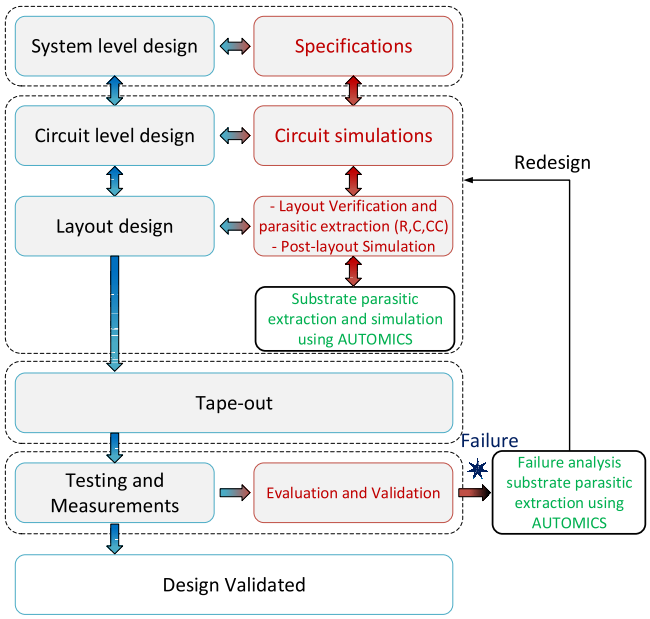

Fig. 2. Proposed smart power IC design flow to extract the substrate parasitic components using the AUTOMICS tool in verification and failure analyses steps.

The technology parameters calibration is performed using industrial test benches. Various test structures are fabricated for the 0.35 μm HV-CMOS technology provided by AMS. Then, these test structures are extracted with AUTOMICS tool and parameters calibration is performed to fit the simulation results and measurements [14].

III. Proposed Smart Power ICs Verification Methodology

The design flow starts with a set of product specifications as shown in Fig. 2. System- and circuit-level models are built to achieve these specifications. In the layout design, many techniques are used for matching and reducing the coupling between different cells [15]. The layout parasitic components are extracted, which are mainly the routing metal layers parasitic resistors, capacitors, and the coupling capacitors between different metal layers. The design modifications in these different

steps are possible; however, each step down in the flow the modification becomes a burdensome task.

Eventually, the chip is available and ready for further testing and measurements to validate and evaluate its functionality. If the chip manages to pass all these tests then the cycle of the design is done and the product is approved. On the contrary, if the product fails in one critical test then we have to start a failure analysis to identify the root cause of the failure and how to avoid it. The failure analysis depends on measurements and hand analysis to locate the root cause. The designer experience plays a major role in this step. After identifying the problem, the redesign cycle starts. Such failures would prolong the design cycle and increase the time-to-market and certainly increase the cost. In practice, this redesign cycle could be repeated several times for one product.

Failures due to the substrate coupling are principally caused by the activation of the lateral parasitic NPN bipolar junction transistor. The conventional state-of-the-art modeling technique is based on TCAD simulations [2], [16]. In addition to the TCAD simulations, fabricated test benches are used to characterize the lateral NPN transistor and set guidelines for the designer to reduce the substrate coupling noise.

The basic concept of the proposed methodology depends on the ability to simulate the failures due to substrate coupling as shown in Fig. 2. If we successfully reproduce the failures, then we are able to prevent such failures before the fabrication. Consequently, the number of redesigns is reduced and hence, the cost and time-to-market are reduced. Besides, all the simulations are done in a SPICE-like simulator environment; hence, the simulation time is significantly shorter than TCAD simulations.

The proposed design flow has two additional stages in the design flow which are as follows:

1) failure analysis and reproduction;
2) substrate parasitic extraction step.

A. Failure Analysis and Reproduction

objective of this stage is to reproduce a failure occurred in a test chip on the simulation environment. After the preliminary failure diagnoses, the failure analysis engineer anticipates that the substrate coupling could be the cause of failure. Then, as shown in Fig. 3, the conventional substrate failure analysis is based on the substrate parasitic components hand extraction. Long time may be spent in the parasitic hand extraction.

sed step is to replace this hand parasitic extraction with automated parasitic extraction using AUTOMICS. With the fast parasitic extraction method, the failure root cause could be identified in short time. This proposed methodology could speed up the failure analysis and add comprehensive explanations based on the substrate noise coupling simulations that can be done. It should be noted that this methodology is based on the preliminary failure analysis decision that the failure is due to the substrate coupling. Hence, it is not a fully automated failure analysis tool.

B. Substrate Parasitic Extraction Step

The substrate parasitic components are extracted from the layout using AUTOMICS tool. The designer can select an active

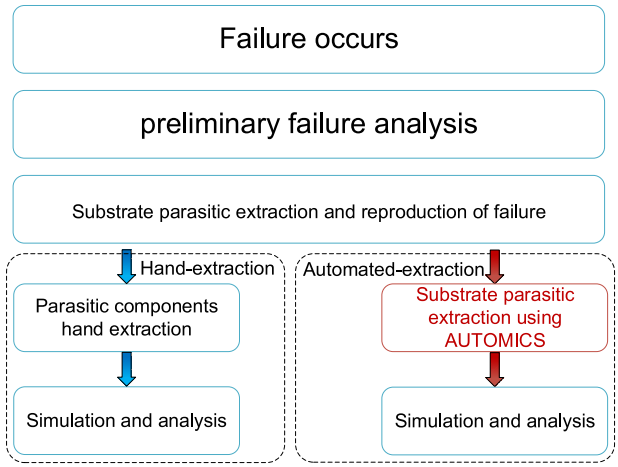

Fig. 3. Proposed failure analysis due to substrate coupling using AUTOMICS tool.

area for extraction. This area would contain an aggressor and a victim. The aggressor is expected to inject minority carriers in the substrate that most probably is an HV switch. The victim is a sensitive circuit to this substrate current that can disturb the operation of the whole system such as a bandgap or an oscillator circuits.

The substrate simulations give the designer an estimation for the coupling substrate currents. This information can be used as a guideline to improve isolation techniques, i.e., guard rings. The substrate extracted netlist can be back annotated to the original design and simulated to check the substrate coupling effects on the original circuit. DC analyses can be done to estimate the amount of dc substrate current coupled to different wells on the substrate. In addition to dc analyses, transient simulations show effects due to junction and diffusion capacitances of different wells on the same substrate.

The usage of the proposed methodology as a verification step before fabrication clarifies the substrate noise coupling effects. Hence, it provides quantitative guidelines to take the proper precautions to reduce the substrate coupling. We are going to apply the proposed methodology in dc and transient simulations on two different test cases in the next sections.

IV. DC Simulation Test Case: DC–DC Buck Converter

In this section, we apply the methodology to simulate the substrate coupling current between HV switches and the bandgap circuit. Then, we illustrate the effect of these minority carriers coupling on the bandgap operation. The dc simulation results and measurements are shown.

A. DC-DC Buck Converter Circuit Operation

The dc–dc buck converter is used to step-down the input voltage to a well-controlled output voltage. A feedback control loop is used to maintain the output voltage constant [17], [18]. Fig. 4 shows our chip basic building blocks on the circuit level. The inductor, capacitor, and load resistance are off-chip components. The chip has three input power supplies: the HV supply (HV_Vin), the low bias voltage for the high-side (HS) switch

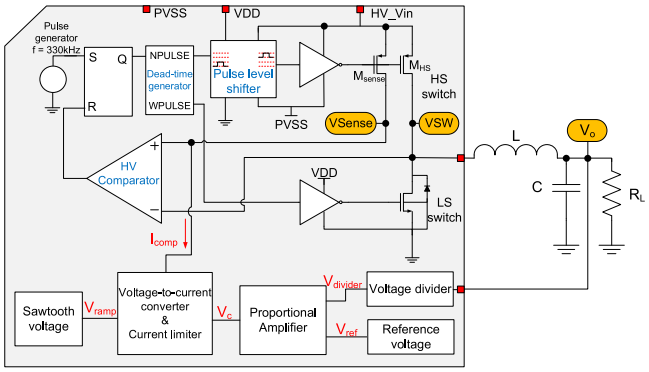

Fig. 4. Basic circuit operation of the designed CPM buck converter.

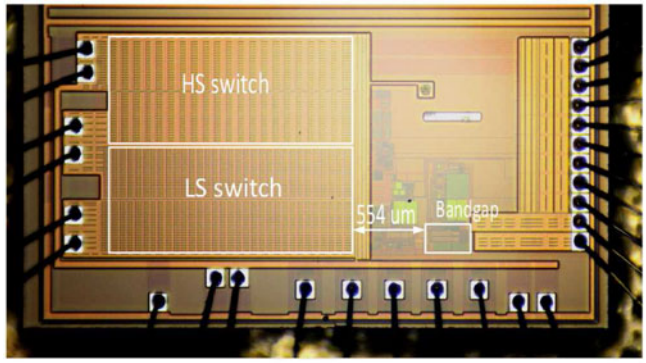

Fig. 6. DC–DC converter chip die photo.

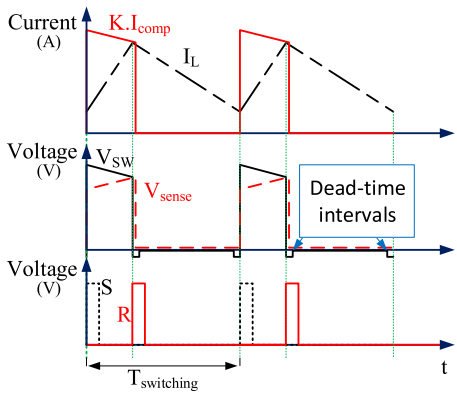

Fig. 5. Transient signals of the inductor current (I_L) and the scaled sense current ($K.I_{\rm comp}$), the sense voltage ($V_{\rm sense}$) and the switching node voltage ($V_{\rm sw}$), and the set and reset signals.

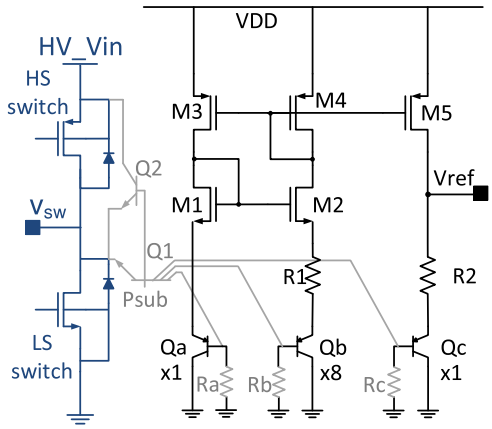

Fig. 7. Bandgap circuit with the output stage. The grey components represent the parasitic components. The resistances $R_{a,b,c}$ represent the parasitic contact resistances to ground. Q1 and Q2 are the lateral NPN transistors.

driver (PVSS), the LV supply (VDD). The HV input (HV_Vin) ranges from 5 to 15 V while the LV bias (VDD) is 5 V. Since the gate source of the used HS switch cannot sustain voltages higher than 5 V, the HS buffer swing is limited to HV_Vin and PVSS where PVSS = HV_Vin − 5 V.

The condition for switching OFF the HS switch can be expressed as

$$V_{\rm sw} < V_{\rm Sense}$$
$$\text{HV\_Vin} - I_L \times R_{\rm HS} < \text{HV\_Vin} - I_{\rm comp} \times R_{\rm sense}$$
$$I_L > K \times I_{\rm comp}$$

where Vsw and $V_{\rm Sense}$ are the switching and the sense nodes voltages, I_L and $I_{\rm comp}$ are the inductor and compensated control currents, $R_{\rm HS}$ and $R_{\rm sense}$ are the on resistances of HS ($M_{\rm HS}$) and sense ($M_{\rm sense}$) transistors, and K is the ratio between the sizes of the HS switch ($M_{\rm HS}$) and the sense transistor ($M_{\rm sense}$). Thus, the HS switch is turned OFF once the inductor current crosses the scaled compensated current as shown in Fig. 5. The factor (K) allows using low compensated control current ($I_{\rm comp}$), hence, reduces the power consumption.

The dead-time intervals are inserted to prevent the shoot-through currents in the HS and low-side (LS) switches. During the dead-time interval, the HS and LS switches are turned OFF. The current in the inductor does not change instantaneously; hence, the convenient current path is through the body diode of the LS switch. Consequently, the switching node (Vsw) voltage is pulled below ground as shown in Fig. 5. This below-ground state injects minority carriers in the substrate. The load current of this chip ranges from 0.1 to 0.6 A.

The chip was fabricated using 0.35 μm HV-CMOS technology. The die photo of the chip is shown in Fig. 6. The HS and LS switches are placed in the corner of the die to minimize the power dissipation and the substrate coupling current. The bandgap is placed about 554 μm apart from the LS switch. The distance is maximized in order to investigate the substrate coupling effects without significant disturbance to the system performance.

B. Effects of the Substrate Coupling on the Bandgap Voltage

In Fig. 7, the bandgap circuit is shown with the output stage, i.e., the LS and HS transistors. Q1 and Q2 are the parasitic NPN transistors. These transistors represent the substrate coupling components under investigation. A cross-sectional area of the output stage and the bipolar junction transistor (BJT) used in the bandgap is shown in Fig. 8.

The minority carriers are going to be collected by the base of the PNP transistors. This electron collection results in reducing the base current [19]. To explore more this effect, we can

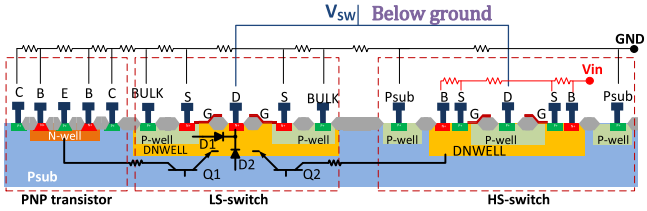

Fig. 8. Cross-sectional area for the output stage and the PNP transistor used in the bandgap circuit.

assume small parasitic resistances at the base terminals, then this electron collection can be translated into a reduction in the base voltage. The effect of lowering the base voltage results in lowering the reference voltage. Consequently, the more the current coupled into the bandgap the less the reference voltage. This is the expected effect from the simulation of the circuit and the substrate extracted netlist.

C. Substrate Injection Current Mechanism

The injection of minority carriers occurs at the dead-time period [T_d(total)]. During this period, the below ground state on the switching node ($V_{\rm sw}$) forces the body diode (D_1) and the substrate diode (D_2) to conduct. Since we are using the isolated NMOS transistor, the major part of substrate current is due to the conduction of the substrate diode (D_2).

The injected current is divided into three main components [20]: leakage current in the MOS transistor (LS switch); body diode current; and substrate diode current. The injected minority carriers in the substrate are going to be either coupled in another N-well or recombined in the substrate. The recombination of electrons in the substrate requires a substrate current to compensate the shortage in holes, which means that the substrate voltage is going to be lowered.

In our extraction, we consider only the deep N-wells (DNWELLs) of the PMOS and NMOS transistors and the N-wells of the BJTs in the bandgap as illustrated in Fig. 8. The DNWELL of the PMOS is connected to the input HV while the DNWELL of the NMOS is pulled down below ground.

To verify the proposed methodology with the dc measurements, we assumed the following two test cases:

1) Test case 1: The LS switch NMOS transistor source terminal is connected to ground. This means that the injected current is divided into the body and substrate diodes.
2) Test case 2: The source of the LS switch transistor is disconnected. This means that the injected current is passed only through the substrate diode.

Through these two test cases we kept the PMOS DNWELL connected to HV of 15 V. We are setting a functional threshold voltage for the bandgap voltage of 1.16 V which represents a 3% deviation from the reference voltage. Below this threshold we assume that the reference bandgap is perturbed.

1) Test Case 1—The Body and Substrate Diodes are Considered: The extracted substrate netlist is back annotated to the original schematic of the LS and HS switches and the bandgap circuit. The injected current is swept from 0.01 to 0.8 A. Fig. 9 shows the reference bandgap voltage versus the injected current

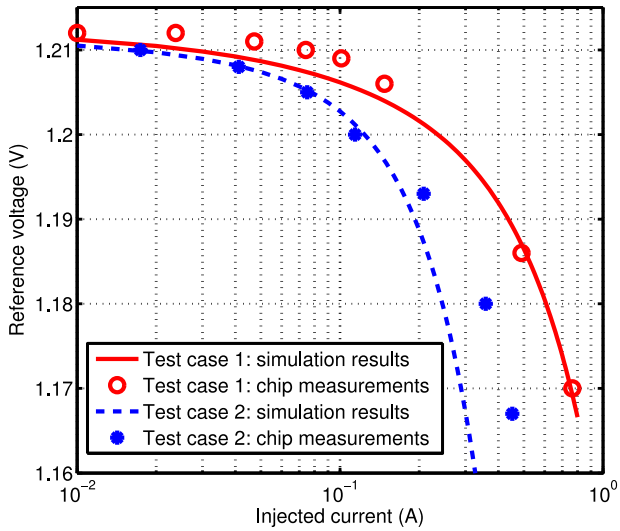

Fig. 9. Bandgap reference voltage versus the injected current. Test case 1 considers the body and substrate diodes while test case 2 considers only the substrate diode.

in the simulations and measurements. The simulation results follow the same trend as the measurement points. The reference bandgap voltage did not pass the functional threshold voltage even when the injected current is about 0.8 A.

Most of the injected current passes through the body diode. The remaining part of the injected current flows inside the substrate through the substrate diode. This injected current can be divided into three components. The first component is coupled to the PMOS HS switch DNWELL and results in increasing the power consumption as it drains more current from the supply in normal circuit operation. The second component is recombined in the substrate. The third part, which is considerably small, is coupled to the bandgap N-wells.

2) Test Case 2—The Substrate Diode is only Considered: The substrate diode injects the current in the substrate. This current is divided into recombination substrate current and current collected by N-wells.

Fig. 9 shows simulated results and the measurements. For high current values, the simulated data show greater effect of the injected current on the bandgap rather than the measurements. The main reason of this deviation is that on the chip many other N-wells can serve as collecting points while in the simulation, we simulate only the injecting point and two other collecting points which are the bandgap and the HS switch DNWELL. In Fig. 9, the bandgap failed to sustain its reference voltage when the injected current becomes higher than 300 mA. This injected current lowers the bandgap voltage below the 3% threshold that we assumed. As in this case, all the injected current is passed directly to the substrate.

In our design, the average current in the dead-time period can be expressed as

$$I_{\rm av}(\text{deadtime}) = \frac{T_d(\text{total})}{T_{\rm switching}} \times I_{\rm av}(\text{load}) \tag{1}$$

where $T_{\rm switching}$ is the switching period and $I_{\rm av}$(load) is the average load current. T_d(total) is approximately 340 ns and the

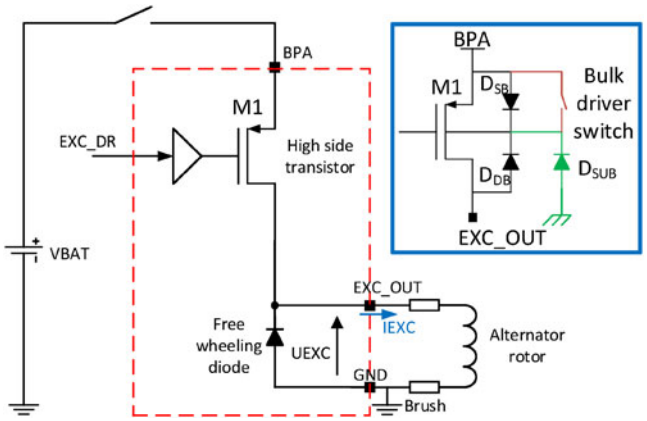

Fig. 10. AUTOCHIP1 power stage principle. In the frame, the HS switch with reverse protection scheme.

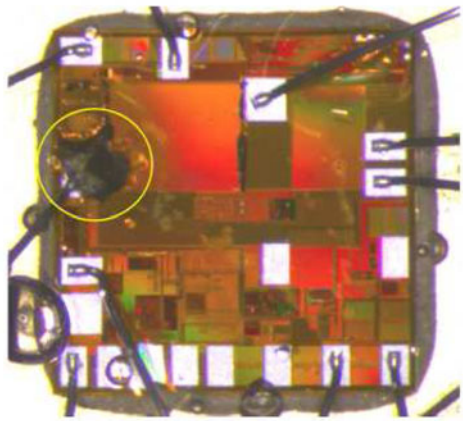

Fig. 11. AUTOCHIP1 damage after battery connection [14].

maximum load current is 0.6 A; hence, the maximum average dead-time current is 67 mA. In the normal operation, the source of the LS switch is connected to ground. Hence, from the test case 1, we can justify that the bandgap reference voltage will not be affected by the current injected in the dead time.

V. Transient Simulation Industrial Case Study: AUTOCHIP1

The AUTOCHIP1 is a smart power IC developed using 0.35 μm HV-CMOS technology from AMS. It has been developed for 24 V Valeo automotive technology applications and is able to sustain overvoltages up to 90 V. It aims at controlling 28 V up to 32 V heavy-duty alternators by rotor high current driver up to 5 A. It integrates on the same die a power stage to drive rotor coil, similar to the one described in [21], different I/O interfaces, a power management block, and a small digital part that manages a serial communication with an external digital core, implemented on a field-programmable gate array (FPGA). The FPGA solution has been chosen to increase the flexibility, as in [22].

The alternator operation is to recharge the battery during the engine rotation. It comprises two parts: the rotor and the stator. The current in the rotor induces a magnetic flux. Its rotation produces a variable magnetic field that cuts the stator coil. Consequently, the stator generates a current that is used to charge the battery. The control of the stator current is performed by controlling the rotor current.

As depicted in the Fig. 10, it includes an HS switch and an LS freewheeling diode. This stage regulates the current of the rotor. The regulation loop is done by monitoring the battery terminal voltage (BPA) defining the pulse width modulator signal duty cycle by comparison with a reference voltage. In order to tolerate the reverse bias voltage conditions on the battery side, a bulk driver circuit is used to avoid the parasitic diode conduction under the reverse bias condition [22]. As shown in Fig. 10, in normal operation the voltage of PMOS source node (BPA) is higher than the drain node voltage; hence, the bulk driver switch is turned ON connecting the bulk and the source of the PMOS switch. In the reverse bias condition, when the PMOS source node is pulled below ground, in order to prevent the parasitic diode D_{DB} from conducting, the bulk driver switch is turned OFF and the floating well reverse voltage protection is formed [23].

One important test is the electrical connection and disconnection of the product that has high *dV/dt* up to 20 V/ns that can be intermittent or during maintenance. AUTOCHIP1 failed to pass the fast connection test; we are going to elaborate the failure root cause in the coming section.

A. Conventional Problem Identification

The complete evaluation of the AUTOCHIP1 performances has been done in AMS and Valeo laboratories in parallel. Many fast battery connections at different temperatures and different voltages have been done. AUTOCHIP1 failed to sustain a fast connection of 50 V battery and it was severely damaged. Fig. 11 shows the microphotograph of the AUTOCHIP1 after the test. The damage is in the battery connection (BPA) pad and its bonding wire.

This damage is due to excessive current drawn from the battery during the fast battery connection test. The preliminary failure analysis starts with preparing another test bench using the same design but adding a limiting resistor in series with the battery. The *Em*ission *Mi*croscope was used to identify the potential origin of the failure. An emission occurs on one side of the PMOS HS switch, which is surrounded by P-substrate contact and N-guard ring biased to ground. Such optical emissions occur due to the recombination of carriers at the base of a BJT. Hence, this preliminary test indicates that there could be an activation of the lateral NPN BJT between the PMOS bulk, substrate, and the guard ring.

The origin of this high current is that during the fast transition of the battery, the bulk driver switch exhibits a high resistance that activates the vertical PNP transistor between the PMOS bulk and source and the P-substrate injecting high current in the substrate. The substrate voltage is shifted up switching ON the lateral NPN transistor and a parasitic semiconductor rectifier (SCR) structure is triggered. The cross section of the PMOS and the guard ring with the parasitic components are shown in Fig. 12. These two BJT parasitic transistors are not included in the model of the PMOS transistor. Consequently, their effects

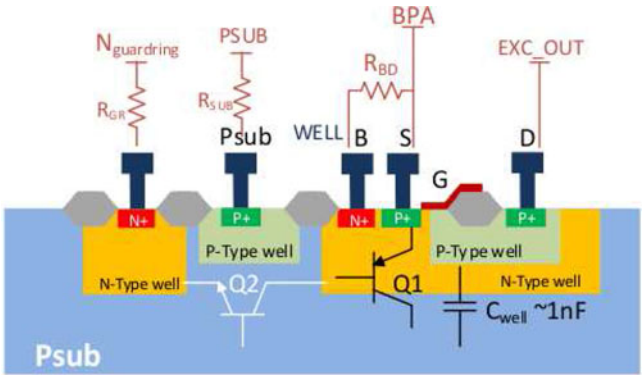

Fig. 12. AUTOCHIP1 parasitic components hand extraction.

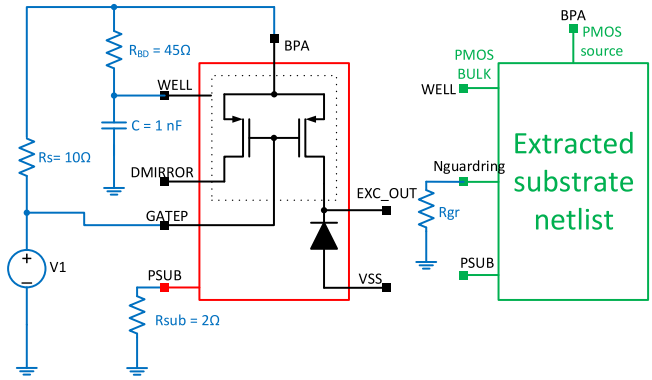

Fig. 13. AUTOCHIP1 simulation test bench.

TABLE I
AUTOCHIP1 SUBSTRATE EXTRACTION PARAMETERS

Parameter	Value	Parameter	Value
Active substrate depth	25 μm	Number of sublayers	5
Layer 1 depth	1.55 μm	Layer 4 depth	15 μm
Layer 2 depth	3.5 μm	Layer 5 depth	25 μm
Layer 3 depth	6.5 μm	# of shapes processed	1900
Extraction elapsed time	232.6 s	Extraction CPU time	199.5 s

are not revealed in the schematic circuit simulations. Also, the resistance of the bulk driver switch R_{BD} must be included in the extraction. The switch resistance during fast transition is approximately 45 Ω. It should be noted that the guard ring is connected to ground and not to the supply in order to avoid injecting minority carriers in case of reverse bias condition.

A new schematic was done involving the substrate parasitic components added by hand and simulated in order to replicate the measurement behavior. Such simulations are needed to increase the confidence level of the redesign and to validate the root cause explanation. This hand-extraction step took more than three months.

B. Proposed Problem Identification

Our proposed methodology can be used to identify such failure. At this stage, the layout of the design is available and can be processed by AUTOMICS tool. The selected area is the PMOS and the guard rings. The main four terminals are the PMOS bulk (WELL), PMOS source (BPA), the N-type guard ring ($N_{\mathrm{guardring}}$) and the P-substrate contact (PSUB). These terminals are preserved in the substrate parasitic extraction.

The active substrate thickness is set to 25 μm to minimize the number of components with an acceptable accuracy. The substrate is divided into five sublayers. The sublayers thicknesses, extraction time, and number of layout shapes processed are reported in Table I. The vertical PNP and lateral NPN transistors are extracted in addition to the parasitic substrate resistances. We added resistances to emulate the parasitic metal tracks and vias resistances for the substrate and guard ring connections.

Fig. 13 shows the test bench used for simulating the substrate network with the original schematic. The voltage source V1 is set to 0 V, and then ramps up to 12 V in 10 ns. Two simulations

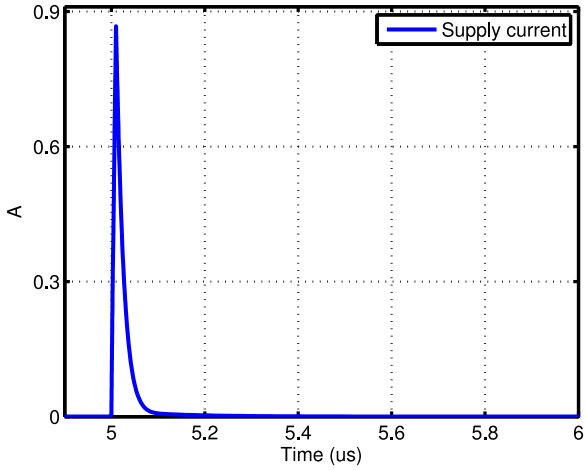

Fig. 14. Simulation of AUTOCHIP1 schematic without the substrate network. Fast transition current occurs due to parasitic capacitance then returns to zero. This indicates the proper operation of the circuit which is not the actual case.

are performed. The first one is simulation of the original circuit only. The second simulation is the original circuit and the extracted substrate network.

In case of simulating the original circuit alone, a current spike is drawn from the supply connection and then the current returns to zero in fraction of a microsecond as shown in Fig. 14. This current spike is due to the parasitic capacitance (C_{well}) of the N-well of the PMOS transistor. As the current returns back to zero, this indicates that the circuit works properly. This is expected since the schematic components does not consider the layout aspects like the guard ring connection, as a result the lateral NPN transistor is not modeled.

Fig. 15 shows the simulation results of the AUTOCHIP1 extracted substrate network. The spike in the supply current appears and does not return to zero. A holding current appears indicating the presence of a latched SCR structure. The substrate voltage across the parasitic resistor is about 0.7 V and is held constant indicating the lateral NPN is turned ON. The results show an acceptable agreement with the measurement on the AUTOCHIP1 reported by AMS. The simulation time and number of extracted components are shown in Table II.

These results could be used by a designer to analyze the latch-up structure and provide solution for this problem before

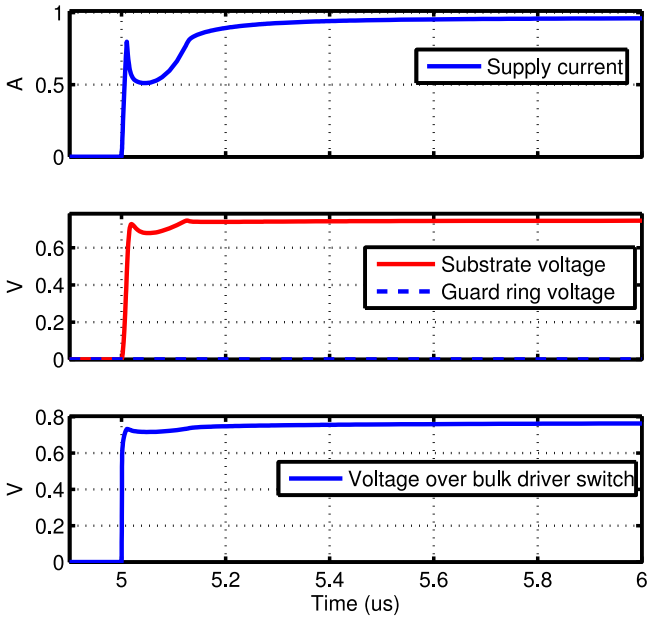

Fig. 15. AUTOCHIP1 substrate network simulation. The substrate voltage is measured at the substrate contact (PSUB). The latch-up occurs and a current of 1 A is drawn from the supply.

TABLE II
SUBSTRATE SIMULATION PARAMETERS FOR TRANSIENT TIME = 8 μS

Parameter	Value	Parameter	Value
Number of nodes	22 511	Number of diodes	2417
Simulation CPU time	611.6 s	Number of resistors	33 795
Simulation elapsed time	616.1 s	Number of homojunctions	583

fabrication. This proposed methodology saves the time required for the substrate parasitic extraction. Also, it could be used before the fabrication as a verification test for the design sensitivity to the latch-up structure. Using such tool would save long time of redesign and, consequently, lower the cost and ameliorate the circuit design.

C. Proposed Solutions for Latch-Up Problems

Fig. 16 shows a simplified circuit for the extracted parasitic components of the PMOS transistor.

In order not to trigger the SCR structure at the fast connection test, we have to ensure that the lateral BJT does not turn ON. Starting with the vertical PNP transistor, the switching ON of this transistor depends on passing a large current through the R_{BD} and the well capacitance. It turns ON as the bulk driver circuit response is slow relative to the input voltage slew rate and its resistance R_{BD} is large. Hence, the first proposed solution is to reduce the resistance of the bulk driver switch at the power up.

The second precaution is to modify the guard ring resistance. Adding a resistance in series with the guard ring requires an excess current through the substrate resistance to switch ON the lateral NPN transistor. Thus, if the vertical transistor is turned ON, the amount of current passing through the substrate resistance will not be sufficient to turn ON the lateral NPN transistor and consequently, the latch-up structure will not be triggered.

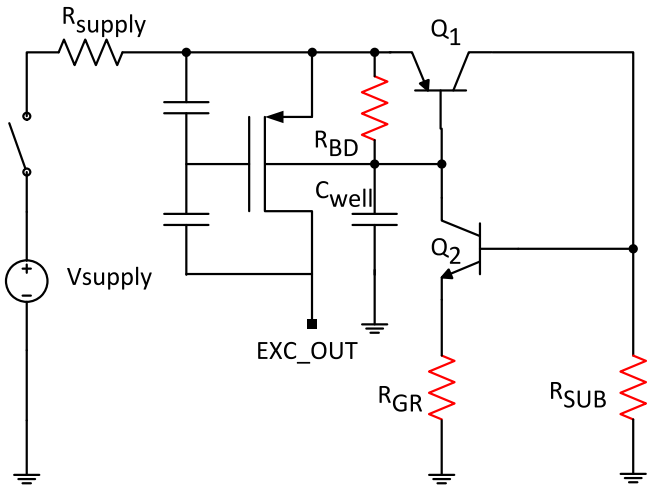

Fig. 16. AUTOCHIP1 HS transistor and its parasitic components equivalent circuit. Resistances in red should be modified to prevent latch-up.

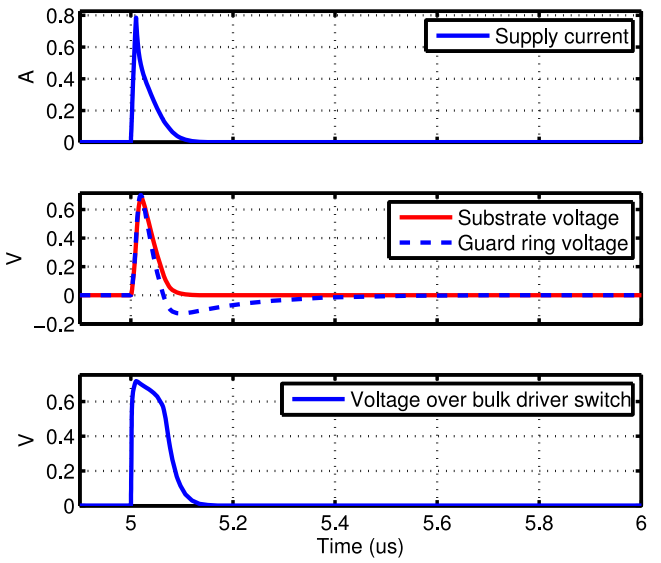

Fig. 17. Simulation of AUTOCHIP1 substrate network with latch-up prevention techniques.

These precautions are done and the bulk driver resistance (R_{BD}) is lowered to 4 Ω and the guard ring resistance (R_{GR}) is risen to 5 kΩ. The simulation results of the extracted substrate network with the modified components are shown in Fig. 17. The substrate voltage rises due to the injection of holes; however, the voltage across the guard ring resistor is also increased. Hence, the latch-up is prevented.

Using the proposed latch-up prevention techniques, AUTOCHIP2 was designed and fabricated. It manages to pass the battery connection test safely.

VI. CONCLUSION

A methodology for analysis and verification of substrate noise coupling was presented. It is based on substrate parasitic

extraction tool referred to as AUTOMICS. The tool employs enhanced models that account for the propagation of minority carriers. The methodology fills the gap due to the absence of the lateral NPN transistor modeling in conventional tools. Hence, it is capable of estimating the coupling current between the HV circuits and the LC circuits. This would be helpful in the design to optimize the circuit protection. Also, it is used to simulate the failures due to the activation of this lateral NPN transistors. Simulating the failure means that we would be able to prevent it before fabrication. The methodology was verified on dc–dc buck converter circuit and the coupling effect of the HV switch and the bandgap was simulated. The simulation and measurement results were consistent. Then, it was verified on an industrial test case AUTOCHIP1 that failed due to fast transition on its supply contact. This fast transition activated the lateral NPN transistor and triggered a latch-up. The simulation results reproduced the failure behavior and were in good agreement with the measurements. Also, failure prevention techniques were verified on simulations. The proposed methodology gives an insight of the substrate noise coupling behavior. Hence, using it in the verification stage before fabrication would reduce the number of redesigns and shorten the time-to-market and consequently, the cost is reduced.

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