Control of a Single-Phase Standalone Inverter Without an Output Voltage Sensor

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***Abstract*—This paper analyzes the possibility of controlling the output voltage of a standalone single-phase inverter by directly controlling the output filter capacitor current without using a dedicated output voltage sensor. The plant modeling and controller design are presented. The proposed method depends on having the value of the output filter capacitance. A method to estimate the output filter capacitance is also presented. Rigorous analysis is done to show that the proposed sensorless scheme is largely insensitive to parameter variations and ensure that the output voltage is within specified regulations at utility level. It is also demonstrated in this paper that compared to the conventional voltage control scheme the proposed control scheme ensures an improved total harmonic distortion of the output voltage waveform. Experimental results presented validate the proposed scheme.**

***Index Terms*—Inverter control, nonlinear load, proportional resonant (PR) controllers, sensorless control, total harmonic distortion (THD), virtual flux.**

I. Introduction

THE single-phase voltage-source inverter is the most widely used power electronic converter for utility-level standalone distributed generation units. The output voltage requirement at the utility level is dictated as in [1] which clearly specifies the voltage rms to be within $\pm 5\%$ of the nominal voltage. General requirements necessitate a control architecture which needs to ensure a negligible steady-state error in the output voltage, a minimum total harmonic distortion (THD) under nonlinear loads, and a fast response during load transients. Thus, the control of such inverters has become a topic of interest among researchers. Unlike a three-phase inverter, a single-phase inverter cannot be directly controlled in the synchronous frame of reference. Authors of [2] and [3] proposed to do so by creating a fictitious quadrature axis. Though the modeling and control of the inverter become simple in the fictitious synchronous frame of reference, the conversion itself involves additional computations and inherently introduces delay in the system. Furthermore, additional controllers as shown in [4] are necessary to maintain the output voltage under nonlinear loads. Over the past years, several nonlinear, adaptive, hysteresis, repetitive, and geometric-based control structures have been proposed for controlling single-phase inverter systems [5]–[15]. However, each of these interesting control structures has their limitations namely modeling complexities, detailed mathematical derivations, unsatisfactory performances under nonlinear loads, parameter sensitivity, etc. Among the proposed control structures for single-phase inverters in the literature, the proportional resonant (PR) controller is arguably the most popular. The PR controller in a stationary frame of reference is the equivalent counterpart of the proportional integral controller in the synchronous frame of reference. Initially proposed in [20], the PR controller has been successfully implemented to track linear and nonlinear currents in current-controlled grid-connected converters [16]–[18]. It has also been applied to standalone converters to control their output voltage [5], [21]. The controller has reported excellent steady-state error tracking under linear loads. However, as shown in [19], the controller has stability issues under nonlinear loads. This is primarily because with the addition of resonant peaks at the dominant harmonic frequencies, namely third, fifth, and seventh, the phase margin of the control loop deteriorates. The system stability thereby puts a limit on the resonant gains at higher harmonic frequencies, thereby requiring additional measures to improve the phase margin and reduce the voltage THD under nonlinear loads [19].

All the previous control architectures discussed for single-phase inverters use an output voltage sensor. In this paper, we take a novel step by eliminating the output voltage sensor and investigate the possibility of controlling a standalone inverter without the voltage sensor. Sensorless control has been proposed for grid-connected converter systems where the power flow between the converter and the grid is controlled without the need of dedicated grid voltage sensors [22]–[24]. However, to the best knowledge of the authors, sensorless voltage control approaches have not been discussed for standalone inverters in the literature. With a regulated dc-bus voltage, faults in single-phase inverter systems are generally caused by overcurrents. Hence, eliminating the output voltage sensor does not compromise the system protection. In fact, the elimination of the voltage sensor saves cost and space. Additional circuitry and wiring requirements are also reduced. The inverter may have to operate in an environment where it is subjected to high temperature, electromagnetic interference, and noises. In such conditions, sensors are prone to errors and physical damage. One such example is the hybrid power train where the power electronics converters have to operate under high temperature, noise, and vibrations. A damaged or inaccurate sensor will jeopardize the entire system. A sensorless control scheme thus adds to the reliability of the overall system. However, it must be ensured that the output voltage meets the desired specifications for utility applications

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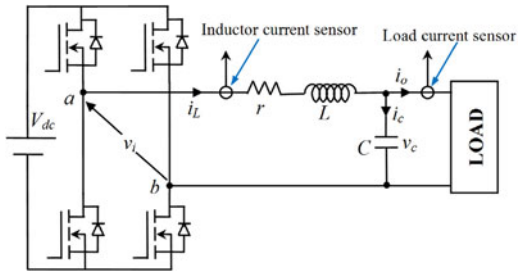

Fig. 1. Circuit of a single-phase standalone inverter.

[1]. Addressing this issue, the control methodology presented in this paper ensures that the output voltage is within the prescribed limits. The approach aims to control the output voltage by directly controlling the output capacitor current. An estimation of the output filter capacitance, required for this purpose, is also discussed. It is demonstrated that the proposed control scheme ensures better THD of the output voltage under nonlinear loads compared to the conventional voltage control approach. A thorough analysis is done to show that such estimation along with the proposed control structure is largely immune to parameter fluctuations.

The rest of this paper is arranged as follows. The proposed control scheme is presented in Section II. This section also includes the estimation of the output voltage and the output filter capacitance prediction. The modeling of the rms voltage control loop and the sensitivity of the output voltage to the parameter variations is shown in Section III. The results are discussed in Section IV, while the conclusion is presented in Section V.

II. Control Architecture

The schematic of a standalone inverter is shown in Fig. 1. In the figure, *L* is the filter inductance, *r* is the resistance representing the ohmic loss of the switches and the filter inductor, *C* is the filter capacitance, i_L is the filter inductor current, i_o is the load current, i_c is the capacitor current, v_c is the output voltage of the converter, and v_i is the output voltage of the bridge. The filter inductor and load current are measured. However, unlike conventional voltage control methods, the output voltage is not measured for the proposed sensorless control scheme.

A. Review of the Conventional Voltage Control Method

The inductor current and output capacitor voltage dynamics for the circuit as shown in Fig. 1 are given as

$$L\frac{di_L}{dt} + ri_L = v_i - v_c \tag{1}$$

$$C\frac{dv_c}{dt} = i_L - i_o. \tag{2}$$

The inductor current, output capacitor current, and load current are related as

$$i_L = i_o + i_c. \tag{3}$$

The multiloop structure with an outer voltage loop and an inner current loop [21] is generally used as the controller structure. The control structure introduces output impedance dependent on the load current. It has been reported that the choice of the capacitor current feedback in the inner current loop ensures much lower output impedance compared to the inductor current feedback approach [21]. The controller structure is presented in Fig. 2. The output voltage feedforward is also added to the control loop. With such a control structure, the open-loop gain is given as [21]

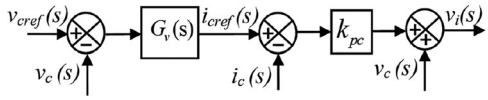

Fig. 2. Conventional voltage control structure with capacitor current feedback.

$$G(s) = \frac{k_{\rm pc}G_v(s)}{s^2LC + (r + k_{\rm pc})sC} \tag{4}$$

where $G_v(s)$ is the voltage compensator and $k_{\rm pc}$ the proportional gain of the inner current loop. The system represented by (4) is a second-order system. With an increase in the controller gain, especially at the higher harmonic frequencies, the phase margin of the system deteriorates. So, there is a tradeoff between achieving a high bandwidth and stability in the open-loop gain represented by (4). Often phase lead compensators are needed to improve the phase margin as reported in [19].

B. Proposed Control Scheme

The overall block diagram of the proposed control scheme is shown in Fig. 3. The control structure has three distinct parts: the voltage RMS controller, the filter capacitor current reference generator, and a current controller. Each of the section is sequentially described in detail. The output voltage of a single-phase inverter can be controlled by controlling the capacitor current. To produce the desired output voltage $v_{\rm cref}$, an inductor current reference can be set as

$$i_{\rm Lref} = i_o + i_{\rm cref} \tag{5}$$

where

$$i_{\rm cref} = C\frac{dv_{\rm cref}}{dt}. \tag{6}$$

It is worth mentioning that metallized polypropylene film capacitors are the most common choice as filter capacitors. These capacitors have negligible equivalent series resistance. On the basis of this knowledge, the resistive drop across the output capacitor has been ignored in (6). It can be seen from (1) that inductor current i_L can be controlled by v_i, the output of the bridge, while the dynamics of output voltage v_c can be controlled by controlling inductor current i_L. Thus, output voltage v_c can be indirectly controlled by controlling v_i. A properly designed controller will ensure that the output of the bridge (v_i) is able to maintain the inductor current at its desired reference $i_{\rm Lref}$ (as in (5)) thereby ensuring that capacitor current $i_{\rm c}$ is maintained at $i_{\rm cref}$ as given in (6). This in turn will ensure that the output voltage is maintained at the desired reference value $v_{\rm cref}$. However, it should be noted that an accurate knowledge of the value of the output filter capacitor is needed in (6). The rms voltage controller in Fig. 3 gives an estimation of the filter capacitor which is used to calculate the capacitor reference

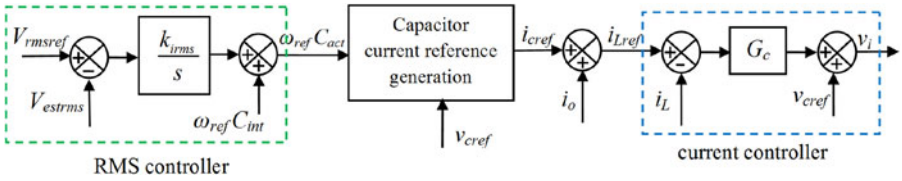

Fig. 3. Overall block diagram of the proposed control scheme.

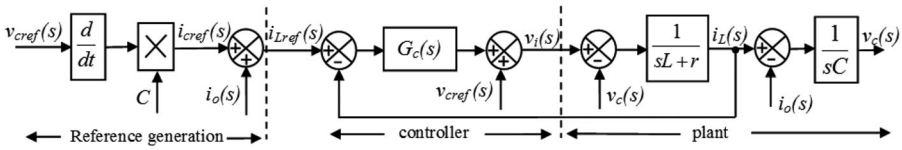

Fig. 4. Current control loop with the corresponding plant.

current (as in (6)). The capacitor reference current generator in Fig. 3 basically implements (6). The estimation of the capacitor and capacitor reference current generation will be addressed in detail in the next section. Capacitor reference current $i_{\rm cref}$ is added to the load current to generate reference inductor current $i_{\rm Lref}$ as in (5). A well-designed current controller ensures that the actual inductor current i_L tracks $i_{\rm Lref}$. The current controller structure is represented as

$$v_i(s) = (i_{\rm Lref}(s) - i_L(s))G_c(s) + \ v_{\rm cref}(s) \tag{7}$$

where $G_c(s)$ represents the current controller. Generally, output voltage v_c is treated as a disturbance input in (1) and is used as the feedforward term in (7) [21]. However, as a voltage sensor is not being used, v_c is not available. So, $v_{\rm cref}$ is used as the feedforward term. The control structure is shown in Fig. 4.

The loop gain of the proposed control structure is derived next. Taking the Laplace transform of (2), (3), (5), and (6) and using them in (7) leads to

$$v_i(s) = (sCG_c(s) + 1)\, v_{\rm cref}(s) - sCG_c(s)\, v_c(s). \tag{8}$$

Also, in the Laplace domain (1) and (2) can be combined as

$$\left(s^2LC + srC + 1\right) v_c(s) + (sL \ + \ r)\, i_o(s) = v_i(s). \tag{9}$$

Substituting $v_i(s)$ from (8) in (9) results in

$$\begin{aligned}&\left(s^2LC + s(r + G_c(s))C + 1\right) v_c(s)\\ &= (sCG_c(s) + 1)\, v_{\rm cref}(s) - (sL \ + \ r)\, i_o(s)\end{aligned} \tag{10}$$

or

$$\begin{aligned}v_c(s) = &\frac{sCG_c(s) + 1}{s^2LC + s(r + G_c(s))C + 1} v_{\rm cref}(s)\\ &- \frac{sL \ + \ r}{s^2LC + s(r + G_c(s))C + 1} i_o(s)\end{aligned} \tag{11}$$

which can be rearranged in the standard form as

$$v_c(s) = \frac{\frac{sCG_c(s)+1}{sC(sL+r)}}{1 + \frac{sCG_c(s)+1}{sC(sL+r)}} v_{\rm cref}(s) - \frac{\frac{1}{sC}}{1 + \frac{sCG_c(s)+1}{sC(sL+r)}} i_o(s). \tag{12}$$

The block diagram representation of (12) is shown in Fig. 5. From (12), treating i_o as a disturbance input, the closed-loop

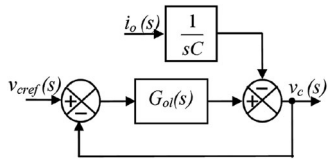

Fig. 5. Closed-loop equivalent representation of the controller structure.

gain is obtained as

$$\frac{v_c(s)}{v_{\rm cref}(s)} = G_{\rm cl}(s) = \frac{\frac{sCG_c(s)+1}{sC(sL+r)}}{1 + \frac{sCG_c(s)+1}{sC(sL+r)}}. \tag{13}$$

From (13), the open-loop gain is obtained as

$$G_{\rm ol}(s) = \frac{sCG_c(s) + 1}{sC(sL + r)}. \tag{14}$$

The controller parameters will be selected based on the open-loop gain in (14). Again, open-loop gain $G_{\rm ol}(s)$ can be simplified as

$$G_{\rm ol}(s) = \frac{1}{sC(sL + r)} + \frac{G_c(s)}{sL \ + \ r} \tag{15}$$

or

$$G_{\rm ol}(s) = G_1(s) + G_2(s) \tag{16}$$

where $G_1(s) = \frac{1}{sC(sL+r)}$ and $G_2(s) = \frac{G_c(s)}{sL + r}$.

It can be observed from (15) and (16) that the open-loop gain at low frequencies is primarily dictated by $G_1(s)$. However, as frequency increases, the influence of $G_1(s)$ decreases. So, at higher frequencies, the open-loop gain is dictated by $G_2(s)$. Hence, it can be asserted that the system bandwidth and response to harmonic frequencies can be controlled by $G_c(s)$. It should also be noted that similar to the voltage control architecture [19], [21], output impedance $Z_o(s)$ is also introduced in this case. From (12), $Z_o(s)$ can be found as

$$\frac{v_c(s)}{i_o(s)} = Z_o(s) = \frac{sL \ + \ r}{s^2LC + s(r + G_c(s))C + 1}. \tag{17}$$

From (3) and (5), it is worth noting that

$$i_{\rm Lref} - i_L = i_{\rm cref} - i_c. \tag{18}$$

TABLE I
SYSTEM PARAMETERS

Part	Manufacturer	Specifications
Inductor(L)	Hammond (195G20)	$L = 5$ mH, $r_{\rm dc} = 40$ mΩ
Capacitor (C)	Epcos (B33364A5206J050)	20 μF, 440 V
Switches ($S_1 - S_4$)	Infineon (IPP600N25N3)	$V_{\rm ds} =$ 250 V, $I_d =$ 25 A, $R_{\rm ds} =$ 80 mΩ
DC-bus capacitor	Epcos (B43704B5338M)	450 V, 3300 μF
Loss resistance (r)	–	$r_{\rm dc} + 2R_{\rm ds} = 0.2\ \Omega$

TABLE II
CONTROLLER PARAMETERS

k_p (V/ A)	80
k_{r1} (V/ A·s)	2000
k_{r3} (V/ A·s)	2500
k_{r5} (V/ A·s)	3000
k_{r7} (V/ A·s)	4000
$\omega_{\rm cut1}$ (rad/s)	10
$\omega_{\rm cut3}$ (rad/s)	20
$\omega_{\rm cut5}$ (rad/s)	30
$\omega_{\rm cut7}$ (rad/s)	40

So, unlike in voltage control structures, it can be concluded that the choice of the inductor current or the capacitor current as the control variable makes no difference to the performance of the control loop for the proposed scheme.

Since a single-phase system is expected to produce a sinusoidal output, a PR controller with the resonant peak at the fundamental frequency is sufficient as the current controller. However, since any standalone system must have the capability to cater nonlinear loads, the controller is augmented with resonant peaks at dominant harmonic frequencies, namely the third, fifth, and seventh harmonic frequencies. Incorporating the additional resonant peaks, the controller structure is given as

$$G_c(s) = k_p + \sum_{n=1,3,5,7} \frac{k_{\rm rn}\omega_{\rm cutn} s}{s^2 + 2\omega_{\rm cutn} s + (n\omega_o)^2}. \qquad (19)$$

In (19), k_p is the proportional gain, $k_{\rm rn}$ and $\omega_{\rm cutn}$ are the resonant gain and cut-off frequency at the *n*th harmonic frequency. The proportional gain and resonant gains are chosen such that the bandwidth is about 3 kHz, while the gain at the fundamental and compensated harmonic frequencies is at least 40 dB. It should be noted that since the open-loop system has a first-order behavior, the phase margin at 3 kHz is sufficiently high (about 75°). Such high phase margin and bandwidth cannot be simultaneously achieved with the conventional voltage control architecture. The different components used for the circuit in Fig. 1 are listed in Table I. It should be noted that in Table I, *r* is taken as the summation of the winding resistance of the inductor and twice the on state resistance of each switch ($r = r_{\rm dc} + 2R_{\rm ds}$). With the controller parameters represented in Table II, the open-loop frequency response of the plant and the controller is shown in Fig. 6. The corresponding closed-loop response is shown in Fig. 7. For the chosen controller parameters, the output impedance Z_o is shown in Fig. 8. It can be seen that the output impedance is very low at the fundamental and compensated harmonic frequencies. The effect of the delay introduced due to the sampling, computation, and pulse width modulation update was not considered in the controller design. The delay adds an additional phase lag to the system [4]. Hence, it is important to verify that the phase lag does not make the closed-loop system unstable. The phase lag introduced due to the delay is approximated as

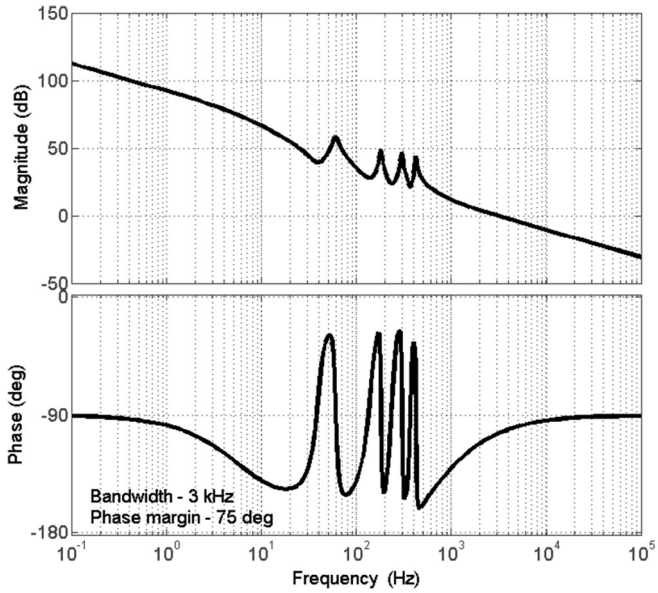

Fig. 6. Open-loop frequency response of the current controller and plant.

$$\phi_{\rm del} = -\tan^{-1}(\omega T_{\rm del}). \qquad (20)$$

For a switching frequency of 20 kHz, a double sample and update scheme in one switching cycle gives $T_{\rm del}$ of 25 ms. Using (20), the phase lag at the crossover frequency of 3 kHz is computed as 25°. Hence, the phase margin at the crossover frequency of 3 kHz decreases from 75° to 50°. This phase margin is still sufficient to ensure the stable operation of the closed-loop system.

C. Estimation of the Output Filter Capacitance

It can be seen from (6) that the value of $i_{\rm cref}$ is dependent on the value of output capacitance *C*. An inaccurate estimate of *C* will cause the output voltage to deviate from the desired reference value. An output voltage rms control loop is proposed to get an estimate of the filter capacitance (see Fig. 3). To get the rms value of the output voltage, an estimation of the output

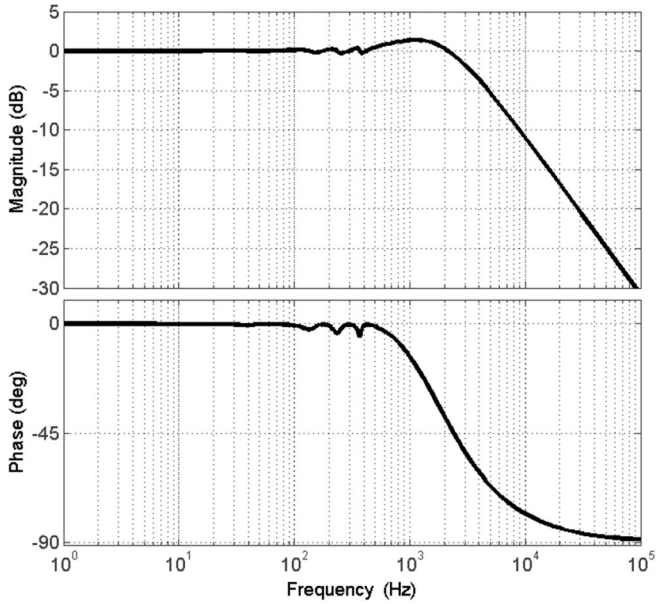

Fig. 7. Closed-loop frequency response of the current controller and plant.

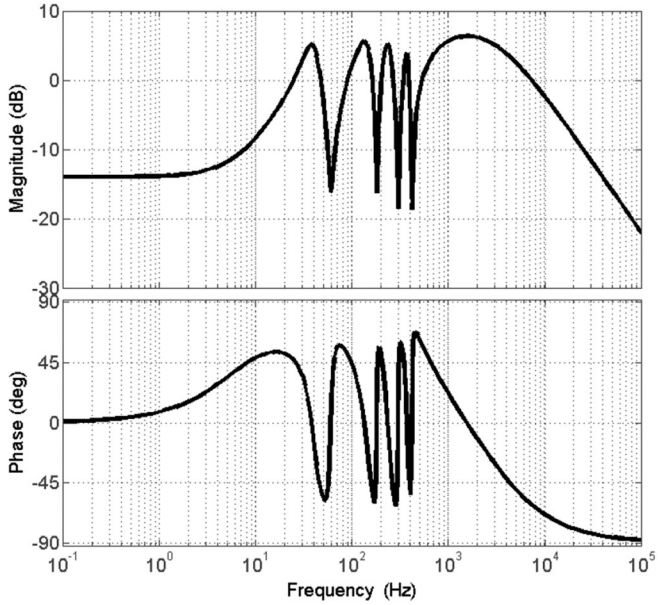

Fig. 8. Frequency response of the output impedance.

voltage is needed. The output voltage estimation is done using the concept of virtual flux [22], [23]. The virtual flux is computed as

$$\psi_{\rm vir} = \int (v_i - r_e i_L) - L_e i_L \tag{21}$$

where r_e and L_e are the assumed value of the resistance and inductance of the filter inductor. A pure integrator has dc drift problems. Hence, the integration in (21) is generally performed by a low-pass filter. However, low-pass filtering is always associated with phase lag and attenuation in the gain. A better alternative is to use the filter

$$G_{\rm fil} = \frac{k\omega_{\rm cut}}{s^2 + k\omega_{\rm cut}s + {\omega_{\rm ref}}^2}. \tag{22}$$

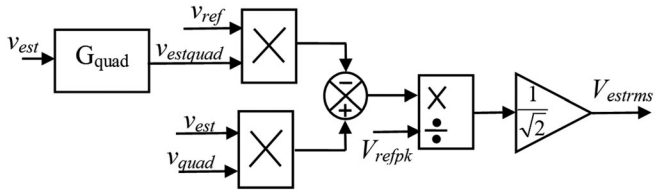

Fig. 9. Computation of the rms value for the filter capacitance estimation.

The filter as shown in (22) is generally used for positive and negative sequence separation [25], [26] and has been used for virtual flux generation in [22]. The virtual flux is multiplied by $\omega_{\rm ref}$ to generate the signal $v_{\rm est}$ which is passed through an orthogonal signal generator (OSG) to generate the signal $v_{\rm estquad}$. The OSG is realized using an all pass filter given as

$$G_{\rm quad} = \frac{\omega_{\rm ref} - s}{\omega_{\rm ref} + s}. \tag{23}$$

Thus, if $v_{\rm ref} = V_{\rm rekpk}\cos\theta$, then $v_{\rm est} = V_{\rm estpk}\sin\theta_1$ and $v_{\rm estquad} = -V_{\rm estpk}\cos\theta_1$. With the knowledge of $v_{\rm est}$ and $v_{\rm estquad}$, an instantaneous computation of the rms of the estimated voltage can be done. To do so, an operation similar to the scalar product between the reference and estimated voltage is performed. The operation is represented as

$$\langle v_{\rm ref}, v_{\rm est}\rangle = v_{\rm quad}v_{\rm est} - v_{\rm ref}v_{\rm estquad} \tag{24}$$

or

$$\langle v_{\rm ref}, v_{\rm est}\rangle = V_{\rm refpk}V_{\rm estpk}\cos\delta_{\rm err} \tag{25}$$

where $v_{\rm quad} = V_{\rm refpk}\sin\theta$, $V_{\rm refpk}$ is the peak value of the reference voltage, $V_{\rm estpk}$ is the peak value of the estimated voltage, and $\delta_{\rm err}$ is the angle between them. The phase shift between the two voltages occurs if actual resistance r and inductance L in the circuit deviate from the assumed resistance r_e and inductance L_e, respectively. However, considering the phase shift to be small $\cos\delta_{\rm err} \approx 1$. So, (25) can be written as

$$\langle v_{\rm ref}, v_{\rm est}\rangle = V_{\rm refpk}V_{\rm estpk} \tag{26}$$

or

$$V_{\rm estpk} = \frac{\langle v_{\rm ref}, v_{\rm est}\rangle}{V_{\rm refpk}}. \tag{27}$$

With the peak of the estimated voltage known, the rms value of the estimated voltage can be calculated as

$$V_{\rm estrms} = \frac{V_{\rm estpk}}{\sqrt{2}}. \tag{28}$$

The rms calculation shown in (28) is valid for sinusoidal waveforms. The calculated virtual flux, $\psi_{\rm vir}$, in (21) involves an integration which is equivalent to low-pass filtering. Hence, $\psi_{\rm vir}$ has negligible higher order harmonics. The estimated voltage $v_{\rm est}$, which is computed from $\psi_{\rm vir}$, is thus sinusoidal and can be safely used in (28) to give accurate estimate of the rms component. The rms calculation is demonstrated in Fig. 9.

The error between the reference rms value and the estimated rms value is processed by an integral controller as shown in Fig. 3. The output of the rms control loop of Fig. 3 serves as the additional capacitive susceptance required to converge the

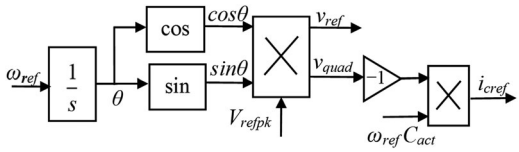

Fig. 10. Generation of the reference value for the filter capacitor current.

estimated rms value with the desired rms value. This output is added to the initial assumed capacitive susceptance. The actual capacitance is now modified to $C_{\rm act}$ to be used in the next cycle for the capacitor current reference generation. The reference capacitor current generation is shown in Fig. 10.

III. Design Guidelines for the RMS Controller and Sensitivity Analysis

A. Modeling the RMS Control Loop

The selection of the parameters of the rms controller can only be done from the knowledge of the corresponding plant. The output of the rms controller serves as the estimated capacitive susceptance (see Fig. 3). To have an idea of the plant, it is necessary to derive a transfer function relating the change in the output rms voltage to the change in the estimated capacitance. To compute the aforementioned transfer function, it is assumed that the current loop is much faster (at least ten times) than the rms voltage control loop and ensures exact tracking of the reference current without any steady-state error. The peak value of the output voltage is given as

$$V_{\rm cpk} = \frac{C_{\rm est}}{C} V_{\rm refpk}. \tag{29}$$

Again neglecting any deviations in r and L ($r_e = r$, $L_e = L$)

$$V_{\rm estpk} = V_{\rm cpk}. \tag{30}$$

Using (29) and (30), the rms value of the estimated voltage is given as

$$V_{\rm estrms} = \frac{C_{\rm est}}{\sqrt{2}C} V_{\rm refpk}. \tag{31}$$

Considering $V_{\rm rmsref}$ to be the rms value of the desired output voltage, the error in the rms voltage is calculated as

$$V_{\rm rmserr} = V_{\rm rmsref} - V_{\rm estrms} \tag{32}$$

or

$$V_{\rm rmserr} = \frac{V_{\rm refpk}}{\sqrt{2}} - \frac{C_{\rm est}}{\sqrt{2}C} V_{\rm refpk} \tag{33}$$

or

$$V_{\rm rmserr} = \frac{V_{\rm refpk}}{\sqrt{2}C} C_{\rm err} \tag{34}$$

or

$$\frac{V_{\rm rmserr}}{C_{\rm err}} = \frac{V_{\rm refpk}}{\sqrt{2}C}. \tag{35}$$

The transfer function relating the change in the output rms voltage to the change in the estimated capacitance is given in (35). Equation (35) serves as the plant transfer function for the rms controller. With this plant model, the closed-loop representation of the rms controller estimating the capacitance is shown in Fig. 11. The controller is taken as a simple integral controller. The frequency response of the loop is shown in Fig. 12. Selecting $k_{\rm irms}$ to be 0.03 Ω^{-1}/ V, the bandwidth is kept at 80 Hz, which is far less than the current control loop.

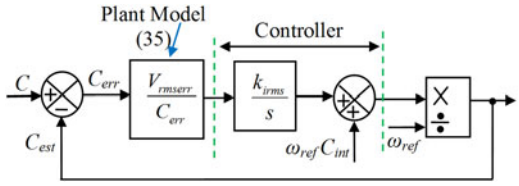

Fig. 11. Closed-loop representation of the RMS control loop for estimating the output filter capacitance.

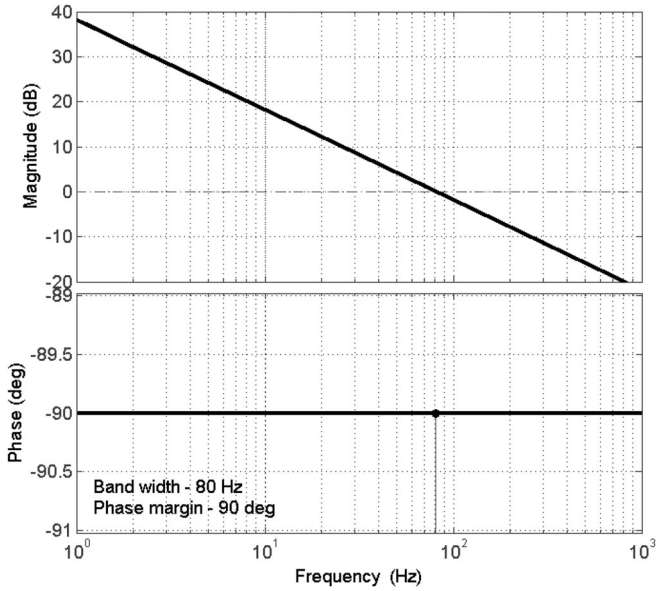

Fig. 12. Open-loop frequency response of the rms voltage controller and plant.

B. Parameter Sensitivity Analysis

It can be seen from (21) that the output voltage is estimated based on the initial assumed values of resistance r_e and inductance L_e of the filter inductor. These parameters change with the circuit-operating conditions. Hence, even an accurate initial estimate of the resistance and inductance will not be able to eliminate deviations in the estimated and actual output voltage. This section presents a sensitivity analysis of the actual output voltage rms value to the changes in the resistance and inductance for a 1 kVA inverter at full-load conditions. For the analysis, we consider the rms voltage control loop and the current control loop to be ideal ensuring no steady-state errors. The rms value of the output voltage at steady state can be expressed as

$$V_{\rm rms} = \frac{C_{\rm est}}{C} V_{\rm rmsref}. \tag{36}$$

From (36), it can be understood that to find the actual output rms voltage, $C_{\rm est}$ has to be calculated under different load conditions. The detailed derivations are shown in the Appendix. Following the derivations in the Appendix, the value of $C_{\rm est}$ is

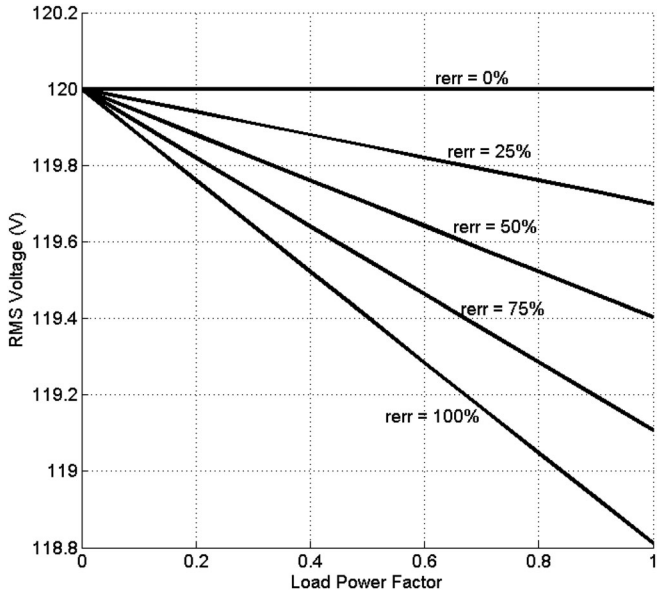

Fig. 13. Theoretical rms output voltage with error in the assumed resistance at different load power factor.

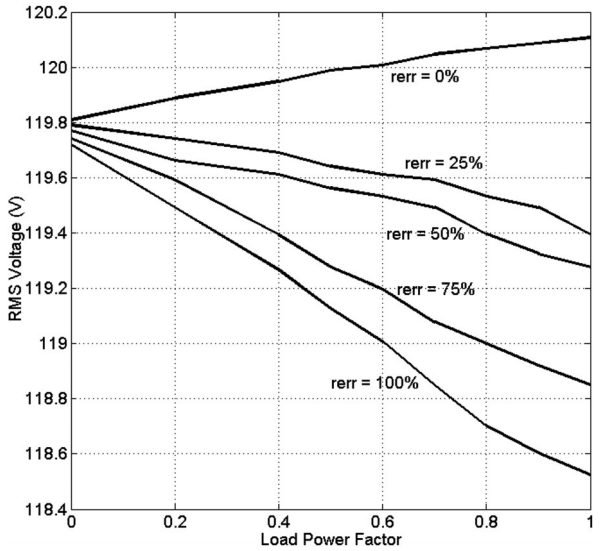

Fig. 14. Simulated rms output voltage with error in the assumed resistance at different load power factor.

given as

$$\frac{1}{C_{\rm est}} = \begin{bmatrix} \dfrac{1}{C} + r_{\rm err}\left(\dfrac{R_L}{C\left(R_L^2 + X_L^2\right)}\right) \\ +\omega L_{\rm err}\left(\dfrac{X_L}{C\left(R_L^2 + X_L^2\right)} - \omega\right) \end{bmatrix} \tag{37}$$

where $r_{\rm err}$ is the deviation in the resistance, $L_{\rm err}$ is the deviation in the inductance, R_L is the load resistance, and X_L the load reactance. The $C_{\rm est}$ under different loads are computed for variations in *r* and *L*. The estimated capacitance as shown in (37) is a function of $r_{\rm err}$ and $L_{\rm err}$. It can also be observed from (37) that $C_{\rm est}$ depends on the load impedance. Having a knowledge of $C_{\rm est}$ under different loads (from (37)) helps compute the actual output rms $V_{\rm rms}$ (using (36)). The deviations in $V_{\rm rms}$ from the desired reference $V_{\rm rmsref}$ under different load conditions with variations in *r* and *L* can then be calculated. The actual rms output voltage under variation in *r* with *L* unchanged for different power factor loads is shown in Fig. 13. The corresponding plot as obtained from simulations is shown in Fig. 14. The plot of the actual rms voltage for variations in *L* with *r* unchanged is shown in Fig. 15, while the corresponding plot obtained from simulations is shown in Fig. 16. It can be observed from the plots that the deviation in the voltage with variations in the resistance increases with the power factor, while the deviation for the variations in the inductance decreases with the increase in the power factor. However, in both cases, the variations are well within the $\pm 5\%$ limits of the nominal rms voltage as specified in [1]. The simulated figures (see Figs. 14 and 16) show similar trajectory as the theoretical figures (see Figs. 13 and 15). Small deviations are contributed to the fact that the theoretical plots were done assuming that the control loops ensures perfect tracking of reference values with no steady-state error (see the Appendix). However, in practice, the current controller does not ensure perfect tracking of the reference value and will have

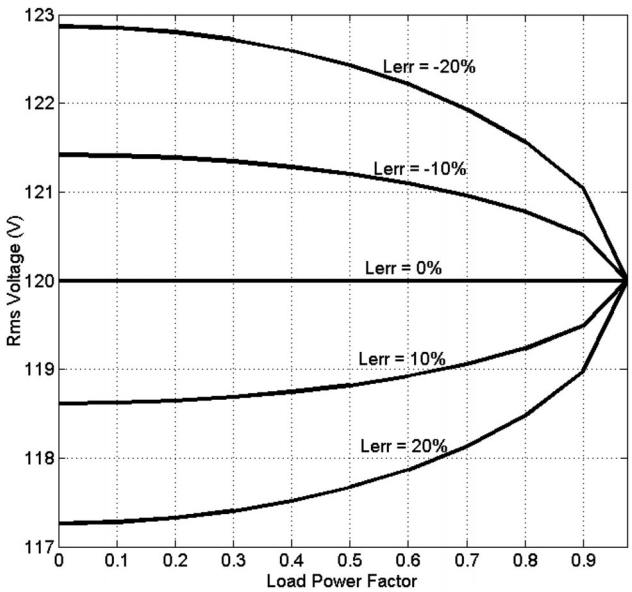

Fig. 15. Theoretical rms output voltage with error in the assumed inductance at different load power factor.

small steady-state error. In addition to the aforementioned assumption, $\delta_{\rm err}$ being small, cos $\delta_{\rm err}$ in (25) was considered to be unity for the theoretical analysis. It should be noted that the plots in Figs. 13 and 15 are under rated load condition. Hence, these plots present the worst case or maximum voltage deviation. Deviation in the output voltage under any other load is expected to be smaller than those presented in theoretical and simulation plots.

IV. Results and Discussions

A. Simulation Studies

The proposed control is verified through preliminary simulations on a on a 400 VA converter in the Simulink/PLECS

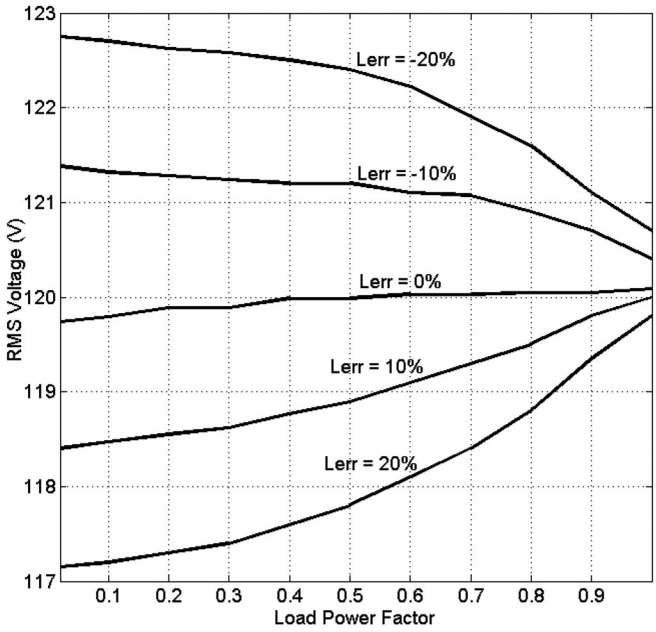

Fig. 16. Simulated rms output voltage with error in the assumed inductance at different load power factor.

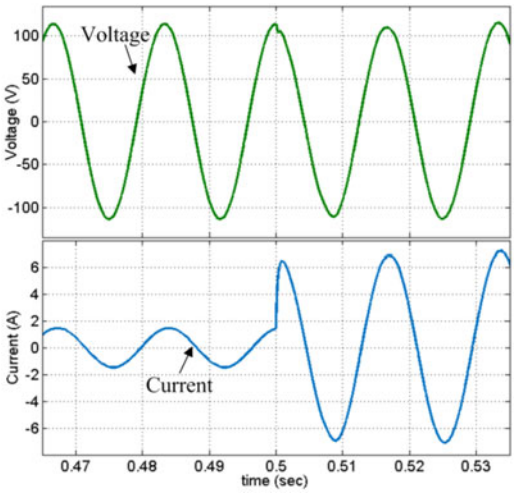

Fig. 17. Simulated voltage and load current waveforms during change in linear load.

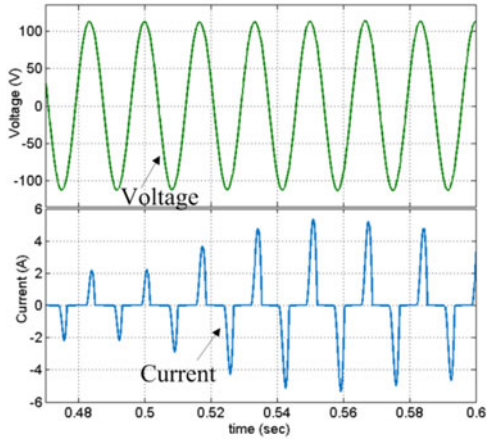

Fig. 18. Simulated voltage and load current waveforms during change in nonlinear load.

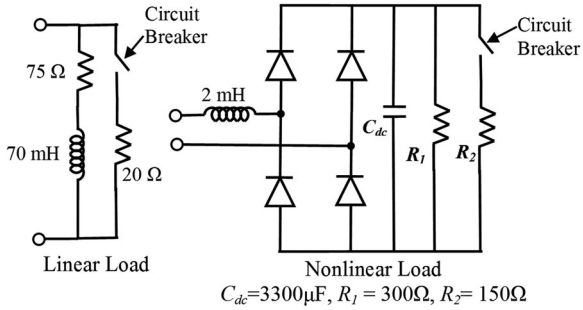

Fig. 19. Configuration of the linear and nonlinear loads using for the experimental study.

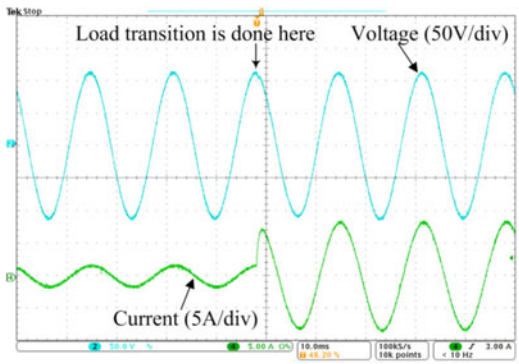

Fig. 20. Output voltage and load current waveforms during change in linear load.

platform. The power circuit and its load are kept similar to the experimental setup (discussed in the next section). The output voltage and the load current during a transition in linear load from 1 to 5 A rms are shown in Fig. 17, while those for change in nonlinear load are shown in Fig. 18. The waveforms show a stable operation under linear and nonlinear loads with negligible distortions in the load voltage.

B. Experimental Verification

The proposed control algorithm is experimentally verified on a 400 VA laboratory prototype. Limitation of the dc power supply in the laboratory restricted the output voltage to 80 V rms value. The circuit parameters details are given in Table I. Hall effect current sensors (LA-55P) were used to measure the filter inductor and load currents. The control algorithm is implemented in the TMS320F28335 digital signal controller from Texas Instruments. The details on the configuration of the linear and nonlinear loads used for the test are shown in Fig. 19.

The controller performance for a step change in the load current from 1 to 5 A rms is reported in Fig. 20. The voltage waveform during a change in nonlinear load is shown in Fig. 21. To verify the improvement in the output voltage THD under nonlinear loads, a comparison of the voltage waveform with the proposed scheme and the conventional voltage control scheme is shown in Fig. 22. The conventional voltage control scheme has an outer voltage loop with an inner current loop as

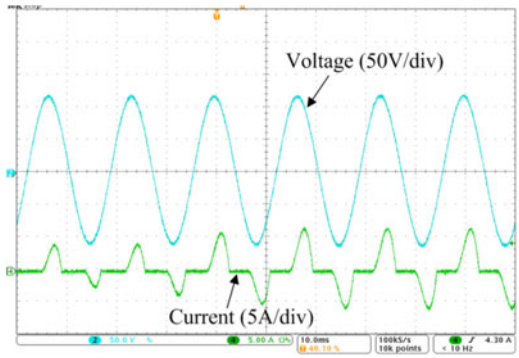

Fig. 21. Output voltage and load current waveforms during change in nonlinear load.

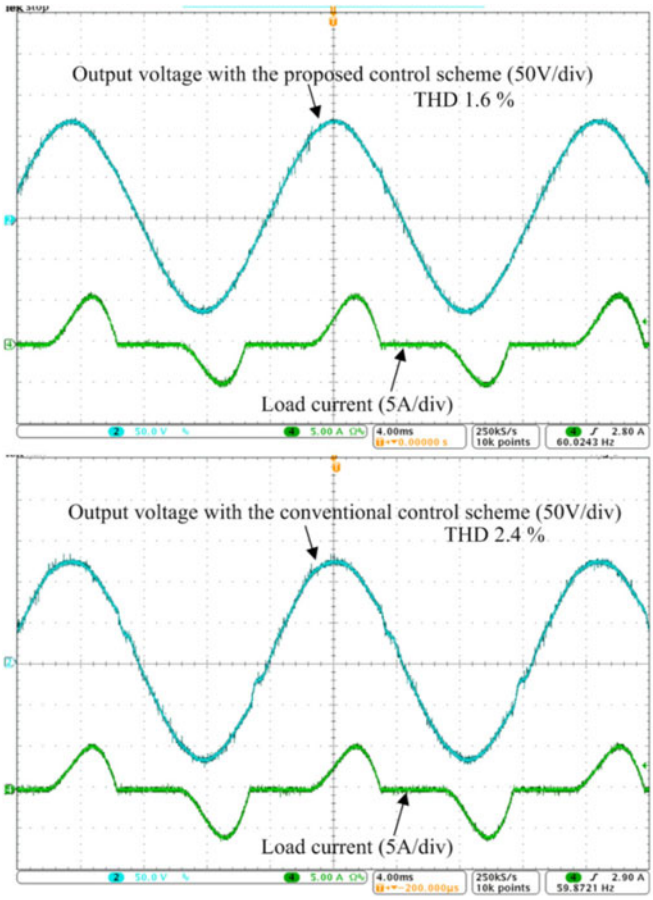

Fig. 22. Output voltage under nonlinear load with the proposed control scheme (top) and conventional voltage scheme (bottom).

shown in Fig. 2. The output voltage feedforward term was also added. The control scheme is similar to the one presented in [21]. For the same filter inductor and filter capacitor, the values of the bandwidth of the voltage control loop were at 1.8 kHz to achieve the same phase margin of 50°. It can be clearly seen from Fig. 22 that the proposed control scheme ensures less distortions in the output voltage with a THD of 1.6% compared to the conventional voltage control scheme which reported a THD of 2.4%. In both cases, the THD results were captured on the spectrum analyzer build in the oscilloscope. The output voltage during the startup of the system with the proposed

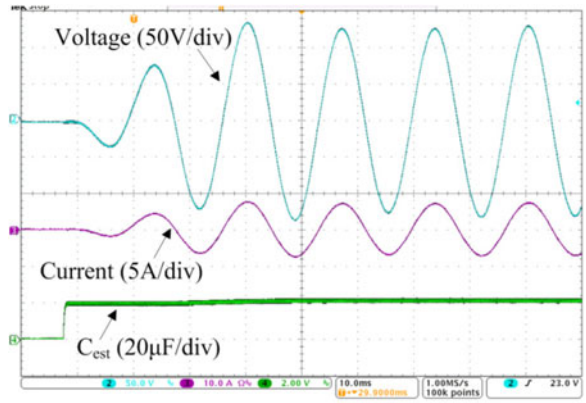

Fig. 23. Output voltage, load current, and estimated filter capacitance during a startup.

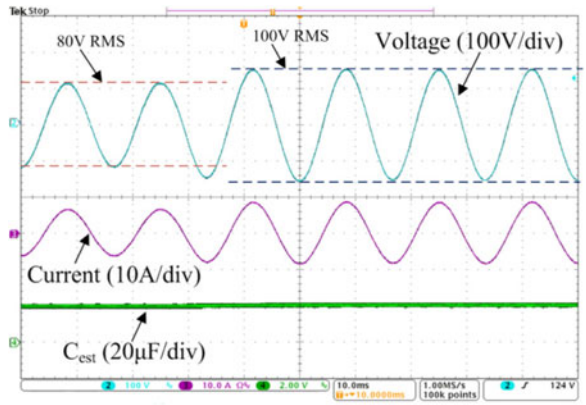

Fig. 24. Output voltage, load current, and estimated filter capacitance during a change in reference from 80 to 100 V rms.

control scheme is shown in Fig. 23. The output voltage shows slight overshoot before settling to its reference of 80 V rms. The load current and estimated capacitance are also shown in Fig. 23. The waveforms show a stable startup of the system with the proposed controller. The performance of the controller for a change in the reference voltage (80–100 V rms) is shown in Fig. 24. The waveforms confirm stable operation with negligible change in the estimated capacitance. The performance of the rms controller in estimating the capacitance is demonstrated in Fig. 25. With the inverter operating at steady state, the rms controller was disabled for three cycles and then enabled again. During this period the estimated capacitance value was forced to be 16 μF in the software. As seen from Fig. 25, with the estimated value not equal to the actual capacitance value, the output voltage deviated from its nominal value of 80 V rms. However, with the rms controller enabled again, the correct value of the estimated capacitance is tracked and the output voltage is brought back to its desired value.

Experimental results are also reported to demonstrate the effect of changes in r and L on the output voltage with the proposed control method. From the sensitivity analysis presented in Section III-B, it is clear that the error in the initial assumed resistance (r_e) creates maximum deviations in the output voltage near unity power factor operation (see Figs. 13 and 14) while the error in the assumed filter inductance (L_e) creates maximum

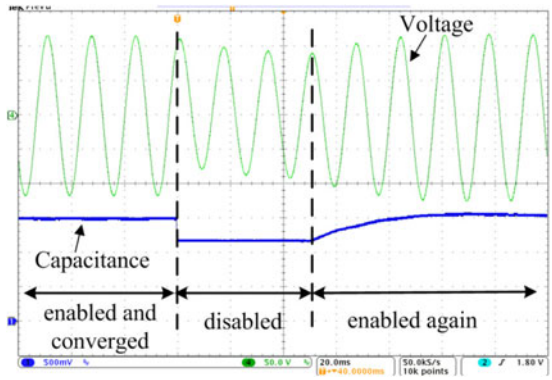

Fig. 25. Output voltage and estimated filter capacitance with rms controller disabled for 3 cycles and enabled again (voltage: 50 V/ div, capacitor: 6.67 μF/ div).

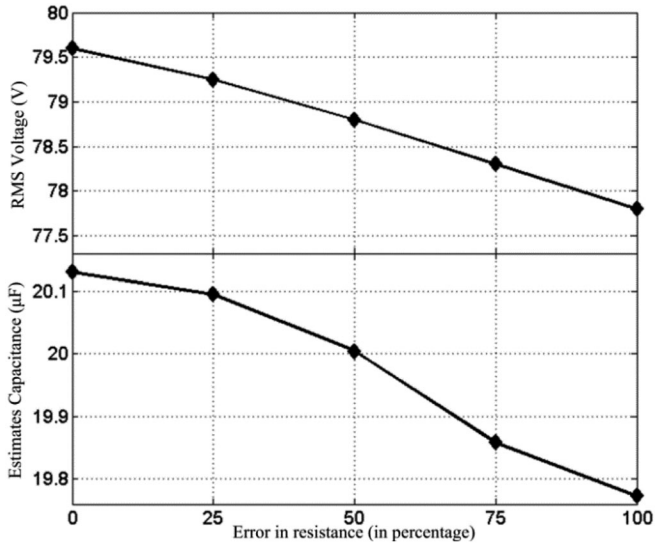

Fig. 26. Actual rms voltage and estimated capacitance for different $r_{\rm err}$ (%) at unity power factor operation.

deviation near zero power factor operation (see Figs. 15 and 16). Experiments were performed for these conditions and the results are reported in Figs. 26 and 27. Fig. 26 shows the rms value of the actual output voltage and the estimated capacitance for error in the resistance at the unity power factor operation. To create the error in the resistance, the assumed resistance (r_e) in the software was changed. The graph of the rms value of the output voltage is similar to the theoretical and simulation results reported in Figs. 13 and 14, where near unity power operation the voltage deviations increase with increase in the error $(r_{\rm err})$. The rms value of the actual output voltage and the estimated capacitance for error in the filter inductance under high inductive loads (power factor 0.1) is shown in Fig. 27. The error in the inductance was created by manipulating the value of the assumed inductance (L_e) in the software. The plot of the rms value of the output voltage is similar to the theoretical and simulation results reported in Figs. 15 and 16, where at near zero power factor operation, the rms value of the output voltage is greater than the desired reference when $L_{\rm err}$ is negative. However, when the assumed inductance is more than the actual inductance ($L_{\rm err}$ is

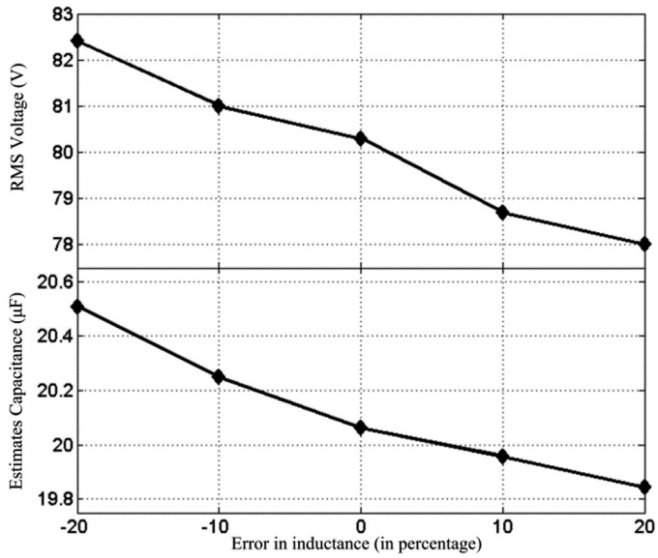

Fig. 27. Actual rms voltage and estimated capacitance for different $L_{\rm err}$ (%) under highly inductive load (load power factor 0.1).

positive), the actual rms value is less than the desired reference. The estimated capacitance in both cases (see Figs. 26 and 27) is maintained around the nominal value of 20 μF by the rms controller. Voltage deviations are within the acceptable range of $\pm 5\%$ of the nominal value of 80 V.

V. Conclusion

This paper presents a scheme to control a single-phase standalone inverter without an output voltage sensor. The control approach, mainly based on the output capacitor current control, is analyzed thoroughly. The system modeling is presented and a controller structure is proposed and designed based on the model. It is demonstrated that the presented control approach ensures better THD of the output voltage under nonlinear load conditions compared to conventional voltage control approach achieving a THD as low as 1.6%. The estimation of the output filter capacitance based on the output voltage rms control loop is also discussed. The output voltage estimation is done based on the virtual flux method. It is shown that the method is largely insensitive to the filter inductor resistance and inductance variations, keeping the output voltage within regulation specifications. Experimental results presented support the validity of the proposed control scheme.

Appendix

The derivation of the estimated capacitance $C_{\rm est}$, due to the variations in *r* and *L*, is presented next. For simplicity, the calculations are presented in a fictitious synchronous (*d*–*q*) frame of reference attached to the output voltage considering that the rms voltage control loop and the current loop ensure perfect reference tracking. Since we are interested in finding the deviation in the steady-state voltage under parameter fluctuations, all equations reported next are at steady state neglecting any dynamics. The subscripts *d* and *q* in the following equations represent the corresponding *d*-axis and *q*-axis quantities.

For a given controller output voltage V_i, the steady-state voltage across the filter capacitor, V_c in the $d-q$ coordinates, is given as

$$V_{\mathrm{id}} = rI_{\mathrm{Ld}} - \omega L I_{\mathrm{Lq}} + V_{\mathrm{cd}} \tag{A1}$$

$$V_{\mathrm{iq}} = rI_{\mathrm{Lq}} + \omega L I_{\mathrm{Ld}} + V_{\mathrm{cq}} \tag{A2}$$

whereas the corresponding estimated voltage V_{est} is given as

$$V_{\mathrm{id}} = r_e I_{\mathrm{Ld}} - \omega L_e I_{\mathrm{Lq}} + V_{\mathrm{estd}} \tag{A3}$$

$$V_{\mathrm{iq}} = r_e I_{\mathrm{Lq}} + \omega L_e I_{\mathrm{Ld}} + V_{\mathrm{estq}}. \tag{A4}$$

Using (A1) and (A2) in (A3) and (A4) leads to

$$V_{\mathrm{estd}} = r_{\mathrm{err}} I_{\mathrm{Ld}} - \omega L_{\mathrm{err}} I_{\mathrm{Lq}} + V_{\mathrm{cd}} \tag{A5}$$

$$V_{\mathrm{estq}} = r_{\mathrm{err}} I_{\mathrm{Lq}} + \omega L_{\mathrm{err}} I_{\mathrm{Ld}} + V_{\mathrm{cq}} \tag{A6}$$

where

$$r_{\mathrm{err}} = r - r_e \text{ and } L_{\mathrm{err}} = L - L_e. \tag{A7}$$

Now, for a given C_{est}, the reference of the output capacitor current in the *d–q* coordinates is given as

$$I_{\mathrm{cdref}} = -\omega C_{\mathrm{est}} V_{\mathrm{refq}} \tag{A8}$$

$$I_{\mathrm{cqref}} = \omega C_{\mathrm{est}} V_{\mathrm{refd}}. \tag{A9}$$

While the output voltage is actually given as

$$V_{\mathrm{cd}} = \frac{I_{\mathrm{cq}}}{\omega C} \tag{A10}$$

$$V_{\mathrm{cq}} = -\frac{I_{\mathrm{cd}}}{\omega C}. \tag{A11}$$

In the *d–q* coordinates $V_{\mathrm{dref}} = V_{\mathrm{refpk}}, V_{\mathrm{qref}} = 0$. Considering the current controller is ensuring perfect tracking under steady-state conditions, $I_{\mathrm{cd}} = I_{\mathrm{cdref}} = 0$, $I_{\mathrm{cq}} = I_{\mathrm{cqref}}$, and $V_{\mathrm{cq}} = 0$

$$V_{\mathrm{cd}} = \frac{C_{\mathrm{est}}}{C} V_{\mathrm{dref}} \tag{A12}$$

$$V_{\mathrm{cq}} = \frac{C_{\mathrm{est}}}{C} V_{\mathrm{qref}}. \tag{A13}$$

For a load impedance of $Z = R_L + jX_L$, the load current I_{o} is given as

$$V_{\mathrm{cd}} = R_L I_{\mathrm{od}} - X_L I_{\mathrm{oq}} \tag{A14}$$

$$V_{\mathrm{cq}} = R_L I_{\mathrm{oq}} + X_L I_{\mathrm{od}}. \tag{A15}$$

Solving (A14) and (A15), for I_{od} and I_{oq}

$$I_{\mathrm{od}} = \frac{R_L V_{\mathrm{cd}}}{R_L^2 + X_L^2} \tag{A16}$$

$$I_{\mathrm{oq}} = \frac{-X_L V_{\mathrm{cd}}}{R_L^2 + X_L^2}. \tag{A17}$$

The inductor current I_{L} can now be found as

$$I_{\mathrm{Ld}} = I_{\mathrm{od}} + I_{\mathrm{cd}} = \frac{R_L V_{\mathrm{cd}}}{R_L^2 + X_L^2} \tag{A18}$$

$$I_{\mathrm{Lq}} = I_{\mathrm{oq}} + I_{\mathrm{cq}} = \frac{-X_L V_{\mathrm{cd}}}{R_L^2 + X_L^2} + \omega C_{\mathrm{est}} V_{\mathrm{refd}}. \tag{A19}$$

The rms control loop ensures that $V_{\mathrm{estd}} = V_{\mathrm{refpk}}$. Using (A18), (A19), and (A12) in (A5), C_{est} turns out as

$$\frac{1}{C_{\mathrm{est}}} = \begin{bmatrix} \dfrac{1}{C} + r_{\mathrm{err}} \left(\dfrac{R_L}{C\left(R_L^2 + X_L^2\right)} \right) \\ + \omega L_{\mathrm{err}} \left(\dfrac{X_L}{C\left(R_L^2 + X_L^2\right)} - \omega \right) \end{bmatrix}. \tag{A20}$$

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