Comparative η–ρ–σ Pareto Optimization of Si and SiC Multilevel Dual-Active-Bridge Topologies With Wide Input Voltage Range

Ralph M. Burkart, *Student Member, IEEE*, and Johann W. Kolar, *Fellow, IEEE*

***Abstract*—This work presents a comprehensive cost-aware comparison of isolated bidirectional Si and SiC dual-active-bridge (DAB) concepts for a 5-kW 100–700-V input voltage range dc microgrid application. A conventional three-level DAB (3LDAB) is compared to an advanced five-level DAB (5LDAB) topology, where the latter enables reduced rms currents within the given voltage range. Both concepts employ a loss-optimized modulation scheme enabling zero-voltage switching. A multiobjective optimization routine is proposed to systematically assess the concepts with respect to the efficiency, power density, and the costs. A novel waveform model and advanced component models are considered, which are verified using a hardware prototype. The calculated Pareto fronts show that SiC MOSFETs enable significantly higher efficiencies and power densities than Si IGBTs, while similar costs can be achieved. The performance comparison between the SiC MOSFET-based 3LDAB and 5LDAB reveals a fundamental superiority of the 3LDAB, which is mainly due to the higher chip area utilization and the lower component count of this concept. Finally, the calculations and the hardware prototype prove that despite the galvanic isolation and wide voltage range, efficiencies above 98 % in a wide operating range are possible, which was previously not seen in the literature.**

***Index Terms*—Costs, dc–dc power conversion, multilevel systems, optimization methods, software prototyping.**

I. Introduction

IN ORDER to combat climate change, the penetration of (distributed) renewable energy sources has rapidly been increasing. Against this background, the implementation of dc microgrids, as depicted in Fig. 1, has been proposed for both residential and commercial applications [1]–[7]. Such dc microgrids are (partly) powered by photovoltaic (PV) and fuel cell energy sources, where the corresponding dc power can be used to directly supply the local loads via a dc bus. Typical dc loads are a wide range of household appliances, battery storage systems, electric vehicles and IT equipment in telecom and data center applications. Expected advantages in contrast to a conventional ac energy system are an increased system-level reliability, stability, and efficiency. As highlighted in Fig. 1, a dc microgrid involves numerous dc/dc converters, which must meet various requirements, such as:

1) *galvanic isolation* for safety reasons and the suppression of circulating currents;
2) *bidirectional power flow*, e.g., for a battery interfacing application;
3) *wide input voltage range* due to the *I–V* characteristics of batteries, PV panels, and fuel cells;
4) *exceptional performance*, i.e., high efficiency and power density at low costs.

This work investigates a dc/dc converter, which meets all of the above requirements in a single system. Such a universal converter can be employed to connect a wide range of different applications to the dc microgrid. Suitable converter topologies that are able to cope with a wide combined input–output voltage range, i.e., $\frac{V_{\mathrm{dc1,max}}}{V_{\mathrm{dc1,min}}} \cdot \frac{V_{\mathrm{dc2,max}}}{V_{\mathrm{dc2,min}}} \geq 2$, have extensively been discussed in the literature. Whereas for unidirectional isolated converters, a multitude of converter topologies have been proposed (e.g., [8]–[11]), bidirectional applications are usually based on the (nonresonant) dual-active-bridge (DAB) topology. In order to deal with the wide voltage range, most contributions propose the employment of a variable switching frequency [12], [13] and/or advanced modulation schemes [14], [15] and/or modified DAB circuits [16]–[18] instead of the originally proposed DAB with two full bridges (cf., Fig. 2(a)) and the conventional phase shift modulation scheme [19]. A five-level DAB

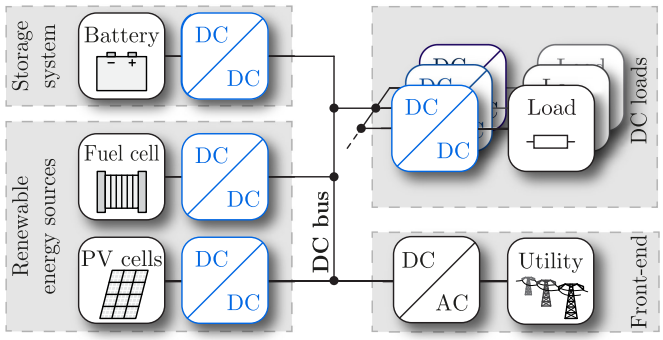

Fig. 1. DC microgrid architecture for residential or commercial applications as part of a future smart grid [21], [22]. In this work, a single dc/dc converter featuring galvanic isolation, bidirectional power flow, and a wide input voltage range is proposed, which can universally be employed to connect renewable energy sources, storage systems, and various dc loads to the common dc bus.

Manuscript received March 4, 2016; revised August 4, 2016; accepted September 13, 2016. Date of publication October 3, 2016; date of current version February 27, 2017. Recommended for publication by Associate Editor R. Ayyanar.

The authors are with the Power Electronic Systems Laboratory, Department of Electrical Engineering, Swiss Federal Institute of Technology (ETH) Zurich, 8092 Zürich, Switzerland (e-mail: burkart@lem.ee.ethz.ch; kolar@lem.ee.ethz.ch).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2614139

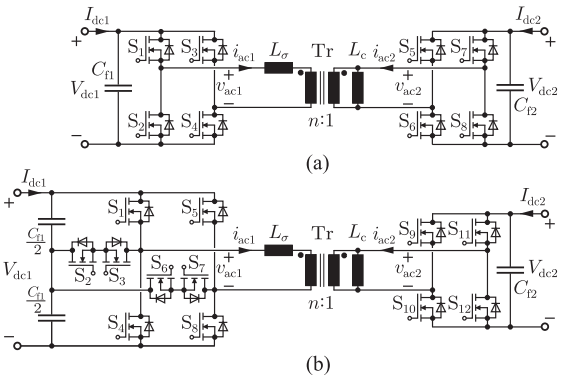

Fig. 2. DAB topologies for wide input voltage range applications. (a) 3LDAB with two-level bridge legs consisting of 1200-V rated semiconductors. (b) 5LDAB with T-type three-level bridge legs on the primary variable-voltage side. The switches S_x $x \in \{2,3,6,7\}$ are 600-V rated, whereas the remaining switches are 1200-V rated.

TABLE I
SPECIFICATIONS OF THE UNIVERSAL DC/DC CONVERTER

Rated power	P_r	5 kW
Input voltage range	$[V_{dc1,min}, V_{dc1,max}]$	[100,700] V
Output voltage	V_{dc2}	750 V
Maximum input current	$I_{dc1,max}$	22 A

(5LDAB) topology, as shown in Fig. 2(b), in combination with a novel modulation scheme was proposed in [20]. The topology extends the standard set of possible voltages applied to the primary side of the transformer, $v_{ac1} \in \{-V_{dc1}, 0, +V_{dc1}\}$, by $v_{ac1} \in \{-\frac{V_{dc1}}{2}, +\frac{V_{dc1}}{2}\}$ when compared to the three-level DAB (3LDAB). This modification is expected to extend the primary voltage range, where the converter can be operated with high efficiency.

The selection of a suitable converter concept and its optimal dimensioning for a given application are typical key issues in industry. In order to address these needs and to offer a reliable decision base, this work proposes a systematic approach to comprehensively benchmark and optimize converter concepts regarding efficiency, power density, and costs. The approach is employed to determine a suitable converter concept and dimensioning for a 5-kW 100–700-V input voltage range dc microgrid application (cf., Table I) as discussed above. In particular, the conventional 3LDAB of Fig. 2(a) is compared to the 5LDAB of Fig. 2(b). The 3LDAB is analyzed due to its relative simplicity and proven practical applicability, which are preferred features in industry. The comparison to the 5LDAB is carried out in order to investigate whether the higher 5LDAB complexity (topology and modulation scheme) can be justified by a better achievable performance. Finally, the two concepts are analyzed for both Si IGBTs and SiC MOSFETs in order to compare the potential of advanced semiconductor technology against state-of-the-art low-cost technology in this application.

The comparison of the Si and SiC 3LDAB and 5LDAB concepts in this work is based on a prior multiobjective optimization of the converter concepts including all relevant components. Three performance criteria are considered, i.e., the efficiency, power density, and the costs. On the one hand, the exclusive consideration of thoroughly optimized systems (instead of random nonoptimized system designs) strongly increases the significance of the comparison. On the other hand, the concurrent consideration of multiple performance criteria instead of only a single criterion increases comprehensiveness and enables a more complete picture of the concepts. Finally, the consideration of costs strongly increases the relevance of the investigations as costs are typically a key criterion in industry. The comparison of the proposed comprehensive and cost-aware optimization scheme in this work to similar multiobjective optimizations found in the literature [23]–[36] reveals that only [27], [35] feature the same combination of incorporating three optimization criteria (others: two) and considering costs. In [27] and [35], however, the numerical values and origin of the cost model parameters are not stated, which considerably reduces the value for practicing engineers or researchers. This is in contrast to this paper where cost models for each component type are proposed and numerical values for the parameters, i.e., the cost data are provided in detail. Another main difference of the approach in this work to the above-cited contributions is the consideration of advanced and experimentally verified loss and thermal models for all considered components. In particular, experimentally determined switching loss energies and core losses are incorporated. Furthermore, the additional switching losses that occur in the case of incomplete zero-voltage switching (ZVS) transitions are accurately determined. This is enabled by a novel waveform model, which accurately predicts the nonlinear switching transitions.

This paper is organized as follows. Section II reasons the selection of the topologies, modulation schemes, and components. Section III presents the employed models and proves their accuracy using a hardware prototype. The modeling framework is subsequently incorporated into the design and optimization routine presented in Section IV. Finally, the resulting optimized converter concepts are comprehensively analyzed and compared in Section V.

II. TOPOLOGIES, MODULATION SCHEMES, AND COMPONENTS

This section details and reasons the selection of the considered topologies, modulation schemes, and components.

A. Topologies and Modulation Schemes

This work investigates the 3LDAB and the 5LDAB, as depicted in Fig. 2. T-type neutral-point-clamped three-level bridge legs are considered in the 5LDAB due to lower attainable ZVS switching losses [37] and the ability of switching directly between the negative and positive rail voltage. The main motivation of considering the 5LDAB topology derives from the observation that a DAB can generally be most efficiently operated if the input–output voltage ratio is close to the transformer turns ratio, i.e., $\frac{V_{dc1}}{V_{dc2}} \approx n$ [20]. The 5LDAB extends the standard 3LDAB set of possible voltages applied to the primary side of the transformer $v_{ac1} \in \{-V_{dc1}, 0, +V_{dc1}\}$, by $v_{ac1} \in \{-\frac{V_{dc1}}{2}, +\frac{V_{dc1}}{2}\}$. In the case of a fixed output voltage V_{dc2}, this enables two instead of one input voltage regimes, where the above condition can be met: consider a given turns ratio and a fixed output voltage, e.g., $n \cdot V_{dc2} = 0.5 \cdot 750\text{V} = 375V$. In the case of high input voltages $V_{dc1} \approx$750 V, the converter can apply $|v_{ac1}| = \frac{V_{dc1}}{2} \approx$

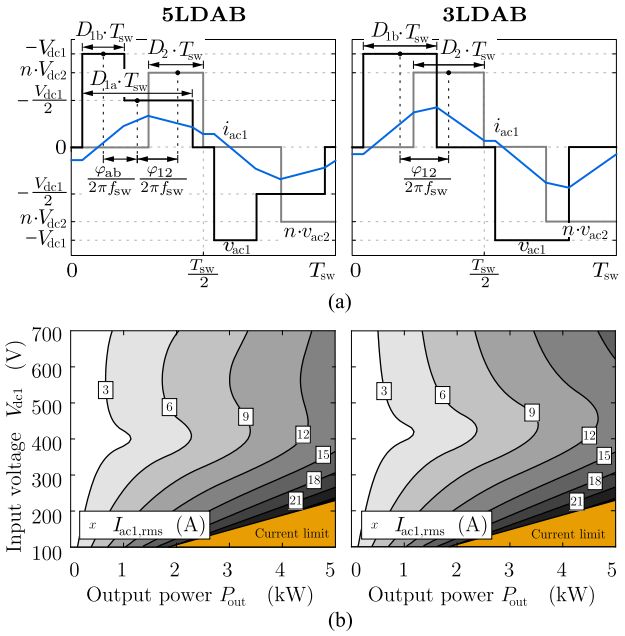

Fig. 3. Ideal generalized waveforms and minimized transformer rms currents. (a) Generalized waveforms of the 5LDAB and 3LDAB and definition of the respective control variables. (b) Minimized transformer rms currents $I_{ac1,rms}$ obtained by means of solving (1) (values for n and $L_\sigma \cdot f_{sw}$ from Table VI; currents in L_c neglected).

375 V to the primary side of the transformer, while at low input voltages $V_{dc1} \approx 375$ V, the converter uses $|v_{ac1}| = V_{dc1} \approx 375$ V in order to meet $\frac{V_{dc1}}{V_{dc2}} \approx n$.

The differing number of possible voltage levels of the 3LDAB and 5LDAB is reflected by three and five available control variables $\vec{\Xi}^*$, respectively (cf., Fig. 3(a)). This work employs the optimized 3LDAB modulation scheme proposed in [15] and the extended 5LDAB scheme proposed in [20]. The modulation schemes choose the control parameters $\vec{\Xi}^*$ so as to minimize the transformer rms current

$$\vec{\Xi}^* = \arg\min_{\vec{\Xi}} \; I_{ac1,rms}(n, L_\sigma, \vec{\Lambda}, \vec{\Xi}) \tag{1}$$

for a given transformer turns ratio n, series inductance L_σ, and any given operating point vector $\vec{\Lambda} = (V_{dc1}, V_{dc2}, P_{out})^\top$. Both modulation schemes allow for ZVS in the entire operating range. Fig. 3(b) shows the resulting operating point-dependent minimized transformer rms currents assuming similar values of n and L_σ. Inspection reveals that in the lower voltage regime ($V_{dc1} < n \cdot V_{dc2}$), the modulation schemes of the 3LDAB and 5LDAB are identical. For the reasons stated above, the 5LDAB scheme does not exploit the additional voltage levels. Consequently, nearly equal rms currents result for both concepts. Contrary, in the higher voltage regime ($V_{dc1} > n \cdot V_{dc2}$), the 5LDAB achieves significantly lower rms currents, which is a direct benefit of the application of the additional voltage levels.

The above analysis provides the main motivation for the comparison of the 3LDAB and 5LDAB. On the one hand, the 5LDAB seems to be better suited for the wide voltage range application considered in this work due to lower achievable rms currents. On the other hand, the proposed comprehensive benchmarking approach is employed to clarify whether the lower achievable rms currents of the 5LDAB translate into a better converter performance (efficiency, power density, and costs) when compared to the 3LDAB. If a significantly better performance results, the higher complexity (component count and modulation scheme) of the 5LDAB concept may be justified.

TABLE II
COMPONENTS AND MATERIALS

Component	3LDAB	5LDAB
Si IGBTs	IKW25N120T2	IKW30N60T / IKW25N120T2
SiC MOSFETs	C2M0080120D with variable chip areas	
Heat sink	Custom optimized Al heat sink	
Fans	NMB DC fan series $1x04$KL-01W-B$y0$	
Magnetics	Pack Feindrähte litz wire [30, 355] µm 1-10 × stacked Epcos ferrite N87 E-/ELP-cores	
Capacitors	Epcos MKP film capacitors B3277x, $V_r \in \{575,1200\}$ V	

B. Components

This section details the selection of the components listed in Table II and their costs. In most cases, the cost models and data from [38] were utilized. Where novel cost data were required, the same empirical methods were employed as discussed in [38] (list prices from manufacturers, large minimum order quantities MOQ > 10 kpcs.).

1) Semiconductors: The main focus of this work is set on the investigation of the achievable converter performance based on SiC MOSFETs. The main benefits of SiC MOSFETs are the low specific turn-on resistance and output capacitance, which facilitate low conduction losses and ZVS, respectively. The analysis incorporates variable chip sizes, where the reference switch was chosen to be the discrete 80-mΩ 1200-V TO-247-3-packaged SiC MOSFETs from Cree (C2M0080120D, 8 € per unit, total/active chip areas of $A_{chip} = 0.1042$ cm^2/$A_{chip,a} = 0.0819$ cm^2). The consideration of variable chip areas facilitates a generic and meaningful comparison between the 3LDAB and the 5LDAB. As a consequence, the corresponding design routine in Section IV-B requires a scaling scheme of the properties of the original switch (denoted by *) with the chip area. Based on the study of fundamental semiconductor physics [39], [40], inverse and linear scaling laws are employed for the on-state resistance $R_{ds,on}$, the thermal junction-to-case resistance $R_{th,jc}$, and the output capacitance C_{oss}

$$R_{ds,on}(A_{chip,a}) = R^*_{ds,on} \cdot \frac{A^*_{chip,a}}{A_{chip,a}} \tag{2}$$

$$R_{th,jc}(A_{chip}) = R^*_{th,jc} \cdot \frac{A^*_{chip}}{A_{chip}} \tag{3}$$

$$C_{oss}(A_{chip,a}) = C^*_{oss} \cdot \frac{A_{chip,a}}{A^*_{chip,a}} \; . \tag{4}$$

The costs are calculated using the linear model proposed in [38], with σ_{chip} being the specific costs per chip area

$$\Sigma_{SC} = 0.55 \text{ €} + \sigma_{chip} \cdot A_{chip} \; . \tag{5}$$

TABLE III
FIGURES OF MERITS OF DIFFERENT MOSFETS

Semiconductor	Type/ $V_{\mathrm{ds,max}}$ (V)	$R_{\mathrm{ds,on}}\cdot A_{\mathrm{chip,a}}$ ($\mathrm{m\Omega\cdot cm^2}$)	$R_{\mathrm{ds,on}}\cdot Q_{\mathrm{oss}}$ [3] ($\mathrm{m\Omega\cdot nC}$)	σ_{chip} ($\mathrm{€\cdot cm^{-2}}$)
C2M0080120D	SiC/1200	6.55	5408	72.01
Scaled C2M [1]	SiC/ 600	4.93	6462	64.81
CoolMOS C7 [2]	Si/ 650	10.00	34190	27.34

[1] Scaled based on [39] and [40]. [2] Average values of series. [3] @ $V_{\mathrm{ds}} = 400$ V.

Since the 5LDAB not only employs 1200-V but also 600-V-rated switches (cf., Fig. 2(b)), the figures of merits of the 600-V switches have been scaled based on the original 1200-V switch and using again [39], [40]. As evident from Table III, a lower specific turn-on resistance due to the thinner and higher doped drift layer results. The higher doping concentration also yields an increased specific output capacitance. The specific costs per chip area are assumed to be 10 % lower than for the original 1200-V switch due to similar findings for 600-/1200-V IGBTs in [38].

In order to obtain a benchmark for the still expensive commercial SiC MOSFETs, both converter concepts are additionally analyzed considering 600-/1200-V IGBTs from Infineon (IKW30N60T / IKW25N120T2, $1.6/2.4$ € per unit). Due to their comparably very low unit costs and the low sensitivity of the conduction losses toward the chip area, a scaling scheme as employed for the SiC MOSFETs is omitted for simplicity. Note that Si superjunction MOSFETs are not considered as a further alternative due to the lack of competitive 1200-V rated devices and the poor resulting performance of a serial connection of two 600-V devices (cf., Table III).

2) Cooling System: Custom aluminum heat sinks in combination with a range of standard axial dc compact fans with unit costs in the range of $[5.23, 6.63]$ € are considered. The heat sink costs are calculated using [38] assuming a manufacturing process based on extrusion.

3) Magnetics: The analysis considers commercial ferrite cores and litz wires, which are suitable for the pure high-frequency (HF) ac operation of the investigated converter concepts. The costs Σ_L are calculated using the formula from [38] and updated cost data

$$\Sigma_L = 10\,{}^{€}\!/_{\mathrm{kg}}\cdot W_{\mathrm{core}} + \left\{24 + \left(\frac{149\,\mu\mathrm{m}}{d_{\mathrm{strand}}}\right)^3\right\}{}^{€}\!/_{\mathrm{kg}}\cdot W_{\mathrm{wdg}} + 2\,€ \tag{6}$$

with W_{core} and W_{wdg} being the core and winding weights, respectively.

4) Capacitors: Film capacitors are employed whose unit costs can be calculated using [38].

5) PCB: A four-layer control and a six-layer power PCB as employed for the prototype (cf., Section III-D) with estimated total costs [38] of $\Sigma_{\mathrm{PCB}} = 7$ € are included into the analysis.

6) Auxiliary Electronics: The control, sensor, and gate driver electronics costs $\Sigma_{\mathrm{AUX}}^{\{3\mathrm{LDAB},\,5\mathrm{LDAB}\}} = \{60.4, 69.2\}$ € were estimated based on the implemented prototype and the methods of [38]. The higher auxiliary costs of the 5LDAB are a result of the higher required number of gate drivers.

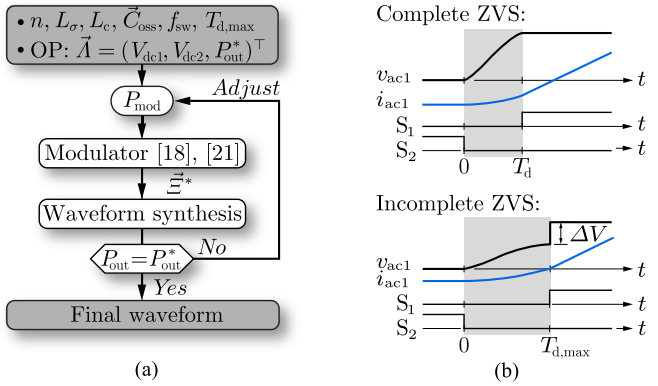

Fig. 4. Waveform model. (a) Routine to synthesize the waveforms for a given operating point $\vec{\Lambda}$. (b) Examples of complete and incomplete ZVS transition waveforms in the primary side of the 3LDAB ($S_3 = 0$, $S_4 = 1$, $n \cdot v_{\mathrm{ac2}} = 0$). The intervals highlighted in gray do not contribute to the active power transfer of the DAB.

III. MODELING

This section discusses the employed models (see Sections III-A–III-C) and experimentally verifies their accuracy using a hardware prototype (see Section III-D).

A. Waveform Model

A waveform model, as depicted in Fig. 4(a), is proposed to synthesize the operating point-dependent waveforms. In a first step, the modulator executes the closed-form expressions derived in [15] and [20], which yield the optimal control parameters $\vec{\Xi}^*(V_{\mathrm{dc1}}, V_{\mathrm{dc2}}, P_{\mathrm{mod}})$ solving (1). In a next step, the waveforms are synthesized in time domain, where the strongly nonlinear finite-speed switching transitions are modeled in detail (cf., Fig. 4(b)). The dynamics of the transitions are mainly governed by the charging/discharging of the parasitic layout and semiconductor output capacitances and the feedback of the resulting nonlinear voltage on the currents in the magnetics. The corresponding differential equations are solved using the Euler forward integration method and a sufficiently small step size. Note that the modulator assumes ideal waveforms (cf., Fig. 3(a)) and thus neglects the switching transition time intervals, which do not contribute to the active power transfer of the DAB. Therefore, the modulator and waveform synthesis must be iterated using adjusted modulator power levels P_{mod} until the actual transferred power P_{out} of the synthesized waveform matches the reference P^*_{out}.

This work distinguishes complete and incomplete ZVS transitions as shown in Fig. 4(b). The analysis conducted in [41] shows that the latter occurs if the switched bridge leg current does not deliver sufficient charge within the adaptive dead time interval $T_{\mathrm{d}} \in [0, T_{\mathrm{dead,max}}]$ to fully charge/discharge the involved output and layout capacitances. In this case, additional and non-negligible losses depending on the residual voltage ΔV occur as described in Section III-B. The proposed detailed modeling of the switching transition waveforms is, therefore, indispensable

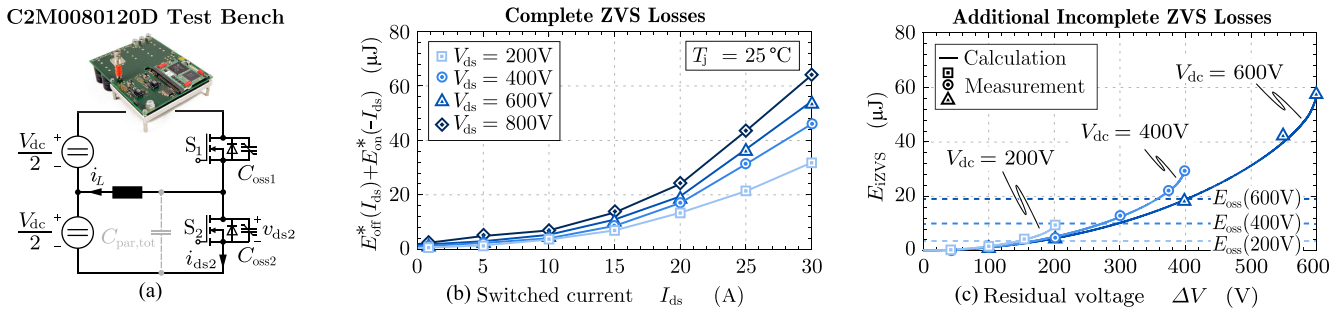

Fig. 5. Switching loss measurements. (a) Test bench for double-pulse measurements of the SiC MOSFET C2M0080120D. (b) Measured combined turn-off and turn-on switching losses under complete ZVS conditions (cf., Fig. 4(b)). The measurements for $T_j = 125\,°C$ yield $\approx 10\,\%$ higher losses. (c) Additional incomplete ZVS losses as a function of the residual voltage ΔV across the turning-on switch (cf., Fig. 4(b) [41]).

to accurately determine the amount of available charge and to identify complete/incomplete ZVS transitions. Note that many publications solely consider the sign of the switched current for this analysis (e.g., [16]–[18]). Such an approach may thus result in significantly underestimated losses. Publications that also employ charge-based approaches are found to be [12], [42]–[44]. These approaches, however, are simplified when compared to the proposed waveform model in this work and are thus likely to yield a reduced accuracy: the additional charge requirement for the parasitic layout capacitance $C_{\text{par,tot}}$ (cf., Fig. 5(a)) is neglected in all cited publications. Furthermore, only linear current and voltage waveforms are assumed during the switching transition in [12], [42], and [43]. Finally, the approach in [44] is limited to stating the conditions for complete ZVS, whereas the residual voltage ΔV cannot be calculated.

B. Semiconductor Models

1) Conduction Losses: The conduction losses P_c are computed considering the current- and junction temperature-dependent output characteristics $V_{ce}\big(i_{ce}(t), T_j\big)$ and $R_{ds,on}\big(i_{ds}(t), T_j\big)$, respectively, of the considered IGBT and MOSFET devices. Interpolated data sheet parameters are employed, which in the case of the SiC MOSFETs are scaled with the active chip area $A_{\text{chip,a}}$ according to (2).

2) Switching Losses: The occurring (regular) switching losses P_{sw} in the case of complete ZVS are calculated using current-, voltage-, and temperature-dependent switching loss energies. For the SiC MOSFET-based converters, the experimentally determined switching losses of Fig. 5(b) are employed. The increasing total switching losses can mostly be attributed to the turn-off losses as a result of the finite speed of the gate driver. The loss energies are scaled with the chip area according to

$$E_{\text{on/off}}\big(I_{\text{on/off}}, V_{\text{on/off}}, T_j, A_{\text{chip,a}}\big) = \frac{A_{\text{chip,a}}}{A^*_{\text{chip,a}}} \cdot E^*_{\text{on/off}}\left(\frac{A^*_{\text{chip,a}}}{A_{\text{chip,a}}} \cdot I_{\text{on/off}}, V_{\text{on/off}}, T_j\right) . \quad (7)$$

Interpolated data sheet switching losses are employed for the IGBT-based converters.

3) Incomplete ZVS Losses: In addition to the regular switching losses P_{sw}, additional losses P_{iZVS} occur in case of incomplete ZVS as depicted in Fig. 4(b). These additional losses occur in the turning-on switch and are partly due to the residual energy in the associated output capacitance $E_{oss}(\Delta V)$, which is dissipated in the switch. The measurements carried out in [41] and shown in Fig. 5(c) reveal, however, that the losses can be well above the energy in C_{oss} due to other effects such as the residual energy in the parasitic layout capacitance $C_{\text{par,tot}}$ (cf., Fig. 5(a)). In this work, the additional incomplete ZVS losses are analytically calculated using the formula derived in [41]. This formula enables a very high accuracy as depicted in Fig. 5(c).

C. Remaining Component Models

1) Cooling System: The cooling system design routine is based on the fluid dynamics and thermodynamics models presented in [46]. The design routine generates optimized combinations of sink geometries and fans and takes into account the possible semiconductor arrangements on the heat sink.

2) Magnetics: The design of the magnetics is based on the experimentally verified loss, thermal, and reluctance models presented in [47] and [48]. The analytical winding loss calculation considers the skin and proximity effects. The core losses P_{core} are computed by means of the improved-improved generalized Steinmetz equation (i^{2}GSE)

$$P_{\text{core}} = V_{\text{core}} \cdot f_{sw} \cdot \sum_i \overline{k}_i \; \Delta T_i^{1-\alpha_i} \; |\Delta B_i|^{\beta_i} \; . \quad (8)$$

ΔB_i denotes the peak-to-peak flux density swings of the piecewise linear HF flux segments and T_i the corresponding time intervals ($\sum T_i = \frac{1}{f_{sw}}$). The operating-point-dependent Steinmetz parameters $(\overline{k}_i, \alpha_i, \beta_i)$ are determined based on experimentally measured core loss data, where the influence of the premagnetization B_{dc} and the temperature T_{core} is taken into account. A subset of the core loss data is depicted in Fig. 6, which reveals a clear improvement of the accuracy when compared to the data sheet.

3) Capacitors: The capacitor losses P_C are calculated based on data sheet loss parameters.

4) PCB: The PCB losses P_{PCB} comprise the copper conduction and the FR4 dielectric losses. The former are calculated using the measured PCB resistances of the prototype. The latter

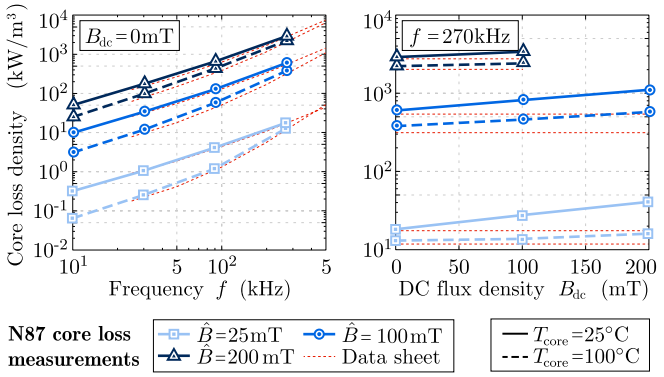

Fig. 6. Subset of the ferrite N87 core losses measured with the resonant capacitive method proposed in [45]. Varying frequencies $f \in [10, 270]$ kHz, flux densities $\hat{B} \in [25, 100]$ mT, DC premagnetization levels $B_{dc} \in [0, 200]$ mT, and temperatures $T_{core} \in [25, 100]$ °C were investigated. A significant impact of B_{dc} on the core losses was observed, which is not revealed by mere data sheet information.

TABLE IV
BOM OF THE SIC 3LDAB HARDWARE PROTOTYPE

Component	Specifications
$S_{\{1,2,3,4\}}$	2 × TO-247-3 80-mΩ 1200-V SiC MOSFET C2M0080120D
$S_{\{5,6,7,8\}}$	1 × TO-247-3 80-mΩ 1200-V SiC MOSFET C2M0080120D
$C_{f\{1,2\}}$	3 × 12-µF 1100-V MKP film capacitor B32776G0126
Tr	5 × E80/38/20 core sets N87 & 9.2 m 2205 × 71 µm litz wire
L_σ	3 × E42/21/15 core sets N87 & 1.5 m 2205 × 71 µm litz wire
L_m	1 × E42/21/20 core set N87 & 12.1 m 120 × 71 µm litz wire
Cooling System	(122 × 80 × 40) mm³ custom Al sink with 41 fins & 3 × (40×40×10) mm³ 12-V 1.08-W fans MC35162

are estimated with

$$P_{FR4} = \frac{\delta_{FR4}}{2\pi\, C_{PCB}} \cdot \sum_n \frac{I^2_{FR4,(n)}}{n \cdot f_{sw}} \tag{9}$$

where $\delta_{FR4} = 1.5\,\%$ is the loss tangent provided by the PCB manufacturer, C_{PCB} the involved PCB capacitance during a switching transition, and $I_{FR4,(n)}$ the harmonics of the current which charges/discharges C_{PCB}.

5) Auxiliary Electronics: The Auxiliary circuit losses P_{AUX} include the gate driver losses P_{GD}, the cooling system fan losses P_{CS}, and the measured power consumption of the control and measurement electronics of the prototype $P_{control} = 3$ W, where a supply efficiency of $\eta_{sup} = 75\,\%$ is assumed

$$P_{AUX} = \frac{1}{\eta_{sup}} \cdot (P_{GD} + P_{CS} + P_{control}). \tag{10}$$

D. Experimental Verification

In this section, the accuracy of the aggregate models is verified using a hardware prototype of a SiC 3LDAB, which employs the discussed modulation scheme. A photograph of the converter is shown in Fig. 7, whereas the bill of material (BOM) is listed in Table IV. The converter operates at a switching frequency of 48 kHz and achieves a maximum efficiency of $\eta_{max} > 98.5\,\%$ (including 9.57-W auxiliary power consumption). The measured system efficiency of the power stage (excluding the auxiliary supply) is depicted in Fig. 8(a). The converter power stage achieves a very high efficiency of $\eta > 98\,\%$ in a wide range of the operating area, which is mainly due to complete ZVS operation (no incomplete ZVS losses) in most operating points. Fig. 8(b) depicts the modeling error of the efficiency calculation of the prototype based on the models in this section. A very high modeling accuracy is achieved where the mean absolute error is 2.5 % and the maximum error below 7 %. Fig. 9 shows the estimated minimum, average, and maximum relative loss shares for each of the considered loss types. It can be observed that the minimum and maximum shares for all loss types vary dramatically within the investigated operating area. It can thus be assumed with high certainty that all individual loss models must feature a high accuracy to achieve the excellent overall accuracy in every operating point as found in Fig. 8(b). Moreover, an accidental compensation of different modeling errors seems to be unlikely. Further support for this conclusion can be found in Fig. 10, which visualizes the accuracy of the thermal models for the magnetics. The measured temperatures deviate from the calculations within [−15,+5] %. An essential key to the obtained close match between models and measurements proved to be the novel waveform synthesis approach, which generates precise predictions of the current and voltage waveforms as demonstrated in Fig. 11.

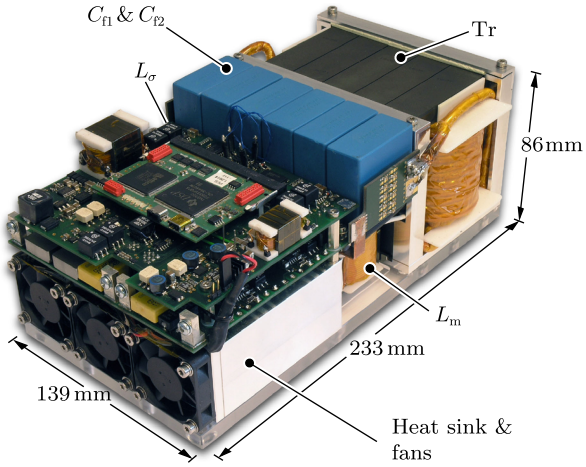

Fig. 7. Photograph of the SiC 3LDAB hardware prototype. The converter volume is 2.79 dm³ (1.8 kW/dm³), whereas the total boxed component volume is $V_{box} = 1.95$ dm³ ($\rho_{box} = 2.56$ kW/dm³).

IV. MULTIOBJECTIVE OPTIMIZATION

This section details the concepts behind the employed DAB multiobjective optimization routine. The optimality criteria employed in this work are the averaged efficiency η_{avg} over the operating points $\vec{\Lambda}_{opt,i}$ shown in Fig. 8, the power density ρ_{box} based on the total boxed volume of the components, and the specific costs $\sigma_P = \frac{P_t}{\Sigma_{tot}}$, with Σ_{tot} being the total component costs. The employed parameters and constraints are listed in Table V.

A. Multiobjective Optimization Routine

The proposed approach is motivated by the work presented in [49]. If parasitic electromagnetic and thermal coupling effects

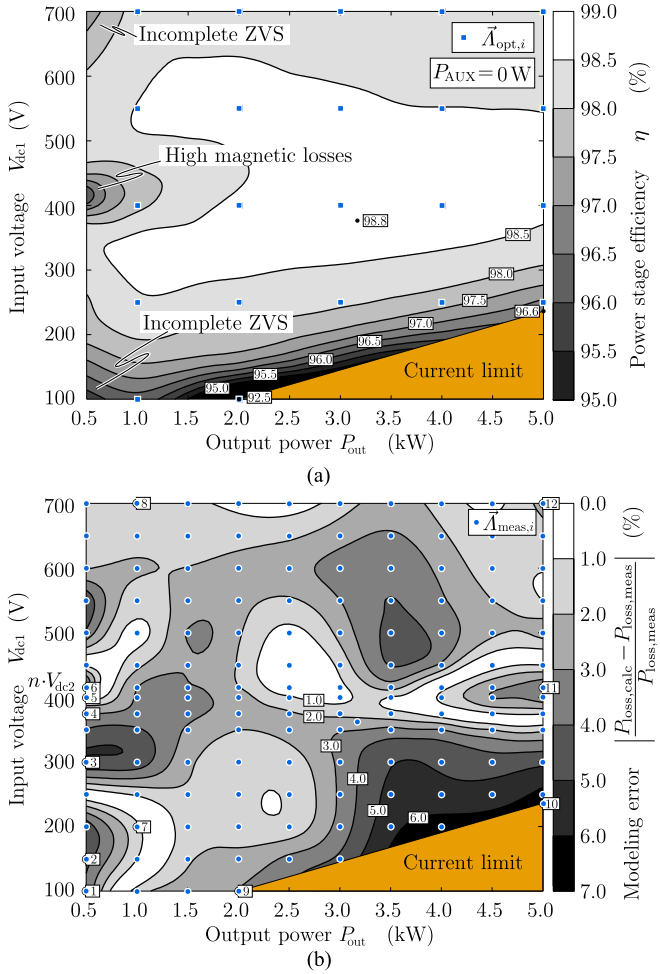

Fig. 8. Loss model verification. (a) Measured efficiency of the power stage of the SiC 3LDAB hardware prototype. Further shown are the operating points $\vec{\Lambda}_{\mathrm{opt}}, i$, which are considered in the optimization routines of Section IV. (b) Relative deviation between the calculated converter losses $P_{\mathrm{loss,calc}}$ and the measured losses $P_{\mathrm{loss,meas}}$ in (a). The mean modeling error across all measured operating points $\vec{\Lambda}_{\mathrm{meas},i}$ is 2.5 %.

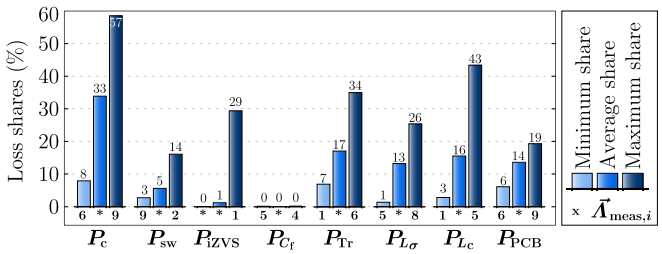

Fig. 9. Calculated loss shares in the prototype: average loss shares across all operating points and minimum and maximum shares with the corresponding operating point number (cf., labels in Fig. 8(b)). The widely varying shares of each loss source in conjunction with the low observed modeling error in the entire operating area Fig. 8(b) suggest a high modeling accuracy of each individual loss model.

are neglected, the DAB components as shown in Fig. 2 are solely coupled through their impact on the current and voltage waveforms in the circuit. From a conceptual point of view, this observation, therefore, suggests to divide the available design variables into two distinct categories.

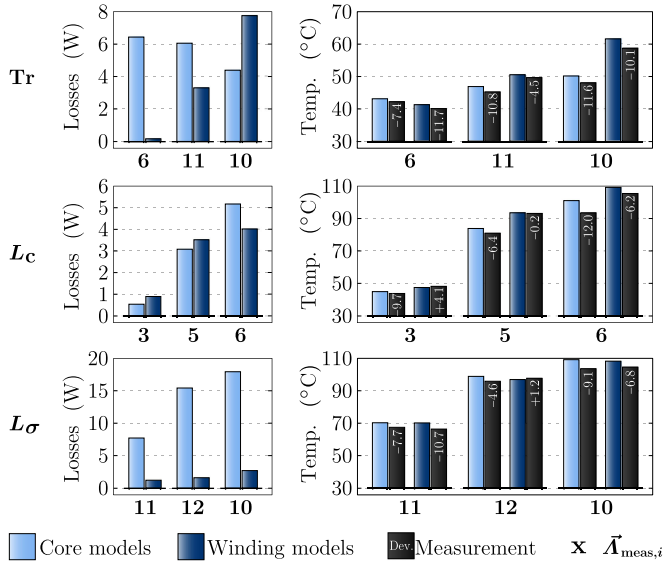

Fig. 10. Verification of the employed magnetics thermal models at $T_{\mathrm{amb}} = 30\,^{\circ}\mathrm{C}$. The shown operating points (cf., labels in Fig. 8(b)) include the component-specific worst cases. The deviations of the measurements lie within −15/+5 %. The generally overestimated temperature rise can mainly be explained by the heat flow leaving the component through the connecting wires, which is neglected in the model.

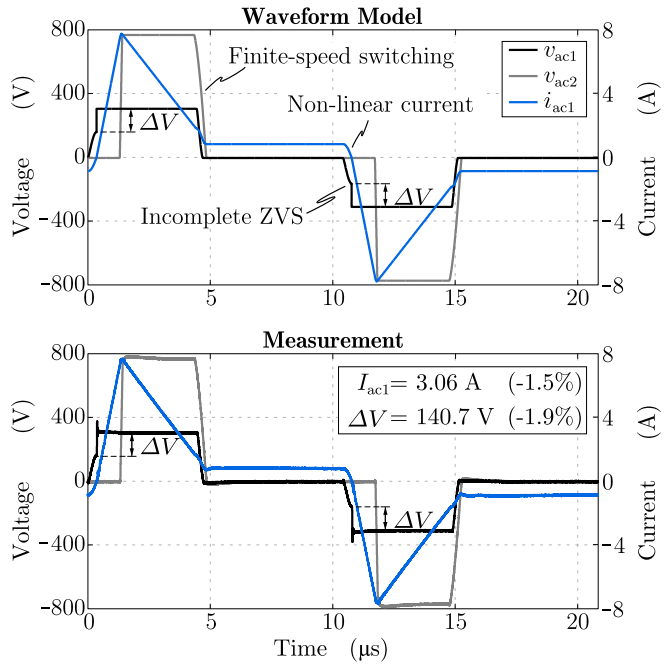

Fig. 11. Example of the experimental verification of the waveform model for $\vec{\Lambda} = \vec{\Lambda}_{\mathrm{meas},3} = (300\,\mathrm{V}, 750\,\mathrm{V}, 500\,\mathrm{W})$. The detailed modeling of the switching transitions facilitates the identification of complete and incomplete ZVS and thus an accurate switching loss prediction.

1) Global variables that affect the waveforms: f_{sw}, T_{dead}, n, L_σ, L_{c}, C_{f1}, C_{f2}, $A_{\mathrm{chip}}^{\mathrm{600p}}$, $A_{\mathrm{chip}}^{\mathrm{1200p}}$, $A_{\mathrm{chip}}^{\mathrm{1200s}}$.
2) Independent groups of local component-level variables with a small or negligible impact on the waveforms:
   a) Five variables per inductor (type and # of stacked cores, # of turns, turn, and strand diameter) and six variables for the transformer (additional: secondary turn diameter);

TABLE V
OPTIMIZATION PARAMETERS AND CONSTRAINTS

SiC MOSFET semicond. costs range	$\Sigma_{\text{SC,tot}}$	{74, 96, 141} €
SiC MOSFET switch. frequency range	f_{sw}	{50, 75,...,300} kHz
Si IGBT switch. frequency range	f_{sw}	{5,6,...,20} kHz
Design switching frequency	f_{sw}^*	50 kHz
Max. rel. dead time per switch. trans.	$k_{\text{d,max}}$	2.5 %
Max. peak-to-peak voltage ripple [1)]	ΔV_{max}	2 V
Max. junction temperature	$T_{\text{j,max}}$	125 °C
Ambient temperature	T_{amb}	25 °C
Total parasitic capacitance [2)]	$C_{\text{par,tot}}$	[230, 300] pF
Max. core stacking factor (magnetics)	$N_{\text{stack,max}}$	5
Max. core temperature	$T_{\text{core,max}}$	100 °C
Max. winding temperature	$T_{\text{wdg,max}}$	125 °C

[1)] Also applicable for the 5LDAB C_{fl} capacitor midpoint potential.
[2)] Depending on topology and bridge leg, values based on prototype (cf., Section III-D).

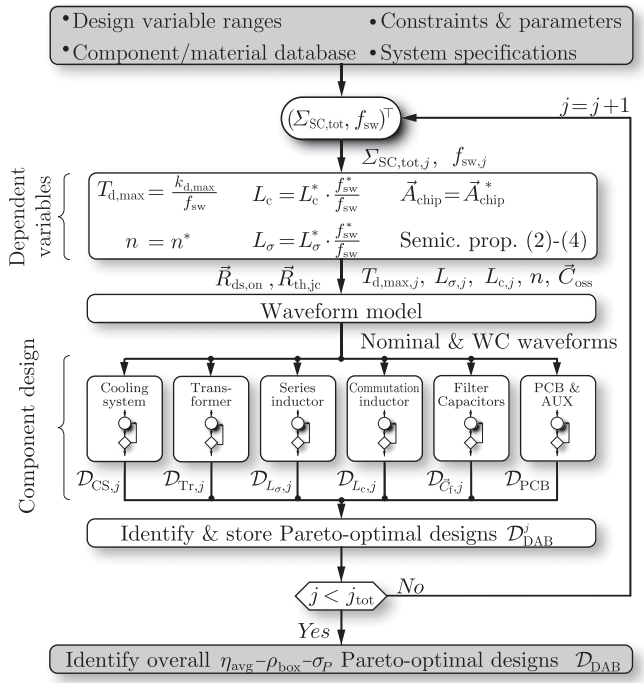

Fig. 12. Flowchart of the proposed main multiobjective DAB optimization routine. The routine calculates and identifies the Pareto-optimal converter designs $\mathcal{D}_{\text{DAB}}$ as a combination of individually optimized components for varying total semiconductor costs and switching frequencies.

b) Four cooling system variables (sink length and # of fins, # and type of fans);
c) One variable for each capacitor (type).

$\vec{A}_{\text{chip}} = (A_{\text{chip}}^{\text{600p}}, A_{\text{chip}}^{\text{1200p}} A_{\text{chip}}^{\text{1200s}})^\top$ denotes the primary-side 600- and 1200-V as well as the secondary-side 1200-V chip areas per switch (cf., Fig. 2). In this work, category 2 variables have a negligible impact on the current and voltage waveforms as the design procedure aims at low loss components. Therefore, the above proposed distinction of the design variables enables the optimization routine depicted in Fig. 12. Here, category 1 variables are defined in an outer (global) loop, where for each iteration, a new set of waveforms is calculated. Based on these waveforms, the components can be individually optimized in inner (local) component-level loops iterating the respective converter designs $\mathcal{D}_{\text{DAB}}^j$ as a combination of the optimized components are identified and stored. After the execution of the main loop, the overall Pareto-optimal converter designs are identified among $\bigcup_j \mathcal{D}_{\text{DAB}}^j$.

It is evident from Fig. 12 that global variables are computationally expensive as the waveform synthesis and component design must be repeated for each iteration of these variables. Therefore, only the most influential category 1 variables, i.e., the switching frequency f_{sw} and in the case of SiC MOSFETs additionally the total chip area are kept as independent design variables. Note that the total chip area is controlled by means of the total semiconductor costs $\Sigma_{\text{SC,tot}}$, whereas the chip area distribution $\vec{A}_{\text{chip}}$ is, together with the remaining global variables, predetermined as described below.

B. Determination of Dependent Global Design Variables

This section describes how the dependent global design variables, i.e., $T_{\text{d,max}}$, n, L_σ, L_{c}, C_{f1}, C_{f2}, and $\vec{A}_{\text{chip}}$ are predetermined in order to reduce the complexity of the main optimization task. The main challenge here is to predetermine these variables in a way that potentially interesting designs that result in a high performance in the subsequent main optimization are not ruled out in the first place.

1) Dead Time: Long relative dead times and switching transition durations impair the minimum duty cycle capabilities of the converter, increase the circulating reactive power, and decrease the maximum possible power transfer (cf., Fig. 4(b)). Therefore, a reasonable value of the maximum permissible relative dead time per switching transition is found to be $k_{\text{d,max}} = 2.5\%$ of the switching period T_{sw} (e.g., $T_{\text{d,max}} = 500$ ns at $f_{\text{sw}} = 50$ kHz).

2) Filter Capacitances: The employed modulation schemes rely on close-to-ideal dc voltages V_{dc1} and V_{dc2} in order to work properly. Therefore, the maximum permissible peak-to-peak voltage ripple is limited to $\Delta V_{\text{max}} = 2\,V$. This constraint implies large capacitances $\vec{C}_{\text{f}} = (C_{\text{f1}}, C_{\text{f2}})^\top$ with a negligible impact on the waveforms.

3) Inductances, Turns Ratio, and Chip Areas: The impact of the remaining design variables $\vec{\Pi} = (n, L_\sigma, L_{\text{c}}, \vec{A}_{\text{chip}})^\top$ on the system performance is strongly coupled: n and L_σ largely determine the current waveforms. The selection of $\vec{A}_{\text{chip}}$ does not only influence the conduction losses but also, based on the resulting $\vec{C}_{\text{oss}}$, the switching transitions and the ZVS losses. Finally, the external commutation inductor L_{c} facilitates ZVS but in turn increases the rms currents and hence the conduction losses. Due to the mutual coupling, $\vec{\Pi}$ must be determined in a concurrent manner. For this purpose, consider the optimization routine depicted in Fig. 13.

In a first step, the semiconductor properties are calculated as a function of $\vec{A}_{\text{chip},j}$ using (2)–(4). In a next step, based on n_j, $L_{\sigma,j}$, and the proposed modulation scheme, the current and voltage waveforms are calculated. The commutation inductance L_{c} (which only introduces reactive power and does not contribute to the power transfer) is then added and adjusted such that complete ZVS can be achieved within $T_{\text{d}} \in [0, T_{\text{dead,max}}]$ for each switching transition and operating point $\vec{\Lambda}_{\text{opt},i}$. In a final step,

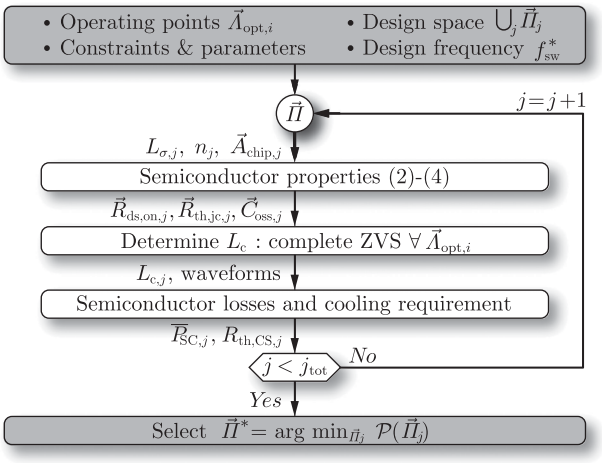

Fig. 13. Flowchart of the offline routine used to determine the reference values $\vec{\Pi}^* = (n^*, L_\sigma^*, L_{\text{c}}^*, \vec{A}_{\text{chip}}^*)$ of the dependent system variables of the main multiobjective DAB optimization routine shown in Fig. 12.

TABLE VI
SiC MOSFET Optimal Design Variables $\vec{\Pi}^*$ for $f_{\text{sw}}^* = 50$ kHz

$\Sigma_{\text{SC,tot}}$ (€)		n^*	L_σ^* (µH)	L_{c}^* (µH)	$\vec{A}_{\text{chip}}^*$ (cm^2)
3LDAB	74	0.5	37.9	727	$(-, 0.1549, 0.0871)^\top$
	96	0.5	37.9	614	$(-, 0.2067, 0.1134)^\top$
	141	0.5	37.9	468	$(-, 0.3117, 0.1647)^\top$
5LDAB	74	0.5	37.8	885	$(0.0391, 0.1242, 0.0750)^\top$
	96	0.5	37.8	753	$(0.0521, 0.1656, 0.1003)^\top$
	141	0.5	37.8	581	$(0.0833, 0.2484, 0.1453)^\top$

and switching losses

$$\overline{P}_{\text{SC}} = \sum_{i=1}^{M} \frac{P_{\text{c,tot},i} + P_{\text{sw,tot},i}}{P_{\text{out},i}} \tag{11}$$

are calculated across the $M = 23$ given operating points $\vec{\Lambda}_{\text{opt},i}$. At the same time, the required thermal resistance of the cooling system $R_{\text{th,CS}}$ is determined to limit the maximum junction temperature to $T_{\text{j,max}} = 125\,^\circ$C. After completion of the iteration over all variables, the cost function

$$\mathcal{P} : \vec{\Pi} \rightarrow \frac{2}{3} \cdot \frac{\overline{P}_{\text{SC}}}{\overline{P}_{\text{SC,min}}} + \frac{1}{3} \cdot \frac{R_{\text{th,CS,max}}}{R_{\text{th,CS}}} \tag{12}$$

is used to determine the optimal choice of design variables $\vec{\Pi}^*$. The cost function (12) is designed so as to find a compromise between weighted total semiconductor losses $\overline{P}_{\text{SC}}$ and required cooling effort with respect to the best achievable values $\overline{P}_{\text{SC,min}}$ and $R_{\text{th,CS,max}}$ within the chosen design space of $\vec{\Pi}$.

The above outlined optimization is carried out for a design switching frequency of $f_{\text{sw}}^* = 50$ kHz, for which low switching and zero incomplete ZVS losses can be achieved with a reasonable amount of additional reactive current in L_{c}. The routine depicted in Fig. 13 is executed for three different values of the total SiC MOSFET semiconductor costs $\Sigma_{\text{SC,tot}} = \{74, 96, 141\}$ € in order to investigate the impact of varying chip areas as discussed above. Note that $\Sigma_{\text{SC,tot}} = 96$ € corresponds to the semiconductor costs of the prototype (cf., Section III-D). Table VI lists the calculated optimal reference design variables $\vec{\Pi}^*$ as a function of $\Sigma_{\text{SC,tot}}$. It can be seen that for both the 3LDAB and 5LDAB, the transformer turns ratio n^*, the series inductance L_σ^*, and the relative chip area distributions are largely invariant from $\Sigma_{\text{SC,tot}}$. Investigations show that these values are mainly determined by the selection of the operating points. Contrary, L_{c}^* is a function of the absolute chip areas, where the SiC 5LDAB requires less reactive power provided by L_{c}^* to achieve complete ZVS in all considered operating points. The latter is a result of the more uniform current waveforms enabled by the 5LDAB modulation scheme. The optimal reference values for the Si IGBT-based concepts are analogously determined, where the fixed semiconductor configurations of Table II were considered (no variable chip areas).

The switching frequency remains, as discussed previously, an independent global variable in the proposed main optimization routine. With respect to switching frequencies differing from the design frequency, i.e., $f_{\text{sw}} \neq f_{\text{sw}}^*$, it is thus proposed to scale the calculated reference inductance values with

$$L_\sigma = L_\sigma^* \cdot \frac{f_{\text{sw}}^*}{f_{\text{sw}}}\,, \quad L_{\text{c}} = L_{\text{c}}^* \cdot \frac{f_{\text{sw}}^*}{f_{\text{sw}}}\,. \tag{13}$$

This approach will largely preserve the waveforms guaranteeing similarly low conduction losses in the components irrespective of f_{sw}. The major difference for $f_{\text{sw}} \neq f_{\text{sw}}^*$ is the ZVS properties of the converter: since the current waveforms do not significantly change, less charge can be provided within $T_{\text{d,max}} = \frac{k_{\text{d,max}}}{f_{\text{sw}}}$ at elevated switching frequencies. As a consequence, incomplete ZVS losses must be expected, which start to occur at low-load operating points first, where less reactive power for ZVS is available. The possible countermeasure of decreasing L_{c} more than in (13), e.g., with $L_{\text{c}} \propto \frac{1}{f_{\text{sw}}^2}$ is a less attractive approach: in that case, increased reactive currents and thus additional conduction losses would result. Since these additional conduction losses would mainly occur at high power levels, not only a similar reduction of the efficiency but also a significant volume increase due to thermal constraints would result.

V. Results

This section presents the results of the η_{avg}–ρ_{box}–σ_{P} multiobjective optimization of the considered SiC and Si 3LDAB and 5LDAB concepts. Approximately 25 000 Pareto-optimal designs were found for each concept based on the routine in Fig. 12, which is entirely implemented in MATLAB. The optimization problem involves a total of 25 design variables: 22 component variables as listed in Section IV-A, the switching frequency, the total semiconductor costs, and the selection of the concept. Standard computational means (workstation with 2×2.4 GHz Intel XEON quad core CPUs, 64 GB RAM) were sufficient to handle the problem and find the solution in less than 5 hours.

A. Comparison of the Concepts

Fig. 14 shows the Pareto fronts of the Si and SiC 3LDAB and 5LDAB concepts. The first main finding is the dramatically lower overall system performance of the IGBT-based concepts when compared to the SiC-based counterparts. Much lower efficiencies and power densities result, and despite the employment

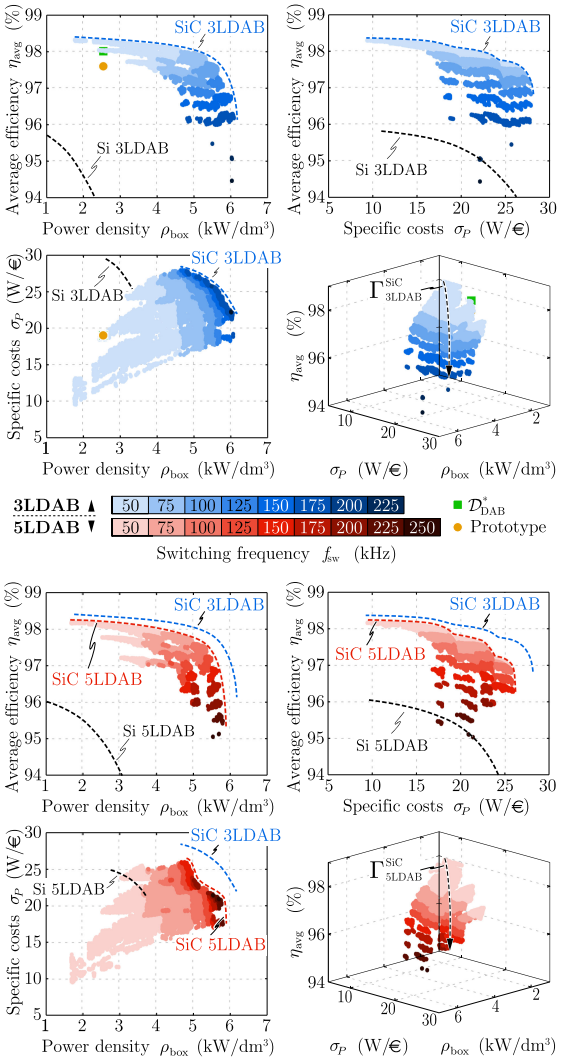

Fig. 14. η_{avg}–ρ_{box}–σ_P Pareto-optimal designs $\mathcal{D}_{DAB}$ of the Si and SiC 3LDAB and 5LDAB concepts found by the optimization routine depicted in Fig. 12. The distinct clusters that form the SiC Pareto fronts are a result of the three considered values for the total semiconductor costs $\Sigma_{SC,tot}$.

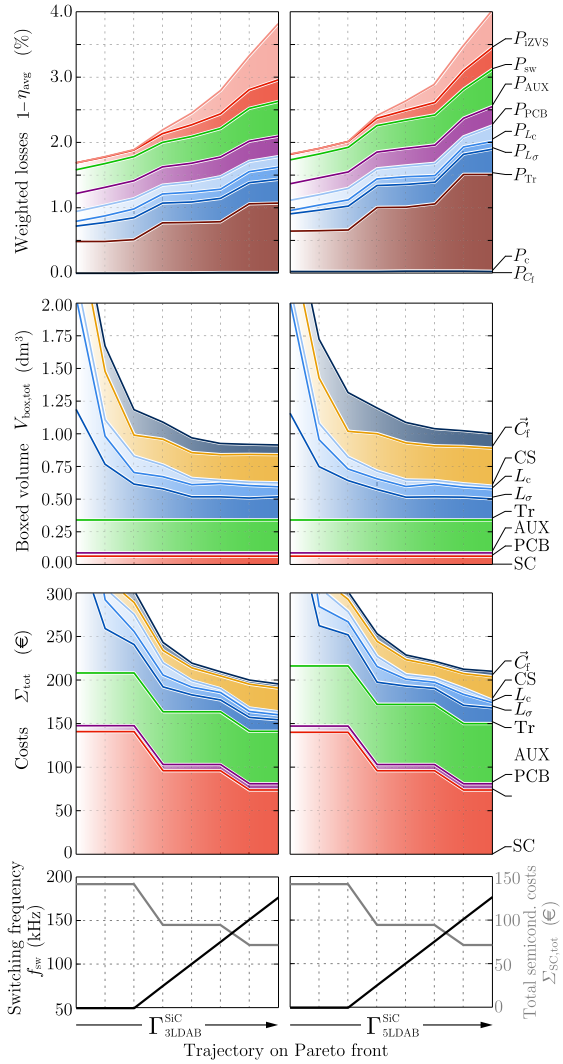

Fig. 15. Component loss, volume, and cost breakdown of the designs forming the trajectories Γ^{SiC}_{3LDAB} and Γ^{SiC}_{5LDAB} on the SiC 3LDAB and SiC 5LDAB Pareto fronts shown in Fig. 14. The trajectories are defined so as to attain an identical evolution of the global variables (f_{sw} and Σ_{SC}).

of low-cost IGBTs, only marginally higher specific costs can be achieved (at very low efficiencies below 94 %). The main reasons for the clear superiority of SiC MOSFETs in this application are their ohmic output characteristics and the absence of stored charge in the conducting device. The former allows for considerably lower conduction losses in part-load operation than the in-built forward voltage drop of the bipolar IGBTs. The latter enables very low ZVS losses, whereas the tail current effect due to the internally stored charge prohibits low-loss ZVS with Si IGBTs [50]. The higher semiconductor losses and thus lower permissible switching frequencies entail a larger and more expensive cooling system and passives, which largely compensate the cost advantage of the Si IGBTs.

The second main finding of Fig. 14 is derived from the comparison of the SiC MOSFET-based concepts. The corresponding Pareto fronts reveal that the SiC 3LDAB is fundamentally superior and dominates the SiC 5LDAB regarding all considered performance criteria. The identification of the underlying reasons is demanding as it requires a comparative analysis of the very large number of SiC 3LDAB and SiC 5LDAB designs, which form the Pareto fronts. In order to facilitate the discussion of this analysis which is presented below, the component loss, volume, and cost shares of selected 3LDAB and 5LDAB designs are shown in Fig. 15. The connection of these designs forms the trajectories Γ^{SiC}_{3LDAB} and Γ^{SiC}_{5LDAB} on the respective Pareto fronts depicted in Fig. 14. The 3LDAB and 5LDAB designs are chosen so that the associated global design variables f_{sw} and $\Sigma_{SC,tot}$ (i.e., the most influential variables) evolve identically along the formed trajectories (cf., Fig. 15), thereby significantly enhancing the comparability.

1) Losses: Inspection of the Pareto fronts and in particular the selected designs in Fig. 15 identifies the higher average conduction losses to be the main reason for the lower 5LDAB efficiency. Most remarkably, higher conduction losses result despite the advantage of lower rms currents featured by the 5LDAB (cf., Fig. 3(b)). This finding can mainly be explained by the higher number of switches in the primary-side bridge legs of the 5LDAB, which yields a lower chip area utilization. This

inherent disadvantage is pronounced enough to overcompensate the advantage of enabling lower rms currents.

2) Volume: Fig. 15 shows that the 5LDAB designs generally feature a lower power density, which is mainly due to the larger capacitor and cooling system volume. The larger capacitor is caused by the requirement of balancing the midpoint potential of the primary filter capacitor C_{f1}, which is not necessary in the 3LDAB. The larger 5LDAB cooling system is partly due to the higher conduction losses, the higher asymmetry of these losses and partly due to the higher number of semiconductor packages (which require a larger area on the heat sink). The total volume of the magnetics of both concepts is comparable, which is mostly because of very similar worst-case operating point conditions.

3) Costs: The comparison of the 3LDAB and 5LDAB designs that feature equal semiconductor costs reveals that the 5LDAB exhibits higher total costs due to the higher number of gate driver units, the larger capacitor and the more expensive cooling system (cf., Fig. 15).

4) Best Converter Concept: The analysis in this section identifies the SiC MOSFET-based 3LDAB to be the overall most suitable concept for the given dc/dc microgrid application. It concurrently achieves a higher efficiency, power density, and lower or similar costs than the other concepts. The superiority of the SiC 3LDAB concept is further emphasized by the fact that the underlying 3LDAB modulation scheme is considerably simpler than the 5LDAB scheme. In addition, the 3LDAB is likely to offer a higher reliability due to the lower component count. Note that the superiority of the SiC 3LDAB over the SiC 5LDAB is invariant with respect to the constraints in Table V as these constraints do have an impact on the absolute achievable performance but do not fundamentally modify the relative differences between the achievable SiC 3LDAB and SiC 5LDAB performance. Finally, the analysis proves that a high converter performance is achievable despite the high required functionality. Most notably, the proposed combination of a 3LDAB, SiC MOSFETs, and an optimized modulation scheme that facilitates minimized rms currents and complete ZVS in a wide operating range achieves considerably higher efficiencies than previously seen in literature. Whereas a large fraction of the SiC 3LDAB designs in Fig. 14 and the hardware prototype presented in Section III-D achieve peak efficiencies between 98.5 % and 99 %, peak efficiencies between 90 % and 97.1 % are reported for the uni- and bidirectional wide voltage range systems in [8]–[18].

B. Impact of Parasitic Capacitances

Inspection of the component loss shares in Fig. 15 reveals the severe impact of the parasitic capacitances in HF operation. Whereas complete ZVS is achieved for $f_{\mathrm{sw}} = f_{\mathrm{sw}}^{*} = 50\,\mathrm{kHz}$ as targeted by the design approach, the incomplete ZVS losses P_{iZVS} grow rapidly for increasing switching frequencies. The main reasons are the frequency-invariant reactive currents and the shortening of the maximum permissible dead times, which amount to less available charge for the charging/discharging of the parasitic capacitances. Note that increasing the reactive currents proportional to the switching frequency results in rapidly increasing additional conduction losses and does thus not represent an attractive countermeasure. It can, therefore, be concluded that low parasitic capacitances are a key requirement for efficient HF operation. On the one hand, low specific output capacitances as applicable for SiC MOSFETs are desirable (cf., Table III). On the other hand, a careful design of the converter layout is essential to reduce the additional parasitic layout capacitance $C_{\mathrm{par,tot}}$ (cf., Fig. 5(a)), which may easily be in the range of the output capacitances of SiC MOSFETs. In this context, the investigations of this work reveal the deficits of the standard packages (such as the employed TO-247), in which many commercial SiC semiconductors are provided: these packages form significant undesired parasitic capacitances to the heat sink (tens of picofarads, depending on the insulation layer). In the case of the prototype in this work, the packages contribute between 25 % and 50 % to $C_{\mathrm{par,tot}}$ (depending on the bridge leg) and hence pose a limiting factor for ZVS.

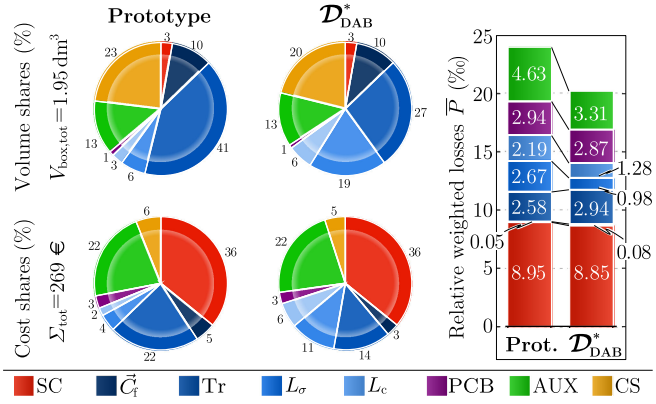

Fig. 16. Comparison of the existing SiC 3LDAB hardware prototype to the theoretical Pareto-optimal converter $\mathcal{D}^{*}_{\mathrm{DAB}}$ depicted in Fig. 14. The designs feature equal costs and volumes, whereas the prototype's weighted efficiency could be increased by more than 0.3 %.

C. Comparison to Existing Hardware Prototype

The existing prototype introduced in Section III-D employs the same modulation scheme as considered in this work and was designed for similar constraints as shown in Table V. Therefore, the existing prototype can directly be compared to the calculated Pareto-optimal SiC 3LDAB designs as depicted in Fig. 14. Inspection of Fig. 14 leads to the conclusion that the calculated Pareto fronts can be trusted with high confidence as they are in close vicinity of the prototype (cf., Fig. 14) and rely on the same modeling framework that accurately predicts the prototype losses (cf., Section III-D). In a second step, it is therefore analyzed how the prototype could be improved in order to be located on the Pareto front. For this purpose, the prototype is compared to the marked Pareto-optimal design $\mathcal{D}^{*}_{\mathrm{DAB}}$ in Fig. 14, which features an equal total component volume and equal costs. A difference in the average efficiency of more than 0.3 % can be observed. The analysis summarized in Fig. 16 shows the differences between the prototype and the Pareto-optimal design $\mathcal{D}^{*}_{\mathrm{DAB}}$. It reveals a selection of too powerful fans for the prototype, which significantly decreases the low-load efficiency due to higher constant fan losses (included in P_{AUX}). The chip area distribution of the prototype (cf., Table IV) is very close to the

theoretical optimum (based on variable chip sizes) of Table VI. Thus, only marginally higher semiconductor losses result for the prototype. Eventually, the analysis finds a nonoptimal volume distribution between the magnetics of the prototype leading to increased losses in these components when compared to $\mathcal{D}^{*}_{\mathrm{DAB}}$. Besides a substantial efficiency improvement of 0.3 % within the given volume, the prototype could also significantly be reduced regarding volume and costs. As evident from Fig. 14, for the same efficiency, the power density could be doubled while reducing the costs by approximately 25 %.

VI. Conclusion

This work presents a comprehensive cost-aware comparison of isolated bidirectional DAB concepts in a 5-kW 100–700-V input voltage range dc microgrid application. A conventional 3LDAB is compared to an advanced 5LDAB topology considering either Si IGBTs or SiC MOSFETs. For this purpose, a multiobjective optimization scheme is proposed, which concurrently optimizes the converter concepts regarding efficiency, power density, and the costs. The optimization scheme employs an advanced modeling framework, which was experimentally verified using a hardware prototype. The observed very good loss (mean deviation: 2.5 %) thermal and waveform modeling accuracy imply that the optimizations can be trusted with high confidence. The calculated Pareto fronts reveal the superiority of SiC MOSFETs in the considered application: SiC enables higher efficiencies and power densities and, at the same time, achieves similar costs on the system level as Si IGBTs. The comparison of the optimized SiC MOSFET-based 3LDAB and 5LDAB concepts shows a fundamental superiority of the conventional 3LDAB regarding all considered performance criteria: the SiC 3LDAB achieves a higher efficiency (better chip area utilization), lower volumes (smaller capacitors as no midpoint balancing), and lower costs (fewer gate drivers) and, at the same time, features a lower component count and a simpler modulation scheme. The fact that the 5LDAB concept that at first glance seems to be more promising (due to lower achievable rms currents) than the conventional 3LDAB is found to be fundamentally inferior emphasizes the value of the proposed comprehensive benchmarking approach. Finally, the calculations and the presented SiC 3LDAB hardware prototype prove that despite the galvanic isolation and wide voltage range efficiencies above 98 % in a wide operating range are possible, which was previously not seen in literature.

The analysis shows that the higher complexity of the 5LDAB cannot be justified for the given application in this work. However, the 5LDAB may still have a potential in other applications. These may include applications with an even wider voltage range and/or applications with a high efficiency weighting of operating points in the high-voltage regime and/or medium-voltage applications. For the latter, similar 5LDAB topologies were proposed in the literature [51]–[53] to eliminate the device dynamic and static voltage sharing problem of otherwise cascaded semiconductors. With regard to alternative applications, it is again proposed to employ the benchmark approach of this paper in order to obtain a comprehensive and quantitative decision base regarding the selection of the 3LDAB or 5LDAB.

References

[1] J. A. Ferreira and H. W. van der Broeck, "Alternative power distribution in residential and commercial buildings," in *Proc. 5th Eur. Conf. Power Electron. Appl.*, Sep. 1993, vol. 7, pp. 188–193.

[2] A. Sannino, G. Postiglione, and M. H. J. Bollen, "Feasibility of a DC network for commercial facilities," *IEEE Trans. Ind. Appl.*, vol. 39, no. 5, pp. 1499–1507, Sep./Oct. 2003.

[3] M. Elshaer, A. Mohamed, and O. A. Mohammed, "Integration of sustainable energy sources into DC zonal electric distribution systems," in *Proc. IEEE Power Energy Soc. Gen. Meeting*, Jul. 2011, pp. 1–7.

[4] J. Maneiro and F. Hassan, "A flexible modular multi-level converter for DC microgrids with EV charging stations," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2013, pp. 1316–1320.

[5] D. Dong, I. Cvetkovic, D. Boroyevich, W. Zhang, R. Wang, and P. Mattavelli, "Grid-interface bidirectional converter for residential DC distribution systems—Part One: High-density two-stage topology," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1655–1666, Apr. 2013.

[6] Emmerson Network Power. DC Power. 2016. [Online]. Available: http://www.emersonnetworkpower.com/en-US/Products/DCPower/

[7] REbus Alliance. DC Microgrid. 2016. [Online]. Available: http://rebuspower.com/

[8] X. Wu, W. Lu, J. Zhang, and Z. Qian, "Extra wide input voltage range and high efficiency DC-DC converter using hybrid modulation," in *Proc. 41st IEEE Ind. Appl. Conf. IAS Annu. Meet. Conf. Record*, Oct. 2006, vol. 2, pp. 588–594.

[9] P. Sun, L. Zhou, and K. M. Smedley, "A Reconfigurable structure DC-DC converter with wide output range and constant peak power," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2925–2935, Oct. 2011.

[10] R. Li, M.-F. Vancu, F. Canales, and D. Aggeler, "High performance DC-DC converter for wide voltage range operation," in *Proc. 7th Int. Power Electron. Motion Control Conf.*, vol. 2, Jun. 2012, pp. 1151–1158.

[11] F. Musavi, M. Craciun, D. Gautam, and W. Eberle, "Control strategies for wide output voltage range LLC resonant DC-DC converters in battery chargers," *IEEE Trans. Veh. Technol.*, vol. 63, no. 3, pp. 1117–1125, Mar. 2014.

[12] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J. W. Kolar, "Charge-based ZVS soft switching analysis of a single-stage dual active bridge AC-DC converter," in *Proc. Energy Convers. Congr. Expo.*, Sep. 2013, pp. 4820–4829.

[13] T. Todorcćević, P. Bauer, J. Ferreira, and R. van Kessel, "A modulation strategy for wide voltage output in DAB based DC-DC modular multilevel converter," in *Proc. 40th Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2014, pp. 4514–4520.

[14] M. Kim, M. Rosekeit, S.-K. Sul, and R. W. A. A. De Doncker, "A dual-phase-shift control strategy for dual-active-bridge DC-DC Converter in wide voltage range," in *Proc. IEEE 8th Int. Conf. Power Electron. ECCE Asia*, May 2011, pp. 364–371.

[15] F. Krismer and J. W. Kolar, "Closed form solution for minimum conduction loss modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 174–188, Jan. 2012.

[16] Z. Wang and H. Li, "A soft switching three-phase current-fed bidirectional DC-DC converter with high efficiency over a wide input voltage range," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 669–684, Feb. 2012.

[17] H. van Hoek, M. Neubert, and R. W. A. A. De Doncker, "Enhanced modulation strategy for a three-phase dual active bridge—Boosting efficiency of an electric vehicle converter," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5499–5507, Dec. 2013.

[18] X. Sun, Y. Shen, W. Li, B. Wang, L. Wang, and X. Li, "Center-tapped transformer based bidirectional DC-DC converter with wide input voltage range," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2015, pp. 5910–5917.

[19] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Jan./Feb. 1991.

[20] P. A. M. Bezerra, F. Krismer, R. M. Burkart, and J. W. Kolar, "Bidirectional Isolated non-resonant DAB DC-DC converter for ultra-wide input voltage range applications," in *Proc. Int. Power Electron. Appl. Conf. Expo.*, Nov. 2014, pp. 1038–1044.

[21] K. Kurohane, T. Senjyu, A. Yona, N. Urasaki, T. Goya, and T. Funabashi, "A hybrid smart AC/DC power system," *IEEE Trans. Smart Grid*, vol. 1, no. 2, pp. 199–204, Sep. 2010.

[22] D. Boroyevich, I. Cvetkovic, D. Dong, R. Burgos, F. Wang, and F. C. Y. Lee, "Future electronic power distribution systems—A contemplative view," in *Proc. 12th Int. Conf. Optim. Elect. Electron. Equipment*, May 2010, pp. 1369–1380.

[23] O. Deblecker, C. Versèle, Z. De Greve, and J. Lobry, "Multiobjective optimization of a power supply for space application using a flexible CAD tool," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Sep. 2013, pp. 1–10.
[24] M. Kasper, D. Bortis, and J. W. Kolar, "Classification and comparative evaluation of PV panel-integrated DC-DC converter concepts," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2511–2526, May 2014.
[25] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," *IEEE. Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, Feb. 2014.
[26] H. Uemura, F. Krismer, Y. Okuma, and J. W. Kolar, "η-ρ Pareto optimization of 3-phase 3-level T-type AC-DC-AC converter comprising Si and SiC hybrid power stage," in *Proc. Int. Power Electron. Conf.*, May 2014, pp. 2834–2841.
[27] C. Versèle, O. Deblecker, and J. Lobry, "Multiobjective optimal choice and design of isolated DC-DC power converters," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, Aug. 2011, pp. 1–10.
[28] M. Mirjafari and R. S. Balog, "Multi-objective design optimization of renewable energy system inverters using a descriptive language for the components," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2011, pp. 1838–1845.
[29] J. W. Kolar *et al.*, "Conceptualization and multiobjective optimization of the electric system of an airborne wind turbine," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 2, pp. 73–103, Jun. 2013.
[30] O. Deblecker, Z. De Greve, and C. Versèle, "Evaluation of power loss and mass gains of SiC versus Si-based switch-mode power supplies using a multiobjective optimization CAD Tool," in *Proc. Int. Symp. Power Electron., Elect. Drives, Autom. Motion*, Jun. 2014, pp. 43–49.
[31] C. Gammeter, F. Krismer, and J. W. Kolar, "Comprehensive conceptualization, design, and experimental verification of a weight-optimized All-SiC 2 kV/700 V DAB for an airborne wind turbine," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 638–656, Jun. 2016.
[32] J. Pinne, A. Gruber, K. Rigbers, E. Sawadski, and T. Napierala, "Optimization and comparison of two three-phase inverter topologies using analytic behavioural and loss models," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sept. 2012, pp. 4396–4403.
[33] H. Mejbri, K. Ammous, and S. Abid, "Bi-objective sizing optimization of power converter using genetic algorithms: application to photovoltaic systems," *COMPEL*, vol. 33, no. 1, pp. 398–422, 2014.
[34] T. Diekhans and R. W. De Doncker, "A pareto-based comparison of power electronic topologies for inductive power transfer," in *Proc. Electron., Intell. Motion, Renewable Energy Energy Manage.*, May 2015, pp. 1–9.
[35] G. Adinolfi, G. Graditi, P. Siano, and A. Piccolo, "Multiobjective optimal design of photovoltaic synchronous boost converters assessing efficiency, reliability, and cost savings," *IEEE Trans. Ind. Informat.*, vol. 11, no. 5, pp. 1038–1048, Oct. 2015.
[36] M. Mirjafari, S. Harb, and R. S. Balog, "Multiobjective optimization and topology selection for a module-integrated inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4219–4231, Aug. 2015.
[37] R. A. Friedemann, F. Krismer, and J. W. Kolar, "Design of a minimum weight dual active bridge converter for an airborne wind turbine system," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 509–516.
[38] R. M. Burkart and J. W. Kolar, "Component cost models for multi-objective optimizations of switched-mode power converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp. 2139–2146.
[39] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York, NY, USA: Springer, 2008.
[40] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. W. De Doncker, *Semiconductor Power Devices*. Berlin, Germany: Springer, 2011.
[41] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.
[42] F. Krismer, "Modeling and optimization of bidirectional dual active bridge DCDC converter topologies," Ph.D. dissertation, ETH Zurich, Zürich, Switzerland, 2010.
[43] N. H. Baars, J. Everts, H. Huisman, J. L. Duarte, and E. A. Lomonova, "A 80-kW isolated DC-DC converter for railway applications," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6639–6647, Dec. 2015.
[44] L. Jiang and D. Costinett, "A triple active bridge DC-DC converter capable of achieving full-range ZVS," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2016, pp. 872–879.
[45] M. Mu, "High frequency magnetic core loss study," Ph.D. dissertation, Virginia Polytech. Inst. State Univ., Blacksburg, VA, USA, 2013.
[46] C. Gammeter, F. Krismer, and J. W. Kolar, "Weight optimization of a cooling system composed of fan and extruded-fin heat sink," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 509–520, Jan./Feb. 2015.
[47] R. M. Burkart, H. Uemura, and J. W. Kolar, "Optimal Inductor design for 3-phase voltage-source PWM Converters considering different magnetic materials and a wide switching frequency range," in *Proc. Int. Power Electron. Conf.*, May 2014, pp. 891–898.
[48] J. Mühlethaler, "Modeling and multi-objective optimization of inductive power components," Ph.D. dissertation, ETH Zurich, Zürich, Switzerland, 2012.
[49] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstübner, "Performance trends and limitations of power electronic systems," in *Proc. 6th Int. Conf. Integr. Power Electron. Syst.*, Mar. 2010, pp. 1 –20.
[50] G. Ortiz, H. Uemura, D. Bortis, J. W. Kolar, and O. Apeldoorn, "Modeling of soft-switching losses of IGBTs in high-power high-efficiency dual-active-bridge DC/DC converters," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 587–597, Feb. 2013.
[51] A. K. Tripathi, K. Hatua, H. Mirzaee, and S. Bhattacharya, "A three-phase three winding topology for dual active bridge and its D-Q mode control," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2012, pp. 1368–1372.
[52] M. A. Moonem and H. Krishnaswami, "Analysis and control of multi-level dual active bridge DC-DC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2012, pp. 1556–1561.
[53] A. Filba-Martinez, S. Busquets-Monge, and J. Bordonau, "Modulation and capacitor voltage balancing control of a three-level NPC dual-active-bridge DC-DC converter," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2013, pp. 6251–6256.

Ralph M. Burkart (S'11) received the M.Sc. degree (with distinction) in electrical engineering and information technology from ETH Zurich, Zürich, Switzerland, in 2011, and the Ph.D. degree from the Power Electronic Systems Laboratory, ETH Zurich, in 2016.

The focus of his research is on developing multiobjective optimization techniques and advanced modeling frameworks for comparative benchmarking of power electronic converter systems. In particular, his research deals with cost-aware investigations of the system-level potential of SiC semiconductors in renewable energy systems.

Johann W. Kolar (F'10) received the M.Sc. and Ph.D. degrees (*summa cum laude/promotio sub auspiciis praesidentis rei publicae*) in industrial electronics and control engineering from the University of Technology Vienna, Vienna, Austria, in 1997 and 1999, respectively.

Since 1984, he has been working as an independent researcher and international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics, and high-performance drives. He has proposed numerous novel pulse width modulation converter topologies, and modulation and control concepts and has supervised more than 60 Ph.D. students. He has published more than 650 scientific papers in international journals and conference proceedings, three book chapters, and has filed more than 120 patents. The focus of his current research is on ultracompact and ultraefficient SiC and GaN converter systems, wireless power transfer, solid-state transformers, power supplies on chip, and ultrahigh speed and bearingless motors.

Dr. Kolar has received 23 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Middlebrook Award, and the ETH Zurich Golden Owl Award for excellence in teaching. He initiated and/or is the founder of four ETH Spin-off companies. He is a member of the Steering Committees of several leading international conferences in the field. From 2001 to 2013, he was as an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS. Since 2002, he has been an Associate Editor of the *Journal of Power Electronics* of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the *IEEJ Transactions on Electrical and Electronic Engineering*.