# A Three-Phase Multioptimal PWM Implemented on 2-Gbit Flash Memory Integrated Circuits

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***Abstract*—This paper further develops the concept of very large size flash-memory-based pulsewidth-modulated (PWM) algorithms for three-phase inverters. Such algorithms differ from the conventional counter-based implementation, and they follow a preprogrammed optimal PWM pattern that is read from a very large size memory with magnitude and phase as coordinates. Any sequence of states is thus possible within a PWM sampling interval. A novel digital structure has been built around the newly released flash memory integrated circuits. The paper demonstrates the feasibility of operation at any PWM sampling frequency up to 20 kHz when using gigabit-size flash memory integrated circuits along any low-cost microcontroller with an SPI peripheral. To empower the concept, a multioptimal PWM has been proposed and implemented on a 2-Gbit memory table. The harmonics of the phase currents are reduced by more than 40% while a constant PWM sampling frequency is maintained in order to comply with the conventional vector control methods for grid or motor applications.**

***Index Terms*—Flash memories, microcontrollers, optimization, power conversion harmonics, pulse width modulation converters, space vector pulse width modulation, three-phase electric power.**

## I. Introduction

FOR a fraction of the cost of complex microcontrollers, gigabit-size memories can implement detailed control laws otherwise impossible to set up on conventional microcontrollers or advanced DSP devices. The cost of flash memory has reduced to as low as ∼$0.35/GB in 2015, with a prediction to go under $0.10/GB by 2020 [1]. Flash memories were first packaged as SD cards or USB flash memory sticks for simple use for computer system file archive in early 2000s. After 2013, large-size flash memory integrated circuits in the gigabit range become offered on the end market for microcontroller expansion.

Following previous research [2]–[5], this paper is capitalizing from the development of flash memory technology with the implementation of multioptimal pulsewidth-modulated (PWM) algorithms on this new hardware support. Various optimal PWM algorithms have been reported in the 1990s but could not be easily implemented in low cost because of their calculation complexity. However, this research demonstrates that today's flash memory support allows implementation of very advanced multiple optimization results at very low cost instead of expensive high-speed computer systems.

Only recently, benefits of using flash memory in PWM have been reported in [2], followed by implementation examples for a SD card [3] for inverters [4], [5]. These successful steps followed immediately after the evolution of the flash memory industry (see Fig. 1), and were using SD cards when other support was not yet available. These papers demonstrated the feasibility of using the massive memory of the SD cards to store multiple lookup tables with pre-programmed PWM state sequences [2]–[5]. Variable-frequency and nonlinear optimized PWM patterns become possible at low-cost that could not otherwise be achieved without expensive computer hardware. However, the implementation was proof of concept only and limited to 1.2 kHz switching frequency due to the specific limitations on communication protocols and digital structures.

Developments on the flash memory market finally makes practical the commercial implementation of PWM generators on flash memory. This paper moves the concept further and provides a solution making use of the recently released flash memory integrated circuits. The memory table was thus expanded from 8 MB (64 Mbit) [5] within the SD card to 256 MB (2 Gbit) within novel integrated circuits, and there is faster communication between the main microcontroller and the flash memory. This allows inverter operation up to 20 kHz PWM constant sampling frequency, making the possibility of flash PWM for industrial three phase inverters finally possible. This research now introduces the proper communication protocol and hardware needed to build such practical and low-cost inverters while implementing advanced PWM algorithms that would otherwise require separate, expensive computer hardware if conventional PWM vector control were implemented.

Specifically, large-size flash memory allows for the first time to merge multiple optimal PWM solutions on the same platform at a very low cost. The philosophy presented in the design process is to create different PWM patterns for different operating circumstances and then store them in the lookup tables. At times, conventional space vector (SV) PWM may be utilized. At other instances, a variable-frequency PWM may be implemented or even other nonlinear PWM patterns. The PWM patterns are designed off-line for the specific applications in mind, and then stored in the GB sized flash memories. This opens the design possibilities of having different PWM for light loads, heavy loads, failure modes, etc., all stored in the same

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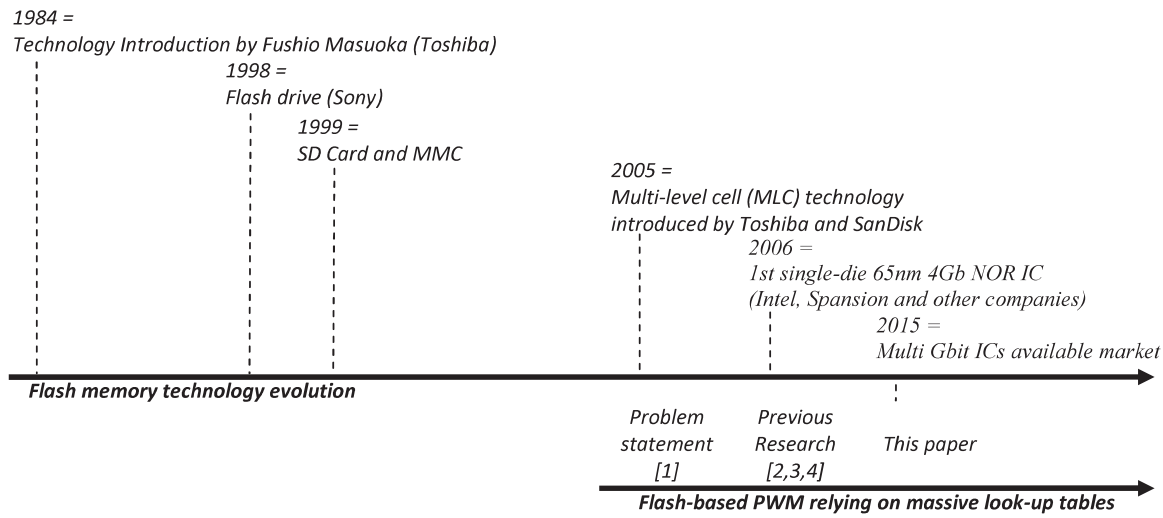



Fig. 1. Technology evolution for flash memory and flash-based PWM.

low-cost platform. This is virtually impossible on conventional processor-based implementation. While this paper presents a new specific type of merged multioptimal PWM algorithm, the methodology and implementation process described later can be followed to provide any types of PWM patterns. Thus, there is the possibility of exciting further research for deriving the best (low cost) implementation for any application specific PWM algorithms on the inexpensive proposed hardware platform using the design process.

The design process for PWM with flash memory is distinct from designing conventional SVPWM algorithms and must first be introduced:

1) first, the application specific industrial requirements should be specified;
2) then, the various PWM algorithms that are desired to be implemented should be selected, there may be multiple algorithms selected for implementation, depending on the various operating conditions;
3) after that, the memory integrated circuits (flash memory) should be selected and the hardware to interface the flash memory from the microcontroller is designed;
4) off-line tables of the PWM should be created, perhaps using MATLAB or another software, and it should be specialized to the format needs of the selected flash memory device;
5) the PWM lookup tables are programmed in the flash memory for its implementation. This design process is sketched in Fig. 2.

This paper also explains how to evaluate the performance of the flash memory PWM inverter system, which would be a vital step in the final design process.

The purpose of this research is to present a design methodology, communication protocol and digital hardware platform that will make it possible to utilize flash memory with low-cost microcontrollers to achieve optimized inverter performance that could not previously be achieved. The major contributions of the paper include:

1) A complete design procedure and flowchart for the implementation of three-phase PWM algorithms on flash memory devices, with applications to motor control and grid interfaces. The approach provides ability to combine different PWM methods on a very affordable platform (flash memory + cheap microcontroller) and could not be accomplished without the contribution of flash memories.
2) Design and explanation of proposed digital circuitry that can be used for the universal implementation of any PWM algorithm when using multi-gigabit memory integrated circuits. A specific experimental validation is presented that achieves PWM sampling frequency up to 20 kHz This represents the first time that the large-size flash-memory-based PWM becomes now a practical solution with impressive industrial potential.
3) Design and implementation of a simple communication protocol for flash memory integrated circuit interface from a low-cost microcontroller using SPI interface. This eliminates the bottleneck of needing to communicate with an SD card with a slow protocol intended for file transfers [6]. This reduces real-time expense and allows operation over the entire industrial range (up to 20 kHz PWM sampling).
4) As an experimental application for validation of the power of the flash based lookup table PWM design methodologies, an advanced new multioptimal PWM algorithm is using different PWM sequences on different sections of the voltage complex plane for current harmonics reduction. Using Gbit integrated circuit for implementation, the merged multioptimal PWM algorithm yields demonstration of results with 45% reduction in load current harmonics. The proposed optimal PWM represents a typical example for the powerful solution offered by flash memory implementation of various nonlinear laws at very low cost. This is a very important practical achievement with industrial applications.

## II. Definition of Digital Format

This section discusses details of the novel digital architecture proposed for usage of flash memory devices in control.

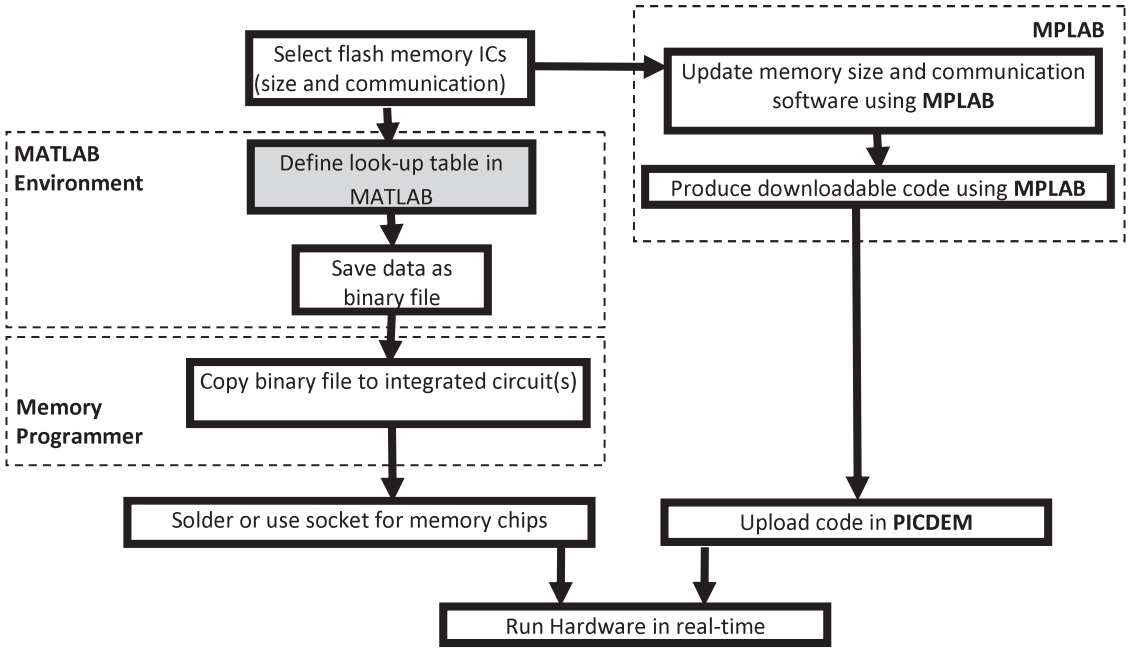



Fig. 2. Flowchart of the design process from memory selection to hardware run, shown when using MATLAB and MICROCHIP.

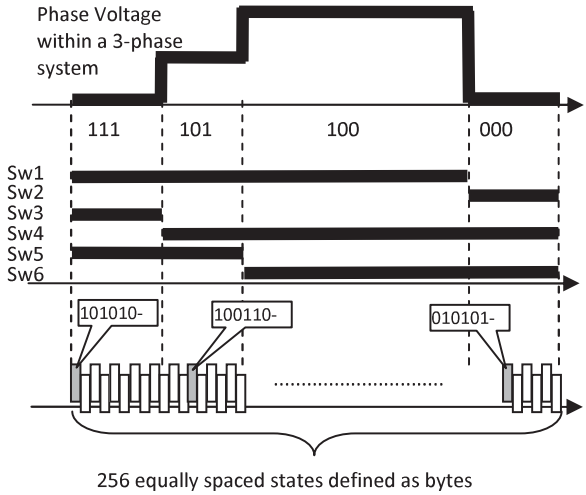



Fig. 3. Gate signals from the memory based PWM generator on a byte-stream organization.

The research novelty consists in byte-stream organization (six parallel lines Sw1–Sw6, clocked at a high frequency rate, Fig. 3) of the gate driver control pulses and the SPI-to-parallel communications protocol adopted in between microcontroller and flash memory.

### A. Principle

The previous research results reported for implementation of PWM algorithms on a very large size flash memory [2]–[5] have considered addressing the memory, as shown in Fig. 4(a). This was imposed by the limited communication bandwidth between the main microcontroller and the SD card. The consequence was a somewhat reduced resolution within the definition of the pulse-width in both vector position and pulsewidth resolution.

The current paper addresses the industry expectations of resolution and provides a major advancement by increasing the size of the memory table with a dedicated digital hardware able to use the addressing format from Fig. 4(b). Furthermore, such coordinates are updated through a combination of a counter and an SPI peripheral, at any frequency up to 20 kHz. All such arrangement was not possible with the previous solution involving the SD card due to different communication protocol and hardware setup, which limited the switching frequency to less than 2 kHz. Moreover, we are using this new hardware with a new and improved multioptimal PWM algorithm, which will be presented in Section IV-B.

The switching frequency is defined with the total count of a device's turn-on processes over a fundamental cycle. It is equal to the count of turn-off processes over a fundamental cycle. This is different from the sampling period used for setting up the control system and the periodic definition of the PWM cycle. In most PWM algorithms, the two are equal with each other. The frequency modulation method allows for a variable switching frequency over the fundamental cycle, while the average switching frequency over a cycle is constant and equals the control sampling frequency.

Since the count of switching processes stays the same with a generic center-aligned SV PWM, the switching loss is about the same, while HCF improved.

### B. Industry Requirements

While a new design for highest performance drive may make use of a 32-bit microcontroller with all peripherals defined with 32-bit data, we attempted to compare the flash memory PWM

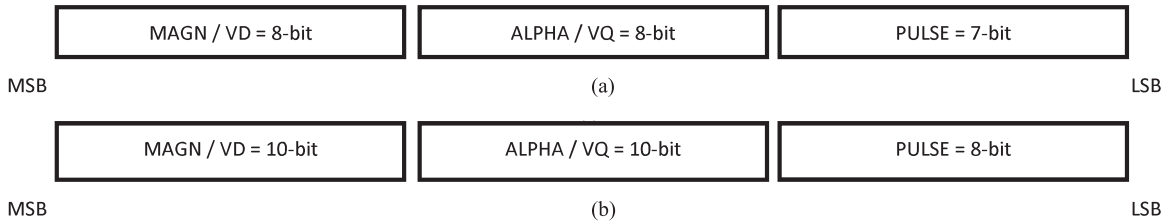



Fig. 4. Memory addressing format: (a) previous research (64 Mbit memory table); (b) current paper (2 Gbit memory table).

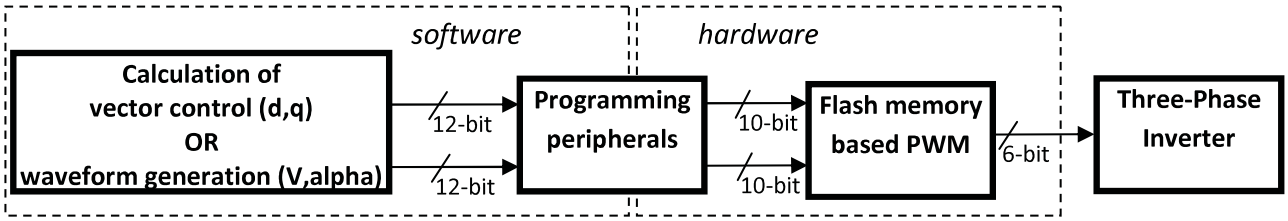



Fig. 5. Data flow arrangement and resolution implications.

implementation with a conventional low-cost drive, designed with anything in between 8-bit and 16-bit data. Hence, we have considered the calculation making available the vector coordinates on 12-bit while the actual memory table is built with 10-bit vector coordinates and the pulse resolution of 8 bit. This is because most A/D acquisition peripherals are working on 12 bit. These remarks yield onto the software arrangement shown in Fig. 5.

Obviously, the same principle can be easily expanded to a 32-bit data processing. This would result in 32-bit programming registers easily achieved with some FPGA structure. There is an infinite number of choices possible for the resolution of partial or final results depending on the actual digital hardware and industrial objectives.

Finally, let us mention the minimum pulse width as a limitation when implementing PWM. Power semiconductor devices have finite commutation times and the pulse width is usually limited to a minimum pulse width at least two times the sum of turn-on and turn-off times [6]. That is, the minimum implementable pulse width possible for an *N*-bit pulse structure is calculated as $(2^N f_s)^{-1}$, where $f_s$ is the switching frequency. This should be at least twice the turn-on and turn-off times of the power switches. For instance, the definition of the pulse structure on 8 bit, as shown in Fig. 4(b), provides a minimum pulse of 195 ns at 20 kHz (our actual 200 ns at 19.53 kHz) or 325 ns at 12 kHz. If these are not large enough, the MATLAB software used to generate the large-size lookup table [3], [4] (see Fig. 2) can be modified to avoid short pulses. This feature works similar to inclusion of the dead-time generator within the memory lookup, which was previously explained in [5]. We should mention here that our experimental setup has incorporated a dead-time generator within the smart power module.

For a general design procedure, the MATLAB definition of lookup table can include provisions for dead-time or minimum pulse width limitation along with the definition of the actual PWM algorithm (see Fig. 2).

### C. Generic Implementation With Discrete ICs

The new digital circuitry uses memory integrated circuits accessed with a 28-bit address bus for a 2 Gbit memory. It is illustrated with the drawing from Fig. 6. The uniqueness of this design provides a very fast access to the data stored in memory and the PWM byte stream can be extracted at 20 kHz.

In order to achieve this, an SPI-to-parallel converter has been included in design to benefit from the fastness of a parallel addressing, uniquely possible with these 2 Gbit devices. This is the most important research achievement of the paper, and it was not possible until the technology behind those particular integrated circuits [7]. Note that despite having the datasheet and engineering samples available since 2012, the actual Parallel NOR Flash ICs [7] of various capacities are commercially available at low-cost since 2014 and 2015.

## III. Flash Memory Circuits in 2015

Flash memory devices store information in an array of memory cells made of floating-gate transistors. The memory cell is similar to a standard MOSFET and it has two gates instead of one. The first is a control gate like any other MOS transistor, while a second floating gate is located between the control gate and the MOSFET channel and it is insulated all around by an oxide layer. Any electrons placed therein are trapped by the oxide layer and cannot be discharged for many years. When the floating gate holds a charge, it partially cancels the electric field from the control gate. More voltage needs to be applied to the control gate to make the MOSFET channel conduct and this can be seen as a change in the threshold voltage. A voltage in between the two possible threshold voltages is applied to the control gate in order to read the state of a cell. The current flow through the MOSFET channel is sensed as a test if the device is conducting or insulating. This forms a binary code, reproducing the stored data.

The way the floating-gate transistors are connected in respect to the control gate defines the NAND-type or the NOR-type flash

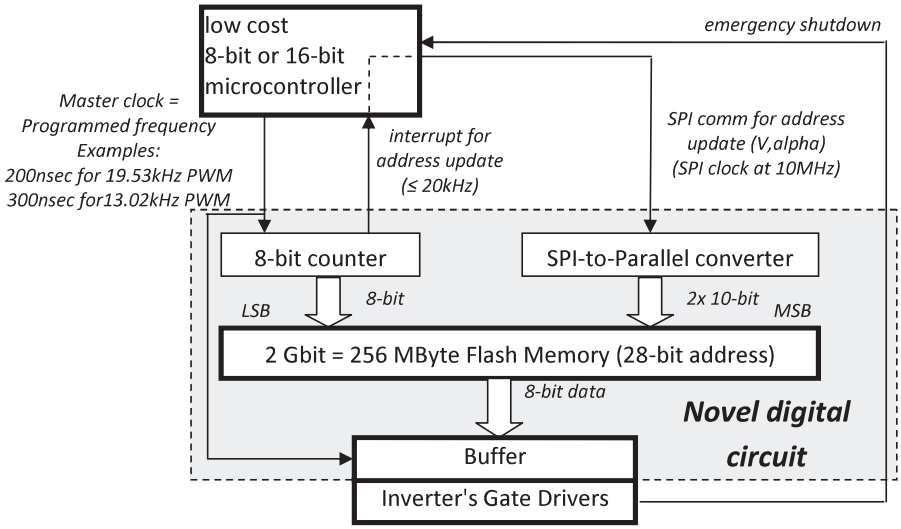



Fig. 6. Principle of PWM generator implemented with flash memory integrated circuits (see also Fig. 18 for the actual).

memory. The NAND type is the most-known flash memory, and it can be packaged as main SPI-accessed memory within digital ICs, memory cards (SD cards, MMC cards, SDXC, SDHC, Sony memory stick, and so on), USB flash drives, and solid-state drives. This was the support for our previous research work [3]–[5].

The NOR-type flash memory is used as a small random byte-to-byte local memory at machine code level in digital circuits like microcontrollers and DSP devices. Larger size parallel or SPI NOR-type flash memory are packaged as individual integrated circuit. This is the support of our current research work, and it is imposed by the common practice in microcontrollers.

At the time of this study, the most common flash memory integrated circuit at an affordable cost of less than $10 in single unit order is 2 Gbit (or 256 MByte). The most common architecture implies the use of communication on a limited 8-bit data bus, with a time-consuming sequence of 8-bit commands for definition of write/read operation and multibyte address. Various examples for this class of devices exist on the market.

Other architectures are featured within PC28F00 BM29EWHA (or JS28F00AM29EWHA with a different package) from Micron Technology or S29GL01GP11TFCR10-ND from Spansion, which allow direct access through a memory address bus of 28 bits (256 MB) when data are organized as bytes. This provides the fastest memory access from all 2-Gbit devices available on the market in 2015, with no requirement for prior knowledge of a special programming sequence of address and command. We built our experimental rig around this idea, with two integrated circuits of 1 Gbit each, using a conventional dual inline package. The addressing circuitry follows Fig. 6, and our memory setup features an 8-bit data organization: 6 bits correspond to gate driver command and 2 bits are unused.

## IV. Multioptimal PWM

This section presents details on the proposed innovative multioptimal PWM algorithm. The major research contribution consists in combining multiple already-reported individual optimal algorithms into a single implementation achieved with a large flash memory. This is very difficult to achieve with any other digital platform. While we limit the presentation to just a single example derived with reduction of current harmonics in mind, the same idea of flash-memory-based implementation can be used within a wider range of applications or for other optimization criteria. Other complex nonlinear solutions can be implemented with a massive lookup table at an extremely low cost.

### A. Space Vector Modulation

Pulse Width Modulation is the key component in the control of a three-phase power converter used for $\mathrm{dc/ac}$ or $\mathrm{ac/dc}$ conversion [8]–[10]. A version of PWM is called *space vector modulation* (SVM) and consists in generation of the control pulses based on a vectorial representation of the output voltage system. Any three-phase system can be represented uniquely with a vector in the complex plane. The trajectory of the tip of the vector corresponds to the desired time evolution of the output voltages. Such position (*Vs*) can be defined with a decomposition onto two neighboring vectors *(Va, Vb)* resulted from the inverter operation. The time intervals to be spent on each such fixed vector can be calculated with an averaging relationship

$$\begin{cases} \underline{V_S} \cdot T_S = \underline{V_a} \cdot t_a + \underline{V_b} \cdot t_b + \underline{V_0} \cdot t_0 \\ T_\mathrm{s} = t_a + t_b + t_0 \end{cases} \tag{1}$$

$$\begin{cases} t_a = \dfrac{3\,V_s}{2\,V_\mathrm{dc}} \cdot T_S \cdot \left(\cos\alpha - \dfrac{1}{\sqrt{3}}\sin\alpha\right) = \dfrac{\sqrt{3}\cdot V_s}{V_\mathrm{dc}} \cdot T_S \\ \qquad\qquad \cdot \sin\left[\dfrac{\pi}{3} - \alpha\right] \\ t_b = \dfrac{\sqrt{3}\cdot V_s}{V_\mathrm{dc}} \cdot T_S \cdot \sin\alpha \\ t_0 = T_S - t_a - t_b \end{cases} \tag{2}$$

where $V_a$ and $V_b$ are the vectors in the complex plane, each associated to an active state; $t_a$ and $t_b$ are the intervals allocated to each active state; $V_0$ is the zero voltage vector; $t_0$ is the sum of time intervals allocated to zero-state intervals; $\alpha$ is an angular coordinate of the desired voltage vector in the complex plane; $V_s$ is the magnitude of the desired voltage vector in the complex plane; $T_s$ is the sampling interval for the PWM generation; and $V_{\rm dc}$ the dc-bus voltage.

These formulas do not impose on the actual sequence of states (order of $V_a$, $V_b$, $V_o$) within the considered sampling interval. This is a degree of freedom generally used for optimization.

### B. Optimization Criteria

Numerous optimization problems have been formulated around the PWM algorithms. Any combination of PWM algorithms can be implemented with large size flash memory devices at a very low cost, using Figs. 3–6 and the methodology presented within this paper. This implementation option was never possible before the flash memories, and it is a major research contribution of this paper.

Among them, we will focus herein on the harmonics of the output phase current, defined for a hypothetical inductive load. Performance is assessed with the content in harmonics of the output current. In this respect, we consider the *harmonic current factor (HCF)* as figure of merit

$$\mathrm{HCF}(\%) = \frac{100}{V_{(1)}} \cdot \sqrt{\sum\nolimits_{n=5}^{\infty} \left[\frac{V_{(n)}}{n}\right]^2} \tag{3}$$

where $V_{(n)}$ are the voltage harmonics in the phase voltage. Results are reported in respect to the modulation index *m* that is defined with respect to the inverter's dc voltage $V_{\rm dc}$ and rms value of the desired reference *V*

$$m = \frac{V \cdot \sqrt{3}}{V_{\rm dc}}, m \in [0, 1]\,. \tag{4}$$

While our optimization targets the reduction of current harmonics as expressed with HCF, similar flash-memory-based approaches can consider directly either common-mode voltage, converter efficiency, motor losses, device utilization, or anything else.

Another important harmonic coefficient is *total harmonic distortion (THD)*, which is calculated as

$$\mathrm{THD}(\%) = \frac{100}{V_{(1)}} \cdot \sqrt{\sum\nolimits_{n=5}^{\infty} \left[V_{(n)}\right]^2}. \tag{5}$$

Finally, the linearity of the converter from modulation index reference to the actual rms value of the phase voltage is also of interest for controller stability.

Some important previous types of optimal methods for three-phase PWM inverters, which possibly can reduce the current harmonics, are as follows:

1) *Discontinuous PWM* (also called two-phase modulation, or flat-top modulation) algorithm that does not switch a power device over 60° in order to reduce the switching loss [10]–[13].
2) *Frequency modulation* suggests changing the PWM sampling interval with the angular coordinate so that more pulses are produced near the 60-degrees sector's bisector [14]–[16].
3) Optimization of the *pulse position* within the PWM sampling interval [17]–[20].

The previous work on flash-memory-based PWM [4], [5] has proposed a multioptimal PWM method taking advantage of the following:

1) a merged-pulse structure at high modulation indices allowing an innovative state sequence;
2) an emulation of the sinusoidal frequency modulation with a frequency change based on a square wave with a limited count of carrier (PWM sampling) frequencies across each 60° sector.

The optimization featured within this novel research work reduces current harmonics when expressed as HCF. Other contemporary research are addressing reduction of common-mode voltages [21] or filter/motor loss [22]. Furthermore, the novel digital architecture and communication protocol allows for a faster PWM up to 20 kHz on a low-cost platform. This is a very powerful novel research contribution of the paper.

Fig. 7 shows the usage of the optimal methods at different modulation indices along certain optimization parameters. A vectorial representation has been adopted for this presentation. The instantaneous values of a three-phase set of output voltages is equivalent to a vector in the complex plane. For a set of sinusoidal voltages, such vector would displace on a circular trajectory. The states of the inverter operation are explained in Fig. 7. The coded notations in Table I are showing the conduction states of the high-side devices. For instance, $\mathrm{V1} = 100$ means the high-side IGBT on the first phase is ON, the low-side IGBTs on the second and third phases are ON, while all the other three devices are OFF. This code representation is further used with Fig. 7 to illustrate the switching sequence on each constant PWM sampling interval, for each region of the complex plane.

Waveform symmetries within the complex plane representation allow us to optimize the PWM algorithm for a 60° sector only. Different PWM algorithms are used on different regions of such 60° sector. This behavior is further repeated on all six sectors of 60°.

The solution reported in Fig. 7(a) [3]–[5] divides the 60° sector in several regions, each using a different PWM approach.

The frequency modulation has been emulated with a square-wave variation of carrier frequency that means the usage of 1, 3, or 4 pulses over a constant PWM sampling period. The angular definition of the regions allocated for each PWM with 1, 3, or 4 pulses are calculated in MATLAB so that an average switching frequency over the entire fundamental cycle of two times the sampling PWM frequency yields, similar to any center-aligned PWM method. This optimization provided a definition of the angular regions with $\mathrm{stpa} \approx 4^\circ$ (defined as shown in Fig. 7).

A MATLAB-based comparison with the most conventional center-aligned SVM has shown, in [4] and [5], the advantage of the novel algorithm above a modulation index of $m = 0.833$, where *m* was defined with (4). This was reported in [4] and [5], and it is similar to our results shown later on Fig. 9.

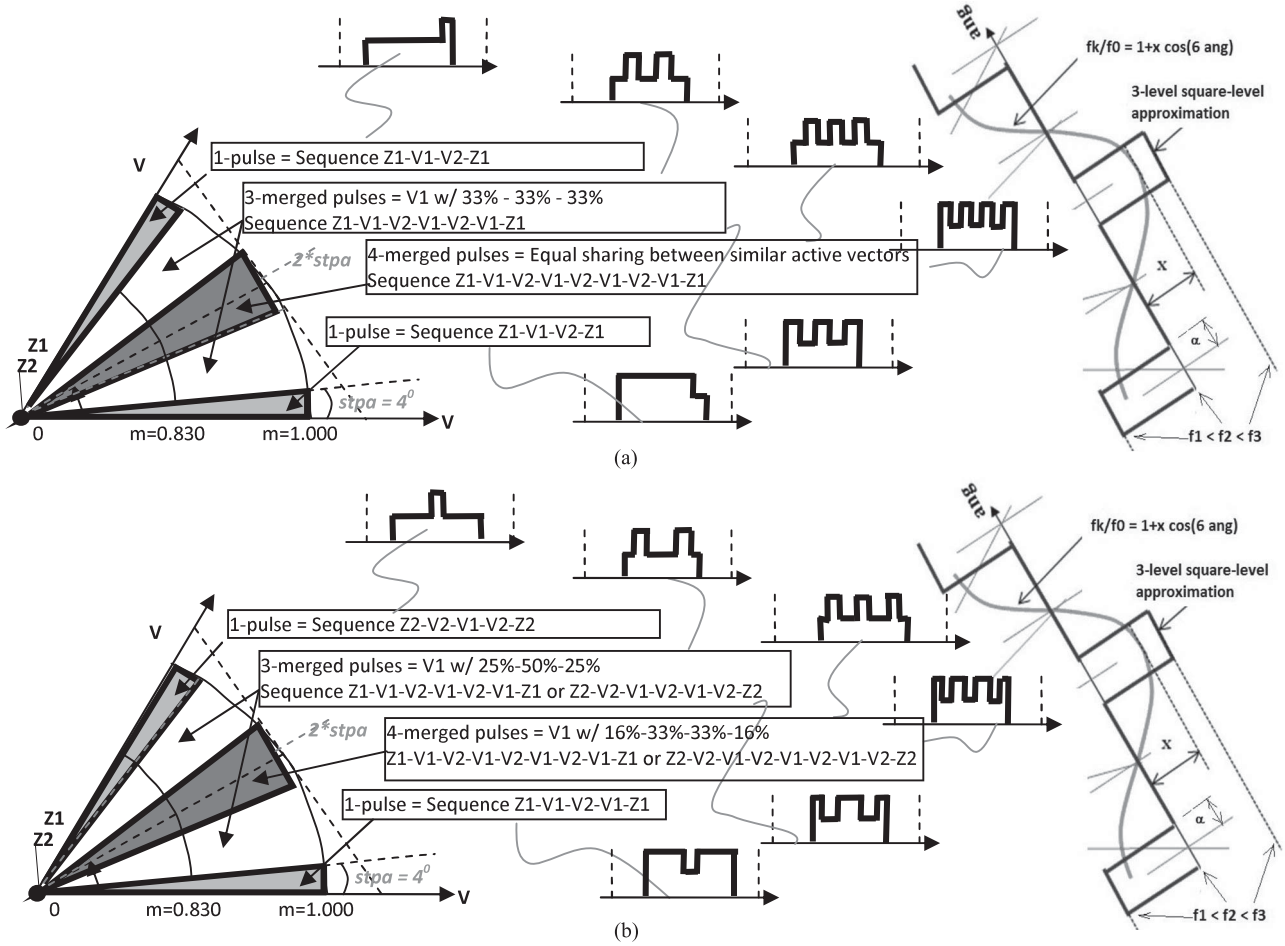



Fig. 7. Diagram of the methods used for memory table generation: (a) previous solution implemented on an SD card; (b) novel solution implemented on gigabit-size memory integrated circuits. "stpa $= 4^0$" and "*m*-threshold $= 0.83$" values optimized in [4] and [5]. Right-hand side shows the variation of carrier frequency according to the emulated frequency modulation

TABLE I
INVERTER STATE REPRESENTATION

| | |
|---|---|
| Z1 = 000 | V4 = 011 |
| V1 = 100 | V5 = 001 |
| V2 = 110 | V6 = 101 |
| V3 = 010 | Z2 = 111 |

The previous implementation with an SD card [3]–[5] has limited the PWM carrier/sampling frequency to around 1.2 kHz due to the required communication protocol of the card. This research, however, demonstrates breakthrough performance by utilizing 1 or 2 Gbit integrated circuits to form a 2-Gbit memory table with an 8-bit data organization that can be addressed through a 28-bit address bus. It also allows operation with a PWM sampling frequency of up to 20 kHz programmable within the controlling microcontroller. Any previous solution was not able to extract byte-stream data from a very large size memory of 2 Gbit (that is, 256 kB) at a rate of $256 \cdot 20$ kHz $= 5$ MHz with a conventional low-cost microcontroller. This is a major research contribution of this paper with a simple digital hardware for a novel architecture able to access the flash-memory at a high byte-stream rate, without the cumbersome communication protocol of a SD card. This achievement opens the door to implementation of multioptimal three-phase PWM compatible to industrial motor drive requirements.

This available transfer speed and size of the available memory allowed for some reconsideration and improvement of the previous method [4], [5]. The previous solution in Fig. 7(a) is further improved in Fig. 7(b). The *new multioptimal PWM* method proposed herein and also shown in Fig. 7(b) implements and demonstrates the following three innovative approaches not previously reported:

1) Changing the pulse resolution from 128 to 256 states improves the harmonic content, especially at low modulation indices where 7.5% HCF improvement at $\mathrm{m} = 0.1$ was observed by experiment and theoretically anticipated in [4] and [5].
2) An optimization of the distribution of time duration for each state during the so-called *Merged Pulse Technique* is performed now for additional HCF harmonic improvements of more than 5% at any high modulation indices above 0.8 when the sequence Z1-V1-V2-V1-V2-V1-Z1 has been implemented with a time distribution of


Fig. 8. Current (or flux) ripple shown in complex plane for (a) the previous single-ended SVM and (b) the novel state distribution (each trajectory direction corresponds to an active vector, V1 or V2 in example).

25%–50%–25% for the three states associated to V1 instead of the previous solution [4], [5] of 33%–33%–33% distribution [see Fig. 7(a) versus Fig. 7(b)].

3) A new state sequence (Z1-V1-V2-V1-Z1) is proposed in this paper for single-ended SVM pulses instead of the well-known Z1-V1-V2-Z2 sequence. This is possible since the two sequences have exactly the same number of commutation processes while the HCF harmonic content yields improved.

This can also be seen within the trajectory drawn in Fig. 8.

## V. MATLAB-Based Optimization and Analysis

According to Fig. 1, the most important step for the proposed technology consists in designing the content of the flash memory in MATLAB. The control process required for PWM generation is considered in MATLAB and the entire map of possible values for magnitude and phase is swept. The core of the multioptimal PWM design is a major research contribution of this paper showing how we can merge various optimal PWM algorithms within the same design.

### A. MATLAB Tools

The content of the actual flash memory is calculated in MATLAB with a special script. The same script is also used along a harmonic calculator for performance optimization. This allows the capability to analyze the harmonic performance of the digital signals intended to be sent to the gate drivers.

MATLAB after Version 6.0 uses an implementation of the FFT called *FFTW* "*Fastest Fourier Transform in the West [23].*". Comparative studies show performance is superior to publicly available FFT software, and it is even competitive with vendor-tuned codes (like in some hardware Spectral Analyzers). The harmonics are calculated herein with FFT from MATLAB for $262\ 144 = 2^{18}$ samples. This can mean one fundamental cycle of 4.7684 Hz resulted from (*256 states during a sampling interval)* $*$ *(1024 angular positions within table)* $* 4 *$ *(200 ns clock for PWM*). Other fundamental frequencies lead to a similar setup. All the available harmonics are used to calculate the HCF defined with (3).

The execution time for 262 144 real samples is less than a fraction of a second for a modern laptop. The acquired data are processed through a Blackman windowing routine. The Blackman window offers a weighting function similar to the Hanning but narrower in shape. Because of the narrow shape, the Blackman window is the best at reducing spectral leakage at the trade-off of spectral peak sharpness.

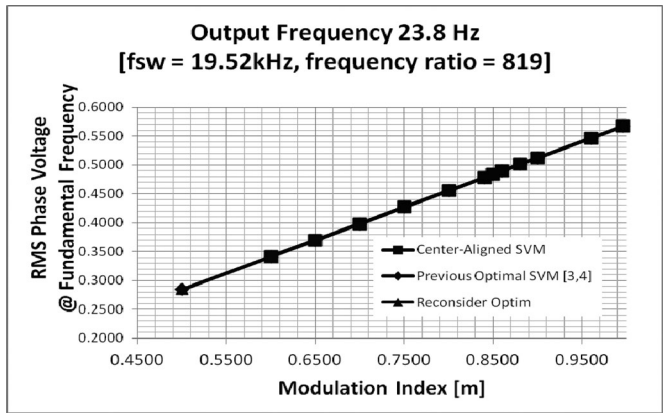



Fig. 9. Linearity of the magnitude of fundamental component for conventional center-aligned SVM, previous optimal SVM [3], [4] (adapted to 256-bit resolution), and improved optimal solution, all for a frequency ratio of 819. (As expected, we get quasi-identical results, which facilitate transition from one method to another at any modulation index.)

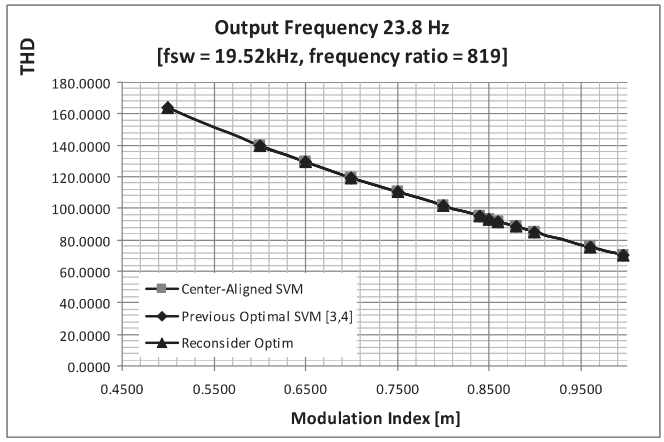



Fig. 10. THD for a conventional center-aligned SVM, previous optimal SVM [3], [4] (adapted to 256-bit resolution), and improved optimal solution, all for a frequency ratio of 819. (As expected, we get quasi-identical results.)

### B. Analysis of Experimental Results

A complete sweep of evaluation for the *new multioptimal PWM*—now implemented on the digital platform allowing PWM sampling frequencies up to 20 kHz (our actual 19.53 kHz)—is shown in Figs. 9–12 for a fundamental frequency of 23.8419 Hz.

For a comparison of results, we have considered three methods: center-aligned SVM implemented on the 2-Gbit flash memory; previous multioptimal solution from [5]; the novel multioptimal PWM algorithm described in Section IV-B.

Fig. 9 shows the inverter linearity for all three PWM methods as well as the actual relationship between the modulation index and the actual rms phase voltage. Fig. 10 illustrates the evolution of the voltage harmonics expressed as THD. Figs. 9 and 10 illustrate the overall content in voltage harmonics is similar for any PWM using the same parameters. Fig. 11 shows the actual HCF after considering multiple operation modes through a series of thresholds previously illustrated in Fig. 7. All Figs. 9–12 prove the feasibility of the *new multioptimal PWM* and the performance improvement in terms of HCF when compared with

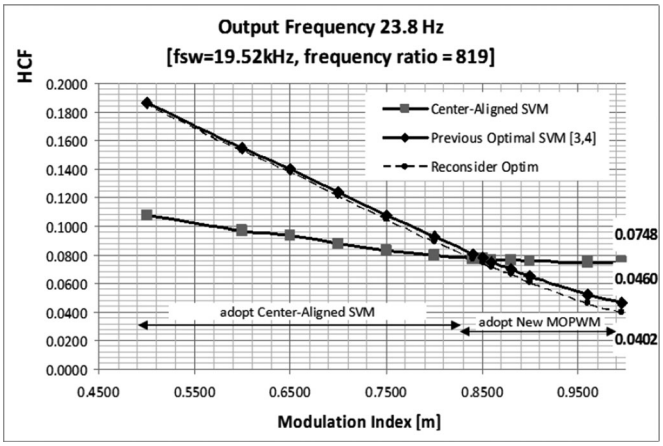



Fig. 11. HCF for a conventional center-aligned SVM, previous optimal SVM [3], [4] (adapted to 256-bit resolution), and improved optimal solution, all for a frequency ratio of 819. At any modulation index, the method with the lower HCF can be adopted for memory implementation.

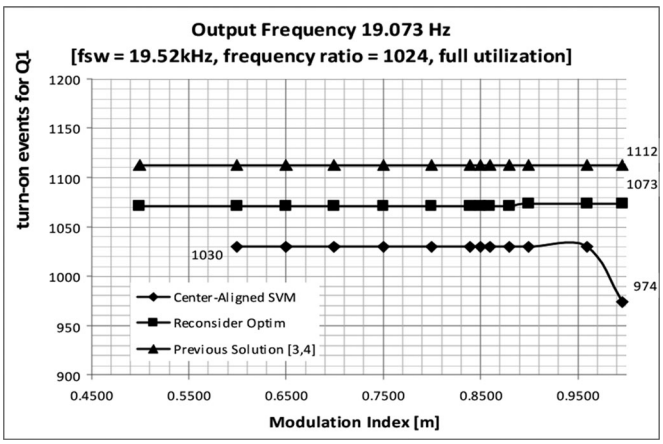



Fig. 12. Actual count of turn-on events for an IGBT device (compare to ideal 1024), for a conventional center-aligned SVM, previous optimal SVM [3], [4] (adapted to 256-bit resolution), and improved optimal solution, all for a frequency ratio of 1024.

other benchmark solutions: the same setup can easily run at any modulation index, fundamental frequency, or PWM sampling frequency. The flash memory ICs within the inverter are following the best results for HCF with modulation index, that is the *center-aligned SVM* pattern under $m = 0.83$ and the *new multioptimal PWM* above $m = 0.83$. This change of PWM methods is possible due to our novel research contribution with a digital architecture based on flash memories. Fig. 9 shows that this arrangement does not produce any discontinuity within the inverter overall linearity (from modulation index to rms voltage) when changing patterns from center-aligned PWM to new multioptimal PWM since all the characteristics are quasi-identical.

Fig. 12 shows the actual count of turn-on processes for one IGBT of the six within the inverter configuration, for all methods under investigation. This is supposed to match the frequency ratio, that is, 1024 for 19.073 Hz at 19.52 kHz sampling in order to have in average one switching per PWM sampling interval. The fundamental frequency of 19.073 Hz has been

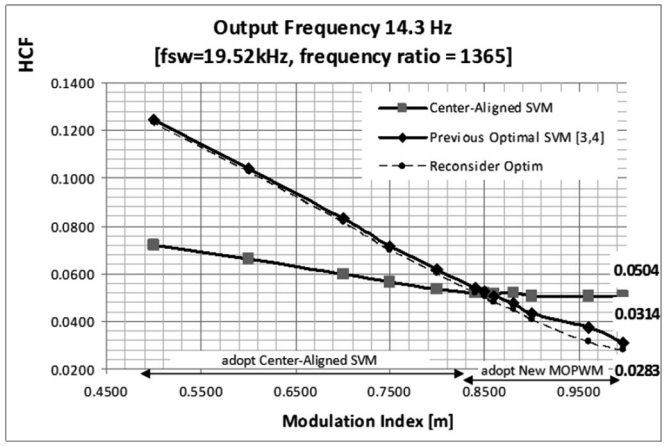



Fig. 13. HCF for a conventional center-aligned SVM, previous optimal SVM [3], [4] (adapted to 256-bit resolution), and improved optimal solution, all for a frequency ratio of 1365.

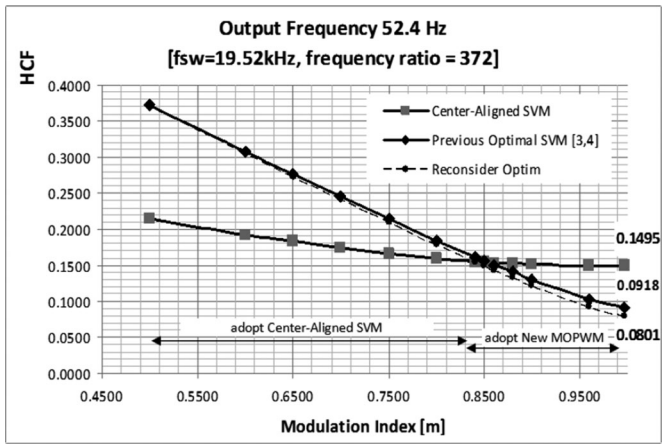



Fig. 14. HCF for a conventional center-aligned SVM, previous optimal SVM [3], [4] (adapted to 256-bit resolution), and improved optimal solution, all for a frequency ratio of 372.

here considered for a full utilization of the flash memory 10-bit angular coordinate. The actual number of switching processes usually yields different from the analytically defined frequency ratio since certain imperfections occur during pulse generation like pulse deletion below a minimum pulse width or arithmetic truncation when digitizing on a low-resolution model. If the analytically defined duration of a pulse is under the minimum pulse width possible within digital hardware, the pulse will not show in the output voltage due to truncation. Hence, no switching will actually occur. For instance, pulse generation along active vectors, at exactly 60°, produces Z1-V1-Z2-V1-Z1 instead of Z1-V1-V2-Z2-V2-V1-Z1 for a conventional center-aligned SVM.

The effect of the HCF improvements introduced by the current solution is shown in Figs. 13 and 14, for two other fundamental frequencies (14.3051 and 52.4521 Hz, respectively) selected arbitrarily to complete the throughout analysis. In both cases, the PWM is generated at 19.52 kHz. Obviously, these PWM patterns can be read faster or slower, and the frequency ratio is what matters. For instance, similar

TABLE II
HCF RELATIVE IMPROVEMENTS FROM THE CONVENTIONAL SVM, SHOWN AT THE HIGHEST MODULATION INDEX AND 20 KHZ (ACTUAL 19.53 KHZ) PWM SAMPLING FREQUENCY (RESULTS MAY BE ALSO INFLUENCED BY A DIFFERENT DIGITIZATION)

| | Fundamental = 14.3051 Hz | Fundamental = 23.8419 Hz | Fundamental = 52.4521 Hz |
|---|---|---|---|
| | Frequency ratio = 1365 | Frequency ratio = 819 | Frequency ratio = 372 |
| Former solution (similar to [3], [4]) | 37.70% | 38.50% | 38.60% |
| Novel solution with three innovative approaches [this paper] | 43.85% | 46.26% | 46.42% |

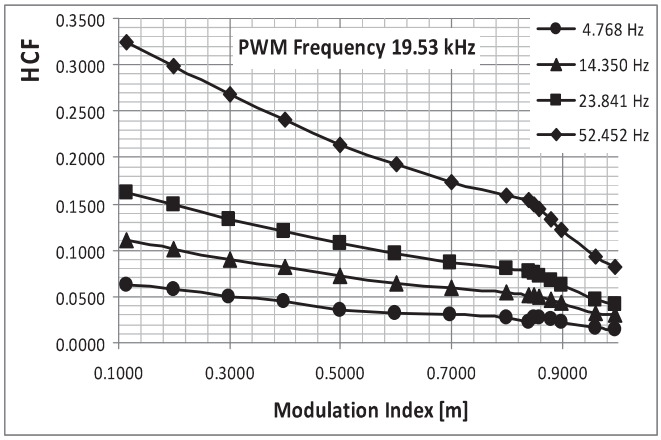



Fig. 15. HCF for the proposed multioptimal PWM at 19.52 kHz sampling PWM frequency and shown fundamental frequencies. Data collected after reading back from written memory chips on MATLAB simulated environment.

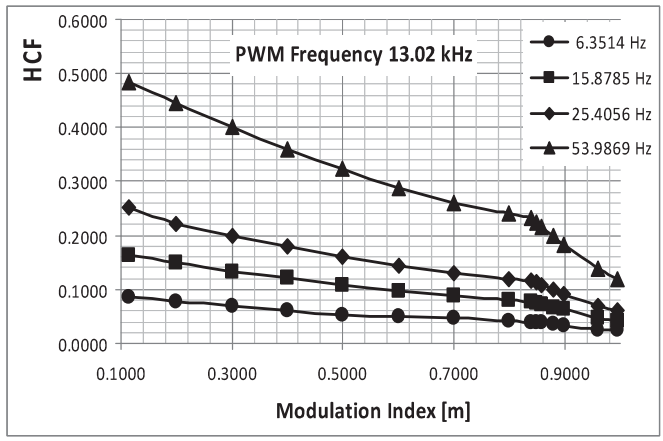



Fig. 16. HCF for the proposed multioptimal PWM at 13.02 kHz sampling PWM frequency and shown fundamental frequencies. Data collected after reading back from written memory chips on MATLAB simulated environment.

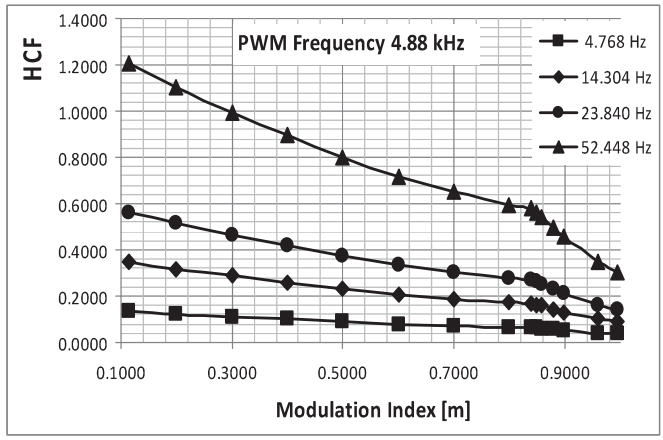



Fig. 17. HCF for the proposed multioptimal PWM at 4.88 kHz sampling PWM frequency and shown fundamental frequencies. Data collected after reading back from memory chips onto MATLAB simulated environment.

HCF harmonic results can be achieved for either the case of 3.90 kHz PWM sampling frequency and 10.490 Hz fundamental frequency or the case of 19.52 kHz PWM sampling frequency and 52.452 Hz fundamental frequency.

Improvements at the highest modulation index are summarized in Table II. The greatest improvement over the conventional SVM or over the previous method are achieved at the highest modulation index, with smaller frequency ratios.

After the content of the memory tables are optimized and tested in MATLAB, data are written to the memory integrated circuits with a programmer. If a programmer device is not available, such service can be provided by the distributor of memory integrated circuits, like *Digikey*.

In order to illustrate the usage of these flash memory ICs with various sampling PWM frequencies, Figs. 15–17 show the same performance index (HCF) for different sampling and fundamental frequencies. This time, data used for calculation were collected after reading back from the actual memory. This was possible on MATLAB-simulated environment and offers a faster automated evaluation of results. Furthermore, such analysis takes advantage of an FFT with larger number of sampling points than most acquisition systems on the market today. Nominally, we have 256 samples per PWM period, that is, 262 144 per fundamental cycle at a 10-bit angular resolution. This is because samples can be acquired at any sampling rate, which is a limitation in dedicated acquisition systems.

Our multistep design procedure is followed within MATLAB-based FFTW analysis at each step: Figs. 9–12 are a pure MATLAB analytical optimization, Figs. 13 and 14 read back data from flash memory into MATLAB for analysis with the same FFTW algorithm, while Figs. 15–17 show that data are collected from inverter- and microcontroller-based hardware and analyzed also in MATLAB with the same FFTW algorithm. This iterative approach verifies and proves consistency of the design. Results from Figs. 15 to 17 may count for possible truncations or limitations of the complete digital implementation. If everything is properly done, they should not differ much from the previous results shown in Figs. 13 and 14. Moreover, they are a stronger demonstration of the hardware, with all components, interrupt routines, and communication flow.

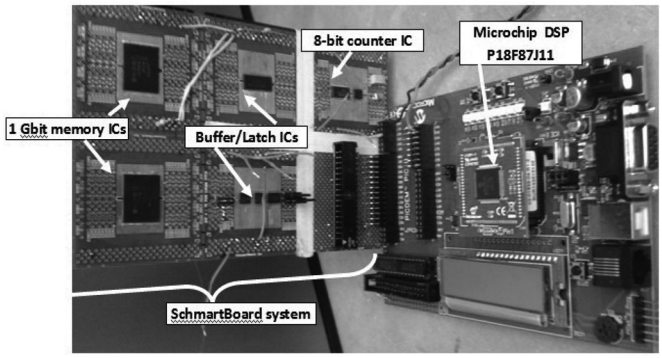



Fig. 18. Digital circuitry on *SchmartBoard* platform following our novel proposal of a digital architecture also shown in Fig. 6.

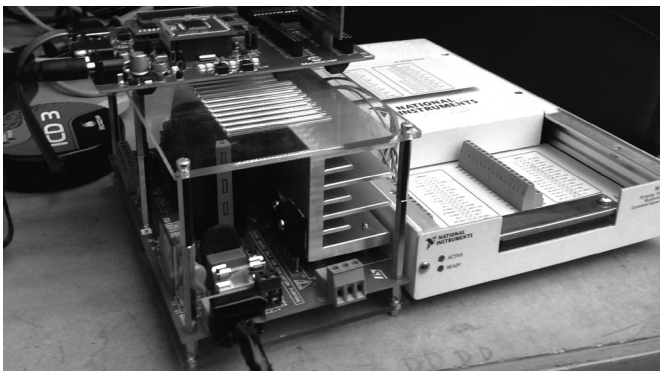
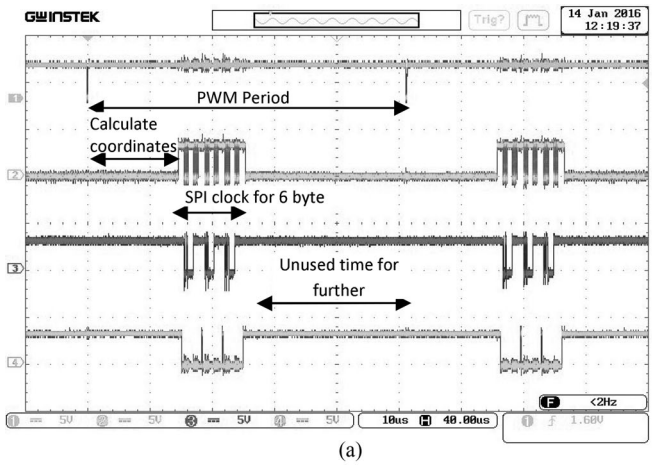
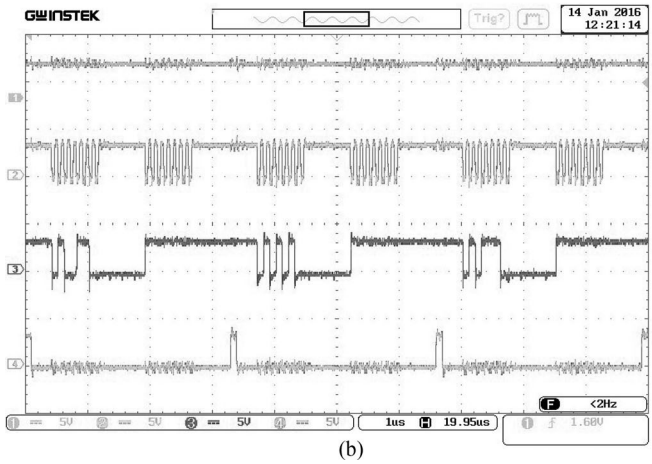


Fig. 19. Overall inverter setup and National Instruments acquisition system.




(a)




(b)

Fig. 20. Scope waveforms characteristic to the circuit for 10 MHz SPI communication: $1 =$ toggle from external counter for microcontroller's interrupt; $2 =$ SPI clock; $3 =$ data out; $4 =$ /CS for SPI: (a) zoom of communication data stream also shown in (b), which presents the entire communication of all 6 B.

## VI. Inverter Setup

This section presents for the first time the hardware required for the implementation of optimal PWM algorithms with flash memory devices. Experiments show and validate the operation of the novel digital controller within a conventional three-phase inverter. The proposed digital controller is a low-cost hardware able to implement features otherwise requiring extremely complex computer infrastructure or impossible to implement.

The digital circuit from Fig. 6 was implemented on a quick development platform carried out with *SchmartBoard* development boards (see Fig. 18). The inverter setup is based on *ST Microelectronics'* inverter STEVAL-IHM025V1, and it has been described in previous references [3], [4]. The complete setup is shown in Fig. 19.

The proposed 20 kHz superior limit of sampling frequency comes from our implementation with a maximum 19.52 kHz sampling, which yields from 256 intervals of 200 ns. Going under 200 ns for each discretization step of the PWM waveform is a challenge and may limit the capability to have feedback control in software. Furthermore, the highest frequency ratio comes from the definition of the software angular coordinate on 12 bit, that is, 4096 intervals of $256 \times 200$ ns, which becomes 209.72 ms, or 4.76 Hz. Lower frequencies can be achieved with software-based pulse multiplication.

Fig. 20 provides timing diagrams for the SPI communication and interrupt generation. These prove the feasibility of operation at 20 kHz (50 $\mu$s), with plenty of time reserve for implementation of field orientation control for a motor drive, current controllers for grid power transfer, or any other load control algorithm. Specifically, there is around 15 $\mu$s time interval from synchronized interrupt to the actual six bytes SPI communication. This time is used in our program to calculate or generate coordinates for the next PWM cycle and to manage the interrupt in C language. There is also around 25 $\mu$s unused time interval after the SPI communication. This proves the feasibility of our proposed novel digital architecture for implementation of multioptimal PWM algorithms on flash memory.

Further, Fig. 21 illustrates the gate control signals for high-side IGBTs at arbitrarily selected operation points, and sampling/switching PWM frequency, fundamental frequency, and modulation index are provided for each scope capture.

These results prove by time-domain waveforms the feasibility of the *new multioptimal PWM* algorithm. They create an image about the complexity of the *new multioptimal PWM* algorithms with different operation modes, depending on angular

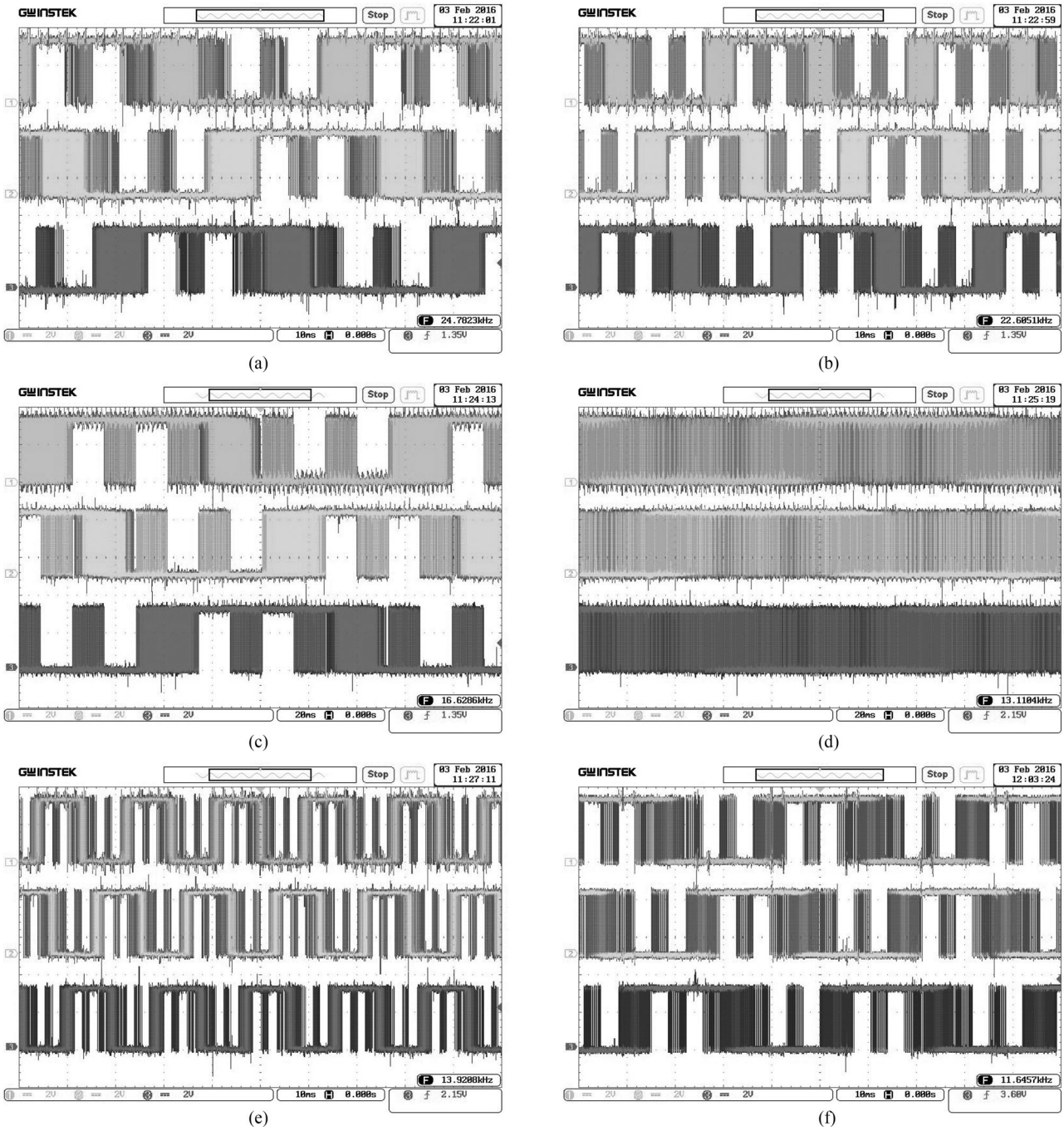



Fig. 21. Gate control signals for the High-Side IGBTs at various measurement points. (a) fsw = 19.53 kHz; f1 = 14.35 Hz; $m = 0.996$. (b) fsw = 19.53 kHz; f1 = 23.84 Hz; $m = 0.900$. (c) fsw = 13.02 kHz; f1 = 6.35 Hz; $m = 0.860$. (d) fsw = 13.02 kHz; f1 = 6.35 Hz; $m = 0.800$. (e) fsw = 19.53 kHz; f1 = 53.98 Hz; $m = 0.960$. (f) fsw = 4.88 kHz; f1 = 23.84 Hz; $m = 0.900$.

coordinate and modulation index. A careful analysis can identify intervals and similarities with Fig. 7(b).

Some other considerations:

1) Operation below $m = 0.83$ with *center-aligned* SVM leads to signals shown in Fig. 21(d), while all the other waveforms are for cases with $m$ above 0.83.
2) The pattern specific for the newly proposed multioptimal PWM is consistent for any combination of values of fundamental and sampling frequencies as shown in Fig. 21 (a)–(c), (e), and (f).

Both the modulation index and angular coordinate are updated on each sampling interval. The system behaves as an open-loop system. No closed-loop feedback current or voltage control has been implemented. The output voltage follows the reference. The transient induced by a change of either one coordinate will be reflected within the next sampling interval. Fig. 22 has been added to show a coordinate change.

A final test has been made with *National Instruments M-series USB-6221* acquisition system (16 bits, 250 kSamples/s). Some resolution of the FFT is lost when compared with


Fig. 22. Transition resulted from a fast change of coordinates from one sampling interval to the next: Channel 3 shows a PWM gate signal; Channel 4 shows the limits of constant PWM sampling intervals.

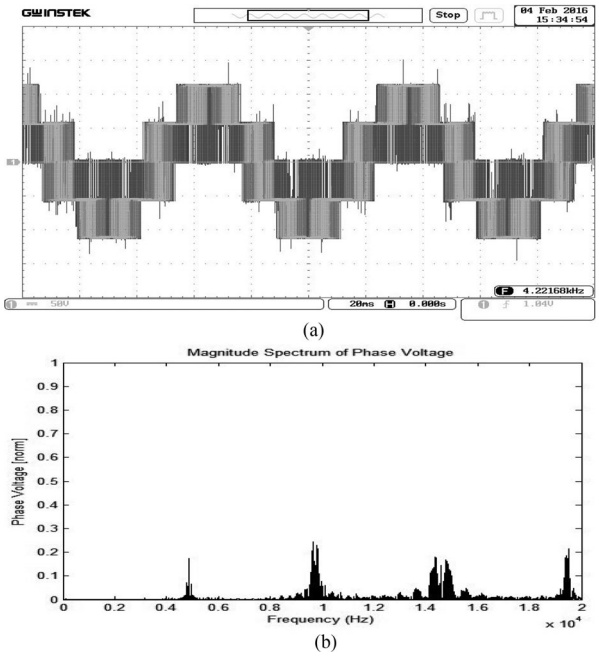



Fig. 23. Phase voltage on the scope and FFT results achieved with signal acquisition through National Instruments USB-6221 and MATLAB FFT post-processing. Analysis at $\mathrm{fsw} = 4.88\,\mathrm{kHz}$; $\mathrm{f1} = 14.30\,\mathrm{Hz}$; $\mathrm{mod} = 0.996$.

previous MATLAB calculation used for analysis of the memory content through computer-based read back. After acquisition of the high-voltage phase voltage with USB-6221, harmonics have been calculated from samples of the measurement through a MATLAB script. Most illustrative results are obtained when the sampling/switching PWM frequency is low (further away from the 250 kSamples/s rate). An example of the analysis is shown in Fig. 23 for a PWM switching/sampling frequency of 4.88 kHz (around 50 acquired samples per PWM period). The FFT results are somewhat worse when compared to the higher resolution analysis performed by reading back from the memory at 256 samples per PWM period. Our oscilloscope cannot allow for an HCF calculation based on these harmonic results. Hence, Fig. 23 mostly demonstrates that the system works without actually being able to prove all required harmonic performance due to laboratory limitations.

## VII. Conclusion

This paper demonstrates for the first time the usage of flash memory integrated circuits to the implementation of multioptimal PWM algorithms for three-phase power converters. The usage of a large-size memory lookup table stored inside flash memory with fast access is also a novel trend in processor architecture often called "*in-memory databases.*"

A digital circuitry has been built as an interface between a low-cost microcontroller and the newly released low-cost gigabit-size memory integrated circuits. It uses a fast serial communication protocol without the complexity of previous communication used for file transfers with SD cards or flash memory. The communication protocol and the connecting glue logic can be set up with any low-cost microcontroller with an SPI interface. The entire hardware is very cost competitive.

A *new multioptimal PWM* algorithm has been proposed to use difference pulse sequences on different locations of the complex plane. It uses a very large-size flash memory for implementation and demonstrates over 40% reduction in current harmonics. Results were compared with conventional *center-aligned SVM,* and the benefits were highlighted.

The operation of the modulator from a very large size memory integrated circuit, at PWM sampling frequencies up to 20 kHz, has been experimentally proven herein for the first time ever. The implemented PWM algorithm is not intended as an ultimate solution even if more than 40% reduction in current harmonics is proven through the HCF coefficient. Once the feasibility of this hardware platform is demonstrated for three-phase inverters at any PWM sampling frequency up to 20 kHz, more work on optimization algorithms is possible and this is a very attractive research field for the future.

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