A Seven-Switch Five-Level Active-Neutral-Point-Clamped Converter and Its Optimal Modulation Strategy

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***Abstract*—Multilevel inverters are receiving more attentions nowadays as one of preferred solutions for medium- and high-power applications. As one of the most popular hybrid multilevel inverter topologies, the five-level active-neutral-point-clamped inverter (5L-ANPC) combines the features of the conventional flying-capacitor type and neutral-point-clamped (NPC) type inverter and was commercially used for industrial applications. In order to further decrease the number of active switches, this paper proposes a seven-switch 5L-ANPC (7S-5L-ANPC) topology, which employs only seven active switches and two discrete diodes. The analysis has shown a lower current rating can be selected for the seventh switch under high power factor condition, which is verified by simulation results. The modulation strategy for 7S-5L-ANPC inverter is discussed. A 1 kVA single-phase experimental prototype is built to verify the validity and flexibility of the proposed topology and modulation method.**

***Index Terms*—Active-neutral-point-clamped (ANPC) inverter, flying-capacitor (FC), multilevel inverter, pulse width modulation (PWM).**

I. Introduction

THE five-level inverter is a good choice for industrial application because of lower total harmonic distortion (THD), reduced switching stress and hence lower switching losses compared to the three-level inverter [1]–[6]. For the conventional five-level neutral-point-clamped (5L-NPC) inverter, as shown in Fig. 1(a), there are three clamping points in the dc-link (P, O, and Q). The control strategy to keep voltages of each clamping points is complicated. Additionally, reverse recovery currents from clamping diodes will increase the switching losses of the system [7], [8]. Another conventional five-level inverter topology type is five-level flying-capacitor (5L-FC) inverter. As shown in Fig. 1(b), the increased number of capacitors leads to increased volume of the system as well as complex control method to balance the voltages of both dc-link capacitors and FCs [9], [10].

Manuscript received May 16, 2016; revised August 1, 2016 and September 15, 2016; accepted September 16, 2016. Date of publication September 28, 2016; date of current version February 27, 2017. Recommended for publication by Associate Editor Dr. D. O Neacsu.

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Digital Object Identifier 10.1109/TPEL.2016.2614265

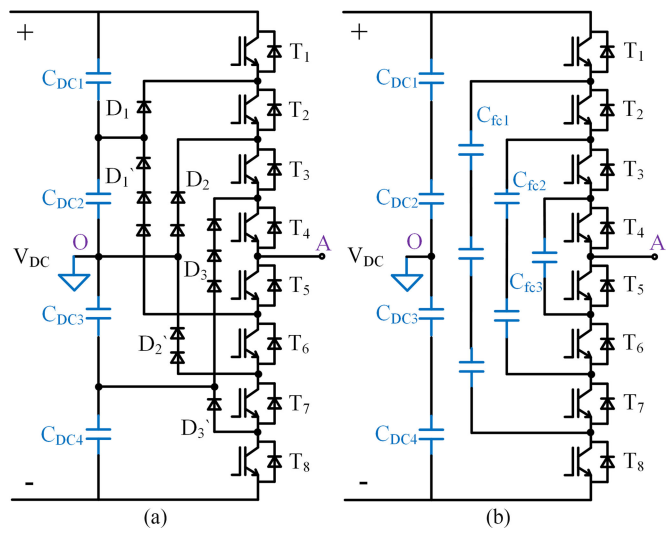

Fig. 1. Conventional five-level inverter topologies. (a) 5L-NPC. (b) 5L-FC.

In recent years, hybrid multilevel inverters are receiving more attentions in both academia and industry because they combine the features of many conventional multilevel inverter topologies [11], [12]. As one of the most popular hybrid multilevel inverter topologies, the five-level active-neutral-point-clamped (5L-ANPC) inverter combines the characteristics of NPC type and flying-capacitor (FC) type inverters [13]–[21]. As shown in Fig. 2(a), the 5L-ANPC inverter combines a three-level ANPC (3L-ANPC) leg with a 3L-FC power cell. This topology enables the modularity factor that is lacking in the neutral-point-clamped (NPC) type inverter by adding the FC power cell to reach higher level without adding series-connected diodes. Additionally, the 5L-ANPC inverter splits the dc link into two capacitors (C_1, C_2), so it is simpler to achieve voltage balance between these two capacitors. Due to the reduced costs, volume and control complexity, the 5L-ANPC inverter has gained increasing attention recently and is already commercially used for medium power level industrial applications. Fig. 2(b) and (c) show additional two types of 5L-ANPC inverter [22].

There are redundant switching states in 5L-ANPC inverters which can be utilized to balance the FC voltage. To generate the switching pulses and simultaneously regulate the FC and neutral point voltage, a variety of modulation strategies have

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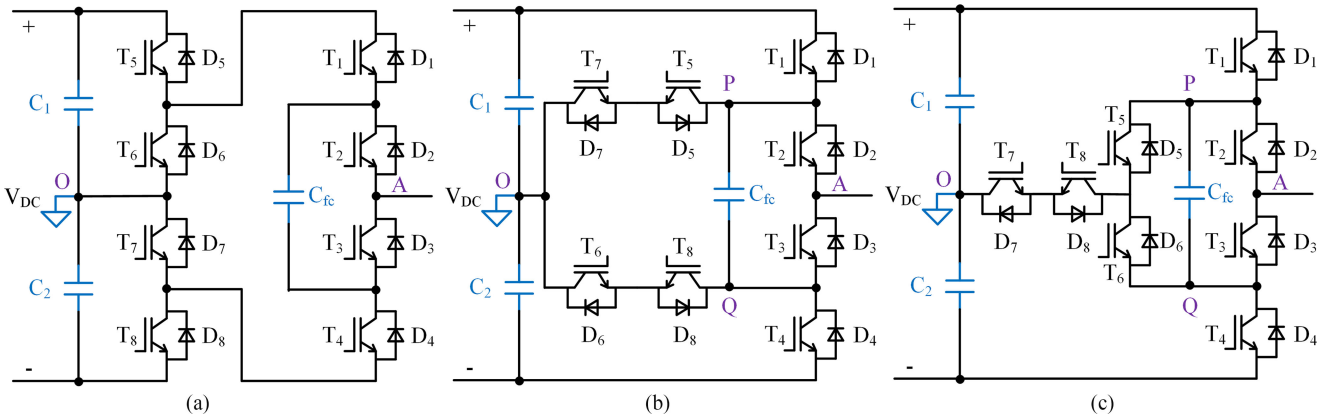

Fig. 2. 5L-ANPC inverter topologies. (a) Type I. (b) Type II. (c) Type III.

been proposed such as carrier-based pulse width modulation (PWM), modified triangular carrier-based PWM [16], real time THD minimization, [23] and selective-harmonic-elimination PWM [24].

In Fig. 2, it can be observed that the existing conventional 5L-ANPC inverter topologies still require eight active switches. For industrial application, it would be more desirable if the cost of the system can be reduced. The motivation of this paper is to reduce the number of active switches. Based on this, a novel seven-switch five-level ANPC (7S-5L-ANPC) inverter topology is proposed [25]. Compared to the conventional 5L-ANPC inverter, the proposed topology uses only seven active switches. Additionally, with special modulation strategy, the proposed topology is capable of operating under reactive power condition and achieving the same performance as the conventional 5L-ANPC inverters.

This paper is organized as follows: Section II introduces the basic idea of the derivation of the proposed 7S-5L-ANPC inverter; Section III describes the operating principles of 7S-5L-ANPC inverter; Section IV makes a comparison between 7S-5L-ANPC and the conventional 5L-ANPC topologies in terms of device voltage stress, switching frequency, conduction loss, and switching loss; Section V discusses the current stress of the seventh switch; Section VI presents the modulation method for 7S-5L-ANPC inverter under reactive power factor (PF) condition; Section VII and VIII give the simulation and experimental results and Section IX draws the conclusion.

II. Derivation of the Proposed 7S-5L-ANPC Inverter

The Type II and Type III conventional 5L-ANPC inverters are shown in Fig. 2(b) and (c). First, the input dc voltage is defined as V_{DC}. The dc link consists of two series-connected capacitors (C_1, C_2), whose voltages are rated at half of dc voltage ($V_{\mathrm{DC}}/2$). A FC (C_{fc}) is required to provide one quarter of dc voltage ($\mathrm{V_{DC}}/4$). Therefore, five output voltage levels $+\mathrm{V_{DC}}/2$, $+\mathrm{V_{DC}}/4$, 0, $-\mathrm{V_{DC}}/4$ and $-\mathrm{V_{DC}}/2$ (which are defined as +2, +1, 0, –1 and –2 respectively for simplification) are obtained by summing algebraically the dc capacitor and FC voltages. As can be observed, the dc neutral point O is connecting to both ends of the FC P and Q through two pairs of series-connected switches and T type switches, respectively, both of which require four active switches.

The motivation of this paper is to decrease the number of active switches. To achieve this, four inner switches ($\mathrm{T_5}$ – $\mathrm{T_8}$) are ignored at first, as shown in Fig. 3(a). When switches ($\mathrm{T_1}$, $\mathrm{T_2}$) or ($\mathrm{T_3}$, $\mathrm{T_4}$) are switched ON, the inverter is generating +2 or –2 output levels. Similarly, for the switching states which generate +1 or –1 levels, ($\mathrm{T_1}$, $\mathrm{T_3}$) or ($\mathrm{T_2}$, $\mathrm{T_4}$) are turned ON. Both switching states are charging the FC under unity PF condition. To keep the FC voltage balanced, additional two switching states which also generate +1 and –1 level to discharge the FC are required, which are called redundant switching states. To achieve this, the FC alone should be connected to output ends to provide the energy. FC is discharging in these intervals. So for the redundant +1 level switching state, point P is connected to output point A through $\mathrm{T_2}$ while additional switches are needed to connect point O to Q. The direction of active current in this situation is from O to Q through FC and then from P to A, so additional active switch T_a and discrete diode D_a are added, as shown in Fig. 3(b). The reason for adding D_a is to prevent FC being directly connected to C_1 when $\mathrm{T_1}$ is ON. However, the main current branch should be bidirectional, thus to obtain the reactive current path, additional switch T_b and diode D_b are added in parallel with D_a. The reactive current will flow through T_a, T_b and D_b. It is noted that the circuit in Fig. 3(b) is also capable of generating zero level when newly added branch and $\mathrm{T_3}$ are ON. Similarly, in Fig. 3(c), two active switches T_c, T_d and two discrete diodes D_c, D_d are added to provide redundant –1 and zero level switching states. To combine the two circuits in Fig. 3(b) and (c), it is noted that (T_b and T_d), (D_b and D_c), (D_a and D_d) can be merged, so the simplified circuit is shown in Fig. 3(d), which is the proposed 7S-5L-ANPC inverter.

The function of $\mathrm{T_7}$ is to provide bidirectional current paths for O to P and O to Q. Two discrete diodes $\mathrm{D_7}$ and $\mathrm{D_8}$ act as the body diode of switch $\mathrm{T_7}$ to limit the reverse voltage, so the selection of $\mathrm{T_7}$ can be IGBT without antiparallel diode, reducing the system cost. In addition, with the proposed modulation strategy which will be discussed in Section VI, the current through $\mathrm{T_7}$ under unity PF condition will be zero, and under high PF condition, a low current will pass through $\mathrm{T_7}$. Therefore, a low-current

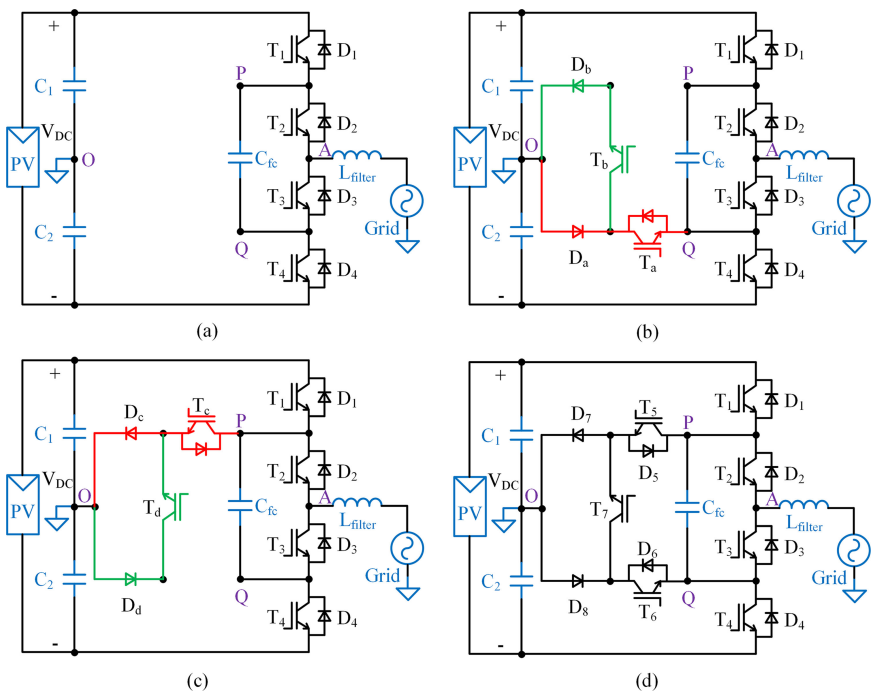

Fig. 3. Derivation of the proposed 7S-5L-ANPC inverter topology. (a) Circuit 1. (b) Circuit 2. (c) Circuit 3. (d) Proposed topology.

TABLE I
SWITCHING STATES, OUTPUT VOLTAGE, AND IMPACT ON THE FC VOLTAGE OF 7S-5L-ANPC INVERTER

	Conduction state of active switch								Flying capacitor C_{fc}		
Switching state	T_1	T_2	T_3	T_4	T_5	T_6	T_7	Output voltage level	$i_{out} > 0$	$i_{out} < 0$	Conduction state of T_7
A	1	1	0	0	0	1	0	+2	–	–	No
B	1	0	1	0	0	1	0	+1	Charge	Discharge	No
C	0	1	0	0	0	1	1	+1	Discharge	Charge	Yes
D	0	0	1	0	0	1	1	+0	–	–	Yes
E	0	1	0	0	1	0	1	–0	–	–	Yes
F	0	0	1	0	1	0	1	–1	Charge	Discharge	Yes
G	0	1	0	1	1	0	0	–1	Discharge	Charge	No
H	0	0	1	1	1	0	0	–2	–	–	No

rating switch can be selected for T_7 under PF condition, leading to a further reduction of system cost.

In contrast to the conventional 5L-ANPC inverters which need eight active switches and other types of five-level inverters which require more devices, the proposed 7S-5L-ANPC inverter only requires seven active switches and two discrete diodes. It can achieve the same performance as the conventional 5L-ANPC inverters. The following section will discuss the detailed operating principles of 7S-5L-ANPC inverter.

III. Operating Principles of 7S-5L-ANPC Inverter

Same as the conventional 5L-ANPC inverters, the 7S-5L-ANPC inverter has eight switching states to generate five output levels: +2, +1, 0, –1, and –2. Eight switching states are named from A to H. Table I lists all eight switching states and their impact on FC voltage and Fig. 4 shows the circuit diagram of the specific eight switching states and bidirectional current paths (active current branch in red solid line while reactive current branch in green dashed line). The output current is defined as i_{out}.

From Table I, it is observed that two pairs of redundant one-level switching states (+1: B and C) and (–1: F and G) have impact on FC voltage regulation. The effect of redundant one-level switching states on the FC voltage is opposite. Therefore, the regulation of FC voltage can be achieved by proper selection of redundant one-level switching states. Additionally, to keep FC voltage balanced, the sign of output current i_{out} and the actual value of FC voltage are required to decide which redundant switching state to be selected. For example, when output current is positive and the actual FC voltage value is lower than its reference value, then states B and F are chosen to charge the FC. In this way, the FC voltage can be balanced at the reference value.

The interval of one-level switching state selection can be at every switching period. The impact of lower PWM frequency on FC voltage regulation will increase this control interval of one-level switching state selection. Therefore, if the switching frequency is lower, then the FC voltage following its reference

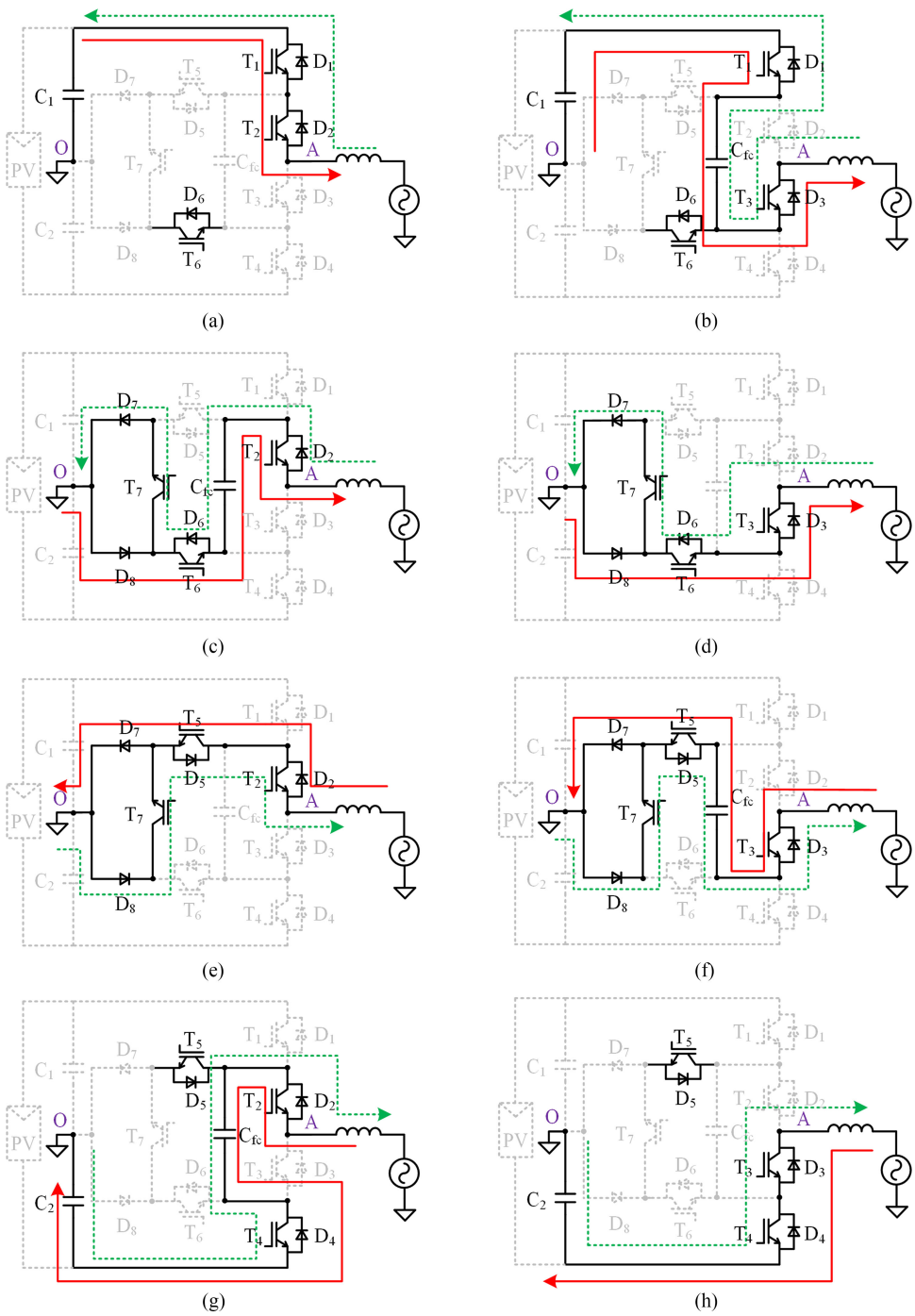

Fig. 4. Eight switching states for 7S-5L-ANPC inverter. (a) State A: +2. (b) State B: +1. (c) State C: +1. (d) State D: 0. (e) State E: 0. (f) State F: -1. (g) State G: -1. (h) State H: -2.

value will be slower. The regulation of dc capacitor voltage can be achieved by controlling the FC voltage [20]. Similarly, the lower switching frequency will lead to slower dc voltage balancing.

All eight switching states have bidirectional current flow paths, so the proposed 7S-5L-ANPC inverter have the same performance as the conventional 5L-ANPC inverters. The proposed topology can be used for three-phase application. The Space Vector Modulation method is usually used for three-phase application and the dc-link capacitor voltage can be balanced by adding zero sequence voltage [26], in which the redundancy of one-level switching states still plays an important role of controlling dc capacitor and FC voltages.

The number of voltage levels can be increased by adding the cascaded two-level inverters. The seven-level topology is shown in Fig. 5. For n-level topology, the number of active switches is $n + 2$, and the number of required FCs is $(n - 3)/2$. The ratio of FC voltages to half dc-link voltage is $1: 2: \cdots: (n - 3)/2: (n - 1)/2$.

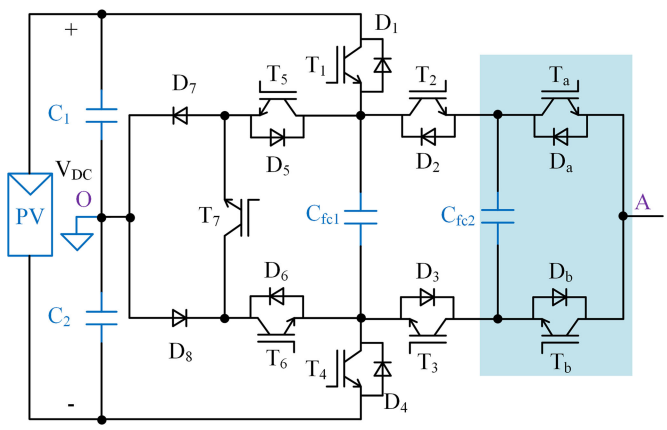

Fig. 5. Extension of voltage levels based on 7S-5L-ANPC topology (seven-level topology).

IV. Comparison Between 7S-5L-ANPC and the Conventional 5L-ANPC Inverters

To better illustrate the advantage of the proposed topology, it is important to make a comparison between 7S-5L-ANPC inverter and the conventional 5L-ANPC inverters in terms of device voltage rating, switching frequency, conduction loss, and switching loss.

A. Device Voltage Stress and Switching Frequency

Table II shows the voltage stress and switching frequency of devices for four types of 5L-ANPC inverters. f_{Line} and f_S represent the line frequency and switching frequency, respectively.

Comparison to Type I 5L-ANPC inverter: the voltage stress of T_1/D_1 and T_4/D_4 for 7S-5L-ANPC inverters is increased to $0.75\ V_{DC}$, which means a higher voltage rating device should be selected for these two switches. However, the switching loss of these two devices are generated in the same way as in Type I 5L-ANPC inverter. For example, T_1/D_1 will carry the output current i_{out} when switched on and block the voltage levels of $0.25\ V_{DC}$ when switched OFF in the positive grid cycle. On the other hand, for Type I 5L-ANPC inverter, T_1/D_1 and T_4/D_4 are switched ON and OFF at switching frequency f_S for the whole grid cycle; while for the proposed topology, T_1/D_1 and T_4/D_4 are only operating at f_S for half-line period and turned OFF for the other half-line period, so the switching loss of these two devices will be lower (approximately half of switching loss in Type I topology). The properties of devices T_2/D_2, T_3/D_3, T_5/D_5, and T_6/D_6 for two topologies are the same. Additionally, for Type I 5L-ANPC topology, the voltage stress of T_7/D_7 and T_8/D_8 is $0.5\ V_{DC}$, operating at line frequency; for the proposed topology, the voltage stress of T_7 is $0.25\ V_{DC}$, operating at switching frequency, and the voltage stress of D_7 and D_8 is also $0.25\ V_{DC}$, operating at switching frequency for half-grid period. The switching loss comparison will be given in Section IV-C.

Comparison to Type II 5L-ANPC inverter: the devices voltage stress of the proposed topology is the same as that of Type II 5L-ANPC topology. The difference is: for Type II 5L-ANPC topology, switches T_7 and T_8 are operating at switching frequency for half-line cycle; for 7S-5L-ANPC topology, switch T_8 is saved and T_7 is operating at switching frequency for whole line cycle.

Comparison to Type III 5L-ANPC inverter: the properties of devices T_1/D_1 to T_4/D_4 of 7S-5L-ANPC topology are the same as that of Type III. The differences are the voltage stress of line frequency devices T_5/D_5 and T_6/D_6 for Type III 5L-ANPC topology is $0.25\ V_{DC}$; for 7S-5L-ANPC topology, the voltage stress of these two devices is $0.5\ V_{DC}$ and for Type III 5L-ANPC topology, switches T_7 and T_8 are operating at switching frequency for half-line cycle; for 7S-5L-ANPC topology, switch T_8 is saved and T_7 is operating at switching frequency for the whole line cycle. However, the conduction loss of Type III 5L-ANPC topology is higher, which will be given in the following part.

B. Conduction Loss Analysis

The conduction loss comparison can be performed considering the number of connected devices in series when they are on, as shown in Table III. The symbols + and – represent the minimum and maximum number of conducting devices.

Comparison to Type I 5L-ANPC inverter: for Type I 5L-ANPC inverter, three devices are always connected in series to carry the main current for all eight switching states; while for the proposed topology: during the switching states A, B, G, and H, the output current is going through only two devices. Therefore, compared to Type I 5L-ANPC topology, the conduction loss of the proposed topology during these four states is reduced by 1/3. In addition, for 7S-5L-ANPC topology, during the switching states C, D, E, and F, the current will flow through three devices when the output current and voltage are in the same directions, and it will pass through four devices when the output current and voltage are in the opposite directions. With the proposed modulation method, the output current can always flow through three devices during the zero-level switching states D and E. But in the region where the output current and voltage are in opposite directions, the output current must go through four devices during the one-level switching states C and F. For high PF applications, such as PV grid-connection applications (PF $>$ 0.9), the region where the output current and voltage are in the opposite directions is small, and the output current of this region is also small because the region is near the current zero-crossing point, so the conduction loss of 7S-5L-ANPC topology during these four switching states is similar to that of Type I 5L-ANPC topology. The total conduction loss of the proposed topology under high PF condition will be lower than Type I 5L-ANPC topology (approximately reduced by 1/6).

Comparison to Type II 5L-ANPC topology: the conduction loss of 7S-5L-ANPC inverter during states A, B, G, and H is the same as that of Type II and similar to the comparison between 7S-5L-ANPC and Type I 5L-ANPC topologies, the conduction loss of 7S-5L-ANPC topology during switching states C, D, E, and F is similar to that of Type II 5L-ANPC topology under high PF condition. So the total conduction loss of the proposed topology under high PF condition will be closed to Type II 5L-ANPC topology.

TABLE II
VOLTAGE STRESS AND SWITCHING FREQUNECY OF DEVICES FOR FOUR TYPES OF 5L-ANPC INVERTERS

	Type I 5L-ANPC		Type II 5L-ANPC		Type III 5L-ANPC		7S-5L-ANPC	
Device	Voltage Stress	Switching Frequency	Voltage Stress	Switching Frequency	Voltage Stress	Switching Frequency	Voltage Stress	Switching Frequency
T_1/D_1	$0.25\ V_{DC}$	f_S	$0.75\ V_{DC}$	f_S for half line cycle	$0.75\ V_{DC}$	f_S for half line cycle	$0.75\ V_{DC}$	f_S for half line cycle
T_2/D_2	$0.25\ V_{DC}$	f_S	$0.25\ V_{DC}$	f_S	$0.25\ V_{DC}$	f_S	$0.25\ V_{DC}$	f_S
T_3/D_3	$0.25\ V_{DC}$	f_S	$0.25\ V_{DC}$	f_S	$0.25\ V_{DC}$	f_S	$0.25\ V_{DC}$	f_S
T_4/D_4	$0.25\ V_{DC}$	f_S	$0.75\ V_{DC}$	f_S for half line cycle	$0.75\ V_{DC}$	f_S for half line cycle	$0.75\ V_{DC}$	f_S for half line cycle
T_5/D_5	$0.5\ V_{DC}$	f_{Line}	$0.5\ V_{DC}$	f_{Line}	$0.25\ V_{DC}$	f_{Line}	$0.5\ V_{DC}$	f_{Line}
T_6/D_6	$0.5\ V_{DC}$	f_{Line}	$0.5\ V_{DC}$	f_{Line}	$0.25\ V_{DC}$	f_{Line}	$0.5\ V_{DC}$	f_{Line}
T_7	$0.5\ V_{DC}$	f_{Line}	$0.25\ V_{DC}$	f_S for half line cycle	$0.25\ V_{DC}$	f_S for half line cycle	$0.25\ V_{DC}$	f_S
T_8	$0.5\ V_{DC}$	f_{Line}	$0.25\ V_{DC}$	f_S for half line cycle	$0.25\ V_{DC}$	f_S for half line cycle	Not needed	Not needed
D_7	$0.5\ V_{DC}$	f_{Line}	$0.25\ V_{DC}$	f_S for half line cycle	$0.25\ V_{DC}$	f_S for half line cycle	$0.25\ V_{DC}$	f_S for half line cycle
D_8	$0.5\ V_{DC}$	f_{Line}	$0.25\ V_{DC}$	f_S for half line cycle	$0.25\ V_{DC}$	f_S for half line cycle	$0.25\ V_{DC}$	f_S for half line cycle

TABLE III
CONDUCTION LOSS OF FOUR TYPES OF 5L-ANPC INVERTERS

Switching State		Type I 5L-ANPC		Type II 5L-ANPC		Type III 5L-ANPC		7S-5L-ANPC	
A (+2)	$i_{out} > 0$	T_1, T_2, T_5	−	T_1, T_2	+	T_1, T_2	+	T_1, T_2	+
	$i_{out} < 0$	D_1, D_2, D_5	−	D_1, D_2	+	D_1, D_2	+	D_1, D_2	+
B (+1)	$i_{out} > 0$	T_1, T_5, D_3	−	T_1, D_3	+	T_1, D_3	+	T_1, D_3	+
	$i_{out} < 0$	D_1, D_5, T_3	−	D_1, T_3	+	D_1, T_3	+	D_1, T_3	+
C (+1)	$i_{out} > 0$	T_2, T_7, D_4	+	T_2, T_6, D_8	+	T_2, T_5, T_8, D_6	−	T_2, T_6, D_8	+
	$i_{out} < 0$	D_2, D_7, T_4	+	D_2, D_6, T_8	+	D_2, D_5, D_8, T_6	−	D_2, D_6, T_7, D_7	−
D (0)	$i_{out} > 0$	T_7, D_3, D_4	+	D_3, T_6, D_8	+	D_3, T_5, T_8, D_6	−	D_3, T_6, D_8	+
	$i_{out} < 0$	D_7, T_3, T_4	+	T_3, D_6, T_8	+	T_3, D_5, D_8, T_6	−	T_3, D_6, T_7, D_7	−
E (0)	$i_{out} > 0$	T_1, T_2, D_6	+	T_2, T_7, D_6	+	T_2, T_5, D_6, D_7	−	T_2, D_5, T_7, D_8	−
	$i_{out} < 0$	D_1, D_2, T_6	+	D_2, D_7, T_5	+	D_2, D_5, T_6, T_7	−	D_2, T_5, D_7	+
F (−1)	$i_{out} > 0$	T_1, D_3, D_6	+	D_3, T_7, D_5	+	D_3, T_5, D_6, D_7	−	D_3, D_5, T_7, D_8	−
	$i_{out} < 0$	D_1, T_3, T_6	+	T_3, D_7, T_5	+	T_3, D_5, T_6, T_7	−	T_3, T_5, D_7	+
G (−1)	$i_{out} > 0$	T_2, D_4, D_8	−	T_2, D_4	+	T_2, D_4	+	T_2, D_4	+
	$i_{out} < 0$	D_2, T_4, T_8	−	D_2, T_4	+	D_2, T_4	+	D_2, T_4	+
H (−2)	$i_{out} > 0$	D_3, D_4, D_8	−	D_3, D_4	+	D_3, D_4	+	D_3, D_4	+
	$i_{out} < 0$	T_3, T_4, T_8	−	T_3, T_4	+	T_3, T_4	+	T_3, T_4	+

Comparison to Type III 5L-ANPC topology: for Type III 5L-ANPC topology, four devices are always needed to conduct the output current during the switching states C, D, E, and F; while for the proposed topology, three devices are needed to conduct the output current when output current and voltage are in same directions, and four devices are required when output current and voltage are in opposite directions. Therefore, under high PF condition (e.g., PF > 0.9), the conduction loss of the proposed topology during the four states C, D, E, and F is reduced approximately by 1/4 as compared to Type III 5L-ANPC inverter, and the total conduction loss is reduced approximately by 1/8.

With above analysis, it is concluded that the conduction loss of the proposed 7S-5L-ANPC topology is affected by system PF: for high PF application such as PV applications, the conduction loss of 7S-5L-ANPC topology is the closed to that of Type II conventional 5L-ANPC topology, and is lower than that of Type I and Type III 5L-ANPC inverters.

C. Switching Loss Analysis

Table IV shows the switching loss in terms of switching states commutations.

For the proposed topology, it is observed that for four switching states commutations (B to D, C to D, G to E, and H to F), two devices are switched ON or OFF when the output current and voltage are in the same directions while three devices are switched ON or OFF when the output current and voltage are in opposite directions.

Comparison to Type I 5L-ANPC inverter, as mentioned earlier, for 7S-5L-ANPC inverter, the devices T_1/D_1 and T_4/D_4 have to block $0.75\ V_{DC}$ voltage for a period of time in which they are not conducting current. However, the switching loss of these two devices are generated in the same way as in Type I 5L-ANPC inverter. From Table IV, it is observed that for all switching state transitions, the device voltage change is $0.25\ V_{DC}$ and the current is output current i_{out}. Under high PF condition, if the device selection for 7S-5L-ANPC and Type I 5L-ANPC is the same, then the switching loss of 7S-5L-ANPC topology will be closed to that of Type I 5L-ANPC topology. If higher voltage rating devices are selected for T_1/D_1 and T_4/D_4 in 7S-5L-ANPC topology, then its switching loss will be slightly higher than that of Type I due to the increased turn-on energy for higher voltage rating device.

Comparison to Type II 5L-ANPC inverter: first, according to Table II, it is observed that the voltage stress of devices in

TABLE IV
SWITCHING LOSS OF FOUR 5L-ANPC INVERTERS

Switching State				Type I 5L-ANPC	Type II 5L-ANPC	Type III 5L-ANPC	7S-5L-ANPC	ΔV	ΔI
A (+2)	$\longleftrightarrow$	B (+1)	$i_{out} > 0$	T_2, D_3	T_2, D_3	T_2, D_3	T_2, D_3	$0.25\ V_{DC}$	i_{out}
			$i_{out} < 0$	D_2, T_3	D_2, T_3	D_2, T_3	D_2, T_3	$0.25\ V_{DC}$	i_{out}
A (+2)	$\longleftrightarrow$	C (+1)	$i_{out} > 0$	T_1, D_4	T_1, D_8	T_1, D_8	T_1, D_8	$0.25\ V_{DC}$	i_{out}
			$i_{out} < 0$	D_1, T_4	D_1, T_8	D_1, T_8	D_1, T_7, D_7	$0.25\ V_{DC}$	i_{out}
B (+1)	$\longleftrightarrow$	D (0)	$i_{out} > 0$	T_1, D_4	T_1, D_8	T_1, D_8	T_1, D_8	$0.25\ V_{DC}$	i_{out}
			$i_{out} < 0$	D_1, T_4	D_1, T_8	D_1, T_8	D_1, T_7, D_7	$0.25\ V_{DC}$	i_{out}
C (+1)	$\longleftrightarrow$	D (0)	$i_{out} > 0$	T_2, D_3	T_2, D_3	T_2, D_3	T_2, D_3	$0.25\ V_{DC}$	i_{out}
			$i_{out} < 0$	D_2, T_3	D_2, T_3	D_2, T_3	D_2, T_3	$0.25\ V_{DC}$	i_{out}
F (−1)	$\longleftrightarrow$	E (0)	$i_{out} > 0$	T_2, D_3	T_2, D_3	T_2, D_3	T_2, D_3	$0.25\ V_{DC}$	i_{out}
			$i_{out} < 0$	D_2, T_3	D_2, T_3	D_2, T_3	D_2, T_3	$0.25\ V_{DC}$	i_{out}
G (−1)	$\longleftrightarrow$	E (0)	$i_{out} > 0$	T_1, D_4	D_4, T_7	D_4, T_7	D_4, T_7, D_8	$0.25\ V_{DC}$	i_{out}
			$i_{out} < 0$	D_1, T_4	T_4, D_7	T_4, D_7	T_4, D_7	$0.25\ V_{DC}$	i_{out}
H (−2)	$\longleftrightarrow$	F (−1)	$i_{out} > 0$	T_1, D_4	D_4, T_7	D_4, T_7	D_4, T_7, D_8	$0.25\ V_{DC}$	i_{out}
			$i_{out} < 0$	D_1, T_4	T_4, D_7	T_4, D_7	T_4, D_7	$0.25\ V_{DC}$	i_{out}
H (−2)	$\longleftrightarrow$	G (−1)	$i_{out} > 0$	T_2, D_3	T_2, D_3	T_2, D_3	T_2, D_3	$0.25\ V_{DC}$	i_{out}
			$i_{out} < 0$	D_2, T_3	D_2, T_3	D_2, T_3	D_2, T_3	$0.25\ V_{DC}$	i_{out}

the proposed topology is the same as that of Type II 5L-ANPC topology; then based on Table IV, it can be concluded that under high PF condition, the switching loss of 7S-5L-ANPC topology is closed to that of Type II 5L-ANPC topology.

Comparison to Type III 5L-ANPC inverter: according to Table IV, it is observed that the switching loss of Types II and III are the same. Therefore, it can also be concluded that under high PF condition the switching loss of 7S-5L-ANPC topology is closed to Type III 5L-ANPC topology.

The analysis developed in this section shows that the power efficiency performance of the proposed 7S-5L-ANPC topology is influenced by the system operating characteristics and device selection. So for high PF applications (PF $>$ 0.9), it can be concluded that:

1) the efficiency of the proposed topology is closed to that of Type II 5L-ANPC inverter;
2) compared to Type I 5L-ANPC topology, the conduction loss of the proposed topology is lower, but the switching loss of the proposed topology is slightly higher. Therefore, under high power level condition whose system switching frequency is low, the proposed topology will show higher efficiency over Type I 5L-ANPC inverter [22]; and
3) compared to Type III 5L-ANPC inverter, the efficiency of the proposed 7S-5L-ANPC inverter is higher because its conduction loss is lower than that of Type III 5L-ANPC topology.

Consequently, for high PF applications such as PV applications, the proposed 7S-5L-ANPC topology is a good choice because it achieves the reduction of one active switch and the same performance as the conventional 5L-ANPC inverters.

V. CURRENT STRESS ANALYSIS OF T_7

It is noted that, from Table I, during the four switching states (C, D, E, and F), the main current branch may pass through additional switch T_7 [the green dashed lines in Fig. 4(c)–(f)], leading to the increased conduction loss. Therefore, selection of redundant states may result in different current through T_7. In order to decrease the T_7 current stress, it is important to optimize the modulation strategy for 7S-5L-ANPC inverter. This section mainly discusses the optimal selection of switching states to reduce T_7 current stress. Among these four states, two states are zero level (D, E), one state is +1 level (C) and one state is –1 level (F). Two kinds of current are defined: same direction current represents the current whose direction is the same as that of output voltage and reverse direction current represents the current whose direction is opposite to that of output voltage.

A. Selection of Zero-Level Switching States D and E

It is observed that in Fig. 4(d) and (e), the red solid current path is only passing through two active switches and one discrete diode without additional T_7. According to this, it is concluded that when output current is going from O to A which also represents the positive output current, switching state D is chosen; while for negative output current, state E is selected. With this combination of zero-level switching states, no current will flow through T_7 when inverter is generating zero levels, and the conduction loss will be reduced.

B. Selection of One-Level Switching States C and F

As mentioned earlier, the FC voltage is regulated by appropriate selection of redundant one-level switching states. Therefore, to keep FC voltage balanced, states C and F are still required in the region where the output current and voltage are in opposite directions even if in this region the reverse direction current will pass through T_7.

C. T_7 Current Stress Analysis

With the above analysis, it is concluded that proper selection of zero-level switching states (D, E) is capable of eliminating the T_7 current in zero output level intervals. For one-level switching states (C, F), under unity PF condition, no current will pass through T_7; while under reactive power condition, the reverse direction current will go through T_7 during these two states, which is inevitable.

TABLE V
ZERO LEVEL SWICHING STATES COMBANATIONS

Case	0 level switching state used when $i_{\rm out} > 0$	0 level switching state used when $i_{\rm out} < 0$
1	D	E
2	E	D
3	D	D
4	E	E

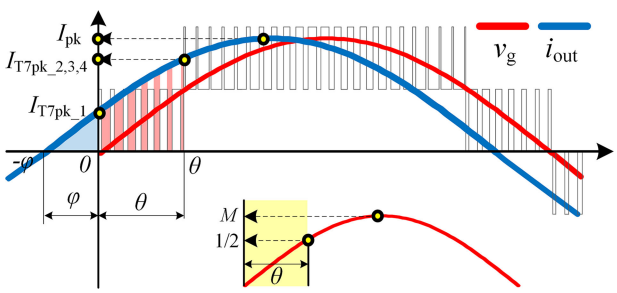

Fig. 6. Waveforms of output current and grid voltage under reactive power condition.

A comparison in four cases is made to verify the proposed zero-level switching states selection: case 1: state D for positive output current and E for negative output current which is the proposed one; case 2: state E for positive output current and D for negative output current; case 3: state D for the whole grid cycle; and case 4: state E for the whole grid cycle. Four cases are shown in Table V.

First, the output voltage which is also grid voltage is defined as v_g

$$\mathrm{v}_g = \mathrm{V}_g \cdot \sin(\omega t) \tag{1}$$

where V_g is the peak value of grid voltage and ω is angular frequency. The modulation index is defined as M which can be calculated by

$$M = \frac{\mathrm{V}_g}{\mathrm{V}_{\mathrm{DC}}/2}. \tag{2}$$

Under reactive power condition, there is a phase shift between output current and voltage, which is defined as φ. In the case of capacitive PF condition, the output current $i_{\rm out}$ is

$$i_{\rm out} = I_{pk} \cdot \sin(\omega t + \varphi) \tag{3}$$

where I_{pk} is the peak value of output current. Then the PF can be defined as

$$\mathrm{PF} = \cos(0 - \varphi) = \cos\varphi \left(-\frac{\pi}{2} \le \varphi \le \frac{\pi}{2}\right). \tag{4}$$

Fig. 6 shows the waveforms of output current and grid voltage under reactive power condition. The red and blue lines represent the gird voltage and output current respectively.

In case 1, the reverse direction current will pass through T_7 during the one-level switching states C and F, so the T_7 current stress in this case I_{T7pk_1} is determined by the peak value of reverse direction current

$$I_{\mathrm{T}_7 pk_1} = I_{pk} \cdot \sin\varphi. \tag{5}$$

Case 2 is opposite to case 1. With reference to the earlier analysis, it is achieved that in addition to the reverse direction current passing through T_7 during the one-level switching states C and F, the same direction current will also flow through T_7 during the zero-level switching states D and E (the red area in Fig. 6). This same direction current portion will lead to the increased T_7 current stress by additional phase angle θ, which

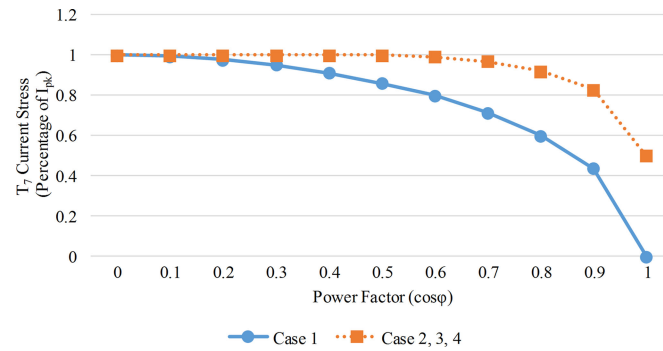

Fig. 7. Comparison of T_7 current stress in fours cases (M = 1).

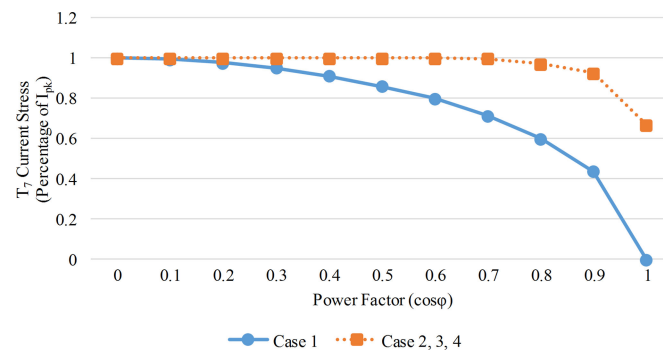

Fig. 8. Comparison of T_7 current stress in fours cases (M = 0.78).

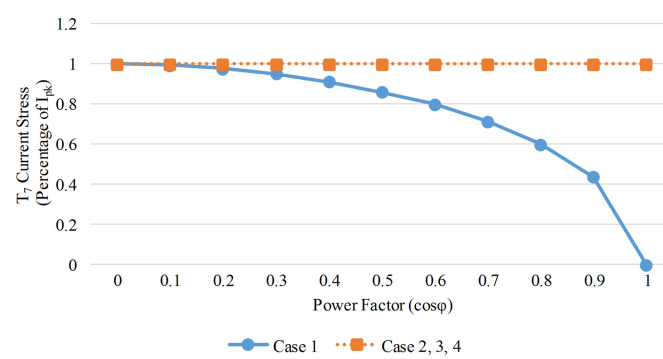

Fig. 9. Comparison of T_7 current stress in fours cases (M = 0.45).

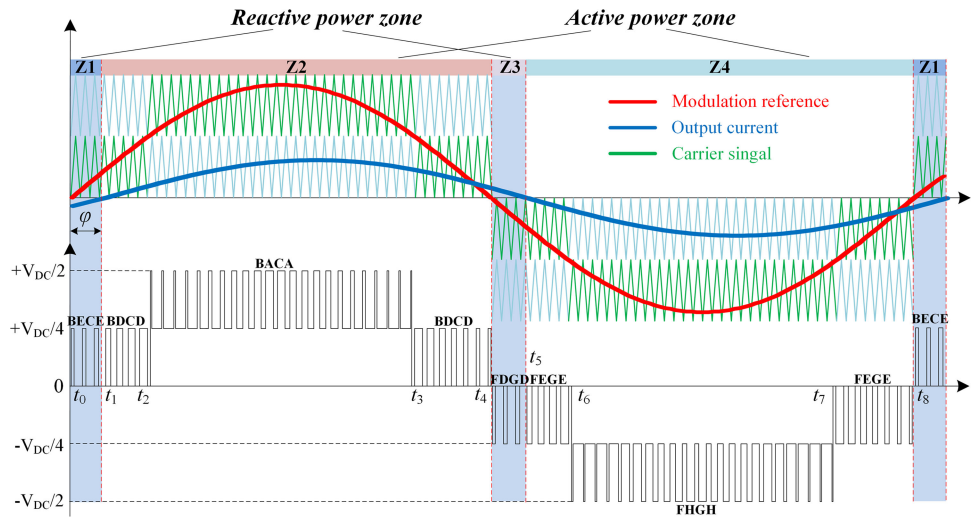

Fig. 10. PWM modulation for 7S-5L-ANPC inverter.

can be calculated by equation

$$M \cdot \sin\theta = \frac{1}{2} \tag{6}$$

$$\theta = \arcsin\left(\frac{1}{2M}\right). \tag{7}$$

So the T_7 current stress in case 2 I_{T7pk_2} is calculated by

$$I_{T_7pk_2} = \begin{cases} I_{pk} \cdot \sin[\varphi+\theta] & \left(M > \frac{1}{2} \text{ and } \varphi+\theta < \frac{\pi}{2}\right) \\ I_{pk} & \left(M \le \frac{1}{2}\right) \text{ or } \left(M > \frac{1}{2} \text{ and } \varphi+\theta \ge \frac{\pi}{2}\right) \end{cases}. \tag{8}$$

When M is lower than 1/2, the inverter is only switched between zero and one levels, so the T_7 current stress is equal to the peak value of output current I_{pk}. Similarly, when phase angle $(\varphi + \theta)$ is greater than $\pi/2$, the T_7 current stress is also equal to the peak value of output current I_{pk}.

For cases 3 and 4, half the same direction current as well as half the reverse direction current is going through T_7, so the calculated T_7 peak current value is the same as the one in case 2

$$I_{T_7pk_2} = I_{T_7pk_3} = I_{T_7pk_4} \tag{9}$$

In terms of modulation index M: the comparison results of T_7 current stress in four cases with $M = 1$ is shown in Fig. 7. As can be observed, under unity PF condition, no T_7 current in case 1 while in other three cases peak value of T_7 current is 50% of peak output current I_{pk}. Under 0.9 PF condition, the T_7 current stress in case 1 is only 43% of output current while in other three cases the current stress is increased to 82% of output current.

Fig. 8 gives the T_7 current stress comparison results under $M = 0.78$. The T_7 current stress in case 1 is unchanged. In cases 2–4, the current stress is increased: under $\mathrm{PF} = 1, \mathrm{I_{T7pk}}$ is increased to 64% of I_{pk}; when $\mathrm{PF} = 0.9, \mathrm{I_{T7pk}}$ is increased from 82% to 91% of I_{pk}.

Fig. 9 shows the comparison results when $M = 0.45$. In this case, the inverter is no longer outputting two level, so the T_7 current stress in cases 2–4 is always equal to output current.

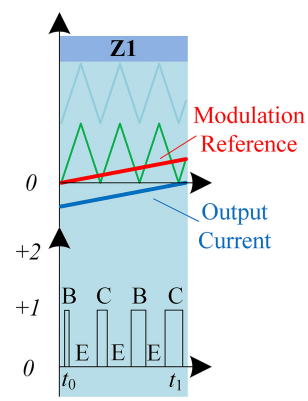

Fig. 11. Modulation in reactive power zone Z1.

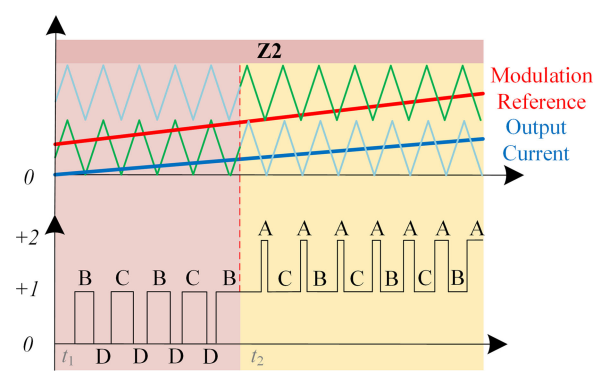

Fig. 12. PWM Modulation in active power zone Z2.

With the above analysis, it is concluded that under high PF condition, a low current rating switch can be selected for T_7 and the system cost can be further reduced.

VI. Modulation Method for 7S-5L-ANPC Inverter

This section discusses the modulation strategy for the proposed 7S-5L-ANPC inverter under reactive power condition which is also suitable for unity PF condition. For single

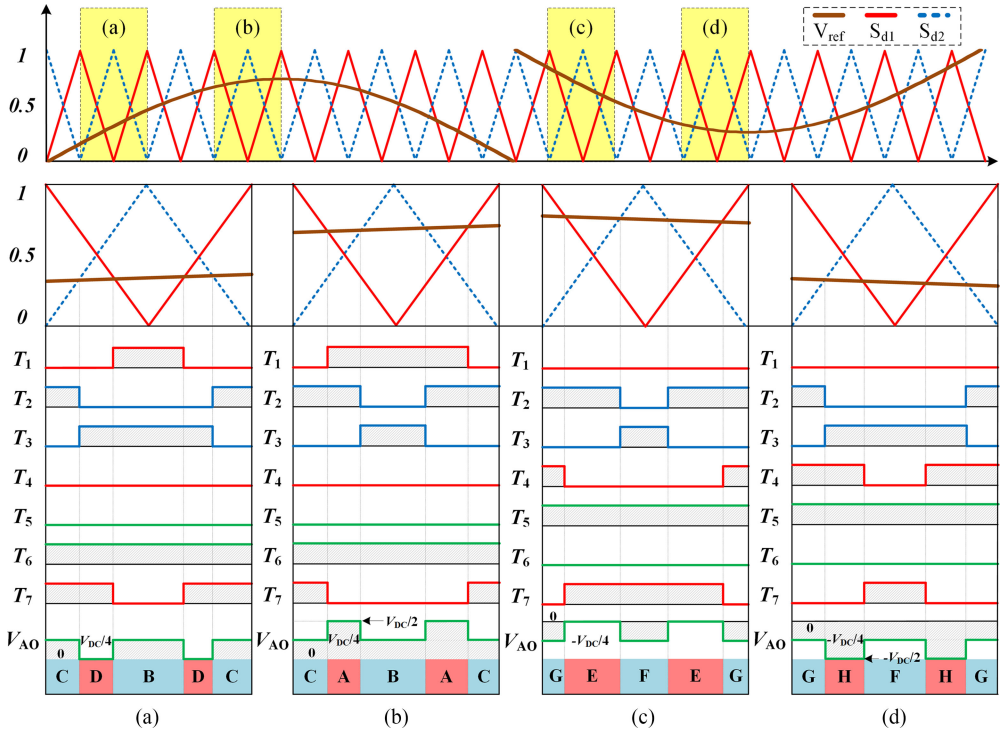

Fig. 13. ASFD PWM for 7S-5L-ANPC inverter. (a) $0 < \text{Vref} < 0.5$. (b) $\text{Vref} > 0.5$. (c) $-0.5 < \text{Vref} < 0$. (d) $\text{Vref} < -0.5$.

phase application, the phase disposition (all carrier signals are in phase) PWM scheme is used in this paper because of its lower THD [27]. The diagram of PWM for 7S-5L-ANPC inverter under reactive power operation is shown in Fig. 10. As can be observed, four carrier signals (green line) and one reference signal (red line) are employed to generate the gate signals for seven switches. There is a phase shift between the reference and output current (blue line). Based on this, four operating zones are identified according to the polarities of output current and reference signal: when reference and output current are in opposite direction, the inverter is entering reactive power zones which are Z1 and Z3; similarly, Z2 and Z4 belong to active power zones.

A. Reactive Power Zone Z1 [from t_0 to t_1]

In Z1, the output voltage is switched between +1 and 0. For zero output level, switching state E is selected due to the negative output current. For +1 level output, both redundant switching states B and C are required to balance the FC voltage. So, the inverter is rotating in the sequence of (B, E, C, E), as shown in Fig. 11.

B. Active Power Zone Z2 [From t_1 to t_4]

From t_1 to t_2 and t_3 to t_4, the output voltage still varies between +1 level and zero level. The difference is the output current is positive, so switching state D is chosen to generate zero voltage level. Both redundant +1 states (B, C) are used to regulate the voltage across FC. When measured FC voltage is lower than its reference value, the switching state B is selected to charge FC; when higher than reference value, switching state C is selected to discharge FC. In this region, the switching state sequence of (B, D, C, D) is obtained.

From t_2 to t_3, the inverter generates +2 level and +1 level. State A is used to generate +2 output level. Similarly, appropriate selection of redundant switching states (B, C) leads to the balancing of FC voltage. Consequently, the switching states sequence of (B, A, C, A) is selected in this region. The modulation in active power zone Z2 is shown in Fig. 12.

C. Reactive Power Zone Z3 [From t_4 to t_5]

In reactive power zone Z3, the inverter is switched between –1 level and zero level. The output current is positive, so switching state D is employed. The redundant switching states (F, G) are used to generate –1 output levels to balance FC voltage, so the switching state rotates in the sequence of (F, D, G, D).

D. Active Power Zone Z4 [From t_5 to t_8]

In this region, the output current is negative, so switching state E is used to generate zero level and guarantee no T_7 current; state H is used to generate –2 output level; redundant switching states (F, G) are employed to generate –1 level. Consequently, during t_5 to t_6 and t_7 to t_8, switching state sequence (F, E, G, E) is selected; from t_6 to t_7, switching state sequence (F, H, G, H) is selected.

The 7S-5L-ANPC inverter is much similar to Type II 5L-ANPC inverter, so its modulation scheme is almost the same as that of Type II topology. The only difference, according to the earlier analysis, is the selection of zero level switching states:

TABLE VI
SYSTEM PARAMETERS

Power	1 kVA	Grid Voltage (RMS value)	110 V @ 60 Hz
DC-link Voltage	400 V	Output Filter Inductance	1.6 mH
FC Capacitance	310 μF (947C311K102CBMS)	Power Factor	0.9–1
DC Capacitance	2000 μF each	Switching Frequency	15 kHz

for Type II 5L-ANPC topology, state D is selected when output voltage is positive while state E is chosen when output voltage is negative; for the proposed 5L-ANPC topology, state D is selected when output current is positive while state E is selected when output current is negative. By doing so, we can achieve no current through T7 during states D and E for the proposed topology.

E. Apparent Switching Frequency Doubling (ASFD) PWM Strategy for 7S-5L-ANPC inverter

The ASFD PWM strategy has been used in three-level (3L) ANPC inverter [28] and has also been applied to the conventional 5L-ANPC inverter [16] to achieve switching to achieve switching frequency doubling. This technique can also be applied to 7S-5L-ANPC inverter topology. Fig. 13 shows the diagram of ASFD PWM for 7S-5L-ANPC inverter. The reference signal is defined as $\mathrm{V_{ref}} = \mathrm{M} \cdot \sin\omega t$. The reference signal $\mathrm{V_{ref}}$ is compared with two carrier waves S_{d1} and S_{d2} that are phase shifted on the horizontal axis with half switching period $\mathrm{T}_S/2$. The switching states and sequences are analyzed at one switching period $\mathrm{T_S}$ under four different situations: (a) $0 < \mathrm{V_{ref}} < 0.5$, (b) $\mathrm{V_{ref}} > 0.5$, (c) $-0.5 < \mathrm{V_{ref}} < 0$, and (d) $\mathrm{V_{ref}} < -0.5$.

The gate signals of T_1, T_4, and T_7 are determined by V_{ref} and S_{d1}. As can be observed, T_4 is OFF when V_{ref} is positive, and T_1 is OFF when V_{ref} is negative; when T_1 or T_4 is ON, T_7 must be switched OFF to prevent FC being connected to dc-link capacitor directly. Carrier signal S_{d2} determines the switching states of T_2 and T_3. The line-frequency switches T_5 and T_6 are switched ON and OFF based on the sign of output current. The high-frequency switches T_1, T_2, T_3, T_4, and T_7 commute at the switching frequency f_S, and the output voltage V_{AO} has an apparent switching frequency equal to $2f_S$. Another advantage of this method is the one-level switching states (B, C, F, and G) will be applied alternately, leading to self-balancing of FC voltage and reduced FC voltage ripple.

VII. SIMULATION VERIFICATION

To verify the feasibility and advantages of the proposed topology and to verify the reduction of T_7 current with proposed modulation strategy, computer simulation by MATLAB Simulink has been carried out. Table VI shows the simulation parameters. The dc-link capacitance is selected to be 2000 F to limit its voltage ripple within 15 V (= 15 V/200 V = 7.5%) according to reference [16]. To demonstrate the feasibility and advantages of the proposed topology, the switching frequency is selected as 15 kHz. It is noted that, for high power applications, the switching frequency should be lower (e.g., 2 kHz or lower).

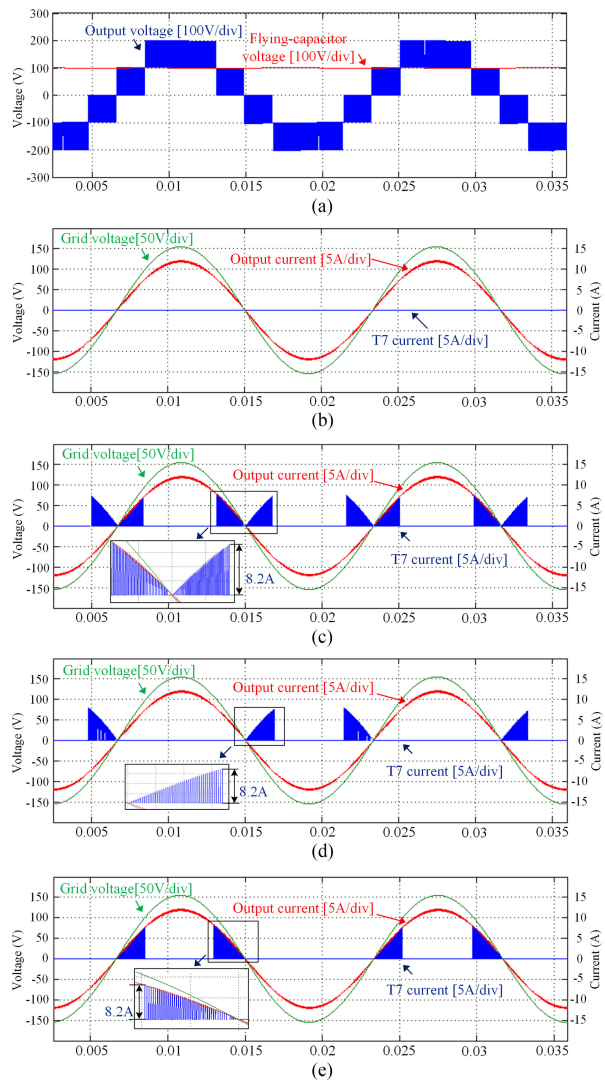

Fig. 14. Simulation results under unity power factor condition. (a) Output voltage and FC voltage. (b) T_7 current in case 1. (c) T_7 current in case 2. (d) T_7 current in case 3. (e) T_7 current in case 4.

Simulation is conducted in two cases: one is unity PF situation, and the other is reactive power condition (PF = 0.9 and PF = 0). Additionally, a comparison in four cases is made to verify the proposed modulation can achieve lowest current through T_7. Four cases are listed in Table V.

A. Unity PF Condition

Fig. 14 gives the simulation waveforms under unity PF condition. Fig. 14(a) shows the five-level inverter bridge voltage and FC voltage. It is observed that FC voltage is balanced at 100 V (a quarter of 400 V dc-link voltage). Fig. 14(b)–(e) show the gird voltage, inverter output current, and T_7 current in four cases (cases 1–4). The grid voltage and output current are in phase. The output current is a sinusoidal wave without distortion and the measured THD value in this case is 1.57%. The measured

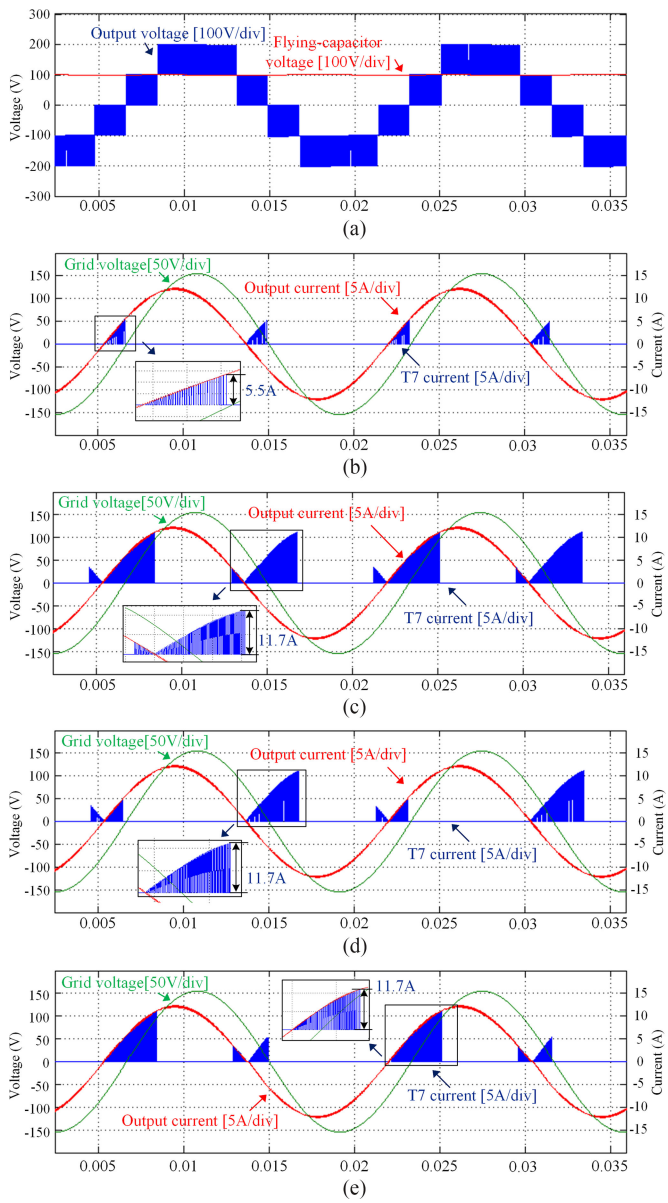

Fig. 15. Simulation results under reactive power condition (PF = 0.9, capacitive). (a) Output voltage and FC voltage. (b) T_7 current in case 1. (c) T_7 current in case 2. (d) T_7 current in case 3. (e) T_7 current in case 4.

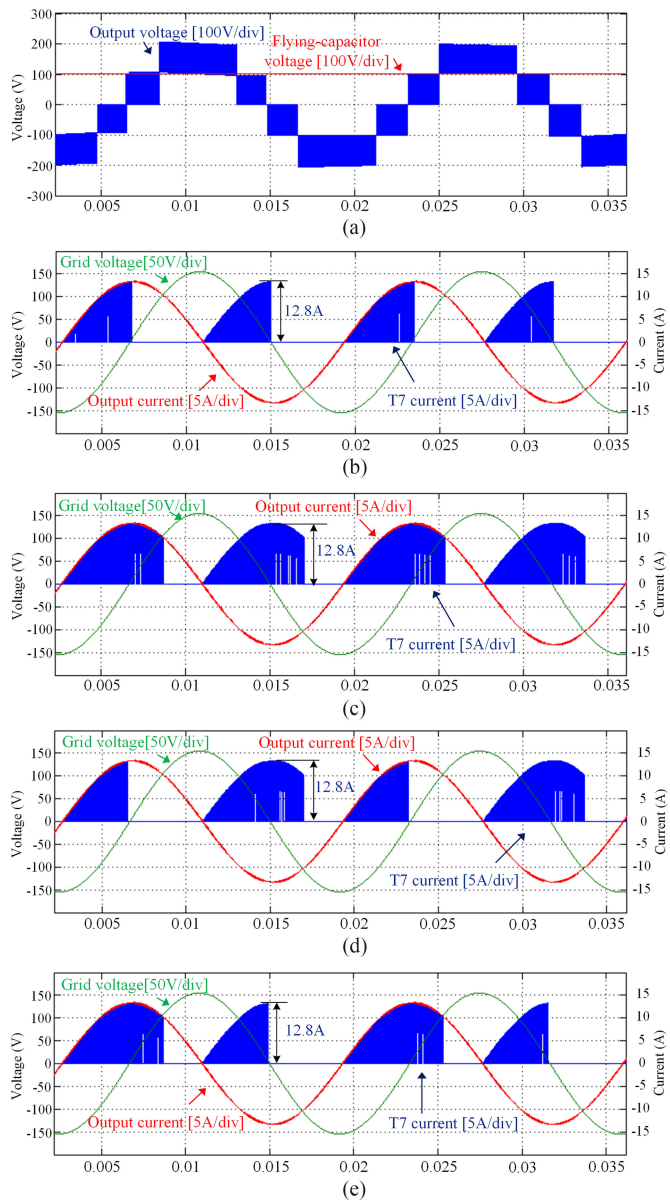

Fig. 16. Simulation results under reactive power condition (PF = 0). (a) Output voltage and FC voltage. (b) T_7 current in case 1. (c) T_7 current in case 2. (d) T_7 current in case 3. (e) T_7 current in case 4.

output current peak value is 12.8 A. The T_7 current waveforms in four cases are consistent with the above theoretical analysis. It can be clearly observed that in case 1, no current is flowing through T_7, and in other three cases, a maximum 8.2 A current (= 8.4 A/12.8 A = 64%) is passing through T_7. Therefore, it can be concluded that the aforementioned zero-level switching states selection in case 1 is the optimal selection.

B. Reacitve Power Condition

Similarly, simulation is also conducted under reactive power condition (PF = 0.9, capacitive) to show T_7 current stress. Waveforms of inverter output voltage, FC voltage, grid voltage, output current, and T_7 current in four cases are shown in Fig. 15.

Fig. 15(b)–(e) shows the output current, grid voltage, and T_7 currents in four situations. In this case, the measure output current THD is still 1.57%. According to the analysis in the previous section, reverse direction current will flow through T_7 in states C and F since in reactive power region both redundant one-level switching states are required to balance the FC voltage which results in the output current flowing through T_7 in states C and F in reactive power zones, so the reactive output current through T_7 is inevitable. However, with the optimal zero level switching states selection, no current will pass through T_7 when inverter is generating zero level. So in case 1, as shown in the detailed waveform of Fig. 15(b), it is observed that only reverse direction current is going through switch T_7, and the measured T_7 current peak value is 5.5A (= 5.5 A/12.8 A = 43%). In case 2, it is shown that when inverter is switched between zero and one

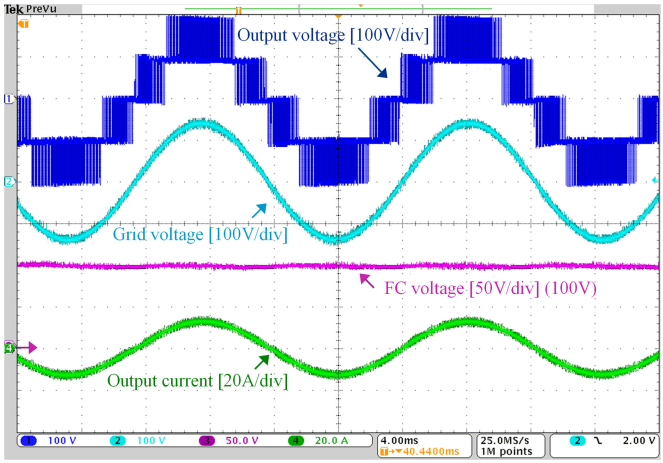

Fig. 17. Experimental results under unity power factor condition: waveforms of inverter output voltage, grid voltage, FC voltage, and output current.

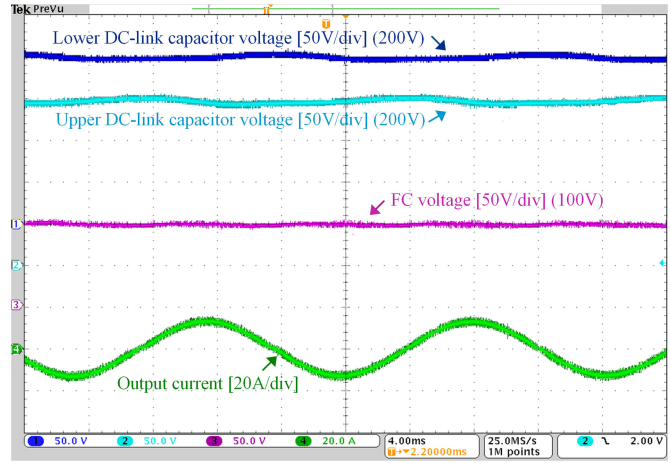

Fig. 18. Experimental results under unity power factor condition: waveforms of lower dc-link capacitor voltage, upper dc-link capacitor voltage, FC voltage, and output current.

levels, the reverse direction current as well as same direction current is passing through T_7, so the T_7 current peak value is increased to 11.7 A (= 11.7 A/12.8 A = 91%). Similarly, in cases 3 and 4, half active and reverse direction current is flowing through T_7, which is also undesirable.

Fig. 16 gives the simulation results under the extreme situation: PF = 0. As can be observed, the peak value of T_7 current in four cases is always equal to the peak value of output current which is 12.8 A. Additionally, the average current or conduction loss of T_7 in case 1 is the lowest. All the simulation results are consistent with the previous analysis and verify the proposed topology is capable of operating under full PF condition.

With simulation results under active and reactive PF conditions, it is concluded that the proposed 7S-5L-ANPC inverter is capable of achieving the same performance as the conventional 5L-ANPC inverters, and the proposed modulation strategy will result in the lowest current through T_7, which means system cost can be further reduced.

VIII. Experiment Verificatoin

A 1 kVA single-phase 7S-5L-ANPC inverter grid-connected laboratory prototype is built up to verify the proposed topology and modulation method. For the control circuit, a combination of the Texas Instruments TMS320F28335 DSP chip and the Altera Cyclone IV EP4CGX22 FPGA card is used to provide precise mathematical calculations and real-time control functions. The experimental parameters are identical to the ones used in simulation section, which are shown in Table VI. The FC capacitance is selected to be 310 μF (part number: 947C311K102CBMS).

The experimental waveforms under unity PF condition are shown in Figs. 17 and 18. The inverter output voltage, grid voltage, FC voltage, and output current of the new 7S-5L-ANPC inverter are shown from top to bottom in Fig. 17. The grid voltage is 110 V@60 Hz. The modulation index is around 0.78. The FC voltage is balanced at 100 V. The measured peak-to-peak FC voltage ripple is 2.1 V (= 2.1 V/100 V = 2.1%). The output

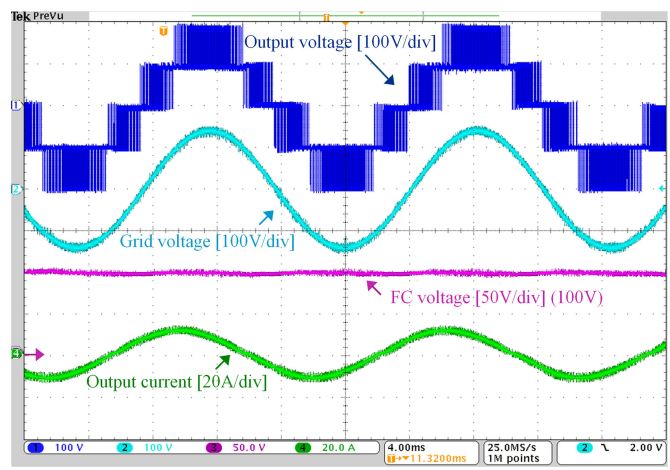

Fig. 19. Experimental results under reactive power operation (PF = 0.9, capacitive): waveforms of inverter bridge voltage, grid voltage, FC voltage, and output current.

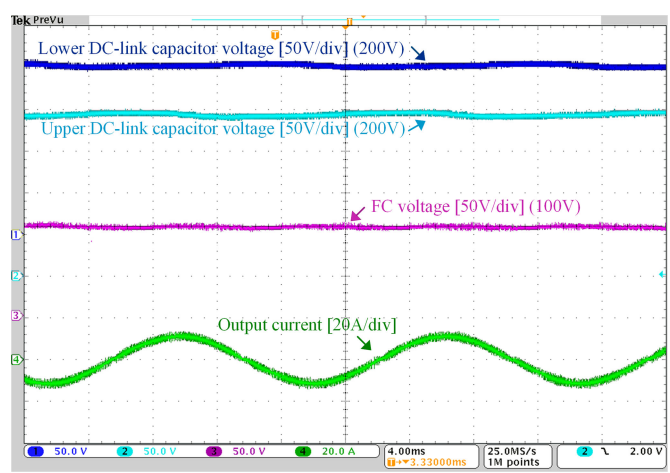

Fig. 20. Experimental results under reactive power condition (PF = 0.9, capacitive): waveforms of lower dc-link capacitor voltage, upper dc-link capacitor voltage, FC voltage, and output current.

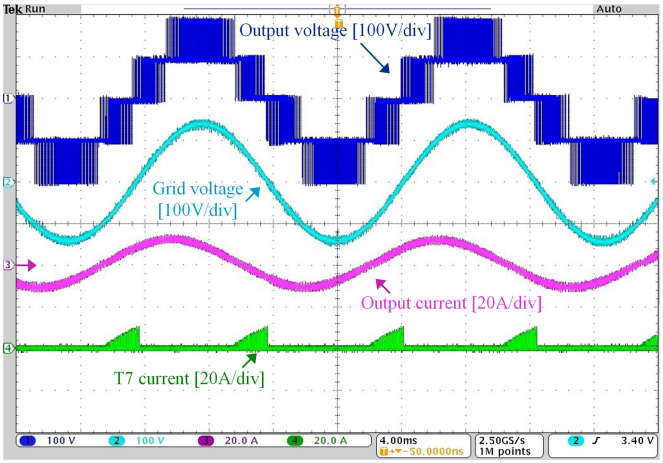

Fig. 21. Waveform of T_7 current in modulation case 1 (PF = 0.9, capacitive).

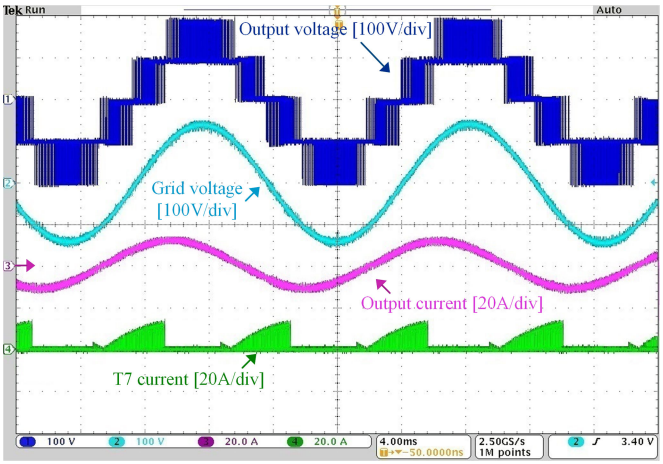

Fig. 22. Waveform of T_7 current in modulation case 2 (PF = 0.9, capacitive).

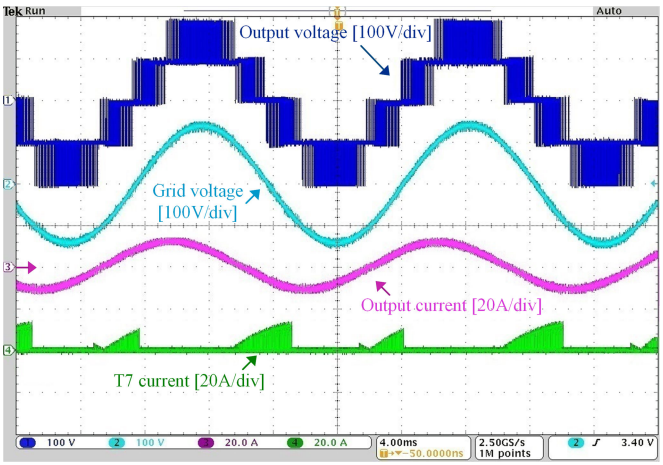

Fig. 23. Waveform of T_7 current in modulation case 3 (PF = 0.9, capacitive).

current is sinusoidal without distortion and in phase with grid voltage. The measured output current THD is 1.6%.

In addition to FC voltage and ac current waveforms, Fig. 18 also shows the voltages of two dc-link capacitors: channel 1 shows the lower dc-link capacitor voltage waveform while channel 2 gives the upper dc-link capacitor voltage waveform. As

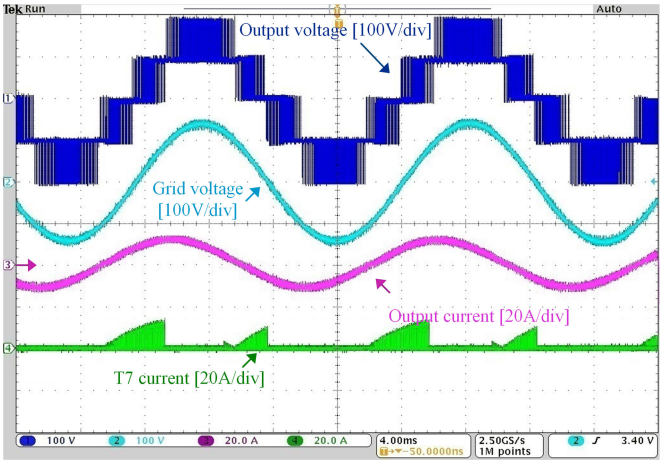

Fig. 24. Waveform of T_7 current in modulation case 4 (PF = 0.9, capacitive).

can be observed, voltages of both dc capacitors have a line-frequency fluctuation since during half-grid cycle only one dc capacitor is providing the energy to the output. The measured dc-link capacitor voltage ripple is 12 V (= 12 V/200 V = 6%). The balanced FC and dc-link capacitors voltages verify the modulation method in active power condition.

The experimental verification is also carried out in reactive PF situation. To be consistent with simulation results, the PF is selected to be 0.9 (capacitive). Figs. 19 and 20 show the experimental results.

From top to bottom, the waveforms are: the five-step bridge voltage, grid voltage, FC voltage, and ac current of 7S-5L-ANPC inverter, as shown in Fig. 19, respectively. In this case, the measured peak-to-peak FC voltage ripple is reduced to 1.9 V (= 1.9 V/100 V = 1.9%). The inverter produces good quality current waveform without distortion. The grid voltage leads the output current by 25.8°. The inverter still produces good quality current waveform without distortion. The measured THD value of output current is still 1.6%. Fig. 20 shows two dc-link capacitors voltages, FC voltage, and output current. Same as waveforms of DC-link capacitors voltages in unity PF, the measured peak-to-peak DC-link capacitor ripple voltage is 11.4 V (= 11.4 V/200 V = 5.7%).

In order to testify the effectiveness of T_7 current stress analysis, the experimental verification under 0.9 PF condition (capacitive) in four cases is done. The results are shown in Figs. 21–24, respectively. As can be observed, the T_7 current stress in case 1 is the lowest, which is consistent with the earlier analysis and simulation results.

IX. Conclusion

In this paper, a novel 7S-5L-ANPC inverter topology has been proposed. As compared with the conventional 5L-ANPC inverter, it requires seven active switches for single phase and a low current rating switch can be selected for the seventh switch under high PF situation. The operating principles and switching states are presented. The detailed comparison between the proposed topology and the conventional 5L-ANPC topologies in terms of voltage stress and efficiency is made. The specific

modulation strategy of 7S-5L-ANPC inverter under reactive power operation has been proposed. Computer simulation and experimental prototype based on a single phase 1 kVA prototype have been carried out in unity power factor condition and reactive power condition. The validity and advantages of the proposed topology and modulation method are demonstrated.

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