Industrial Inverter Current Sensing With Three Shunt Resistors: Limitations and Solutions

Zhendong Zhang, *Member, IEEE*, David Leggate, *Member, IEEE*, and Takayoshi Matsuo, *Member, IEEE*

***Abstract*—As inverter powered variable speed drives become popular and technically mature, cost control becomes the core competence for inverter manufacturers. Under minimum performance requirement specifications, the inverter is tailored in every aspect, from the main power device to various sensors to enhance its competitiveness. This paper mainly focuses on various issues associated with the downgrade of current sensors from standard Hall sensor to shunt resistors. The limitation of current sensing by shunt resistors is reviewed and method to expand the maximum achievable modulation index on the vector plane is implemented. Experiments are conducted to verify the analysis and to validate the effectiveness of the reconstruction algorithm.**

***Index Terms*—Current reconstruction, feedback shunts, modulation index (MI), pulse width modulation (PWM) pulse expansion, sampling moment shift.**

I. Introduction

CURRENT information is desired for controlling and monitoring electrical and electronics devices. Various current sensing methods, such as Hall effect sensors, current transforms, shunts, Rogowski coils, and magnetoresistance effect sensors have been developed and reviewed in [1] and [2]. In industrial motor drive, Hall effect sensor is the standard, most efficient, and reliable choice for current sensing because of its high accuracy, hassle-free maintenance, and fully isolated structure, especially in certain safety-critical applications. During recent years, current reconstruction techniques using single resistor on dc bus are widely applied in those low-end small horse-power drives, targeting cost reduction, smaller and flexible package sizes. Industrial drives rarely show too much interest on this mainly because of performance and safety considerations. However, as cost control evolves to be a more important competitive factor for low end industrial drives, current reconstruction through shunt resistors has been adopted gradually. Three shunts on the lower arms are used rather than single shunt on negative dc bus to balance the performance and cost. Algorithm development is necessary to meet the performance and safety requirements.

In literatures, there has been significant interest for reconstructing of phase current using only a single dc shunt resistor [3]–[12]. While, three shunts scheme does not attract too much research interest since the three-phase currents are measurable naturally without applying any special reconstruction techniques at low MI [13]. However, current sensing with three shunt resistors could be problematic at high MI. Patent [14] and paper [15] expand the measurable region by eliminating sampled current from the phase with largest instantaneous voltage compare value. This is straight forward but can only expand the measurable region to a certain extent. In [16]–[18], Parasiliti *et al.* further sketch the immeasurable region on the voltage vector plane and propose to modify the command voltage vector when the current is immeasurable and compensate afterwards. Current becomes immeasurable only when the command voltage stretches to its maximum boundary. Very limited space is available to insert another compensation vector. Moreover, the compensation, targeting to reduce output current harmonics, can be less meaningful since pulse dropping occurs when voltage vector touches its boundary. The pulse dropping associated current harmonics can be overwhelming. In [19], a current observer is employed to estimate the current when more than two-phase currents are immeasurable, but this method relies on the accuracy of system parameters and the extra feedback loop could be troublesome in certain scenario.

In this paper, the general limitation of shunt current sensing is reviewed in Section II. Then, the strict prediction of the highest achievable MI at each modulation stages are explored in Section III. In Section IV, by shifting the current sampling moment or expanding PWM pulse, a further increasing of the MI is attainable with minimum processor overhead. Finally, a complete current sensing scheme on the voltage vector plane is presented and experimental results are used to validate the analysis and the solutions.

II. Inverter Topology and Current Sampling

A. Shunt Resistor Topology and PWM Configuration

Three common shunt current reconstruction solutions for a general three-phase inverter are shown in Fig. 1. Similar to traditional Hall sensors, the shunt resistor could be configured in series with the output phase lines (solution a). Supplemental power supply and voltage isolation are needed, which mitigates its financial advantage. An alternative scheme is to relocate these three shunt resistors to be in series with power devices on lower legs (solution b). Single shunt resistor inserted in negative dc bus is the most cost-efficient solution (solution c). This requires specifically PWM pattern in order to extract the current information, which may be intolerable for some of the applications.

Manuscript received February 9, 2016; accepted July 18, 2016. Date of publication August 1, 2016; date of current version February 11, 2017. Recommended for publication by Associate Editor F. W. Fuchs.

The authors are with Rockwell Automation, Mequon, WI 53092 USA (e-mail: zhdzhang@gmail.com; dleggate@ra.rockwell.com; tmatsuo@ra.rockwell.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2596778

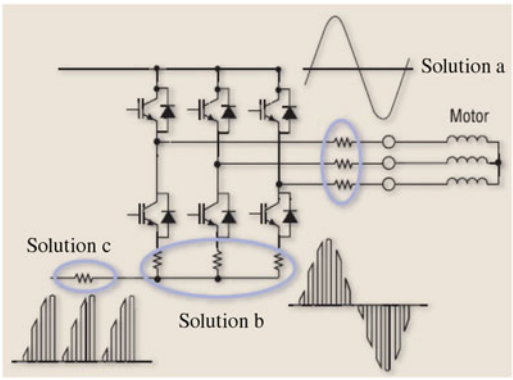


Fig. 1. Shunt resistor location comparison. (a) Three shunts in output phase lines. (b) Three shunts in lower power legs. (c) Single shunt in negative dc bus.

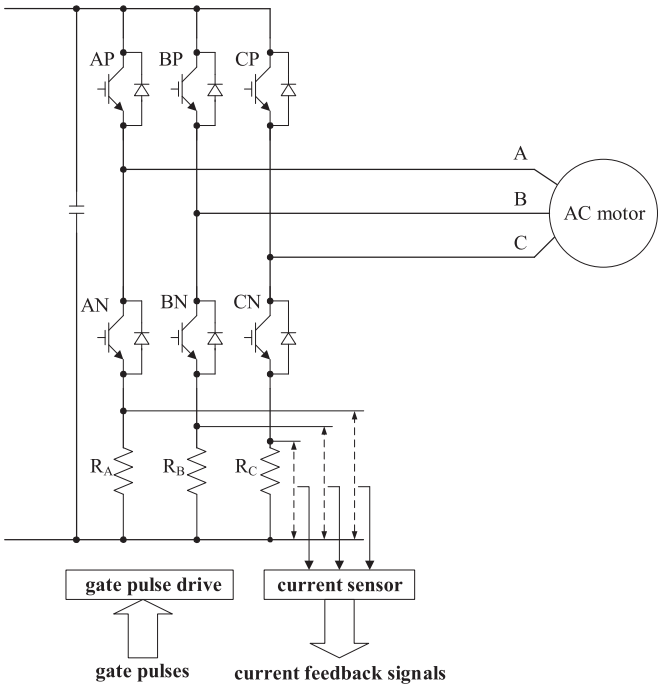


Fig. 2. Standard drive configuration with three shunt resistors.

A standard industrial PWM-VSI inverter with three shunt resistors in series with the lower power devices becomes the basic development setup. A typical inverter topology is shown in Fig. 2.

The most common space-vector PWM modulation (SVPWM) method is applied. The ideal is to reconstruct the three-phase currents by sampling the voltage over those three resistors with least intervention to the original PWM pattern. The sampling of current through the lower leg resistor relies on the length of conducting period of the device around the sampling moment. This sampling window varies as the voltage command changes. The synchronization pattern between PWM voltage pulse updating moment and current sampling moment is also a key factor. Different patterns could result in different control performances mainly because of potential delay associated. Generally, the sampling moment and pulse updating moment are stitched together near the carrier valley to

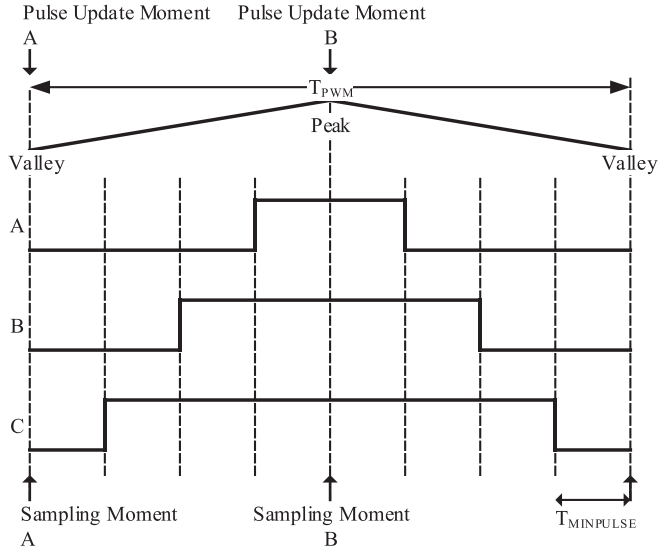


Fig. 3. Carrier triangle and PWM signal in active high mode.

synchronize the DSP processing time period with the PWM period. This moment is tagged-out at moment A in Fig. 3. Therefore, the output PWM pulse voltage is symmetrical about the carrier peak and the pulses on lower legs would be unsymmetrical about the carrier valley. If the carrier peak at moment B is selected, there are significant differences in terms of shunt current reconstruction which will be covered in detail in Section III.

B. Minimum Pulse Width Requirement

For a neutral point floating three-phase drive, at least two-phase currents out of three need to be sampled correctly. However, the voltage over the lower leg shunt resistor is not always available. As the MI becomes higher, the pulse width on the lower device becomes shorter and ultimately current sampling becomes impossible.

This minimum pulse width is determined by several factors:

$T_{\rm dt}$*:* dead time to prevent device shoot-through across the dc bus. The dead-time may or may not affect current sampling depending on current polarity.

$T_{\rm rs}$*:* the time for current to stabilize itself after the lower leg switch turns on. This includes the propagation delay of the PWM signal and the rising and settling time of phase current.

T_{sh}*:* the time delay of the current feedback path, which includes signal conditioning time delay or more specifically filter circuit delay and sampling time delay.

For different applications, the weight ratio of these time delays could be different. Comparing with $T_{\rm rs}$ and $T_{\rm sh}$, the dead time $T_{\rm dt}$, though occupying only a small portion of the total time delay, always results in processing complexity because of its dependence on current polarity. To simplify the design, the dead time is always considered as a portion of the minimum pulse width to eliminate an extra current feedback loop. For the inverter under test, the *RC* filter circuit time constant, being part of $T_{\rm sh}$, presents the longest time delay in the system. Here, a single time constant $T_{\rm MINPULSE}$ equals to the

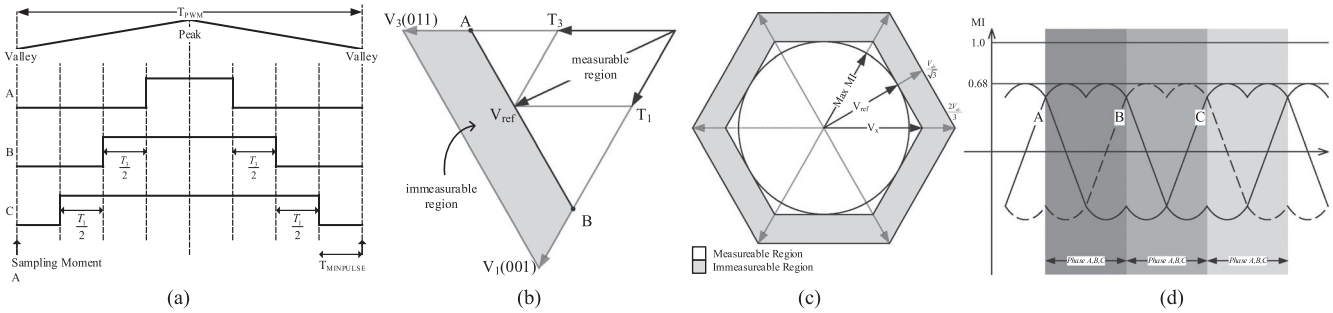


Fig. 4. Maximum achievable modulation at low MI without modification to existing modulation scheme. (a) PWM waveform of voltage vector in time domain. (b) Voltage vectors on boundary line on voltage vector plane. (c) Measurable area on voltage vector plane. (d) Maximum achievable three-phase modulation waveform.

summation of $T_{\rm rs}$, $T_{\rm sh}$, and $T_{\rm dt}$ is defined and used in the whole document to represent the minimum pulse width required for reliable current detection.

Since the lower device conducting time is associated with two consecutive PWM periods, a single MI cannot explain the maximum achievable voltage vector at different MI stages. However, most of the analysis below associates the lower device conducting period with only a single PWM period for easy explanation. While two MIs for consecutive periods are used when a more accurate prediction is required.

III. Current Sampling at Different MI

As mentioned earlier, at different MI stages, the schemes to obtain correct current feedback value are different. In this section, for each stage, the sampling scheme is described and the maximum MI is predicted.

A. MI Period 1: All Three-Phase Currents Capable of Being Sampled

At low MI, the pulse width on lower legs for all the three-phases is long enough for reliable current sampling at the carrier valley. As MI increases, the length of the zero vector shrinks and the length of zero vector (0 0 0) before carrier valley reduces to the minimum pulse width $T_{\rm MINPULSE}$, which is shown in Fig. 4(a). Equivalently, the length of total active vectors should be less than $T_{\rm PWM} - 4 \cdot {\rm T_{MINPULSE}}$. In Fig. 4(b), for any reference vectors on line AB, the active vector length $T_1 + {\rm T_3}$ would always be the same. As line AB moves toward the outer contour of voltage hexagon, the sum of T_1 and T_3 would reach to $T_{\rm PWM} - 4 \cdot {\rm T_{MINPULSE}}$, which becomes the limits for period 1. This limit, translated as maximum MI limit, is shown both on the voltage vector plane and on the three-phase voltage modulation waveform in Fig. 4. Fig. 4(c) shows the measurable and immeasurable region on the whole voltage vector plane. The maximum achievable linear MI is the inscribed circle of the inner hexagon. This maximum MI is also predicted using three-phase modulation waveform shown in Fig. 4(d). This maximum MI "0.68" denoted on the vertical axis is calculated below. The phase labels at the bottom of Fig. 4(d) represent the phases that the current can be sampled.

By referencing to Fig. 4(c) again, the maximum MI is calculated using

$$MI_{\max} = \frac{V_{ref}}{\frac{V_{dc}}{\sqrt{3}}} = \frac{V_x}{\frac{2V_{dc}}{3}} = \frac{T_{\rm PWM} - 4 \times T_{\rm MINPULSE}}{T_{\rm PWM}}. \quad (1)$$

For the inverter under test, $T_{\rm PWM}$ is 250 μs (PWM switching frequency is 4 kHz) and $T_{\rm MINPULSE}$ is chosen to be 20 μs for the actual inverter. Equation (1) gives the maximum achievable modulation index $MI_{\max}$ at 0.68. Apparently, this maximum MI is far from fully utilizing the dc bus.

B. MI Period 2: Only Two-Phase Currents Capable of Being Sampled

As the peak of SVPWM modulation waveform increases beyond the 0.68 shown in Fig. 4(d), only the current from two phases can be sampled at a time. Fortunately, for a neutral point floating system, the third-phase current can always be calculated based on the measurable two-phase currents [13].

In Fig. 4, if reference voltage vector increases further, the PWM waveform becomes the one shown in Fig. 5(a). Phase *C* current cannot be sampled because the length of zero vector before current sampling moment is less than $T_{\rm MINPULSE}$. Phase *B* current is barely measurable since its zero vector length before sampling moment equals $T_{\rm MINPULSE}$. This is reflected on the voltage vector plane in Fig. 5(b). Line AB represents the trajectory of voltage vector where phase *B* has fixed zero vector length before current sampling moment (Equivalently fixed duty ratio)

$$T_B = T_3 + \frac{T_0}{2} \quad (2)$$

$$T_{\rm PWM} = T_1 + T_3 + T_0 \quad (3)$$

$$T_B = \frac{T_{\rm PWM}}{2} + \frac{T_3 - T_1}{2} \quad (4)$$

$$T_3 - T_1 = 2T_B - T_{\rm PWM}. \quad (5)$$

Equations (2)–(5) calculate the condition when phase *B* has a fixed duty ratio T_B. Since T_B and $T_{\rm PWM}$ are constants, $T_3 - {\rm T_1}$ which is the length of vector $\overrightarrow{OB}$, would also be a constant. By projecting a line from point B toward the contour edge of hexagon, any voltage reference vector on line AB has exact the

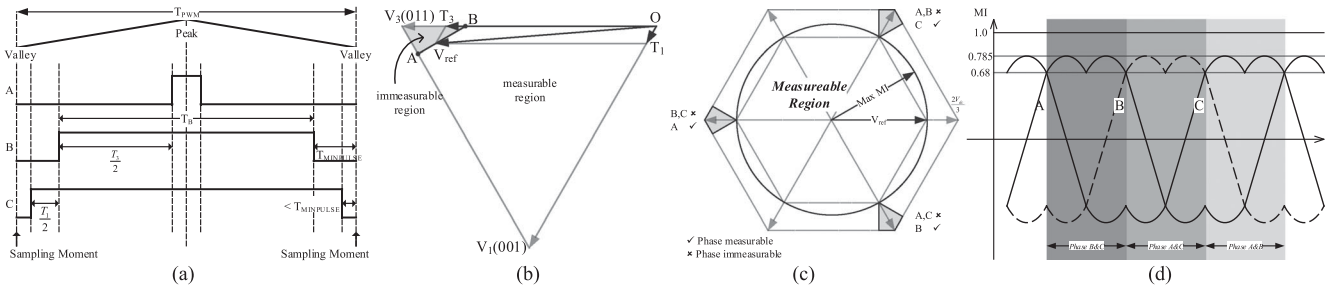


Fig. 5. Maximum achievable MI by two-phase current selectively sampling. (a) PWM waveform of voltage vector in time domain. (b) Voltage vectors on boundary line on voltage vector plane. (c) Measurable area on voltage vector plane. (d) Maximum achievable three-phase modulation waveform.

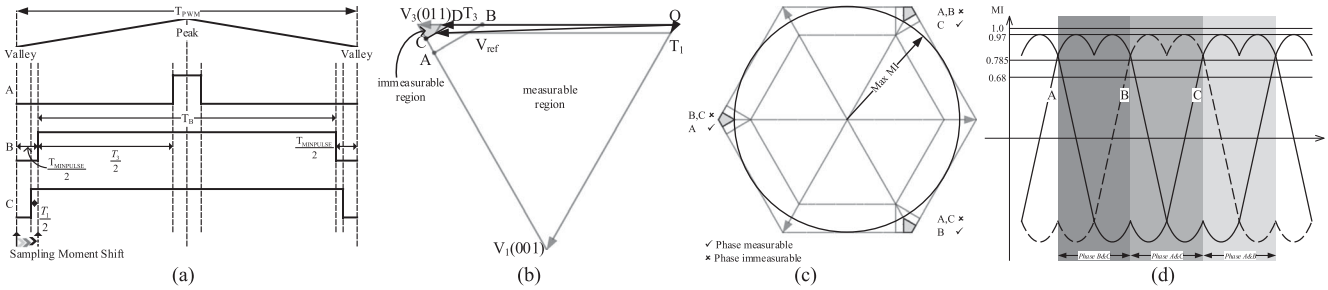


Fig. 6. Maximum achievable MI by current sampling moment shift. (a) Voltage vectors on PWM waveform in time domain. (b) Voltage vectors on boundary line on voltage vector plane. (c) Measurable area on voltage vector plane. (d) Maximum achievable three-phase modulation waveform.

same phase *B* on time T_B. Current becomes immeasurable when voltage vector falls inside the immeasurable triangle region. By examining all the six sectors on voltage vector plane, the immeasurable region is plotted in Fig. 5(c).

Since the output voltage vector determines the phases for correct current sampling, the applicable feedback current would alternate between different phases as the voltage vector rotating continuously on the vector plane shown in Fig. 5(d).

Similar to the MI calculation in Section III-A, the maximum MI can be calculated as

$$\frac{V_{\rm ref}}{\frac{2}{3}V_{\rm dc}} = \frac{T_{\rm PWM} - 4 \times T_{\rm MINPULSE}}{T_{\rm PWM}} \tag{6}$$

$$MI = \frac{V_{\rm ref}}{\frac{V_{\rm dc}}{\sqrt{3}}} = \frac{2}{\sqrt{3}} \frac{T_{\rm PWM} - 4 \times T_{\rm MINPULSE}}{T_{\rm PWM}}. \tag{7}$$

Using the same configuration parameters, the maximum modulation index $MI_{\max}$ is 0.785. The voltage limit circle corresponding to this maximum MI is plotted in Fig. 5(c).

Comparing to that in Section III-A, this maximum MI increases considerably. If comparing Fig. 5(a) with Fig. 4(a), the immeasurable region shrinks from the outer band of hexagon to only three corners. However, the maximum achievable MI is still limited by inner vertex of immeasurable quadrilaterals.

C. MI Period 3: Only One-Phase Current Capable of Being Sampled

When the MI needs further to be expand to near the outer contour of the voltage hexagon, two phase out of three may lose current detection capability. It is essential to adopt a new method when voltage vector falls in these regions.

1) Phase Current Measurement Based on Sampling Moment Shift: As long as two-phase current sampling at triangle valley is no longer feasible, the sampling moment can be repositioned since the $T_{\rm MINPULSE}$ is more a confinement to limit the pulse on lower leg before the sampling moment. By shifting the pulse sampling moment rightward, extra sampling area can be created for reliable two-phase current sampling. Fig. 6(a) depicts the PWM waveform and sampling moment shift length. The immeasurable region shrinks further by pushing the boundary from line AB in Fig. 5(b) to line CD in Fig. 6(b). It is clearly shown in Fig. 6(c) that the immeasurable region shrinks to only one fourth of that at period 2 in Section III-B above.

The shift distance should be strictly calculated to ensure the sampling moment is still within the pulse range on lower legs. The detailed calculation of shift distance is presented in Section IV.

Here, the maximum modulation is calculated again using the same criterion as in Section III-A and III-B

$$\frac{V_{\rm ref}}{\frac{2}{3}V_{\rm dc}} = \frac{T_{\rm PWM} - 2 \times T_{\rm MINPULSE}}{T_{\rm PWM}} \tag{8}$$

$$MI = \frac{V_{\rm ref}}{\frac{V_{\rm dc}}{\sqrt{3}}} = \frac{2}{\sqrt{3}} \frac{T_{\rm PWM} - 2 \times T_{\rm MINPULSE}}{T_{\rm PWM}}. \tag{9}$$

By inserting all the parameters, the maximum achievable modulation index $MI_{\max}$ becomes 0.97.

The calculations above still rely on the initial presumption that only a single MI for one PWM period is used during deduction. When this modulation limits are expanded close to the contour of

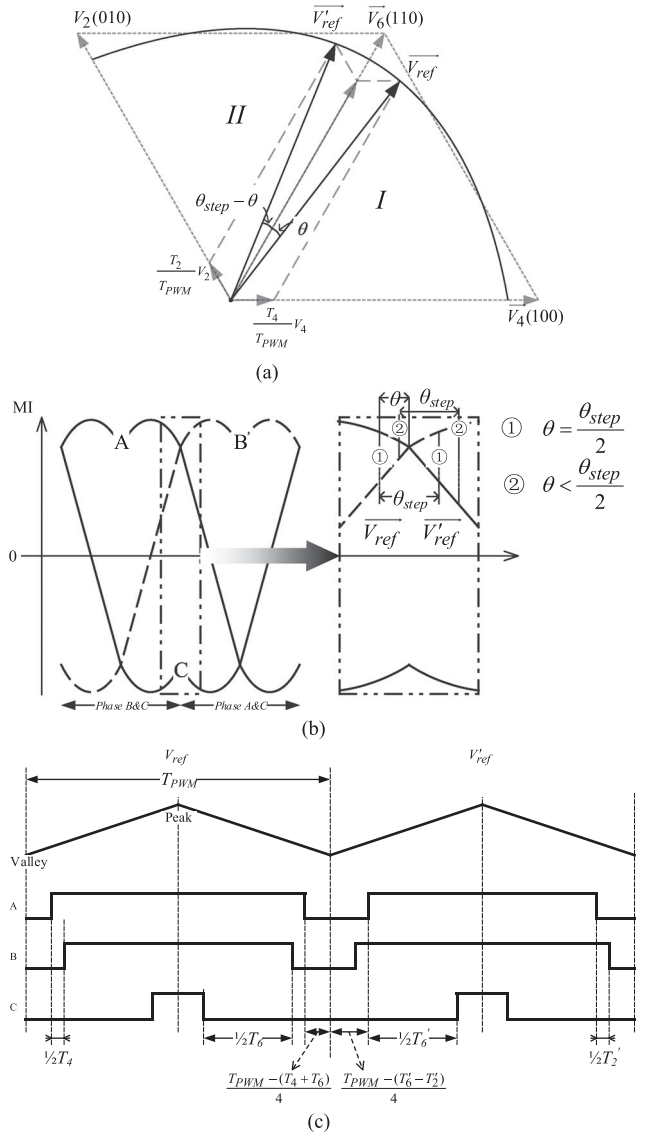


Fig. 7. Detailed analysis of maximum MI by referencing to two rotating vectors near immeasurable region. (a) Example voltage vectors on vector plane. (b) Example voltage vectors on three-phase modulation waveform. (c) Example voltage vectors on PWM waveform in time domain.

voltage hexagon, the error of using only a single MI to estimate the limit becomes prominent. A more accurate analysis by using two consecutive MI values is exerted below to predict the limit precisely. The asymmetry of three-phase pulses on the lower leg about the carrier valley is utilized to shift the sampling moment and measure the current.

Generally, the drive runs at rated output frequency (60 Hz in this case) with almost rated output voltage. The amount of angle the fundamental voltage vector sweeps over one PWM period (250 μs) can be defined as $\theta_{\rm step}$ and is equal to 5.4° in reference to Fig. 7(a).

Referencing to the modulation waveform in Fig. 7(b), the moment that current sampling is most likely to be affected is the crossing point of the modulation waveform of any of the two phases on the positive side. One example is the transition from $\overrightarrow{V_{\rm ref}}$ in sector I to $\overrightarrow{V'_{\rm ref}}$ in sector II in Fig. 7(a). Fig. 7(c) depicts these two vectors using PWM waveform in time domain and the duration of all the vectors are tagged out. The maximum MI is thus predicted by the following calculation.

$\overrightarrow{V_{\rm ref}}$ is a vector synthesized by active vector $\overrightarrow{V_4}$ and $\overrightarrow{V_6}$. Their corresponding vector length T_4 and T_6 are calculated as

$$V_{\rm ref}\cos(\theta) - \frac{V_{\rm ref}\sin(\theta)}{\tan 60^\circ} = \frac{T_6}{T_{\rm PWM}}V_6 \tag{10}$$

$$V_{\rm ref}\cos(60^\circ - \theta) - \frac{V_{\rm ref}\sin(60^\circ - \theta)}{\tan 60^\circ} = \frac{T_4}{T_{\rm PWM}}V_4. \tag{11}$$

The θ in above equations is defined as the angle between $\overrightarrow{V_{\rm ref}}$ and active vector $\overrightarrow{V_6}$ shown in Fig. 7(a). As for SVPWM modulation, one PWM period is made up of two active vectors and two zero vectors. As the PWM period is already know, the duration of active vector would be

$$T_{\rm PWM} = T_4 + T_6 + T_0 \tag{12}$$

$$T_4 + T_6 = \left(\frac{\sqrt{3}}{2}\cos\theta + \frac{1}{2}\sin\theta\right) \times T_{\rm PWM} \times MI. \tag{13}$$

In (13), the active vector duration is associated with voltage vector angle, MI, and PWM period. The similar calculation is applied to vector $\overrightarrow{V'_{\rm ref}}$

$$V'_{\rm ref}\cos(\theta_{\rm step} - \theta) - \frac{V'_{\rm ref}\sin(\theta_{\rm step} - \theta)}{\tan 60^\circ} = \frac{T'_6}{T_{\rm PWM}}V_6 \tag{14}$$

$$V'_{\rm ref}\cos(60^\circ - (\theta_{\rm step} - \theta)) - \frac{V'_{\rm ref}\sin(60^\circ - (\theta_{\rm step} - \theta))}{\tan 60^\circ}$$

$$= \frac{T'_2}{T_{\rm PWM}}V_2 \tag{15}$$

$$T_{\rm PWM} = T'_2 + T'_6 + T_0 \tag{16}$$

$$T'_6 - T'_2 = \left(\frac{\sqrt{3}}{2}\cos(\theta_{\rm step} - \theta) - \frac{3}{2}\sin(\theta_{\rm step} - \theta)\right) \times T_{\rm PWM} \times MI'. \tag{17}$$

If $\theta < \frac{\theta_{\rm step}}{2}$ (② in Fig. 7(b)), phase *A* is with medium pulse width and the total length of pulse on lower leg is calculated as

$$T_{\rm mid} = \frac{T_{\rm PWM} - (T_4 + T_6)}{4} + \frac{T_{\rm PWM} - (T'_6 - T'_2)}{4} = (2 - (a + \sqrt{3}b)MI)\frac{T_{\rm PWM}}{4} \tag{18}$$

where *a* and *b* in (18) can be expressed as

$$a = \frac{\sqrt{3}}{2}\cos\theta + \frac{1}{2}\sin\theta, b = \frac{1}{2}\cos(\theta_{\rm step} - \theta) - \frac{\sqrt{3}}{2}\sin(\theta_{\rm step} - \theta). \tag{19}$$

The θ is an arbitrary value ranging from 0 to $\theta_{\rm step}$ when $\overrightarrow{V_{\rm ref}}$ rotates to $\overrightarrow{V'_{\rm ref}}$. However, the maximum achievable MI becomes the smallest when $\theta = \frac{\theta_{\rm step}}{2}$. This MI can be calculated

by simplifying (18) as

$$\left(\frac{\sqrt{3}}{4}\cos\frac{\theta_{\text{step}}}{2}-\frac{1}{4}\sin\frac{\theta_{\text{step}}}{2}\right)MI<\left(\frac{1}{2}-\frac{T_{\text{MINPULSE}}}{T_{\text{PWM}}}\right) \tag{20}$$

So, the maximum MI is limited to

$$MI<\frac{1}{\cos(\frac{\theta}{2}+30^{\circ})}\times\left(1-\frac{2T_{\text{MINPULSE}}}{T_{\text{PWM}}}\right). \tag{21}$$

Using the same parameter for T_{PWM} and T_{MINPULSE} as previous, its maximum achievable modulation index $MI_{\max}$ is calculated as 0.998. This is very close to unity value which is the boundary of linear modulation region.

On the contrary, the most aggressive MI happens when $\theta=0$ as shown in,

$$\left(\frac{\sqrt{3}}{8}+\frac{\sqrt{3}}{8}\cos\theta_{\text{step}}-\frac{3}{8}\sin\theta_{\text{step}}\right)MI<\frac{1}{2}-\frac{T_{\text{MINPULSE}}}{T_{\text{PWM}}}. \tag{22}$$

The maximum achievable MI reaches 1.05857, slightly larger than linear modulation boundary.

If all above strategies at different MI level are adopted, the drive can fully utilize the bus voltage if overmodulation operation is not mandatory. While PWM pulse shaping is mandatory if operation in overmodulation region is required.

2) Phase Current Measurement Based on PWM Pulse Edge Shift: If drive enters overmodulation region, the pulse width of the phase with medium pulse width on lower leg power device will be narrower than T_{MINPULSE} at a certain period of the fundamental cycle. Reliable two-phase current sampling with original PWM pattern becomes impossible. PWM pulse edge shift is inevitable in this case. The detailed analysis will be presented in detail in Section IV.

IV. Proposed Solution

Before in-depth exploration of the algorithm, the synchronization of the timing of the actual PWM output waveform with reference to the timing of control algorithm execution period needs to be examined since any execution step mismatch may cause the failure of the proposed solution. The control algorithm samples current near the valley of carrier triangle and calculates voltage output in that PWM period, which is used to update the PWM waveform for the next PWM period.

Fig. 8 shows the algorithm executions cycle with the proposed solution. In PWM period 1, for instance, the PWM pattern is determined in the previous PWM cycle and the future implemented PWM pattern in period 2 is known at the time the proposed algorithm executes. The necessary modification is performed either by shifting the current sampling moment rightward or by modifying PWM pulse edge in PWM period 2 to gain correct current information.

Three criterions are epitomized as the operation guidelines when modifications are carried out:

1) shift the sampling moment as little as possible because the shifting of sampling moment can squeeze the available processing time in each PWM period;

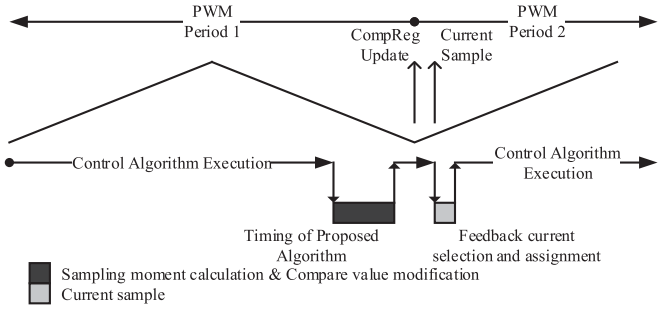


Fig. 8. PWM period and algorithm timing.

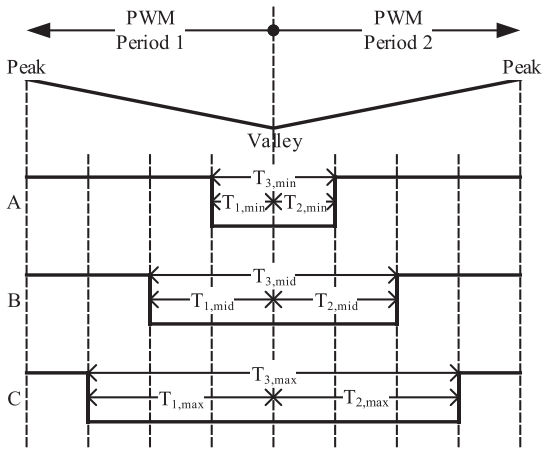


Fig. 9. Typical PWM pattern.

2) avoid sampling current at one phase, while another phase is switching to reduce sampling noise;
3) avoid the modification of the PWM pattern or always choose the method with smallest modification.

Per investigation in Section III, the sampling moment shift algorithm is implemented when the MI falls inside certain area. The exact start and end points are examined dynamically online by looking at the PWM pattern.

Fig. 9 is made up of half the PWM period 1 and half the PWM period 2. In period 1, its PWM pattern is determined by calculation one PWM period earlier and the algorithm running during this period is to calculate the PWM pattern for PWM period 2. With all the three-phase lower leg conducting time periods known, they are ranked as $T_{1,\max}$, $T_{1,\text{mid}}$, $T_{1,\min}$ by comparing the individual pulse width. The currents are about to be sampled at the valley of carrier triangle in Fig. 9. Current is always detectable for the phase with maximum pulse width $T_{1,\max}$, since it is always larger than T_{MINPULSE}. The current from the phase with minimum pulse width $T_{1,\min}$ may or may not be detectable. The phase with medium pulse width $T_{1,\text{mid}}$ is the most important. If $T_{1,\text{mid}}$ is larger than the minimum required time T_{MINPULSE}, the current can be sampled directly. On the contrary, $T_{1,\text{mid}}$ could be smaller than T_{MINPULSE} as MI increases. The moment when $T_{1,\text{mid}}$ equals to T_{MINPULSE} is the starting point of implementing the sampling moment shift algorithm.

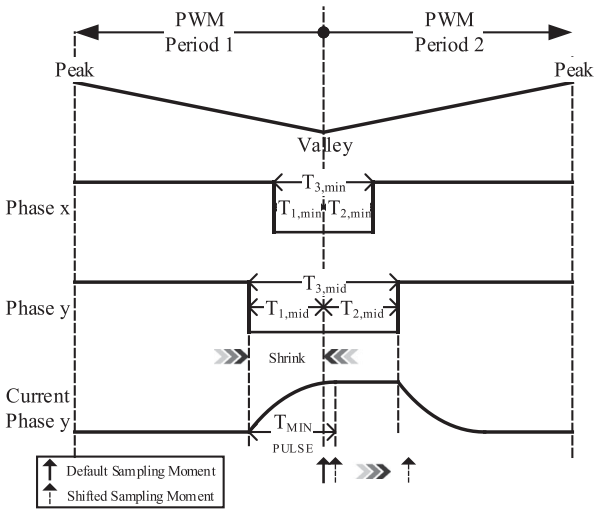


Fig. 10. Sampling moment shift.

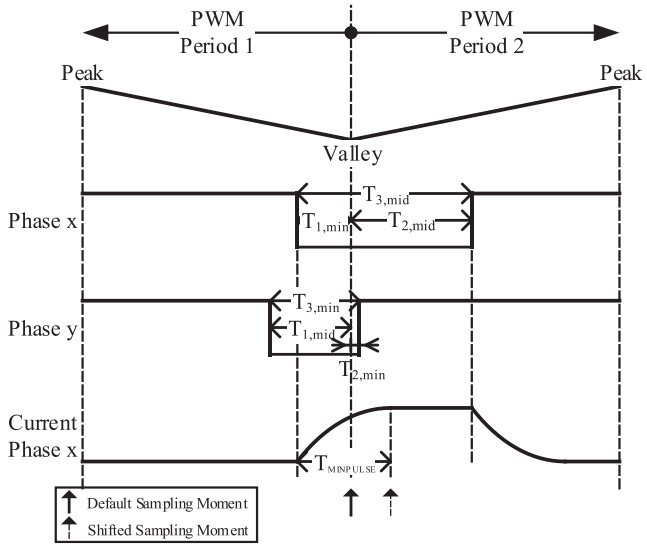


Fig. 11. Current sampling by sampling moment shift.
Note: the pulse width is scaled up intentionally for clear explanation and easier understanding. The original scale is much smaller. The asymmetry of the pulse about the valley is because the new voltage command for PWM period 2 is updated at the valley. This would be the same for all the figures in this section.

Fig. 10 depicts the sampling moment shift algorithm. The default carrier valley aligned sampling moment denoted using solid arrow line is shifted rightward to the moment denoted with dash arrow line. As the MI keeps increasing, the shift distance becomes larger due to the shrink of $T_{1,\mathrm{mid}}$. Eventually, the sampling moment after shift may reside outside of right pulse edge and the sampled current is no longer valid. In this case, the total low leg conducting period, which straddles over two PWM periods, needs to be investigated to further determine the correct sampling phase and appropriate shift distance.

When observing the whole pulse width, $T_{3,\mathrm{min}}$, $T_{3,\mathrm{mid}}$ in Fig. 10, the minimum and medium pulse widths may not necessarily associate with the same phase as compared with $T_{1,\mathrm{min}}$, $T_{1,\mathrm{mid}}$. Hence, two separate cases need to be considered.

A. Case I: Mid and Min Pulses are Associated With Same Phases

If $T_{1,\mathrm{mid}}$ and $T_{3,\mathrm{mid}}$ are associated with the same phase, the current is sampled from this exact phase. This is further separated into two different situations: $T_{3,\mathrm{mid}} > T_{\mathrm{MINPULSE}}$ and $T_{3,\mathrm{mid}} < T_{\mathrm{MINPULSE}}$. If $T_{3,\mathrm{mid}}$ is larger, which means the total pulse width is larger than the minimum sampling pulse requirement, then the sampling moment is shifted by the length $T_{\mathrm{MINPULSE}} - \mathrm{T}_{1,\mathrm{mid}}$. However, if it is smaller, the PWM pulse edge shift method mentioned in Section III-B will take charge of that. Eventually, $T_{3,\mathrm{mid}}$ would be made equal to T_{MINPULSE}.

B. Case II: Mid and Min Pulses are Associated With Different Phases

If $T_{1,\mathrm{mid}}$ and $T_{3,\mathrm{mid}}$ are associated with different phases, three different cases can be separately considered:

1) $T_{3,\mathrm{min}} > T_{\mathrm{MINPULSE}}$ and $T_{3,\mathrm{mid}} > T_{\mathrm{MINPULSE}}$;
2) $T_{3,\mathrm{min}} < T_{\mathrm{MINPULSE}}$ and $T_{3,\mathrm{mid}} > T_{\mathrm{MINPULSE}}$;
3) $T_{3,\mathrm{min}} < T_{\mathrm{MINPULSE}}$ and $T_{3,\mathrm{mid}} < T_{\mathrm{MINPULSE}}$;

For case 1, both the minimum pulse $T_{3,\mathrm{min}}$ and medium pulse $T_{3,\mathrm{mid}}$ are larger than T_{MINPULSE}, current can be detected by shifting the sampling moment in reference to either one of them. The shifting distance would be $T_{\mathrm{MINPULSE}} - \mathrm{T}_{1,\mathrm{mid}}$ in reference to $T_{3,\mathrm{min}}$ and would be $T_{\mathrm{MINPULSE}} - \mathrm{T}_{1,\mathrm{min}}$ in reference to $T_{3,\mathrm{mid}}$. Since $T_{1,\mathrm{mid}} > T_{1,\mathrm{min}}$, the sampling moment would be shifted in reference to $T_{3,\mathrm{min}}$, since this complies with criterion 1 above.

For case 2, only $T_{3,\mathrm{mid}}$ is larger than T_{MINPULSE}, and sampling shift can only be implemented in reference to $T_{3,\mathrm{mid}}$, which is $T_{\mathrm{MINPULSE}} - \mathrm{T}_{1,\mathrm{min}}$. Fig. 11 depicts this situation.

For case 3, none of the pulses for both phases are long enough for reliable current sampling when merely applying sampling moment shift algorithm. One of the pulse needs to be widened. Here comes the dilemma. If $T_{3,\mathrm{min}}$ pulse is selected to be modified, the pulse on the lower leg is extended by time $T_{\mathrm{MINPULSE}} - \mathrm{T}_{3,\mathrm{min}}$, and the sampling moment is shifted rightward by $T_{\mathrm{MINPULSE}} - \mathrm{T}_{1,\mathrm{mid}}$. If $T_{3,\mathrm{mid}}$ pulse is modified, the pulse is extended by time $T_{\mathrm{MINPULSE}} - \mathrm{T}_{3,\mathrm{mid}}$, and the sampling moment is shifted by $T_{\mathrm{MINPULSE}} - \mathrm{T}_{1,\mathrm{min}}$. Since $T_{\mathrm{MINPULSE}} - \mathrm{T}_{3,\mathrm{min}}$ is larger than $T_{\mathrm{MINPULSE}} - \mathrm{T}_{3,\mathrm{mid}}$ as for pulse-width expansion length and $T_{\mathrm{MINPULSE}} - \mathrm{T}_{1,\mathrm{mid}}$ is smaller than $T_{\mathrm{MINPULSE}} - \mathrm{T}_{1,\mathrm{min}}$ as for sampling moment shift distance, the minimization of modification to the existing vector and the minimization of sampling moment shift are conflicted with each other. The minimization of voltage vector is prioritized here because it can cause adverse effect to the total harmonics of output current.

Taking Fig. 12 as an example, Pulse x with the medium length of total pulse is modified to expand conducting time of power device on lower leg.

In [15]–[17], the analysis of expansion of measurable area is all based on voltage vectors because compensation needs voltage information thereafter. While, all the manipulation in this paper is purely based on PWM pulse width, easier to analyze and implement.

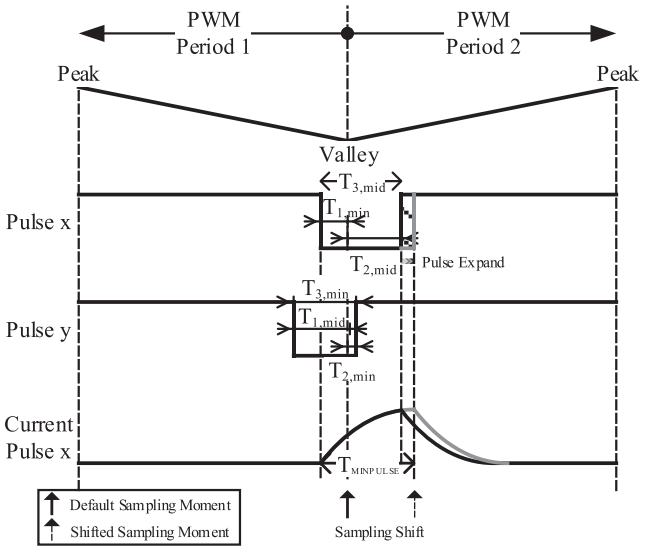


Fig. 12. Current sampling by PWM pulse edge modification.

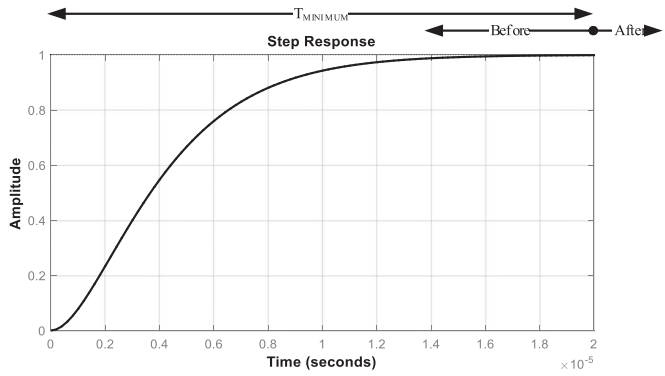


Fig. 13. Current feedback filter step response.

Adjustment of pulse width affects the output voltages which can result in current harmonics. If the PWM pulse is left intact, the sampled current also contains harmonics due to wrong sampling moment. An optimized selection based on minimum distortion is theoretically achievable but practically unnecessary because this only happens at three corners on the voltage vector plane in the overmodulation region. The added harmonics caused by PWM pulse edge shift may not have a noticeable effect.

V. Experimental Verification

All the predictions and analysis are verified through experiments.

The simplest V/Hz control without any load is used to verify the prediction of these theoretical maximum MI for sampling methods at each MI stages in Section III. Fig. 13 shows the step response of the current feedback filter for $T_{\mathrm{MINIMUM}}(20\ \mu\mathrm{s})$. Apparently, the amplitude of any points on the curve right before, at, or after T_{MINIMUM} does not show much difference. Hence, in Table I, selected MI values away from predicted MI boundaries in section III are used to clearly show the effect.

For the sampled current of each phase, only two corner sectors apart 120° on voltage vector plan could be impacted, no dominant harmonic can be gauged to determine the waveform quality. The total harmonic distortion (THD) serves as the comparison criterion.

The collected data are shown in Table I below. For each row at the same modulation stage, the THD of feedback current waveform increase as MI goes beyond its predicted max presented in Section III above. While for each column with same MI, the THD drops as the sampling strategy changes at different stage.

The improvement of current quality can be easily recognized from the feedback waveform. Fig. 14 presents the measured current waveforms from the same test as in Table I. Comparing Fig. 14(b) to (a), the quality of feedback current waveform is improved by adopting the sampling moment shift method. Now comparing Fig. 14(d) to (c), the same conclusion can be drawn after adopting the PWM edge shift method.

TABLE I
THD of Feedback Current at Different MI Stages

Modulation Stage	Modulation Index 0.6	0.73	0.98	1.02
III.A	2.24%	5.35%		
III.B		2.22%	3.64%	
III.C			2.48%	8.83%
III.D				3.19%

III.A: Three-phase currents sampling;
III.B: Two-phase currents sampling;
III.C: Two-phase currents sampling with sampling moment shift;
III.D: Two-phase currents sampling with sampling moment shift and PWM edge shift.

Finally, full load test are conducted on two different power rating 480-V standard industrial drives. Since bootstrap circuit is used to drive the inverter upper leg, the maximum MI is set at unity to prohibit six-step operation.

The first test is carried out on a 10HP drive with basic V/Hz control. So, the sampled current is used only for monitoring and does not affect the control. The drive is set to run at 60 Hz.

Fig. 15 shows the phase current waveform on oscilloscope as well as sampled data from microcontroller. The sampled current has glitches on it. After applying these methods in Section III, the glitches on sampled current in Fig. 15(a) disappears and the sampled current is tracking the actual current tightly as shown in Fig. 15(b).

The second test is conducted on a 1HP drive with current closed-loop field orientated control. The drive is commanded to run at 90 Hz which resides in the field weakening region.

Fig. 16(a) shows the two currents. More severe glitches appear on the sampled current compared to that in Fig. 15(a) because the active feedback of the current into control loop

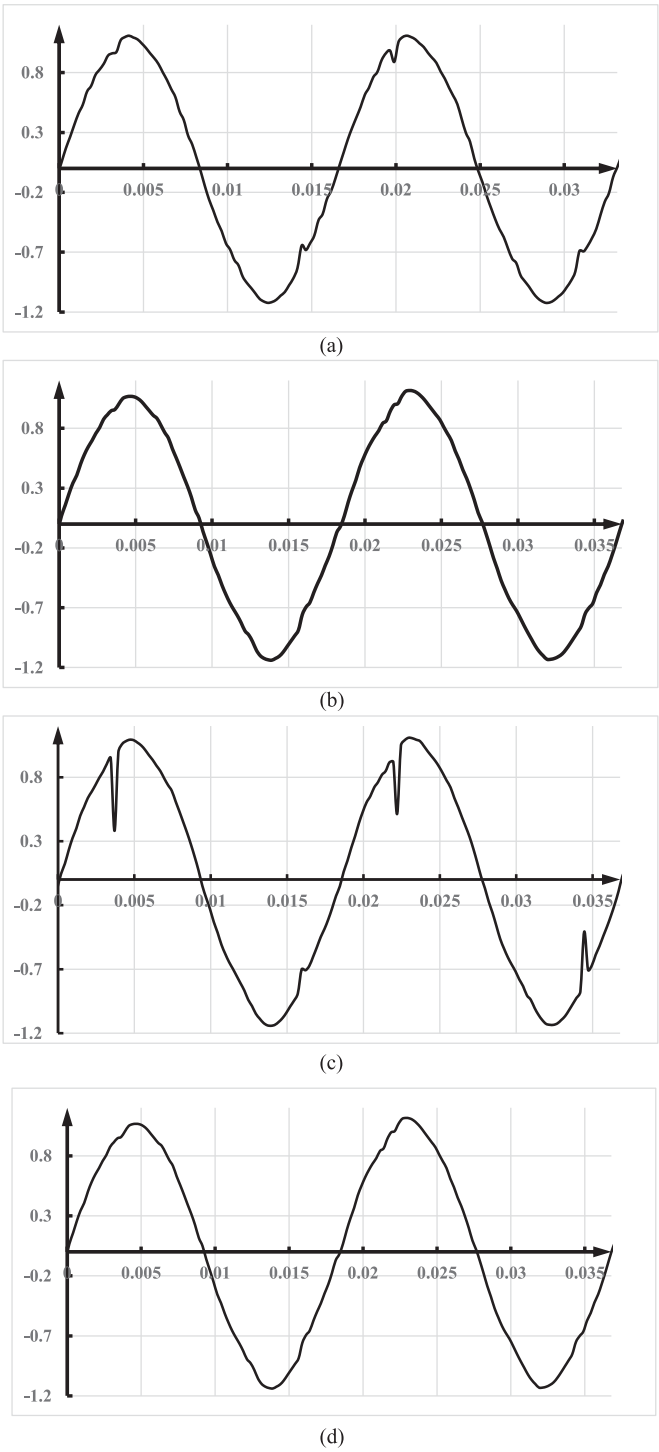


Fig. 14. Current waveform before and after adopting sampling strategy. (a) Current feedback without sampling moment shift when MI is at 0.98. (b) Current feedback with sampling moment shift when MI is at 0.98. (c) Current feedback without pulse edge shift when MI is at 1.02. (d) Current feedback with pulse edge shift when MI is at 1.02.

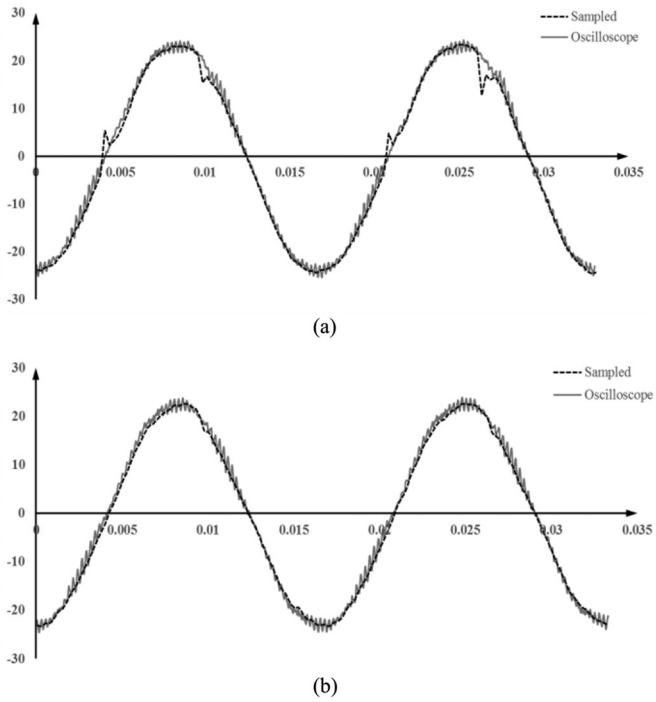


Fig. 15. Phase current in V/Hz mode. (a) Without proposed algorithm. (b) With proposed algorithm.

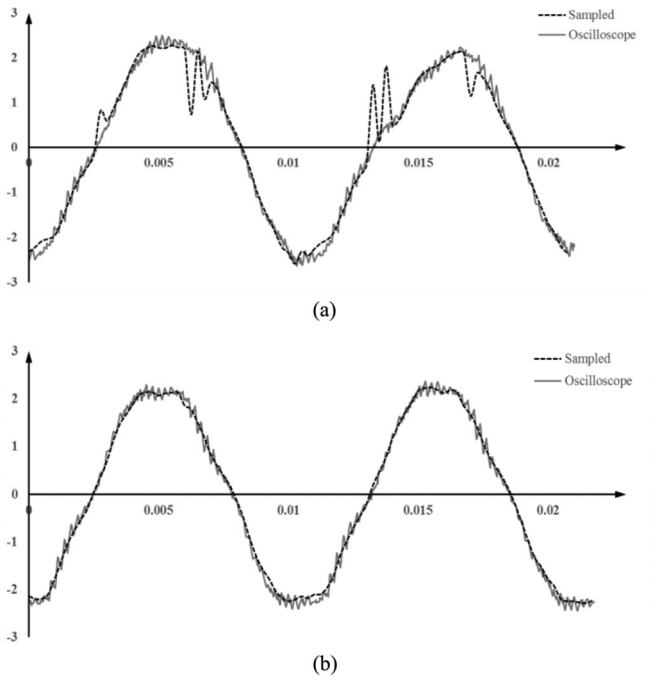


Fig. 16. Phase current in vector control mode. (a) Without proposed algorithm. (b) With proposed algorithm.

can introduce disturbances inside the current loop. Significant torque ripple is observed on the rotor shaft, which can potentially cause mechanical damage. Fig. 16(b) shows significant waveform improvement after switching to these added sampling measures.

VI. Conclusion

In this paper, phase current reconstruction strategies at different MI stages through three shunts on lower legs is investigated.

The limitation of each method at different MI stage is well analyzed and presented by calculating the exact maximum achievable MI.

Solutions at high MI combining both sampling moment shift and PWM pulse expansion methods are examined in detailed by referencing to the specific PWM and sampling pattern.

No-load test is conducted to validate that the feedback current quality degrades when MI goes beyond the predicted maximum. While it recovers when adopting the sampling strategy for that particular MI stage. The improvement of feedback current waveform quality is observed by comparing the waveform without and with all the proposed algorithm at full-load test.

REFERENCES

[1] C. Xiao, L. Zhao, T. Asada, W. G. Odendaal, and J. D. Van Wyk, "An overview of integratable current sensor technologies," in *Proc. 38th Annu. Meet. Ind. Appl. Conf.*, Oct. 2003, vol. 2, pp. 1251–1258.

[2] S. Ziegler, R. Woodward, H.-C. Iu, and L. Borle, "Current sensing techniques: A review," *IEEE Sensors J.*, vol. 9, no. 4, pp. 354–376, Apr. 2009.

[3] J. F. Moynihan, S. Bolognani, R. C. Kavanagh, M. G. Egan, and J. M. D. Murphy, "Single sensor current control of AC servo drives using signal processors," in *Proc. Eur. Conf. Power Electron. Appl.*, 1993, vol. 4, pp. 415–421.

[4] T. C. Green and B. W. Williams, "Derivation of motor line-current waveforms from the DC-link current of an inverter," *Electr. Power Appl., IEE Proc. B*, vol. 136, no. 4, pp. 196–204, Jul. 1989.

[5] Y. Xue, X. Xu, T. G. Habetler, and D. M. Divan, "A low cost stator flux oriented voltage source variable speed drive," in *Proc. IEEE Conf. Rec. Annu. Meet. Ind. Appl. Soc.*, Oct. 1990, vol. 1, pp. 410–415.

[6] F. Blaabjerg, J. K. Pedersen, U. Jaeger, and P. Thoegersen, "Single current sensor technique in the DC-link of three-phase PWM-VS inverters. A review and the ultimate solution," in *Proc. IEEE 31st Conf. Rec. Annu. Meet. Ind. Appl. Conf.*, Oct. 1996, vol. 2, pp. 1192–1202.

[7] F. Blaabjerg and J. K. Pedersen, "A new low-cost, fully fault-protected PWM-VSI inverter with true phase-current information," *IEEE Trans. Power Electron.*, vol. 12, no. 1, pp. 187–197, Jan. 1997.

[8] B. Andersen, T. Holmgaard, J. G. Nielsen, and F. Blaabjerg, "Active three-phase rectifier with only one current sensor in the DC-link," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst.*, 1999, vol. 1, pp. 69–74.

[9] W.-C. Lee, D.-S. Hyun, and T.-K. Lee, "A novel control method for three-phase PWM rectifiers using a single current sensor," *IEEE Trans. Power Electron.*, vol. 15, no. 5, pp. 861–870, Sep. 2000.

[10] W.-C. Lee, T.-K. Lee, and D.-S. Hyun, "Comparison of single-sensor current control in the DC link for three-phase voltage-source PWM converters," *IEEE Trans. Ind. Electron.*, vol. 48, no. 3, pp. 491–505, Jun. 2001.

[11] H. Kim and T. M. Jahns, "Phase current reconstruction for ac motor drives using a dc link single current sensor and measurement voltage vectors," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1413–1419, Sep. 2006.

[12] H. Lu, X. Cheng, W. Qu, S. Sheng, Y. Li, and Z. Wang, "A three-phase current reconstruction technique using single dc current sensor based on TSPWM," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1542–1550, Mar. 2014.

[13] F. Parasiliti, R. Petrella, and M. Tursini, "Low cost phase current sensing in DSP based AC drives," in *Proc. IEEE Int. Symp. Ind. Electron.*, 1999, vol. 3, pp. 1284–1289.

[14] Z. Yu, "Phase current sensor using inverter leg shunt resistor," U.S. Patent 6 529 393 B1, 2003.

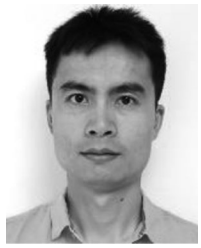
[15] H. Kim, S. Yi, N. Kim, and R. D. Lorenz, "Using low resolution position sensors in bumpless position/speed estimation methods for low cost PMSM drives," in *Proc. 14th Annu. Meet. Rec. Ind. Appl. Conf.*, Oct. 2005, vol. 4, pp. 2518–2525.

[16] F. Parasiliti, R. Petrella, and M. Tursini, "A novel solution for phase current sensing in PWM-VSI based AC drives," in *Proc. 9th Eur. Conf. Power Electron. Appl.*, 2001.

[17] B.-G. Cho, J.-I.Ha, and S.-K. Sul, "Analysis of the phase current measurement boundary of three shunt sensing PWM Inverters and an expansion method," *J. Power Electron.*, vol. 13, no. 2, pp. 232–242, Mar. 2013.

[18] B.-G. Cho, J.-I.Ha, and S.-K. Sul, "Voltage injection method for boundary expansion of output voltages in three shunt sensing PWM inverters," in *Proc. IEEE 8th Int. Conf. Power Electron. ECCE Asia*, May/Jun. 2011, pp. 411–415.

[19] S. Chi, X. Wang, Y. Yuan, Z. Zhang, and L. Xu, "A current reconstruction scheme for low-cost PMSM drives using shunt resistors," in *Proc. IEEE 22nd Annu. Appl. Power Electron. Conf.*, Mar. 2007, pp. 1701–1706.



Zhendong Zhang (S'09–M'14) received the B.S. degree in electrical engineering from Southeast University, Nanjing, China, in 2006. He was a Graduate Student with Tsinghua University from 2006 to 2008. From 2008 to 2013, he was receiving the Ph.D. degree from the Department of Electrical Engineering, The Ohio State University, Columbus, OH, USA.

He was an Intern with United Technology Research Center in 2013. He is currently with Standard Drives Division, Rockwell Automation, Mequon, WI, USA. His primary interest includes application of power electronics to variable-speed drive and its industry applications.

David Leggate (S'90–M'93) received the A.A.S, B.S., and M.S. degrees in electrical engineering from Milwaukee School of Engineering, Milwaukee, WI, USA, in 1985, 1992, and 1998, respectively.

Since 1980, he has been with Rockwell Automation, Mequon, WI, where he is currently a Principle Engineer in the Control Theory Group. He has contributed to improvements in the design and development of new Rockwell Automation AC Motor Drives. His current research interests include control of power electronics and the development of control algorithms for general-purpose industrial ac drives.

Takayoshi Matsuo (S'90–M'92) received the B.E. degree in electrical engineering and the M.E. degree in applied electronics from Tokyo Institute of Technology, Tokyo, Japan, in 1975 and 1977, respectively, and the M.S. and Ph.D. degrees in electrical engineering from the University of Wisconsin–Madison, Madison, WI, USA, in 1983 and 1994, respectively.

From 1977 to 1989, he was an Electrical Engineer in the Power Electronics Department, Mitsubishi Electric Corporation, Japan. From 1994 to 1997, he was a Research Associate with the Wisconsin Power Electronics Research Center, Department of Electrical and Computer Engineering, University of Wisconsin–Madison. Since 1997, he has been with Rockwell Automation, Mequon, WI. His research interests include ac drives, electrical machines, and power electronics.