Implementation of a 3.3-kW DC–DC Converter for EV On-Board Charger Employing the Series-Resonant Converter With Reduced-Frequency-Range Control

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***Abstract*—A control method that improves performance of series-resonant converters that operate with a wide input voltage and/or output voltage range by substantially reducing their switching frequency range is introduced. The switching-frequency-range reduction is achieved by controlling the output voltage with a combination of variable-frequency and delay-time control. Variable-frequency control is employed to control the primary switches, while delay-time control is used to control secondary-side rectifier switches provided in place of diode rectifiers. A series-resonant converter with the proposed control method is employed as the output stage of the on-board charger module that operates with a wide battery-voltage range. By substantially reducing the switching frequency range, the overall operating frequency is increased to reduce the sizes of the passive components, and hence, increase power density. The performance evaluation of the proposed series-resonant converter with delay-time control was done on a 3.3-kW prototype delivering energy from 400-V bus, which is the output of the power factor correction front end, to a battery operating with voltage range between 180 and 430 V. Two implementations of the prototype circuit, one employing gallium nitride (GaN) and the other employing silicon (Si) switches, were evaluated and compared. The prototype with Si switches that at full load over the entire output voltage range operates with a switching frequency variation from approximately 150 to 190 kHz exhibits the maximum full-load efficiency of 98.1%, whereas the corresponding frequency range and efficiency of the prototype with GaN devices are 145–190 kHz and 97.4%, respectively.**

***Index Terms*—Delay-time control, frequency control, gallium nitride (GaN), on-board charging module (OBCM), series-resonant converter, zero-voltage switching (ZVS).**

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I. Introduction

RESONANT converters use a resonant tank circuit to shape switch voltage and/or current waveform to minimize switching losses and allow high-frequency operation while maintaining high conversion efficiencies. As a result, resonant converters are extensively used in state-of-the-art power supplies that offer the highest power densities and efficiencies [1]–[17]. Generally, resonant converters operate with variable switching-frequency control. When operating above the resonant frequency, a resonant converter operates with zero-voltage switching (ZVS) of the primary switches. Generally, variable switching-frequency control is seen as a drawback of a resonant converter especially in applications with a wide input voltage and/or output voltage range. Specifically, as the input or output voltage range increases, the control frequency range also increases so that driving and magnetic component losses also increase, thereby reducing conversion efficiency. Furthermore, in many applications, converters are restricted to operate within a relatively limited frequency range to avoid interfering with other parts of the system. While resonant converters can operate at a constant frequency ("clamp-mode" operation) [18], such an operation is not desirable because the increased circulating energy in the resonant tank circuit significantly degrades conversion efficiency. As a result, there have been several attempts to improve performance of resonant converters operating in a wide input voltage range and/or a wide output voltage range by reducing the switching frequency range by using additional "range" windings and/or switches to effectively change the turns ratio of the transformer [19]–[23]. While these approaches have been proven to improve performance, their major drawbacks are additional cost and complexity.

In this paper, a new control method that improves the performance of resonant converters that operate with a wide input voltage range and/or a wide output voltage range by substantially reducing their switching frequency range is introduced. Reduction in the switching frequency range is achieved by controlling the output voltage with a combination of variable-frequency feedback control and open-loop delay-time control. Variable-frequency control is used to control the primary switches of an isolated resonant converter, while delay-time control is used

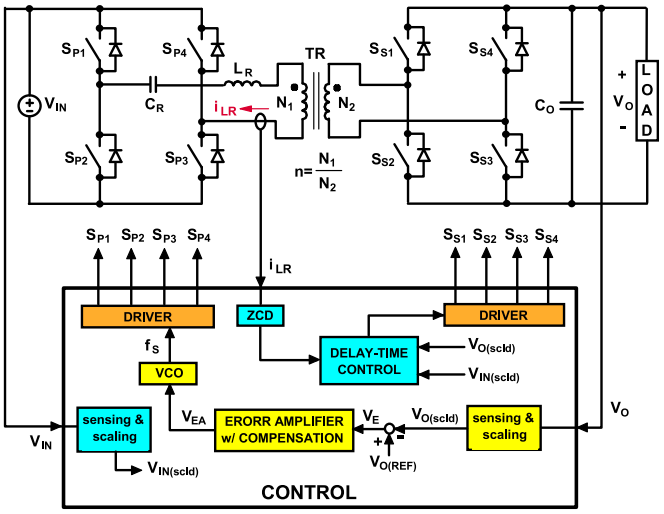

Fig. 1. Series-resonant converter with proposed secondary-side switch delay-time control.

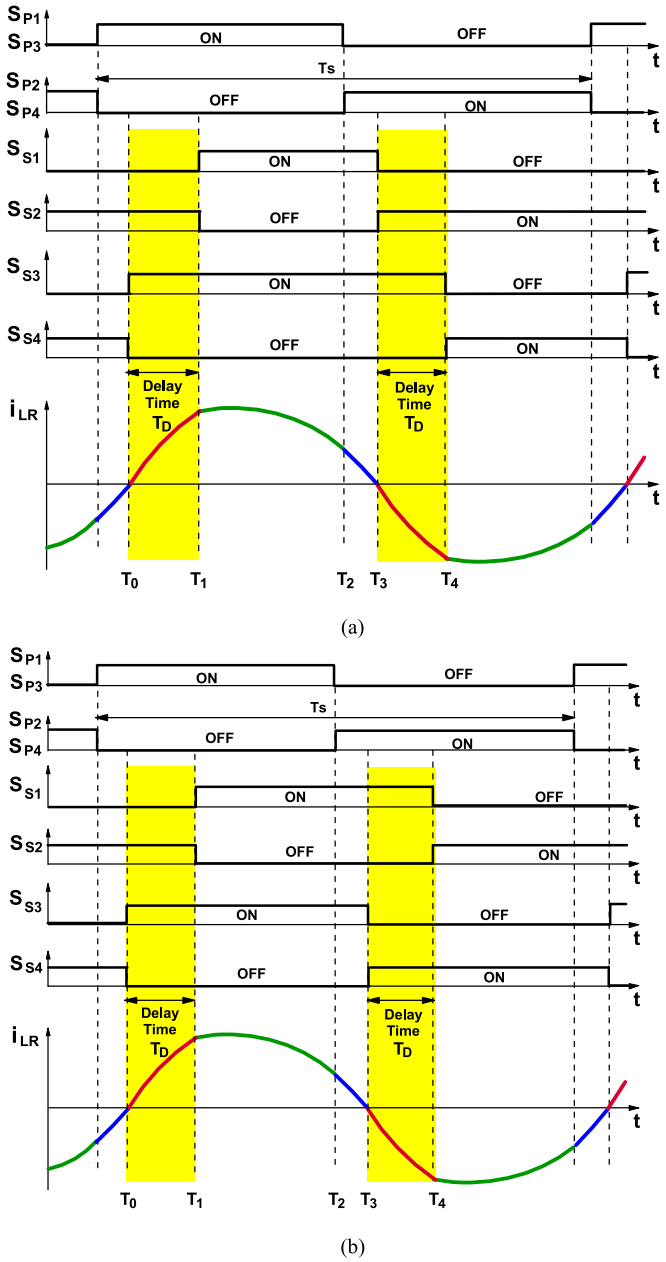

Fig. 2. Switch-gating and resonant inductor current waveforms of the series-resonant converter with the proposed delay-time control: (a) asymmetric gating and (b) symmetric gating.

to control secondary-side rectifier switches provided in place of diode rectifiers. The secondary-side control is implemented by sensing the secondary current and/or the primary current and by delaying the turning-off of the corresponding secondary switch(es) with respect to the zero crossings of the secondary or the primary current. Generally, the delay time is determined by the input voltage and/or the output voltage and is set to properly adjust the voltage gain. Since delay-time control increases the energy in the resonant tank circuit and makes the series-resonant converter exhibit a boost characteristic, delay-time control is typically designed to supplement the variable-frequency feedback control at low input and/or high output voltages. The introduced control method [24] is applied to a dc–dc series-resonant converter employed as the output stage of an on-board charger module (OBCM) operating with a wide output voltage range. By substantially reducing the switching frequency range, the overall operating frequency is increased to reduce the sizes of the passive components, and hence, increase power density without sacrificing its performance. The performance of the proposed dc–dc converter was verified on a 3.3-kW prototype operating with a 400-V input and an output that varies between 180 and 430 V.

II. Series-Resonant Converter With Combination of Variable-Frequency Control and Secondary-Side Switch Delay-Time Control

Fig. 1 illustrates the proposed control method in a series-resonant converter with a full-bridge secondary synchronous rectifier. However, it should be noted that the described control method is also applicable to the center-tap secondary implementation. As illustrated in Fig. 1, output voltage regulation is achieved using a combination of variable-frequency feedback control and open-loop delay-time control. Specifically, variable-frequency control is applied to primary switches $S_{P1} - S_{P4}$, and delay-time control is applied to secondary-side switches $S_{S1} - S_{S4}$. Fig. 2(a) and (b) shows waveforms of primary switches $S_{P1} - S_{P4}$, secondary switches $S_{S1} - S_{S4}$, and resonant inductor current i_{LR} for two secondary-side control methods: one with asymmetric gating and the other with symmetric gating. As shown in Fig. 2(a) and (b), in both implementations, all same-leg pairs of switches operate in a complementary fashion with a small dead time between their commutations to achieve ZVS.

In Fig. 2(a), the delay-time control is implemented by delaying the turn-off of switches S_{S2} and S_{S3} with respect to corresponding zero crossings of resonant current i_{LR} so that both switches S_{S2} and S_{S3} are turned on during delay-time intervals $[T_0 - T_1]$ and $[T_3 - T_4]$ shorting the secondary of transformer TR. This control method is easy to implement since it requires modulation of only two secondary-side switches. As illustrated in Fig. 2(a), switches S_{S2} and S_{S3} are modulated to provide necessary time delay, while switches S_{S1} and S_{S4} are operated with complimentary gate signals to that of switches

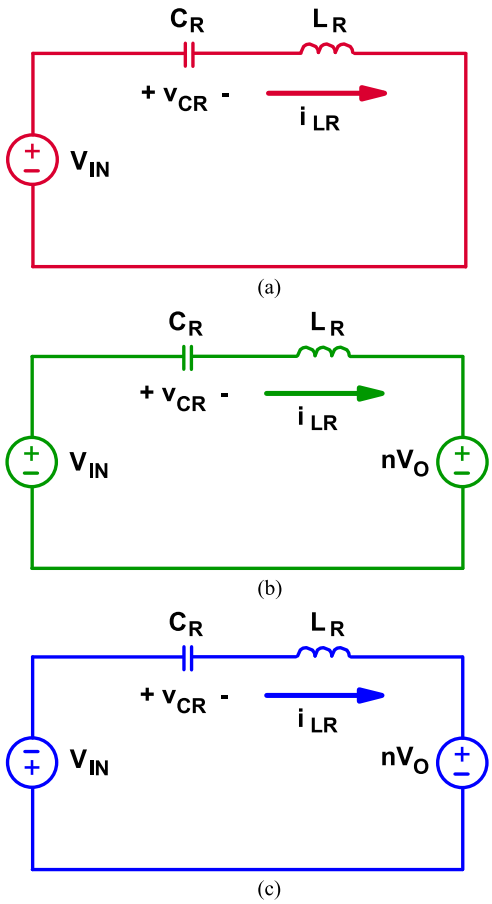

Fig. 3. Topological stages of the series-resonant converter with the proposed delay-time control during half of switching period when resonant inductor current is positive $[\mathrm{T}_0 - \mathrm{T}_3]$.

S_{S2} and S_{S3}, respectively. Because switches S_{S1} and S_{S4} are not actively modulated, they can be replaced by diode rectifiers, which further simplifies the circuit and may be beneficial in some applications. However, since in this asymmetrical-gating control implementation, switches S_{S2} and S_{S3} operate with a greater duty cycle compared to switches S_{S1} and S_{S4}, they also carry greater average currents and, consequently, exhibit increased thermal stress compared to switches S_{S1} and S_{S4} and require better thermal design. The uneven thermal stress of the secondary-side switches can be eliminated by implementing a symmetric-gating control shown in Fig. 2(b). In this implementation, all secondary-side switches operate with the same duty cycle of 50%. The delay-time control is implemented by delaying the turn-off of switches S_{S1} and S_{S2} with respect to corresponding zero crossings of resonant current i_{LR} so that switches S_{S2} and S_{S3} are turned on during the delay-time interval $[\mathrm{T}_0 - \mathrm{T}_1]$ and switches S_{S1} and S_{S4} are turned on during the delay-time interval $[\mathrm{T}_3 - \mathrm{T}_4]$ shorting the secondary of transformer TR. In this implementation, if advantageous, switches S_{S3} and S_{S4} can be replaced by diode rectifiers.

To facilitate explanation of operation, Fig. 3 shows the topological stages of the converter with the proposed delay-time control during a half of the switching period. The converter exhibits three topological stages. In the first topological stage, shown in Fig. 3(a), that occurs during the delay-time period $[\mathrm{T}_0 - \mathrm{T}_1]$, the secondary of the transformer is shorted. As a result, no energy is transferred from the $L_R - C_R$ resonant tank to the output and the resonant tank is driven by input voltage V_{IN} only. The second topological stage, shown in Fig. 3(b), occurs during the $[\mathrm{T}_1 - \mathrm{T}_2]$ period. Since during this stage the resonant current flows to the output, resonant tank energy is transferred to the load. During this stage, the voltage driving the resonant tank is given by the difference between input voltage V_{IN} and primary-reflected output voltage nV_O, i.e., by $V_{\mathrm{IN}} - \mathrm{nV_O}$. In the third topological stage that occurs during the $[\mathrm{T}_2 - \mathrm{T}_3]$, shown in Fig. 3(c), the resonant tank energy continues to be delivered to the output. However, since during this stage the input voltage polarity is negative because of the commutation of primary switches at $t = \mathrm{T}_2$, a part of the resonant tank energy is returned to the input. In fact, this circulating energy is used to achieve ZVS of the primary switches. During this stage, the voltage driving the resonant tank is given by the difference between the negative input voltage V_{IN} and primary-reflected output voltage nV_O, i.e., by $-V_{\mathrm{IN}} - \mathrm{nV_O}$.

As seen from Fig. 3(a), because in this topological stage the secondary of the transformer is shorted, the voltage across resonant tank $C_R - \mathrm{L_R}$ during delay-time interval $[\mathrm{T}_0 - \mathrm{T}_1]$ is V_{IN} instead of $V_{\mathrm{IN}} - nV_O$ which is the case with no delay-time control. Therefore, with the delay-time control, a higher voltage is applied across resonant inductor tank and, consequently, a higher amount of energy is stored in resonant inductor L_R. Therefore, at the same input voltage and switching frequency, secondary-side delay-time control provides a higher output voltage compared to the conventional frequency control. This boost characteristic makes optimizing circuit performance possible by enabling selection of a higher turns ratio in the transformer to reduce the primary conduction losses and a larger magnetizing inductance to reduce the circulating (i.e., magnetizing) current loss. Because of its boost characteristic, the proposed delay-time control is most effective when applied in a low input voltage range or in a high output voltage range. Specifically, the maximum delay time is set at the minimum input voltage or the maximum output voltage. This delay time is progressively reduced for higher input voltage or lower output voltage. In typical applications, the delay-time control is not used at the middle and high input voltages, or nominal and low output voltages.

The proposed control method can be implemented by either analog or digital technique, or their combination. A microcontroller- or DSP-based implementation is preferred since the delay time that depends on input or output voltage can be easily programmed.

III. Derivation of DC-Voltage Conversion Ratio

To provide tools for design optimization of the series-resonant converter with the proposed delay-time control, its dc conversion ratio $M = \mathrm{nV_O}/\mathrm{V_{IN}}$ is derived using the normalized state-plane analysis. The normalization was done with the following base parameters:

Base voltage $\quad V_{\mathrm{BASE}} = \mathrm{V_{IN}}.$

Base impedance $\quad Z_{\mathrm{BASE}} = Z_O = \sqrt{\dfrac{L_R}{C_R}}.$

Base current $I_{\rm BASE} = \dfrac{V_{\rm BASE}}{Z_{\rm BASE}} = \dfrac{V_{\rm IN}}{Z_O}$.

Base time $T_{\rm BASE} = T_S$.

Base frequency $f_{\rm BASE} = f_O = \dfrac{1}{2\sqrt{L_R C_R}}$.

Base angular frequency $\omega_{\rm BASE} = \omega_O = \dfrac{1}{\sqrt{L_R C_R}}$.

The normalized variables are defined as follows:

Normalized input voltage $V_{\rm IN\_N} = \dfrac{V_{\rm IN}}{V_{\rm BASE}} = 1.$

Normalized output voltage $V_{O\_N} = \dfrac{nV_O}{V_{\rm BASE}} = \dfrac{nV_O}{V_{\rm IN}}$.

Normalized resonant capacitor voltage $v_{\rm CR\_N} = \dfrac{v_{\rm CR}}{V_{\rm BASE}} = \dfrac{v_{\rm CR}}{V_{\rm IN}}$.

Normalized peak resonant capacitor voltage $v_{\rm CR\_PK\_N} = \dfrac{v_{\rm CR\_PK}}{V_{\rm BASE}} = \dfrac{v_{\rm CR\_PK}}{V_{\rm IN}}$.

Normalized output current $I_{O\_N} = \dfrac{I_O}{nI_{\rm BASE}} = \dfrac{Z_O I_O}{nV_{\rm IN}}$.

Normalized resonant inductor current $i_{LR\_N} = \dfrac{i_{\rm LR}}{I_{\rm BASE}} = \dfrac{Z_O i_{\rm LR}}{V_{\rm IN}}$.

Normalized delay time $T_{D\_N} = \dfrac{T_D}{T_S}$.

Normalized switching frequency $f_{S\_N} = \dfrac{f_S}{f_{\rm BASE}} = \dfrac{f_S}{f_O}$.

Other variables and parameters used are defined as follows:

Transformer turns ratio $n = \dfrac{N_1}{N_2}$.

Quality factor $Q = \dfrac{Z_O}{n^2 R_L}$.

Delay-time stage [see Fig. 3(a)] angle $\alpha = \omega_O [T_0 - T_1]$.

Energy-delivery stage [see Fig. 3(b)] angle $\beta = \omega_O [T_1 - T_2]$.

Energy-circulating stage [see Fig. 3(c)] angle $\gamma = \omega_O [T_2 - T_3]$.

Half-switching period angle $\lambda = \alpha + \beta + \gamma = \dfrac{\omega_O T_S}{2} = \dfrac{\pi}{f_{S\_N}}$.

Fig. 4 shows the normalized state trajectory of the converter during one half of a switching cycle. Since the proposed converter exhibits three topological stages during a half-switching cycle, trajectory consists of three corresponding arcs, as shown in Fig. 4. It should be noted that the centers of these arcs are on the $v_{\rm CR\_N}$ axis with the distances from the origin that are equal to the respective normalized voltage across resonant tank $L_R - C_R$. Since according to Fig. 3(a)–(c), the resonant tank voltages during the three topological stages are $V_{\rm IN}, V_{\rm IN} - {\rm nV_O}$, and $-V_{\rm IN} - nV_O$, respectively, the centers of the corresponding arcs in the normalized $v_{\rm CR\_N} - i_{\rm LR\_N}$ state plane are at (0, 1), (0, 1–*M*), and (0, –1–*M*).

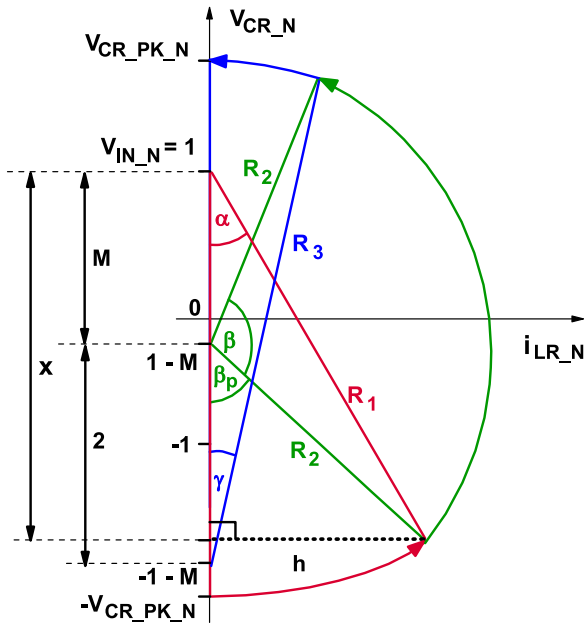

Fig. 4. State plan representation for one half of switching cycle $[{\rm T_0} - {\rm T_3}]$ where $v_{\rm CR\_N}$ and $i_{\rm LR\_N}$ are normalized resonant capacitor C_R voltage and resonant inductor L_R current, respectively.

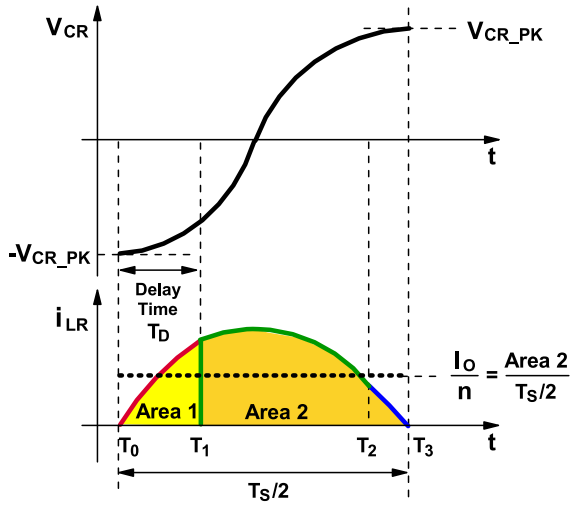

Fig. 5. Steady-state waveforms of resonant capacitor voltage $V_{\rm CR}$ and resonant inductor current $i_{\rm LR}$ during half-switching period where resonant inductor current is positive $({\rm i_{LR}} > 0)$.

To be able to complete the construction of the state-plane trajectory in Fig. 4, it is necessary to determine radius R_1 of the arc that corresponds to the stage in Fig. 3(a) which is the first stage in the half-cycle. To facilitate this derivation, Fig. 5 shows resonant voltage $v_{\rm CR}$ and current $i_{\rm LR}$ waveforms during a

half-switching cycle when resonant inductor current $i_{\rm LR}$ is positive. As can be seen from Fig. 5, during the shown half-switching period, the positive resonant inductor current continuously charges the resonant capacitor so that the voltage across resonant capacitor increases from its negative to its positive peak, i.e., changes for $2V_{\rm CR\_PK}$. The relationship between the resonant capacitor voltage change and stored charge $q_{\rm CR}^{\rm tot}$ during the half-switching cycle is given by

$$\begin{aligned} q_{\rm CR}^{\rm tot} &= \int_{T_0}^{T_3} i_{\rm LR}\,dt = \int_{T_0}^{T_1} i_{\rm LR}\,dt + \int_{T_1}^{T_3} i_{\rm LR}\,dt \\ &= C_R \cdot 2V_{\rm CR\_PK} \qquad (1) \\ \text{or } q_{\rm CR}^{\rm tot} &= \ Area1 + Area2 \ = C_R \ \cdot 2V_{\rm CR\_PK} \qquad (2) \end{aligned}$$

where *Area1* and *Area2* are defined in Fig. 5. Since during the delay-time topological stage shown in Fig. 3(a), i.e., during the $[\mathrm{T}_0 - \mathrm{T}_1]$ interval, the resonant inductor current is given by

$$\begin{aligned} i_{\rm LR}\,(t) &= \frac{V_{\rm IN} + V_{\rm CR}\,(0)}{Z_O} \cdot \sin\omega_0 t \\ &= \frac{V_{\rm IN} + V_{\rm CR\_PK}}{Z_O} \cdot \sin\omega_0 t \qquad (3) \end{aligned}$$

where, as shown in Fig. 5, initial capacitor voltage $V_{\rm CR}\,(0) = \mathrm{V_{CR\_PK}}$, *Area1* can be calculated as follows:

$$Area1 \ = \frac{V_{\rm IN} + V_{\rm CR\_PK}}{Z_O} \cdot \int_{T_0}^{T_1} \sin\omega_0 t \cdot dt. \qquad (4)$$

Area2 can be calculated by recognizing that the output (load) current reflected to the primary is the average of the resonant inductor current $i_{\rm LR}$ over a half-switching period. Since $i_{\rm LR}$ flows through the output only during the interval $[\mathrm{T}_1 - \mathrm{T}_3]$, the reflected output current at the primary side is given by

$$\frac{I_O}{n} = \frac{2}{T_S} \int_{T_1}^{T_3} i_{\rm LR}\,dt = \frac{2}{T_S} Area2. \qquad (5)$$

From (2)–(5), it follows that

$$\frac{V_{\rm IN} + V_{\rm CR\_PK}}{Z_O} \cdot \int_{T_0}^{T_1} \sin\omega_0 t \cdot dt + \frac{I_O}{n} \cdot \frac{T_S}{2} = C_R \ \cdot 2V_{\rm CR\_PK} \qquad (6)$$

which after normalization with replacing $C_R = 1/(\omega_0 Z_0)$ and assuming that $t = \mathrm{T}_0 = 0$ can be written as follows:

$$(1 + V_{\rm CR\_PK\_N}) \cdot \int_0^{\alpha} \sin\theta \cdot d\theta + \lambda \cdot \ I_{O\_N} = \ 2V_{\rm CR\_PK\_N}. \qquad (7)$$

Finally, from (7), normalized peak resonant capacitor voltage can be solved as

$$V_{\rm CR\_PK\_N} = \frac{1 - \cos\alpha + \lambda \cdot I_{O\_N}}{1 + \cos\alpha}\ . \qquad (8)$$

From the normalized state-plane diagram in Fig. 4, it follows that radii R_1, R_2, and R_3 are related to $V_{\rm CR\_PK\_N}$ as

$$\begin{aligned} R_1 &= V_{\rm CR\_PK\_N} + 1 \qquad (9) \\ R_2 &= \sqrt{(x - M)^2 + h^2} \\ &= \sqrt{(R_1\cos\alpha - M)^2 + (R_1\sin\alpha)^2} \qquad (10) \\ R_3 &= V_{\rm CR\_PK\_N} + M + 1. \qquad (11) \end{aligned}$$

By using the law of cosines that is formed by radii R_2 and R_3, as well as angles $\beta+\beta_{\rm P}$ and γ, dc conversion ratio *M* of the series-resonant converter with the proposed delay-time control can be derived as follows:

$$2^2 = R_2^2 \ + R_3^2 - 2R_2R_3\cos\left[\pi - (\beta + \beta_P) - \gamma\right] \qquad (12)$$

where

$$\beta_P = \tan^{-1}\ \frac{h}{x - M} = \tan^{-1}\ \frac{R_1\sin\alpha}{R_1\cos\alpha - M}. \qquad (13)$$

Since $\lambda = \alpha + \beta + \gamma$, (12) can be rewritten as

$$4 \ = R_2^2 \ + R_3^2 - 2R_2R_3\cos\left(\pi - \lambda + \alpha - \beta_P\right). \qquad (14)$$

Using (9), (10), and (11), (14) can be expressed as follows:

$$\begin{aligned} &(V_{\rm CR\_PK\_N} + 1)^2 + M^2 + M(V_{\rm CR\_PK\_N} + 1)(1 - \cos\alpha) \\ &\quad + (V_{\rm CR\_PK\_N} + 1 + M) \\ &\quad \times \sqrt{(V_{\rm CR\_PK\_N} + 1)^2 + M^2 - 2M(V_{\rm CR\_PK\_N} + 1)\cos\alpha} \\ &\quad \times \cos\left(\lambda - \alpha + \beta_P\right) - 2 = 0. \qquad (15) \end{aligned}$$

Relationship in (15) can be rewritten in terms of design parameters T_{D_N}, f_{S_N}, M, and Q by recognizing that variables α, λ, and β_P are given by

$$\begin{aligned} \alpha &= \frac{2\pi T_{D\_N}}{f_{S\_N}} \qquad (16) \\ \lambda &= \frac{\pi}{f_{S\_N}} \qquad (17) \\ \beta_P &= \tan^{-1}\ \frac{R_1\sin\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right)}{R_1\cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right) - M} \\ &= \tan^{-1}\ \frac{(V_{\rm CR\_PK\_N} + 1)\sin\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right)}{(V_{\rm CR\_PK\_N} + 1)\cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right) - M} \qquad (18) \end{aligned}$$

and that normalized peak resonant capacitor voltage $V_{\rm CR\_PK\_N}$ can be expressed as

$$\begin{aligned} V_{\rm CR\_PK\_N} &= \frac{1 - \cos\alpha + \lambda \cdot I_{O\_N}}{1 + \cos\alpha} \\ &= \frac{1 - \cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right) + \left(\frac{\pi}{f_{S\_N}}\right) \cdot Q \cdot M}{1 + \cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right)} \qquad (19) \end{aligned}$$

since normalized output current I_{O_N} is given by

$$I_{O\_N} = \frac{Z_O I_O}{nV_{\mathrm{IN}}} = \frac{Qn^2 R_L I_O}{nV_{\mathrm{IN}}} = \frac{QnV_O}{V_{\mathrm{IN}}} = Q \cdot M. \qquad (20)$$

Substituting (16)–(20) into (15), it is obtained

$$\left(\frac{1 - \cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right) + \left(\frac{\pi}{f_{S\_N}}\right) \cdot Q \cdot M}{1 + \cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right)} + 1 \right)^2 + M^2$$

$$+ M \left(\frac{1 - \cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right) + \left(\frac{\pi}{f_{S\_N}}\right) \cdot Q \cdot M}{1 + \cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right)} + 1 \right)$$

$$\times \left[1 - \cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right) \right]$$

$$+ \left(\frac{1 - \cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right) + \left(\frac{\pi}{f_{S\_N}}\right) \cdot Q \cdot M}{1 + \cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right)} + 1 + M \right)$$

$$\times \sqrt{\begin{array}{l} \left(\frac{1-\cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right) + \left(\frac{\pi}{f_{S\_N}}\right) \cdot Q \cdot M}{1+\cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right)} + 1 \right)^2 + M^2 \\ -2M \left(\frac{1-\cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right) + \left(\frac{\pi}{f_{S\_N}}\right) \cdot Q \cdot M}{1+\cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right)} + 1 \right) \cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right) \end{array}}$$

$$\times \cos\left[\left(\frac{\pi}{f_{S\_N}}\right) - \left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right) + \tan^{-1}\left[\frac{\left(\frac{1-\cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right) + \left(\frac{\pi}{f_{S\_N}}\right) \cdot Q \cdot M}{1+\cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right)} + 1 \right) \cdot \sin\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right)}{\left(\frac{1-\cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right) + \left(\frac{\pi}{f_{S\_N}}\right) \cdot Q \cdot M}{1+\cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right)} + 1 \right) \cdot \cos\left(\frac{2\pi T_{D\_N}}{f_{S\_N}}\right) - M} \right] \right]$$

$$- 2 = 0. \qquad (21)$$

Because an explicit solution for dc conversion ratio $M = \mathrm{nV}_O / V_{\mathrm{IN}}$ given by (21) is not available, it is numerically calculated for a given quality factor Q and normalized delay time $T_{D\_N} = \alpha/(2\lambda) = T_D/T_S$. As examples, Fig. 6(a) and (b) shows the plots of dc conversion ratio M as function of normalized switching frequency and normalized delay time T_{D_N} as a parameter for $Q = 1$ and $Q = 0.2$, respectively. When delay time is zero ($\alpha = 0°, \mathrm{T_D} = 0$), the converter characteristic is the same as that of a conventional series-resonant converter. As delay time T_D increases, dc gain M increases and exhibits a boost characteristic. It should be noted that for normalized delay times T_{D_N} smaller than 0.25 dc gain M monotonically increases across the given frequency range as T_{D_N} increases, i.e., as shown in Fig. 6(a) and (b), at any given frequency, gain M for $T_{D\_N} = 0.25$ is greater than the gain for $T_{D\_N} = 0.15$. However, for T_{D_N} greater than 0.25, as T_{D_N} increases, dc gain M monotonically increases only in a limited frequency range in the vicinity of the resonant frequency. For example, in Fig. 6(a)

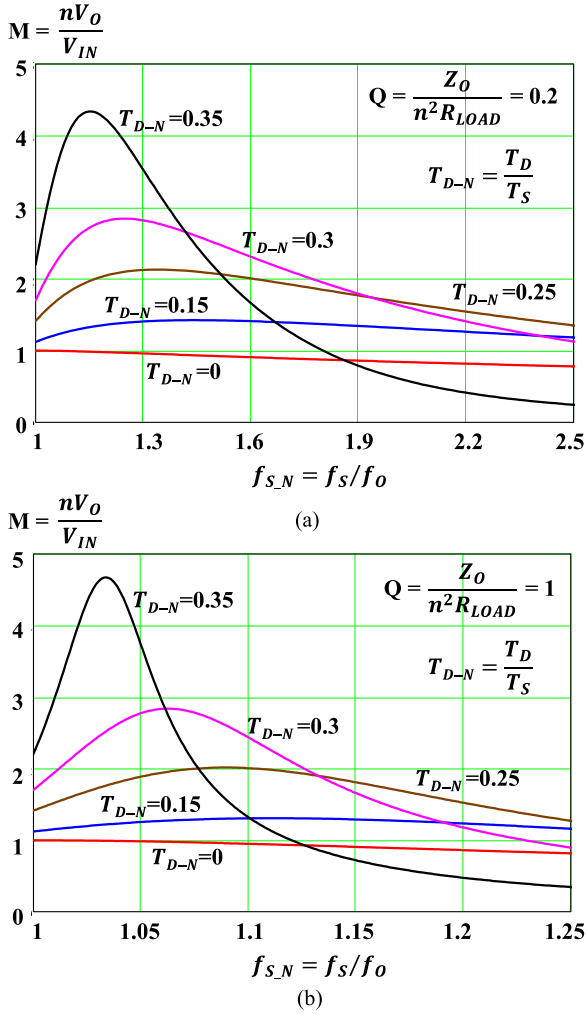

Fig. 6. Calculated dc-voltage conversion ratio characteristics of the series-resonant converter with the proposed delay-time control for Q-factor: (a) $Q = 0.2$. (b) $Q = 1$.

and (b), dc gain M for $T_{D\_N} = 0.3$ is smaller than dc gain M for $T_{D\_N} = 0.25$ above normalized switching frequency $f_{S\_N} = 1.9$ and $f_{S\_N} = 1.13$, respectively. To avoid design constraints imposed by nonmonotonically changing dc gain M, it is recommended to limit T_{D_N} to below 0.25.

To illustrate the effectiveness of the delay-time control to reduce control-frequency range, Fig. 7(a), (b), and (c) shows, respectively, the control-frequency range of the *LLC* converter, *LC* series-resonant converter, and the proposed series-resonant converter with delay-time control designed for 180–430 V output voltage range and 400 V input. For comparison, magnetizing inductance L_M was chosen to be four times larger than the resonant inductance L_R in the case of *LLC* resonant converter, whereas magnetizing inductance L_M of the conventional *LC* series-resonant converter and the proposed series-resonant converter is assumed infinite. For both *LLC* resonant converter and the proposed converter, turns ratio of the transformer is $n = \mathrm{N}_1/\mathrm{N}_2 = 1.25$. However, the transformer's turns ratio of the conventional *LC* series-resonant converter is $n = \mathrm{N}_1/\mathrm{N}_2 = 0.83$. Operating points marked A, B, and C in

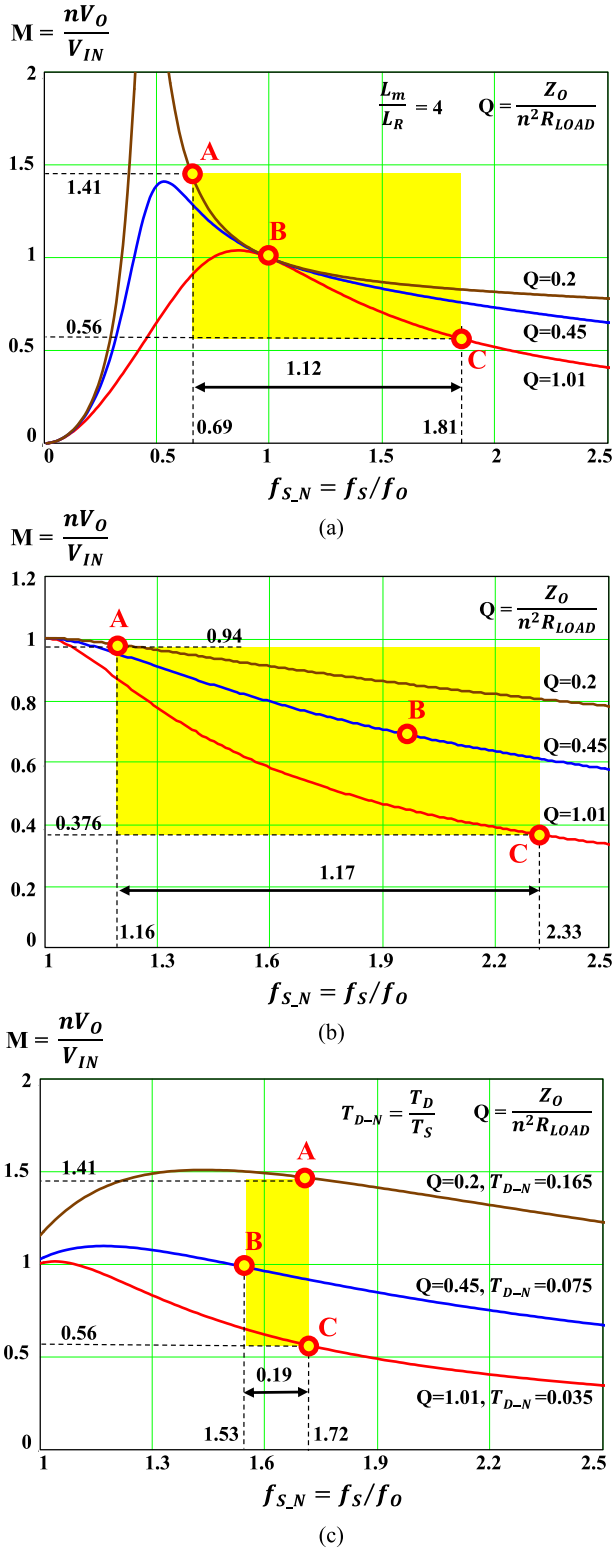

Fig. 7. Comparison of control-frequency ranges of: (a) conventional *LLC* resonant converter, (b) conventional *LC* series-resonant converter, and (c) proposed series-resonant converter with delay-time control. Points A, B, and C represent operating points when converters deliver full power to output voltages 430, 320, and 180 V, respectively. Input voltage of all converters is $V_{\rm IN} = 400$ V. Transformer's turns ratio of (a) *LLC* resonant converter and (c) proposed converter is $n = 1.25$ while that of (b) *LC* series-resonant converter is $n = 0.83$.

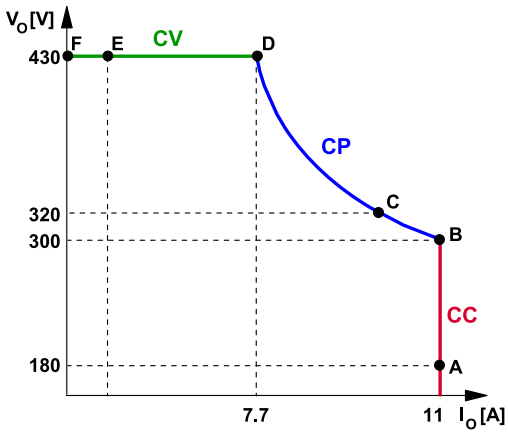

Fig. 8. Output characteristic of the experimental prototype.

Fig. 7 represent operating points when the converter delivers full power to output voltage 180, 320, and 430 V, respectively. As can be seen from Fig. 7, the series-resonant converter with the proposed delay-time control exhibits a significantly narrower frequency range compared to that of the *LLC* converter and the conventional *LC* series-resonant converter. Specifically, as shown in Fig. 7(a)–(c), the frequency range of the *LLC* resonant converter is from $f_{S\_N\_\rm MIN} = 0.69$ (operating point A) to $f_{S\_N\_\rm MAX} = 1.81$ (operating point C), the frequency range of the conventional *LC* resonant converter is from $f_{S\_N\_\rm MIN} = 1.16$ to $f_{S\_N\_\rm MAX} = 2.23$ and the frequency range of the proposed resonant converter with delay-time control is from $f_{S\_N\_\rm MIN} = 1.53$ to $f_{S\_N\_\rm MAX} = 1.72$. Therefore, the proposed series-resonant converter with delay-time control exhibits approximately six times smaller frequency range compared to both the *LLC* converter $(1.12/0.19 = 5.89)$ and the *LC* series-resonant converter $(1.17/0.19 = 6.15)$.

IV. Design Considerations

For performance evaluation, the proposed dc–dc converter for electric vehicle on-board charger has been designed and built according to the following key specifications:

Input voltage $V_{\rm IN}$:	400 $V_{\rm DC}$
Output voltage V_O:	180–430 $V_{\rm DC}$
Maximum output current $I_{O-\rm MAX}$:	11 A
Maximum output power $P_{O-\rm MAX}$:	3.3 kW
Efficiency η:	>96% above 50% load
Dimension:	250 mm × 180 mm × 75 mm.

A. Selection of Resonant Tank Components

Generally, in battery-charging applications, the main objective is to design an efficient and cost-effective charger that minimizes the charging time for a given battery-charging profile. According to the specifications, the charging characteristic of the evaluation prototype is given by plot shown in Fig. 8. When the battery is deeply discharged, i.e., when the battery voltage is in the 180–300 V range (between operating points A and B),

the charger operates in a constant-current (CC) mode, i.e., it charges the battery with the maximum current of 11 A. After the battery voltage exceeds 300 V, the battery is charged with a constant power (CP) of 3.3 kW until the battery voltage reaches maximum voltage of 430 V and the charger starts operating in a constant-voltage (CV) mode. During the CP charging (between operating points B and D), as the battery voltage increases, the charging current decreases from 11 A at 300 V to around 7.7 A at 430 V. Once the charger enters the CV mode (between operating points D and F), the charging current rapidly deceases to a very small float (trickle-charge) current (operating point F), which is the current that compensates for the battery self-discharge. It should be noted that while lead acid, NiCd, NiMH can be and are designed to continuously trickle charge, Li-ion batteries cannot absorbed overcharge and the charging current must be cut off once they are fully charged. Since the charging time spent in the CV mode is much shorter than that spent in the CC and CP modes, to maximize charging efficiency, it is important to maximize the efficiency in the CC and CP modes.

To determine the values of the resonant tank components, it is necessary to select turns ratio of the transformer *n*, minimum switching frequency f_{S_MIN}, and frequency range Δf_S for operation in the CC and CP modes. The turns ratio of the transformer is determined so that the efficiency of the charger in the mid-voltage range (260–360 V) is maximized since the charger is expected to work most of the time in this range. Specifically, for the prototype circuit, turns ratio *n* is determined by assuming that the converter operates with gain $M = \mathrm{nV_O}/\mathrm{V_{IN}} = 1$ for the output voltage $V_O = 320$ V (operating point C) so that the turns ratio is $n = \mathrm{MV_{IN}}/\mathrm{V_O} = 1 * 400/320 = 1.25$. With this selection of *n*, the converter needs to operate as a boost converter for output voltages greater than 320 V, i.e., it requires delay-time control, whereas it operates as a conventional series-resonant converter without delay-time control for output voltages below 320 V. To provide a design margin, i.e., to ensure that the circuit can operate at 320 V in the presence of losses brought about by nonideal components, in the prototype circuit the delay-time control is implemented starting from 300 V, i.e., in the 300–430 V range (between operating points B and D). As a result, the minimum switching frequency of the prototype occurs in the CC mode when the output voltage is 300 V and the output current is 11 A (operating point B). Generally, the selection of the minimum switching frequency is based on the tradeoff between efficiency and size. In this design, to meet the required power density, the minimum switching frequency is set at $f_{S\_\mathrm{MIN}} = 140$ kHz.

As the output voltage either decreases from 300 V toward 180 V or increases toward 430 V, the switching frequency increases. Maximum switching frequency f_{S_MAX} in the CC mode occurs at the minimum output voltage of 180 V (operating point A), whereas the maximum switching frequency in CP mode occurs at the maximum voltage of 430 V (operating point D). Frequency range $\Delta \mathrm{f_S} = \mathrm{f_{S\_MAX}} - \mathrm{f_{S\_MIN}}$ in the CC mode when the converter operates as a conventional series-resonant converter without delay-time control is set by properly selecting the value of resonant inductor L_R and resonant capacitor C_R. The frequency range in the CP mode when the converter operates with the delay-time control is set by proper selection of the maximum delay-time that occurs at the output voltage of 430 V.

It should be noted that in the CV mode as the output current decreases, the switching frequency increases above maximum frequency f_{S_MAX} in the CV mode. In this design, the absolute maximum switching frequency is limited to 350 kHz to prevent excessive high-frequency switching losses (operating point E in Fig. 8). To regulate the output voltage for light-load currents that require switching frequencies above 350 kHz (between operating points E and F), either the burst mode or the delay-time fold-back (decreasing T_D as current decreases) control can be used.

In this design, it is assumed that the frequency range when the charger operates in the CC and CP modes is $\Delta \mathrm{f_S} = 40$ kHz, i.e., that the maximum frequency is $f_{S\_\mathrm{MAX}} = f_{S\_\mathrm{MIN}} + \Delta f_S = 180$ kHz. Based on experience, this selection of the frequency range offers a good balance between the switching and circulating-energy losses.

To calculate the values of resonant inductor L_R and resonant capacitor C_R, it is necessary to determine the resonant frequency f_O and *Q*-factor of the converter so that when it operates in the CC mode with the maximum output current $I_{O-\mathrm{MAX}} = 11$ A its switching frequency at $V_{O\_B} = 300\,\mathrm{V}$ (operating point B in Fig. 8) is $f_{S\_\mathrm{MIN}} = 140$ kHz and at $V_{O\_A} = 180$ V (operating point A) is $f_{S\_\mathrm{MAX}} = 180\,\mathrm{kHz}$. Since in the CC mode the converter operates as a conventional series-resonant converter without delay-time control, the dc-gain characteristic in (21) for $T_{D\_N} = 0$ is used to determine f_O and *Q*. Setting $T_{D\_N} = 0$ in (21), the dc gain of the series-resonant converter is obtained as

$$\left(\frac{\pi}{2}\cdot\frac{Q\cdot M}{\frac{f_S}{f_O}}+1\right)^2 + M^2 + \left(\frac{\pi}{2}\cdot\frac{Q\cdot M}{\frac{f_S}{f_O}}+1+M\right) \times \sqrt{\left(\frac{\pi}{2}\cdot\frac{Q\cdot M}{\frac{f_S}{f_O}}+1\right)^2 + M^2 - 2M\left(\frac{\pi}{2}\cdot\frac{Q\cdot M}{\frac{f_S}{f_O}}+1\right)} \times \cos\frac{\pi}{\frac{f_S}{f_O}} - 2 = 0. \tag{22}$$

Since for operating point B in Fig. 8, $M_B = nV_{O_B}/V_{\mathrm{IN}} = 1.25 * 300/400 = 0.938$ and $f_{S\_B} = f_{S\_\mathrm{MIN}} = 140$ kHz, (22) for operating B is given by (23) that is shown at the bottom of the next page.

For operating point A, $M_A = nV_{O_A}/V_{\mathrm{IN}} = 1.25 * 180/400 = 0.563$, $f_{S\_A} = f_{S\_\mathrm{MAX}} = 180$ kHz, and the *Q*-factor in points A and B is related as follows:

$$\frac{Q_A}{Q_B} = \frac{\frac{Z_O}{n^2 R_{L\_A}}}{\frac{Z_O}{n^2 R_{L\_B}}} = \frac{R_{L\_B}}{R_{L\_A}} = \frac{\frac{V_{O\_B}}{I_{O\_\mathrm{MAX}}}}{\frac{V_{O\_A}}{I_{O\_\mathrm{MAX}}}} = \frac{V_{O\_B}}{V_{O\_A}} = \frac{300\ \mathrm{V}}{180\ \mathrm{V}} = 1.667$$

so that (22) for operating point A is given by (24) that is shown at the bottom of the next page.

Solving (23) and (24) using MathCad, the resonant frequency and Q-factor are

$$f_O = \frac{1}{2\pi\sqrt{L_R C_R}} = 123 \text{ kHz} \quad (25)$$

$$Q_B = \frac{Z_O}{n^2 R_{L\_B}} = 0.815. \quad (26)$$

From (26), characteristic impedance Z_O is calculated as follows:

$$Z_O = \sqrt{L_R/C_R} = Q_B \cdot n^2 \cdot R_{L_B} = 0.815 \cdot 1.25^2 \cdot \frac{300\,\text{V}}{11\,\text{A}} = 34.7\ \Omega. \quad (27)$$

Solving (25) and (27), the calculated values of the resonant tank components are

$$L_R = \frac{Z_O}{2\pi f_O} = 44.95\ \mu\text{H} \quad (28)$$

$$C_R = \frac{1}{2\pi f_O Z_O} = 37.2\ \text{nF}. \quad (29)$$

Since the closest standard value of capacitance is 33 nF, in the prototype circuit C_R= 33 nF is used. The value of the resonant inductor in the prototype circuit is 46 μH.

B. Delay-Time Selection

To keep the maximum switching frequency between operating points B and D below $f_{S\_\text{MAX}} = 180$ kHz, it is necessary to properly set up the delay time. Since in (21) for given output voltage V_O, i.e., gain $M = \text{nV}_\text{O}/\text{V}_\text{IN}$, and given output (charging) current I_O, i.e., $Q = \frac{Z_O \cdot I_O}{n^2 V_O}$, two variables f_{S_N} and T_{D_N} are unknown, there is a degree of freedom in selecting the delay time. Specifically, the delay time at any operating point between operating points B and D can be calculated by assuming any switching frequency f_S in the desired 140–180 kHz range. In the prototype circuit, the delay time is determined by assuming that the maximum switching frequency occurs at operating point D in Fig. 8, so that required normalized delay time $T_{D\_N\_D}$ can be calculated from (21) by recognizing that for operating point D, $M_D = nV_{O\_D}/V_{\text{IN}} = 1.25 * 430/400 = 1.344$, $Q_D = \frac{Z_O}{n^2 R_{L\_D}} = \frac{Z_O \cdot I_{O\_D}}{n^2 V_{O\_D}} = \frac{34.7 \cdot 7.7}{1.25^2 \cdot 430} = 0.398$, and $f_{S\_N\_D} = \frac{f_{S\_\text{MAX}}}{f_O} = \frac{180 \cdot 10^3}{123 \cdot 10^3} = 1.46$, i.e., that (21) is

$$\left(\frac{1-\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)+1.15}{1+\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)}+1\right)^2 + 1.344^2 + 1.344 \times \left(\frac{1-\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)+1.15}{1+\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)}+1\right)\left[1-\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)\right] + \left(\frac{1-\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)+1.15}{1+\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)}+1+1.344\right) \times \sqrt{\left(\frac{1-\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)+1.15}{1+\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)}+1\right)^2 + 1.344^2 - 2 \times 1.344\left(\frac{1-\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)+1.15}{1+\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)}+1\right)\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)} \times \cos\left[2.15-\left(\frac{T_{D\_N\_D}}{0.233}\right)+\tan^{-1}\left[\frac{\left(\frac{1-\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)+1.15}{1+\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)}+1\right)\cdot\sin\left(\frac{T_{D\_N\_D}}{0.233}\right)}{\left(\frac{1-\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)+1.15}{1+\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)}+1\right)\cdot\cos\left(\frac{T_{D\_N\_D}}{0.233}\right)-1.344}\right]\right] - 2 = 0. \quad (30)$$

Using MathCad, the solution of (30) is

$$T_{D\_N\_D} = \frac{T_{D\_D}}{T_{S\_\text{MAX}}} = f_{S\_\text{MAX}} \cdot T_{D\_D} = 0.167 \quad (31)$$

$$\left(\frac{\pi}{2}\cdot\frac{Q_B\cdot 0.938}{\frac{140\cdot 10^3}{f_O}}+1\right)^2 + 0.938^2 + \left(\frac{\pi}{2}\cdot\frac{Q_B\cdot 0.938}{\frac{140\cdot 10^3}{f_O}}+1+0.938\right) \times \sqrt{\left(\frac{\pi}{2}\cdot\frac{Q_B\cdot 0.938}{\frac{140\cdot 10^3}{f_O}}+1\right)^2 + 0.938^2 - 2\cdot 0.938\left(\frac{\pi}{2}\cdot\frac{Q_B\cdot 0.938}{\frac{140\cdot 10^3}{f_O}}+1\right)} \times \cos\frac{\pi}{\frac{140\cdot 10^3}{f_O}} - 2 = 0. \quad (23)$$

$$\left(\frac{\pi}{2}\cdot\frac{1.667\cdot Q_B\cdot 0.563}{\frac{180\cdot 10^3}{f_O}}+1\right)^2 + 0.563^2 + \left(\frac{\pi}{2}\cdot\frac{1.667\cdot Q_B\cdot 0.563}{\frac{180\cdot 10^3}{f_O}}+1+0.563\right) \times \sqrt{\left(\frac{\pi}{2}\cdot\frac{1.667\cdot Q_B\cdot 0.563}{\frac{180\cdot 10^3}{f_O}}+1\right)^2 + 0.563^2 - 2\cdot 0.563\left(\frac{\pi}{2}\cdot\frac{1.667\cdot Q_B\cdot 0.563}{\frac{180\cdot 10^3}{f_O}}+1\right)} \times \cos\frac{\pi}{\frac{180\cdot 10^3}{f_O}} - 2 = 0. \quad (24)$$

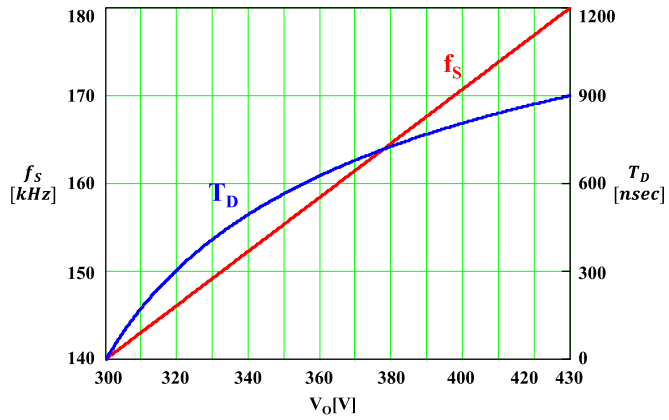

Fig. 9. Calculated delay time T_D and switching frequency f_S as a function of output voltage V_O.

so that required delay time T_{D_D} at operating point D is

$$T_{D\_D} = 0.167 \cdot \frac{1}{f_{S\_\mathrm{MAX}}} = 927 \text{ ns}. \tag{32}$$

To minimize the circulating current that can be generated by excessive delay time for a given operating point, the delay time for the operating points between B and D, i.e., between 300 and 430 V, is determined by assuming linear increases of the switching frequency, i.e.,

$$\begin{aligned} f_S &= \frac{f_{S\_\mathrm{MAX}} - f_{S\_\mathrm{MIN}}}{V_{O\_D} - V_{O\_B}} (V_O - V_{O\_B}) + f_{S\_\mathrm{MIN}} \\ &= \frac{180\,\mathrm{kHz} - 140\,\mathrm{kHz}}{430\,\mathrm{V} - 300\,\mathrm{V}} (V_O - 300\,\mathrm{V}) + 140\,\mathrm{kHz} \\ &= \frac{40\,\mathrm{kHz}}{130\,\mathrm{V}} (V_O - 300\,\mathrm{V}) + 140\,\mathrm{kHz}. \end{aligned} \tag{33}$$

Fig. 9 shows calculated delay time T_D as a function of the output voltage that is obtained from (21) for operating points in the CP mode, assuming the relationship in (33). This dependence of delay time T_D is coded into a lookup table of the DSP-based control circuit.

C. Transformer Construction

The transformer was designed using ferrite cores and Litz-wire windings with the following specifications:
Core: A pair of PQ4040-PC40 ferrite cores.
Primary winding:
$N_1 = 20$ turns, Litz wire (435 strands /AWG #40).
Secondary winding:
$N_2 = 16$ turns, Litz wire (435 strands /AWG #40).
Air gap: 0.02 mm.

The measured magnetizing and leakage inductances are 1.85 mH and 1.6 μH, respectively. The maximum flux density in steady-state operation is approximately 0.23 T, which gives plenty of margin from the saturation limit of the ferrite core.

D. Resonant Capacitor Selection

A high-frequency film capacitor is a suitable candidate for resonant capacitor C_R because of its cost and long-term reliability. However, its maximum permissible ac voltage is inversely proportional to frequency. For example, a 33-nF, 2000-VDC, FKP 1 type film capacitor from WIMA has the ac-voltage rating of 700 $\mathrm{V_{AC-RMS}}$ at line frequency of 50/60 Hz and only 180 $\mathrm{V_{AC-RMS}}$ at approximately 140 kHz. Therefore, to properly select the resonant capacitor, the maximum peak voltage of the capacitor needs to be known.

Since the average of the resonant inductor current i_{LR} over a half-switching period is equal to the output (load) current reflected to the primary, stored charge $q_{\mathrm{CR}}^{\mathrm{tot}}$ during the half-switching cycle can be calculated as follows:

$$q_{\mathrm{CR}}^{\mathrm{tot}} = \int_{T_1}^{T_3} i_{\mathrm{LR}}\,dt = \frac{I_O}{n} \cdot \frac{T_S}{2}. \tag{34}$$

From (1) and (34), it follows that

$$V_{\mathrm{CR\_PK}} = \frac{I_O \cdot T_S}{4nC_R} = \frac{I_O}{4nC_R f_S}, \tag{35}$$

where $n = \mathrm{N_1/N_2}$ is the turns ratio of transformer TR. The maximum of capacitor peak voltage $V_{\mathrm{CR\_PK}}$ occurs at minimum frequency (minimum input voltage) and full load. The peak voltage across a 33-nF capacitor is calculated as follows:

$$\begin{aligned} V_{\mathrm{CR\_PK}} &= \frac{I_{O(\max)}}{4nC_R f_{S(\min)}} \\ &= \frac{11}{4 \cdot \frac{20}{16} \cdot 33 \cdot 10^{-9} \cdot 140 \cdot 10^3} = 476\ \mathrm{V}. \end{aligned}$$

Since the voltage waveform across the resonant capacitors is a sine wave shape, rms voltage across the serially connected two capacitors is approximately 337 V. To keep the maximum voltage stress of capacitor within the 180 $\mathrm{V_{AC-RMS}}$ limit, two sets of series-connected two 33-nF, 2000-VDC, 700-$\mathrm{V_{AC-RMS}}$, FKP 1 type film capacitors are connected in parallel.

E. Resonant Inductor Design

To obtain the desired 46-μH inductance, the resonant inductor was built using a pair of ferrite cores (PQ-40/40, PC40) with a 3.8-mm gap in all three legs. The winding was implemented with 28 turns of Litz wire (435 strands of AWG#40) to reduce the fringing-effect-induced winding loss near the gap of the inductor core. For this inductor design, the maximum flux density which occurs at full load and the minimum switching frequency is approximately 0.28 T.

It should be noted that resonant inductor could be implemented as a leakage inductance of the transformer. However, in its simplest implementation where the separation of the primary and secondary winding is intentionally increased to provide enough leakage inductance, the transformer suffers from increased eddy-current-induced winding losses and electromagnetic interference (EMI) problems caused by the flux coupling to nearby components. More complex magnetic structures that integrate the resonant inductor and transformer could also be employed, [2], [25]. Generally, these integrated magnetics implementations offer lower winding losses and acceptable EMI performance because of better containment of the leakage flux within the magnetics structure. In the prototype circuit, a

separate resonant inductor and transformer are used because in our experience this approach offers the best performance and packaging flexibility.

F. Semiconductor Device Selection

Because the voltage stresses of primary switches $S_{P1}-S_{P4}$ and secondary switches $S_{S1}-S_{S4}$ are approximately equal to input voltage V_{IN} and output voltage V_O, respectively, i.e., they are below 450 V, it is necessary to use switches that are rated at least 600 V to maintain the desirable design margin of 20%. In the prototype circuit implemented with GaN switches, a TPH3205WT ($V_{DS} = 600\,V$, $R_{DS} = 0.051\,\Omega$, $C_{OSS} = 108$ pF, $Q_{rr} = 138\,nC$, $V_F = 1.6$ V at 12 A) from Transphorm was used for each switch, whereas in the prototype circuit implemented with Si switches IPW65R048CFDA Si MOSFETs ($V_{DS} = 650$ V, $R_{DS} = 0.048\,\Omega$, $C_{OSS} = 350$ pF, $Q_{rr} = 1.8\,\mu$C, $V_F = 0.9$ V at 44 A) from Infineon were employed. It should be noted that the body diode of the employed GaN switch has much smaller reverse recovery charge compared to that of the Si device. However, forward voltage V_F of the GaN device is much higher than that of the Si device.

G. Control Implementation

Fig. 10 shows detailed control waveforms of the proposed series-resonant converter with delay-time control shown in Fig. 1. In this implementation, as shown in Fig. 10, primary switches S_{P2} and S_{P4} and secondary switch S_{S3} turn on together at $t = T_0$ (waveforms ① and ⑦), whereas primary switches S_{P1} and S_{P3} and secondary switch S_{S2} turn on together at $t = T_3$ (waveforms ② and ⑪). To implement the delay-time control, the zero crossing of resonant inductor current i_{LR} at $t = T_1$ should be detected for gating of switch S_{S3}, whereas the gating of switch S_{S2} requires zero-crossing detection of the inductor current at $t = T_4$. Generally, the sensing of the zero crossings of resonant current i_{LR} can be done by using a current transformer. However, at light loads, the magnitude of resonant current i_{LR} is too small to be used for reliable detection of the zero crossings. As a result, in this paper, the drain-to-source voltage waveforms of secondary-side switches S_{S2} and S_{S3} are used to indirectly determine the zero crossings.

This zero-current-detection method is based on the fact that at the zero crossings of the secondary current, the drain-to-source voltage of the secondary-side switch experiences an abrupt change without commutation delay. Specifically, for the zero crossings that occur when the secondary current changes from positive to negative, such that at $t = T_1$, the drain-to-source voltage of switch S_{S2}, V_{DS-SS2} (waveform ④), changes from V_O to zero because of the commutation of the secondary current from rectifier D_{S1} to antiparallel diode of switch S_{S2}. Similarly, for the zero crossings that occur at negative-to-positive secondary-current transitions, e.g., at $t = T_4$, the drain-to-source voltage of switch S_{S3}, V_{DS-SS3} (waveform ⑧), changes from V_O to zero because of the commutation of the secondary current from rectifier D_{S4} to antiparallel diode of switch S_{S3}.

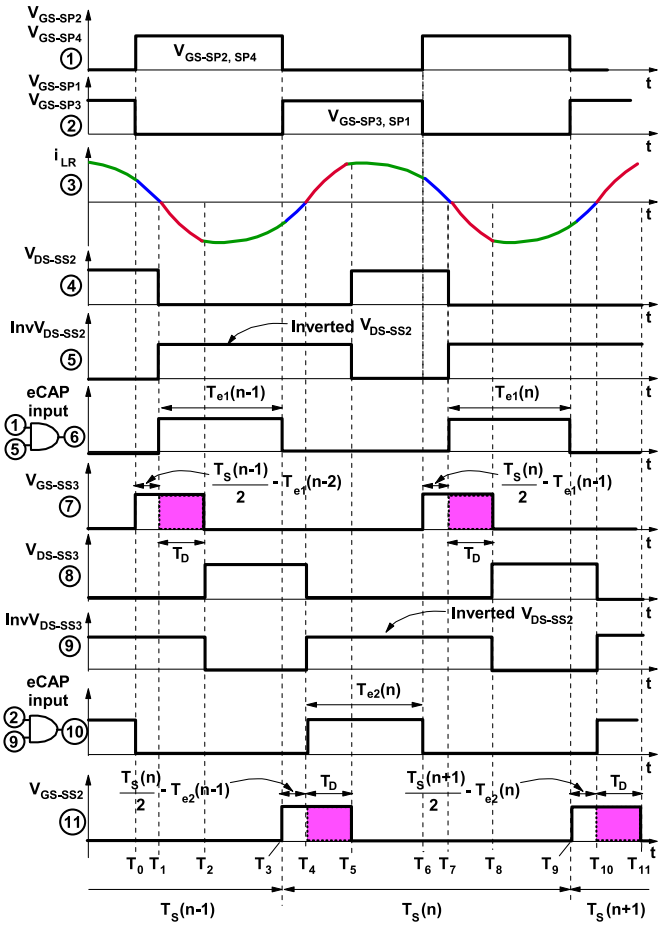

Fig. 10. Detailed control waveforms of the proposed series-resonant converter shown in Fig. 1.

In the digital implementation of the controller, the zero crossings can be determined by the time differences between the primary switch commutation instants and the instants the drain-to-source voltage of the corresponding secondary-side switch transitions from V_O to zero, i.e., by calculating the durations of time intervals $[T_1 - T_0], [T_4 - T_3], [T_7 - T_6]$, etc. For the calculation of these time intervals at positive-to-negative current transitions, the inverted signal of drain-to-source voltage V_{DS-SS2} (waveform ⑤) and gate-to-source voltage V_{GS-SP2} (waveform ①) are processed by the AND gate as shown in the (waveform ⑥) of Fig. 10. The output signal of the AND gate is read by Enhanced Capture (eCAP) Module of the microcontroller (TMS320F28069) that captures the pulse width and stores its value as T_{e1}. During the next switching cycle, the duration of the time intervals $[T_1 - T_0], [T_7 - T_6]$, etc., is calculated by subtracting T_{e1} from one half of the current switching period T_S, i.e., as $T_S[n]/2 - T_{e1}[n-1]$. Finally, the gate pulse width of switch S_{S3} is determined by the sum of the calculated time interval $(T_S/2 - T_{e1})$ and required delay time T_D, as shown in the waveform ⑦ of Fig. 10. It should be noted that although the duration of these time intervals changes over the input voltage, output voltage, and load range, they can be considered to be near constant during a single switching cycle since the voltage and load changes are much slower than the switching period. For

gating of switch S_{S2}, the time interval between primary switch gate transition at $t = T_3$ and zero crossing of resonant inductor current i_{LR} at $t = T_4$ should be calculated. For the calculation of this time interval, the inverted signal of drain-to-source voltage V_{DS-SS3} (waveform ⑨) and gate voltage V_{GS-SP1} (waveform ②) are processed by the AND gate as shown in the waveform ⑩ of Fig. 10. The gate pulse width of switch S_{S2} is determined by the sum of the calculated time interval $(T_S[n]/2 - T_{e2}[n-1])$ and required delay time T_D, as shown in the waveform ⑪.

It should be noted that in the control implementation in Fig. 10, secondary-side switches S_{S2} and S_{S3} are conducting only during time intervals that implement the delay-time control, i.e., they are not used as synchronous-rectifier switches. As a result, the body diodes of the switches are utilized as output rectifiers. In the battery-charging application, the reverse current (discharging current) from the output-side battery should be prevented from any accidental overlapping gate signals. As a result, secondary-side switches S_{S2} and S_{S3} are conducting only during the delay-time intervals. However, the control method in Fig. 10 can also be extended to synchronous implementation operation by extending the conduction of the secondary-side switches beyond that required by the delay-time control if an additional reverse current protection diode is connected in series.

The output control of the converter was implemented by a TMS320F28069 digital controller from TI. To implement the battery-charging profile, a CC, CP, and CV output control is employed. The flowchart of the employed control is shown in Fig. 11. It should be noted that converter starts with frequency soft start, i.e., the switching frequency starts from the maximum and gradually reduces until the output voltage reaches the desired level. At very light load, the converter enters burst-mode operation. As shown in the flowchart in Fig. 11, the burst-mode operation begins when switching frequency f_S that is continuously calculated by the DSP reaches burst-mode lower limit frequency f_{SL}, which in the prototype circuit is $f_S = f_{SL} =$ 350 kHz, and the burst-mode flag is set high. As switching frequency f_S continues to increase and reaches burst-mode higher limit frequency f_{SH}, i.e., $f_S = f_{SH} = 380$ kHz, all switches are turned off until calculated switching frequency f_S decreases to lower limit frequency f_{SL}. This frequency-hysteresis-based ON–OFF burst-mode operation continues until switching frequency f_S decreases below burst-mode lower limit frequency f_{SL}, when the burst-mode flag is reset and the converter resumes regular operation.

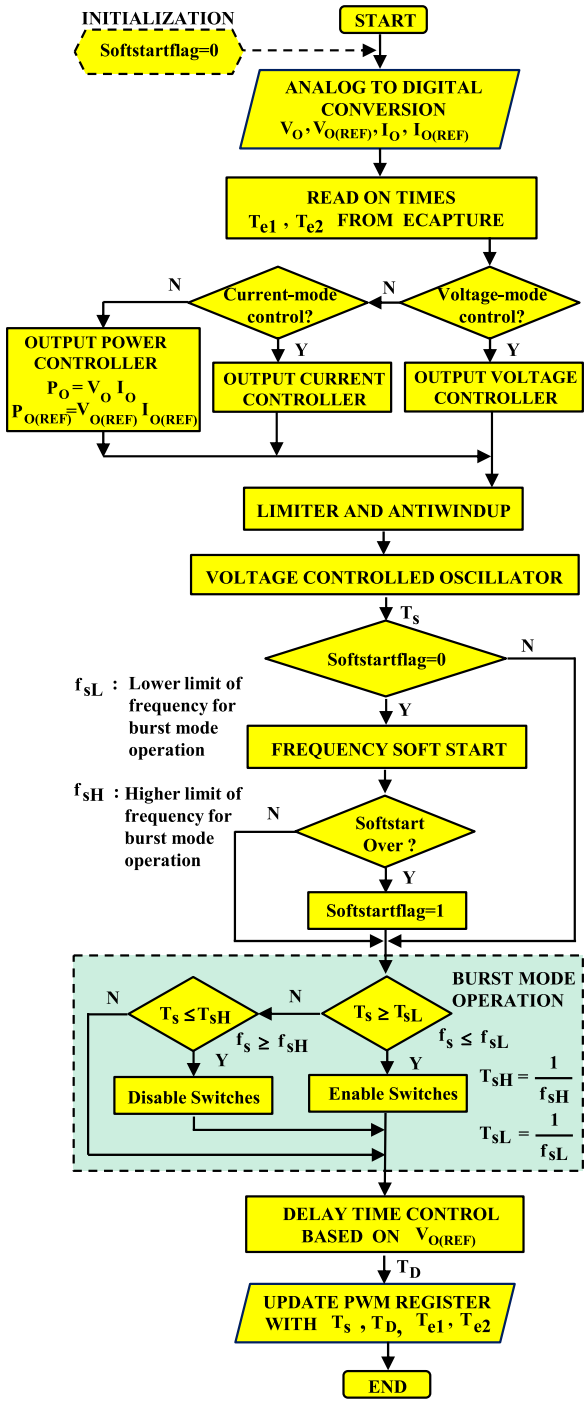

Fig. 11. Flowchart of the proposed control scheme.

V. Experimental Results

The performance of the proposed converter with the delay-time control shown in Fig. 1 was evaluated on a 3.3-kW prototype circuit that is designed to operate from a 400 V input and deliver power over 180–430 V output voltage range as described in Section IV. Fig. 12 shows a view of the OBCM with the cover removed. The on-board charger in Fig. 12 consists of the proposed dc–dc stage and the front-end power factor correction (PFC) stage which is not discussed in this paper.

Fig. 13 shows the circuit diagram along with component specifications. Two implementations of the prototype circuit were evaluated. One using TPH3205WT GaN switches (V_{DS} = 600 V, R_{DS}= 0.051 Ω, C_{OSS} = 108 pF, Q_{rr} = 138 nC, V_F = 1.6 V at 12 A) for all primary and secondary switches and the other employing IPW65R048CFDA Si MOSFET switches (V_{DS} = 650 V, R_{DS} = 0.048 Ω, C_{OSS} = 350 pF, Q_{rr} = 1.8 μC, V_F = 1.6 V at 44 A). Since in these implementations secondary switches S_{S1} and S_{S2} are not operated as synchronous rectifiers, their body diodes are utilized as output rectifiers.

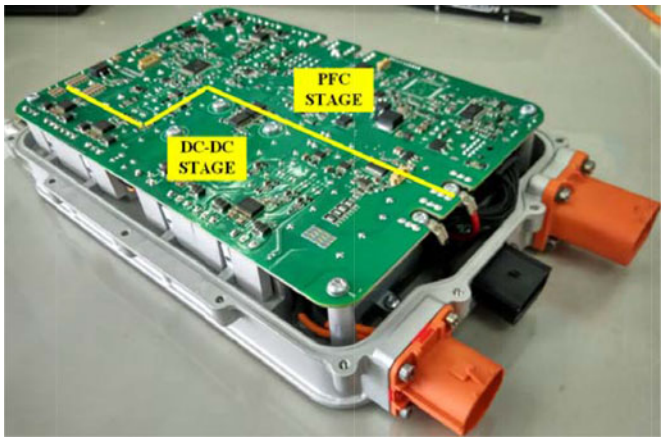

Fig. 12. Experimental prototype circuit.

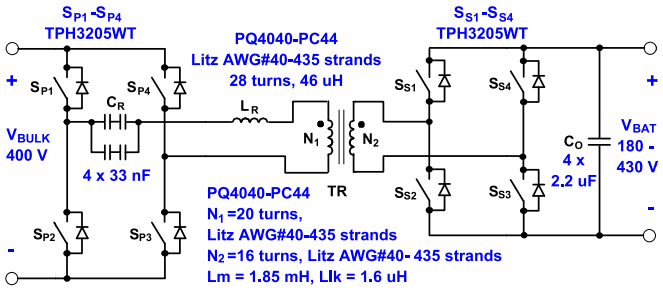

Fig. 13. Prototype circuit diagram with details of employed power components. It should be noted that all primary and secondary switches are GaN devices.

Fig. 14 shows the measured waveforms of gate and drain voltages of primary switch S_{P3}, resonant current i_{LR}, and resonant capacitor voltage V_{CR} of the experimental circuit when it delivers full power at 430, 320, 300, and 180 V output. The waveforms show ZVS of primary switch S_{P3}. Although Fig. 14 only shows waveforms of switch S_{P3}, the waveforms of all other primary switches are similar to that of switch S_{P3} and achieve ZVS as well. As shown in Fig. 14, during a half-switching period, the positive resonant inductor current continuously charges the resonant capacitor so that the voltage across resonant capacitor C_R increases from its negative to its positive peak, i.e., changes for $2V_{CR\_PK}$. The maximum peak capacitor voltage occurs at 300 V output as shown in Fig. 14(b), which is approximately 450 V. As a result, the rms voltage across each 33-nF resonant capacitor is approximately 159 V at 143 kHz.

Fig. 15 shows the measured waveforms of gate and drain voltages of secondary switches S_{S2} and S_{S3} of the experimental circuit when it delivers full power at 430, 320, 300, and 180 V output. As shown in Fig. 15, all the secondary switches operate with ZVS. Fig. 15 also shows delay time T_D. Delay time T_D is the period when both drain voltages of switches S_{S2} and S_{S3} are zero, i.e., both switches conduct and the secondary winding of TR is shorted. It should be noted that the turns ratio of transformer TR is chosen to make input-to-output control characteristic *M* equal to 1 when the output voltage is approximately 320 V. However, to properly regulate the output voltage with component tolerances as well as under transient

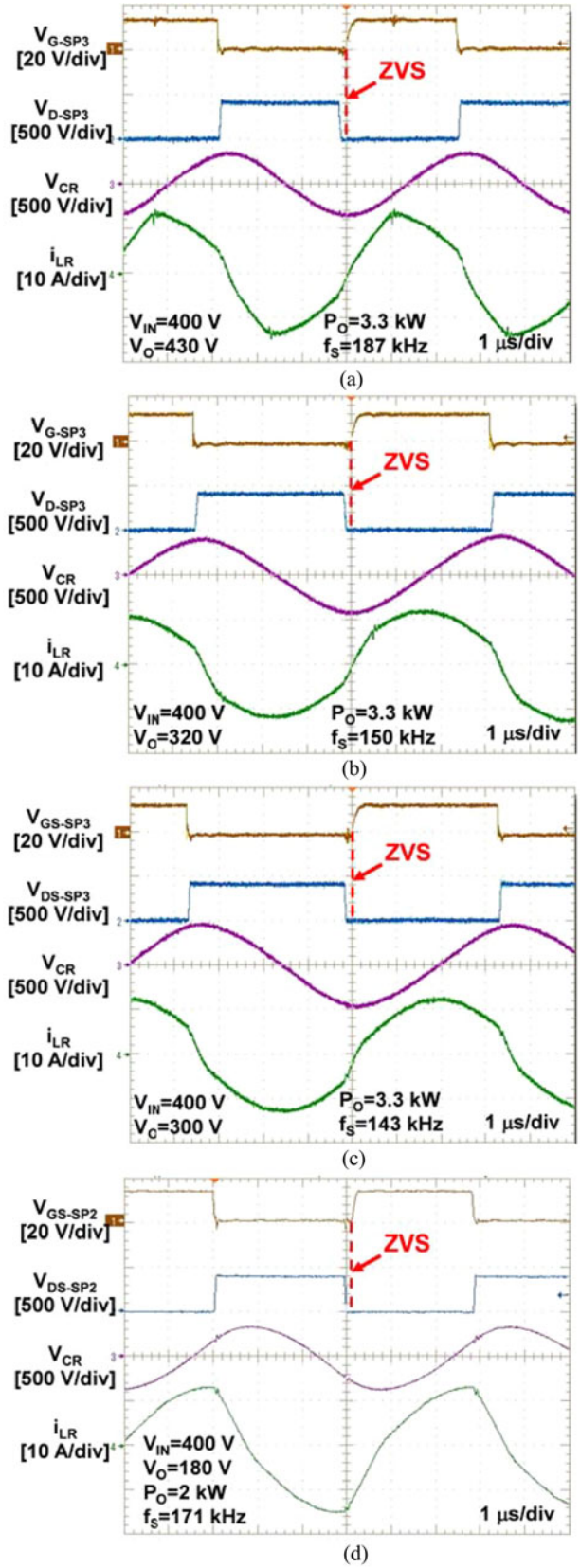

Fig. 14. Measured drain and gate voltage waveforms of primary switch S_{P2} voltage waveforms of resonant capacitor C_R and current waveform of resonant inductor L_R for output voltages: (a) 430 V, (b) 320 V, (c) 300 V, and (d) 180 V. Time scale is 1 μs/div.

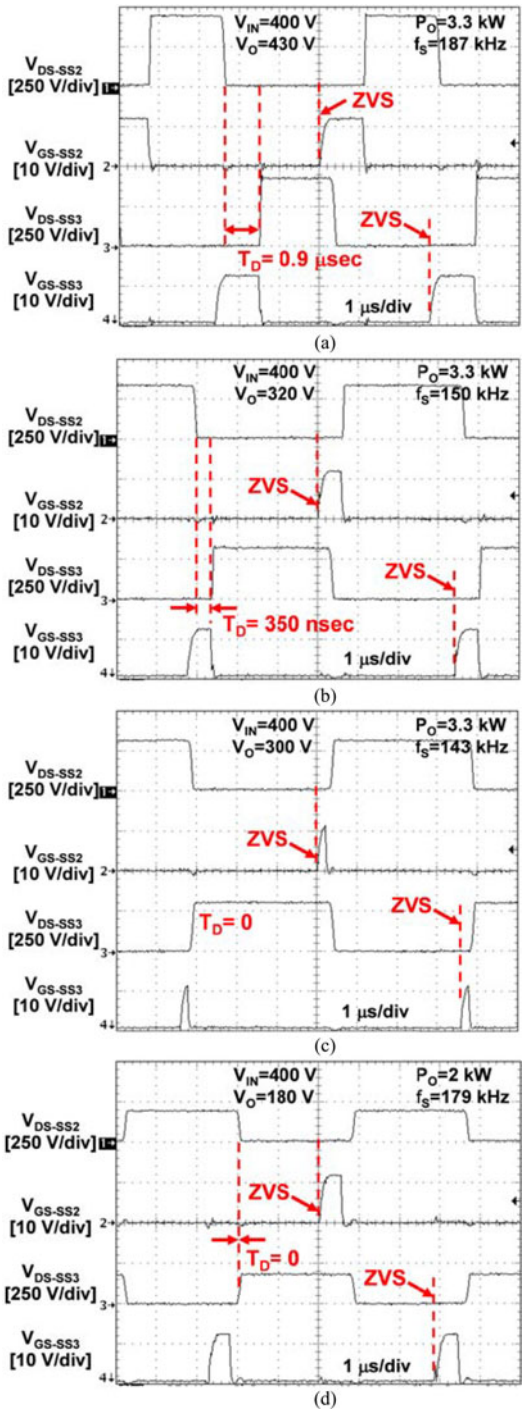

Fig. 15. Measured drain and gate voltage waveforms of secondary switches S_{S2} and S_{S3} for output voltages: (a) 430 V, (b) 320 V, (c) 300 V, and (d) 180 V. Time scale is 1 μs/div.

conditions, delay time T_D is introduced at approximately 300 V output. As a result, the delay time of the secondary switching is set to zero when the converter operates from 180 V to approximately 300 V output. When the output voltage increases above 300 V, the controller increases the delay time to provide the boost characteristic to maintain the output voltage regulation with the selected turns ratio of transformer TR.

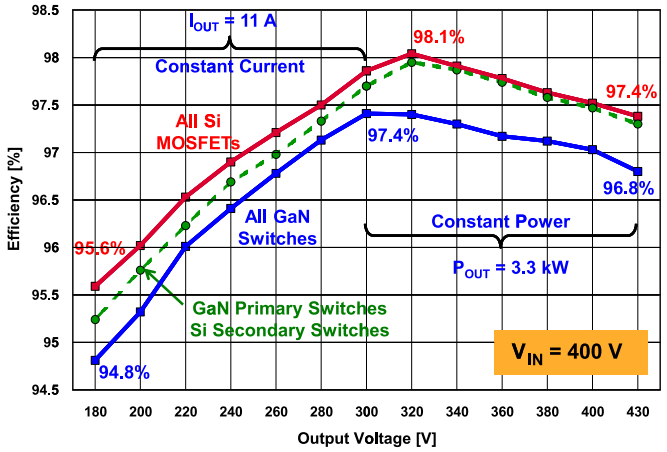

Fig. 16. Measured efficiencies of the experimental prototype as functions of output voltage. Efficiency measurement does not include control and gate-drive loss.

Fig. 16 shows the measured efficiency of the prototype converter as a function of the output voltage for both Si- and GaN-device implementations. The efficiency measurements in Fig. 16 do not include the measured 2.4-W loss of the control circuit and the gate-drive loss that is 1.7 and 2.35 W at 150 and 350 kHz, respectively. For both implementations, the prototype converter exhibits the best full-load efficiency when the output voltage is between 280 and 360 V, which is the operating range it most frequently operates. Specifically, the converter implemented with the Si devices exhibits the maximum full-load efficiency of 98.1% at 320 V output, whereas the maximum full-load efficiency of the GaN implementation is 97.4% at 300 V output. Slightly better efficiency of the Si-device implementation is attributed to a greater conduction loss of the body diode of the GaN switch. To support this conclusion, the measured efficiency of the prototype circuit that employs the GaN devices for primary switches $S_{P1}-S_{P4}$ and the Si devices for secondary switches $S_{S1}-S_{S4}$ is also shown in Fig. 16. As can be seen in Fig. 16, for the output voltages greater than 320 V, the efficiency of the implementations employing the Si secondary switches is higher compared to that with the GaN secondary switches and virtually independent of the choice of the primary switch. Since the major difference between the employed Si and GaN switches is in their body-diode forward-voltage drop, the lower efficiency of the GaN implementation is caused by significantly higher forward-voltage drop of the GaN device. For the output voltages below 320 V, the implementation with the primary-side GaN switches and secondary-side Si switches exhibits a slightly lower efficiency than that of all Si-switch implementation. This difference increases as the output voltage decreases and is around 0.35% at the minimum voltage of 180 V. This efficiency loss is also caused by the higher forward-voltage drop of the body diode of the GaN device. Namely, as the output voltage decrease from 300 to 180 V (CC mode), the switching frequency increases from 152 to 187 kHz, as shown in Fig. 17. Since the converter operates further away from the resonant frequency as the output voltage decreases, its circulating current also increases as the output voltage decreases. Because this

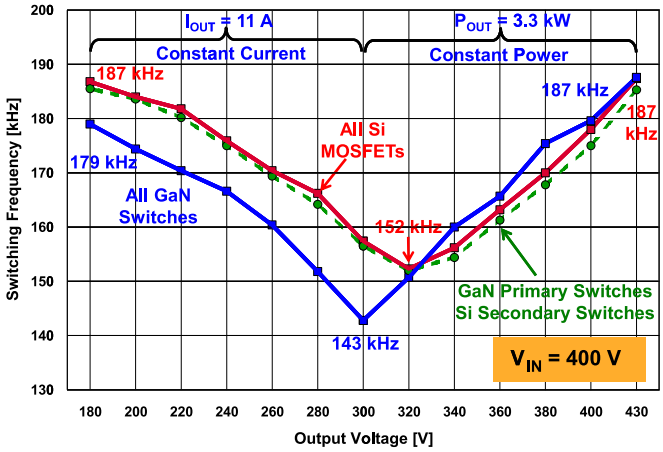

Fig. 17. Measured switching frequency of the experimental prototype as function of output voltage.

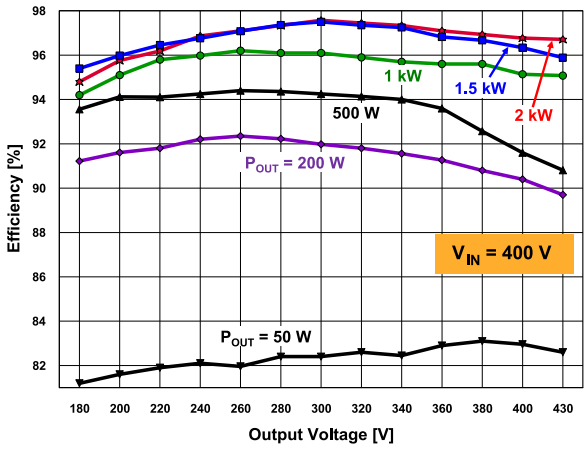

Fig. 19. Measured partial-load efficiencies of the experimental prototype implemented with GaN switches as functions of output voltage. Efficiency measurement does not include control and gate-drive loss.

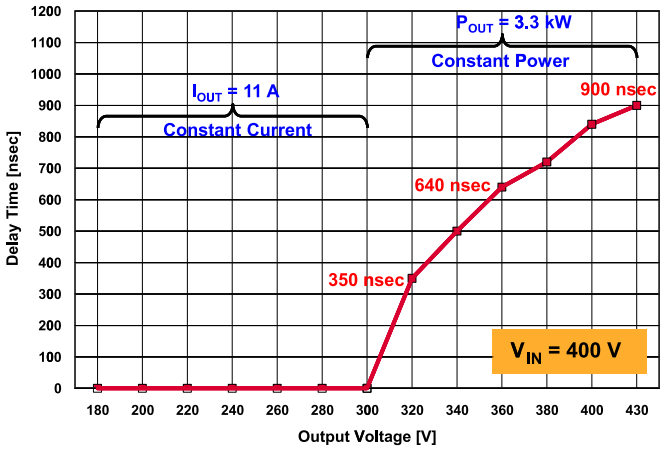

Fig. 18. Measured delay time T_D of the experimental prototype implemented with GaN switches as function of output voltage.

circulating current flows through the body diode of the primary switches, the primary switch loss with GaN switches is higher than that with the Si primary switches.

Fig. 17 shows the measured full-load switching frequency of the experimental prototype with Si and GaN devices as a function of the output voltage. The measured full-load switching frequencies are in a 143–187 kHz range over the entire output voltage range. It should be noted that for an output voltage below 300 V the switching frequency of the prototype with Si devices is slightly higher than that of the converter with GaN devices. Although both implementations operate without the delay-time control for output voltages below 300 V, the slow body diode of the Si MOSFETs introduce an effective delay time that causes the converter implemented with Si devices to regulate with higher switching frequency. The switching frequency of the prototype circuit that employs GaN devices for the primary switches and Si devices for the secondary switches is also measured and plotted in dashed line as shown in Fig. 17. The measured switching frequencies of the prototype circuit with Si secondary switches are similar to each other regardless of the primary switch type.

Fig. 18 shows the measured delay time as a function of the output voltage. The measured switching frequency and delay time shown in Figs. 17 and 18, respectively, are well matched with the calculated switching frequency and delay time shown in Fig. 9.

Finally, Fig. 19 shows measured partial-load efficiency of the prototype converter with GaN devices as a function of the output voltage. As can be seen from Fig. 19, across the entire output voltage range the prototype operates with efficiency greater than 94% when it delivers approximately 1 kW and above. It should be noted that the converter operates in burst mode at loads that are approximately 700 W and below. Due to the burst-mode operation, even at very light loads, the converters maintain a high efficiency across the entire input voltage range. Specifically, at the output power of 500 and 200 W, which are 15% and 6% of the full-load power, respectively, the converter operates with an efficiency greater than 90%. Furthermore, for P_O = 50 W, which is only 1.5% of the full-load power, the efficiency of the converter is still above 82%.

VI. Summary

In this paper, a control method that offers improved performance of series-resonant converters that operate with a wide input- and/or output voltage range by substantially reducing their switching frequency range has been introduced. Reduction in the switching frequency range is achieved by regulating the output voltage with a combination of closed-loop variable-frequency control of primary-side switches and open-loop delay-time control of secondary-side switches. The proposed converter is designed as the output stage of an OBCM that operates with a wide battery-voltage range. The delay-time control which is implemented by the modulation of secondary-side switches is used to assist the conventional variable-switching-frequency control of primary switches. The performance evaluation of the proposed series-resonant converter with

delay-time control was done on a 3.3-kW prototype delivering energy from 400-V bus, which is the output of the PFC front end, to a battery operating with voltage range between 180 and 430 V. The prototype circuit exhibits the maximum full-load efficiency of 98.1% with full-load and switching-frequency variation from 143 to 187 kHz over the entire output voltage range with full load.

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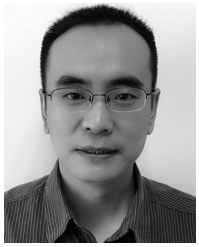

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