Extended Bandwidth Instantaneous Current Sharing Scheme for Parallel UPS Systems

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***Abstract*—This paper investigates the suitability of instantaneous average current sharing scheme (IACS) for the parallel operation of three-phase uninterruptible power supply systems. A discrete-time model is developed for the analysis and design of the control loops. Some key issues are discussed based on the model and it is found that there is a compromise between system stability and current sharing performance with the conventional IACS scheme when the lengths of interconnecting cables are not negligible. Subsequently, an improved IACS scheme is proposed that ensures proper current sharing by extending the close-loop bandwidth. Its performance is analytically predicted and subsequently validated by experimental results on a 15-kW laboratory prototype.**

***Index Terms*—Active damping (AD), instantaneous current sharing, parallel operation, resonant frequency, UPS systems.**

I. Introduction

REDUNDANCY and aggregate power requirements naturally lead to parallel operation of several uninterruptible power supply (UPS) units, often having similar characteristics and power ratings. However, parallel operation requires an effective control strategy to avoid circulating currents and ensure proportionate sharing of the total load current among the parallel dc/ac inverter units, both in steady state and transient conditions.

A traditional current-sharing solution is the frequency and voltage droop method [1]–[6], its chief appeal being communicationless control among inverter units. However, this technique has several drawbacks that limit its application. For instance, the conventional droop control requires the addition of virtual impedance, in series with the line, to decouple the real and reactive power flows. With nonlinear loads, the additional voltage drop on the virtual impedance degrades the voltage quality at the point of the common ac bus. Also, due to mismatched line impedance, reactive power cannot be shared accurately. Moreover, although it is possible to share harmonics currents of nonlinear loads by using harmonic droop coefficients [6], it requires the use of extra droop coefficients for each harmonic. Hence, this solution is limited to lower order harmonics due to poor dynamics of the method. However, recent reports [7]–[13] to overcome these limitations invariably depend on low-bandwidth communication among the inverters, which negates its original advantage.

In contrast to the droop control method, instantaneous average current sharing (IACS) schemes [14]–[17] offer wide control bandwidth by regulating the inverter output current in every switching cycle. This ensures proportional load current sharing under both dynamic and steady-state conditions, even with nonlinear loads. Although [14],[16] presents some analysis of the effect of line impedances on sharing performance, these are carried out in the continuous time domain. Hence, it provides an incomplete description of system behavior, especially when the inverters are switched at low frequency and the control law is realized on a digital platform.

This paper develops a discrete-time model which exactly incorporates digital pulse width modulation (PWM) and computation delays. Using this, it is shown that the conventional IACS gives best performance when multiple UPS units are directly connected to the common ac bus. But in many practical situations, the different UPS units can be located somewhat away from each other and, therefore, connected to the common ac bus through long cables, with considerable inductive impedance. Under such conditions, low inverter switching frequencies demand a tradeoff between system stability and current sharing performance. To overcome this limitation, an improved IACS scheme is proposed which extends the close-loop bandwidth while maintaining sufficient stability margins. Analytical derivation of the discrete-time control law is presented and validated by experimental results on a 2 $\times$ 7.5-kVA laboratory prototype.

II. System Configuration

Fig. 1 shows the conceptual layout of n parallel inverters being fed from a common dc power source. Each inverter, with its ripple filter and interconnecting cable, forms a basic unit of the multimodular three-phase UPS system. Each phase of the second-order ripple filter comprises a tuned pair, L_f and C_f, while r_f represents the internal resistance of the filter inductor. Per phase cable impedance of the pth inverter is denoted by $Z_p(= r_p + sL_p)$.

Modulation signals for pth three-phase inverter are synthesized by the voltage control scheme, consisting of inner active damping (AD) loop using the filter capacitor current i_{cp} feedback and outer capacitor voltage (v_{op}) feedback loop. The

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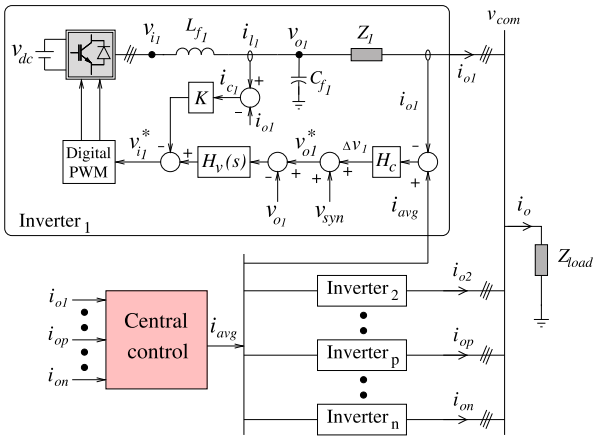

Fig. 1. Multimodular three-phase UPS inverter system.

TABLE I
NOMINAL SYSTEM PARAMETERS

L_f	C_f	r_f	f_{sw}	f_{samp}	ω_o
0.7 mH	50 μF	0.1 Ω	10 kHz	2 f_{sw}	2π.50 rad/s

Cable Parameters: $r_c = 4.95$ mΩ/m, $l_c = 0.8\,\mu$H/m

voltage control loop tracks the common synchronized reference v_{syn} along with correction signal Δv_p from the outer IACS loop [14]–[16] to minimize current imbalance among parallel units. The common current reference i_{avg} is the averaged signal of output currents from all inverters and i_{op} is output current from the pth inverter. Nominal parameters for an inverter unit are listed in Table I.

This double-loop voltage control structure has been used variously [14]–[17] to achieve the following control objectives:

(1) high relative stability: L_fC_f resonance damping;
(2) accurate tracking of reference voltage: unity gain, minimal phase shift;
(3) minimal regulation and voltage total harmonic distortion (THD): low-output impedance magnitude.

Details of the plant modeling and controller design criteria for the inner and outer control loops of the voltage controller are presented in the following section.

III. REVIEW OF DOUBLE-LOOP VOLTAGE CONTROLLER

Fig. 2(a) shows the block diagram representation of a voltage-controlled voltage source inverter (VSI) unit in the continuous-time domain. Three-phase inverter can be modeled as a linear amplifier with gain $v_{\text{dc}}/2$, where v_{dc} is the dc link voltage. For convenience, this gain is assumed unity. Low-frequency effect of inverter nonlinearities, such as dead-time and switching delays, is modeled as a disturbance voltage v_h [17]–[18]. From Fig. 2(a), the filter capacitor voltage $v_o(s)$ is expressed as

$$v_o(s) = G_{\text{ol}}(s)\, v_i^*(s) + G_{\text{ol}}(s)\, v_h(s) - Z_{\text{ol}}(s)\, i_o(s) \qquad (1)$$

where $v_i^*(s)$ is the control input and $v_h(s)$ and $i_o(s)$ are the disturbance inputs. $G_{\text{ol}}(s)$ and $Z_{\text{ol}}(s)$ are respectively the open-loop voltage gain and output impedance as expressed in Table II.

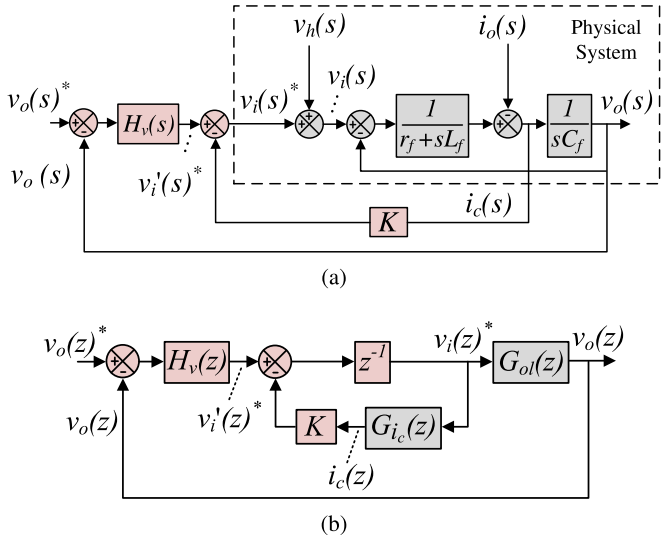

Fig. 2. Block diagram schematic of double-loop voltage control. (a) Continuous-time model. (b) Discrete-time model.

A. AD Loop

AD loop is generally realized using the filter inductor or capacitor current feedback. However, inductor current feedback has a less satisfactory performance than capacitor current feedback scheme in terms of load-current disturbance rejection capability [19], [20]. Therefore, AD through the filter capacitor current is the preferred approach.

The resultant plant transfer functions after closing the capacitor current-based AD loop are expressed in Table II. From expressions, the natural frequency and damping ratio, respectively, are

$$\omega_f = 1/\sqrt{L_fC_f} \quad \text{and} \quad \zeta = \{(r_f + K)/2\}\sqrt{C_f/L_f}. \qquad (2)$$

Obviously, the resonance peak reduces monotonically with increasing AD coefficient (K), implying an arbitrarily high K leads to a better damped system as well as lower output impedance around resonance frequency. Although a larger K increases the phase shift in G'_{ol} at the operating frequency, this can however be compensated by the outer voltage loop.

B. Voltage Control Loop

The design of the voltage controller $H_v(s)$ is based on the resultant plant $G'_{\text{ol}}(s)$ listed in Table II. For this minimum-phase plant, zero steady-state error is theoretically ensured with infinite loop gain at the operating frequency. Since conventional proportional-integral controller ensures zero steady-state error for dc references only, perfect command following requires mapping the operating frequency to dc, through a synchronous reference frame transformation. However, this approach requires dedicated phase synchronization, forward and inverse axis transformation for all measured variables and vector decoupling stages for proper realization [21], [22]. This additional complexity in control realization is totally avoided with the proportional resonant (PR) controller which is hence considered here.

TABLE II
TRANSFER FUNCTIONS DERIVED FROM VOLTAGE CONTROL LOOP

	Control Voltage Gain	Disturbance Voltage Gain $\{v_o(s)/v_h(s)\}$	Output Impedance $\{v_o(s)/i_o(s)\}$
Open-loop transfer functions	$G_{\text{ol}}(s) = v_o(s)/v_i^*(s) = 1/\delta(s)$ where, $\delta(s) = L_f C_f s^2 + r_f C_f s + 1$	$G_{\text{ol}}(s)$	$Z_{\text{ol}}(s) = (r_f + sL_f)/\delta(s)$
Plant after Closing the AD Loop	$G'_{\text{ol}}(s) = \frac{v_o(s)}{v_i'^*(s)} = \frac{1}{\delta(s) + sKC_f}$	$G'_{\text{ol}}(s)$	$Z'_{\text{ol}}(s) = \frac{r_f + sL_f}{\delta(s) + sKC_f}$
Closing the Voltage Control Loop	$G_{\text{cl}}(s) = \frac{v_o(s)}{v_o^*(s)} = \frac{G'_{\text{ol}}(s)H_v(s)}{1 + G'_{\text{ol}}(s)H_v(s)}$	$G_{h\_\text{cl}}(s) = \frac{G'_{\text{ol}}(s)}{1 + G'_{\text{ol}}(s)H_v(s)}$	$Z_{\text{cl}}(s) = \frac{Z'_{\text{ol}}(s)}{1 + G'_{\text{ol}}(s)H_v(s)}$

Since an ideal PR controller requires infinite gain at the fundamental frequency, it inevitably leads to numerical overflow when realized with fixed-point processors. Hence, its realizable form [23] is considered and is expressed by

$$H_v(s) = k_p + k_i \frac{s + \omega_c}{(s + \omega_c)^2 + \omega_r^2} \tag{3}$$

where k_p, k_i are the proportional and integral constants for the resonant frequency ω_r, and ω_c is the low-frequency cutoff that limits the peak controller gain. The closed-voltage loop transfer functions are expressed in Table II.

IV. DISCRETE-TIME DESIGN OF DOUBLE-LOOP VOLTAGE CONTROLLER

Controller design is based on the forward and feedback path transfer functions only, which are obtained by setting the disturbance inputs, i_o and v_h, to zero. The discrete-time plant model $G(z)$ is derived from the zero-order-hold (ZOH) equivalent [24] of the continuous-time physical plant, conveniently described by its transfer function $G(s) = y(s)/x(s)$. Thus

$$G(z) \triangleq y(z)/x(z) = (1 - z^{-1})\mathcal{Z}\{G(s)/s\}. \tag{4}$$

This analysis requires the ZOH equivalents of $G_{\text{ol}}(s)$, expressed in Table II, and $G_{i_c}(s)$, defined as

$$G_{i_c}(s) \triangleq i_c(s)/v_i^*(s) = sC_f v_o(s)/v_i^*(s) = sC_f G_{\text{ol}}(s). \tag{5}$$

Using (4), $G_{\text{ol}}(z)$ and $G_{i_c}(z)$ are obtained with a sampling period of $T = 1/f_{\text{samp}}$ as

$$G_{\text{ol}}(z) = \frac{a_{v1}z + a_{v0}}{\Delta(z)} \quad \text{and} \quad G_{i_c}(z) = \frac{a_v(z-1)}{\Delta(z)} \tag{6}$$

where $\Delta(z)$ and coefficients a_v, a_{v0}, a_{v1} are expressed in the Appendix. Applying the Tustin transformation [24] to (3), the equivalent discrete-time controller is given as

$$H_v(z) = k_p + \frac{k_i T\{T\omega_c(z+1)^2 + 2(z^2-1)\}}{(b_v + 4\omega_c T + 4)z^2 + 2(b_v - 4)z - 4\omega_c T + 4} \tag{7}$$

where b_v is defined in Appendix. Fig. 2(b) shows the dual-loop voltage controller, modeled in z-domain, where the unit delay (z^{-1}) in the forward path accounts for computation delay.

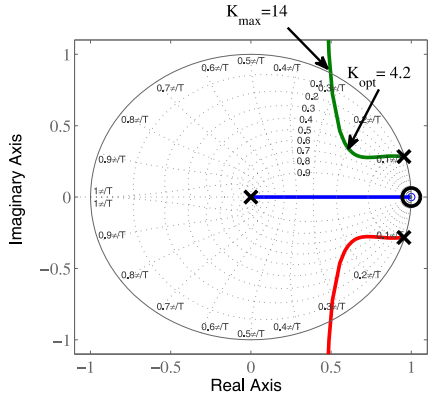

Fig. 3. Root locus of $1 + T_{\text{ic}}(z)$ with varying K.

TABLE III
VOLTAGE CONTROLLER PARAMETERS

K	k_p	k_i	ω_r	ω_c	ω_{bw}	$\%e_{ss}$
4.2	0.8	3400	ω_o	20 rad/s	5400 rad/s	1

A. Selection of AD Coefficient

From Fig. 2(b), the loop gain of the AD loop is

$$T_{\text{ic}}(z) = Kz^{-1}G_{i_c}(z). \tag{8}$$

Applying Jury's stability criterion to the characteristic equation $1 + T_{\text{ic}}(z) = 0$, a maximum limit K_{max} for K is found as

$$K < 1/a_v = K_{\text{max}} \tag{9}$$

which sharply contrasts with the absence of upper bound in continuous-time analysis. Although (9) defines the maximum limit, it does not necessarily ensure the best possible damping, quite unlike the continuous-time system.

A root locus pole placement strategy was used to determine the value of K that ensures maximal damping. Fig. 3 shows the root locus diagram, where the resonant poles move deeper inside the unit circle, but eventually diverges out as the damping coefficient K increases further. Clearly, there is an optimal value $K = K_{\text{opt}}$ which ensures maximum damping factor. This is listed in Table III.

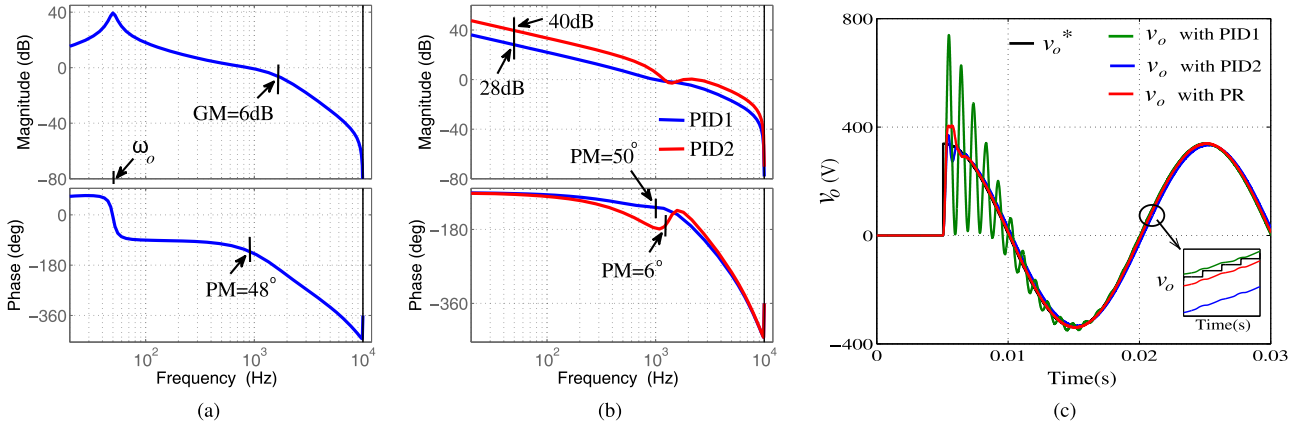

Fig. 4. Frequency response of $T_{\text{vo}}(z)$ with (a) PR controller (b) PID controller. (c) Transient and steady-state response of voltage controller.

B. Selection of Voltage Controller Parameters

Closing the inner AD loop gives the plant transfer function for the outer voltage control loop as

$$G'_{\text{ol}}(z) = z^{-1}G_{\text{ol}}(z)/\{1 + T_{i_c}(z)\} \tag{10}$$

and the corresponding loop gain is given as

$$T_{\text{vo}}(z) = z^{-1}G_{\text{ol}}(z)H_v(z)/\{1 + T_{i_c}(z)\}. \tag{11}$$

Within the parameter set $\{k_p, k_i, \omega_c, \omega_r\}$ of $H_v(z)$, appearing in (7), ω_r is set equal to the fundamental operating frequency ω_o to provide high open-loop gain at ω_o. Also, ω_c must be at least a decade lower than the resonant frequency ω_r to ensure integrator characteristic around ω_o [23]. Using (11), k_p and k_i are obtained from the criteria of allowable steady error e_{ss} at ω_o and required close-loop bandwidth ω_{bw}. These criteria are mathematically represented as

$$|1 + T_{\text{vo}}(z \to e^{j\omega_o T})| = 1/e_{\text{ss}} \tag{12}$$

$$|T_{\text{vo}}(z \to e^{j\omega_{\text{bw}} T})| = 1. \tag{13}$$

For a specific choice of e_{ss} and ω_{bw}, the corresponding values of the controller parameters are listed in Table III.

Fig. 4(a) shows the frequency response of $T_{\text{vo}}(z)$, where, clearly, a high gain (40 dB) at the fundamental operating frequency ω_o is ensured by the PR controller at a specified bandwidth with adequate stability margins.

C. Comparison With PID Controller

Since, arguably, satisfactory close-loop performance could be achieved with a conventional proportional-integral-derivative (PID) controller [17], a comparative evaluation is provided to highlight the advantages with the PR algorithm. Starting with the continuous-time PID algorithm

$$H'_v(s) = k'_p + k'_i/s + k_d s. \tag{14}$$

Its discrete-time equivalent, amenable for digital realization, is obtained as follows. The integral term in (14) is discretized using the Tustin approach, while backward-Euler method is used for the derivative term. This is necessary since the Tustin map of the differentiator yields infinitely large magnitude response at the Nyquist frequency, which leads to system instability [25], [26].

TABLE IV
PID PARAMETERS

PID1:	$k'_p = 1,$	$k'_i = 8000,$	$k_d = 0.00014$
PID2:	$k'_p = 0.4,$	$k'_i = 30\,000,$	$k_d = 0.0004$

Comparison with the PR algorithm, under the given operating conditions, is carried out using two complementary design approaches. Objective of the first design (PID1) is to minimize steady-state error, with the constraint of exact match with the stability margin and bandwidth obtained with the PR. The second approach (PID2) interchanges the objective and constraints of PID1, with the problem specified as one of maximization and the equality constraint on steady-state error fixed at 1%.

PID parameters with both approaches are listed in Table IV and Fig. 4(b) shows the corresponding frequency responses of $T_{\text{vo}}(z)$, obtained using (11). It is clearly observed that the equality constraints are satisfied in both cases. In case of PID1, the loop gain at ω_o is 28 dB which is equivalent to 4% steady-state error as evidenced from (12). In contrast, PID2 results in a marginally stable system and slight variations in plant parameters are liable to cause instability.

Fig. 4(c) shows simulated waveforms of the output voltages (phase "a"), obtained with the PR and the two PID variants as the voltage controller. Transient performance is investigated by applying a 100% step change in the reference voltage, under no-load condition. It is clear that PID1 ensures smooth voltage transition as compared to PID2 whereas in steady state, PID2 gives better reference tracking performance. In contrast, PR ensures smooth voltage transition as well as good reference tracking performance.

In conclusion, both the control specifications, viz., very low steady-state error and adequate stability margin, together cannot be met by the PID controller at the given switching/sampling frequency. In contrast, the resonant characteristics of the PR controller enable arbitrary reduction in the steady-state error without compromising system stability.

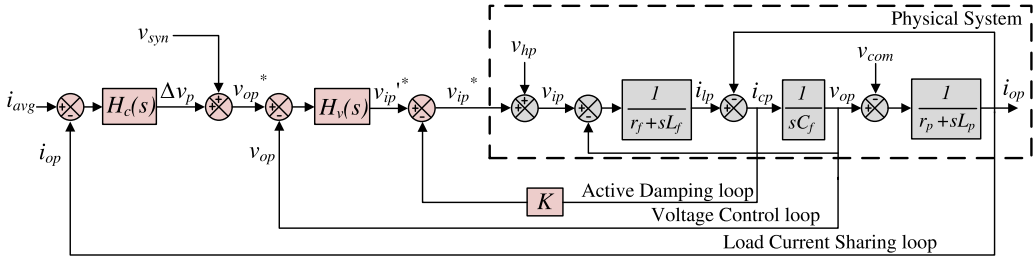

Fig. 5. Per phase schematic of complete control loop for pth inverter.

V. Conventional IACS Scheme

The current sharing loop, as shown in Fig. 1, ensures proportional current sharing among the parallel units. Current reference i^*_{op} for the pth inverter is derivable from the instantaneous weighted average of the load current [15]. In this paper, without loss of generality, all inverters are considered to be of identical rating. Hence

$$i^*_{\text{op}} = \frac{1}{n}\left(\sum_{k=1}^{n} i_{\text{ok}}\right) \triangleq i_{\text{avg}} \tag{15}$$

which is identical for the other $n-1$ inverters.

To track the current command i_{avg}, current sharing controller $H_c(s)$ generates a correction voltage term Δv_p. The voltage control loop tracks the common synchronized reference v_{syn} along with correction signal Δv_p.

To enable performance evaluation of the current-sharing loop, the equivalent control schematic for the pth inverter is shown in Fig. 5. Details of the plant modeling and design criteria for the current sharing loop are presented in the following sections.

A. Plant Modeling

Output voltage for the pth inverter is expressed in terms of its cable impedance $Z_p = r_p + sL_p$ as

$$v_{\text{op}}(s) = i_{\text{op}}(s)Z_p + v_{\text{com}}(s). \tag{16}$$

Using (16) in (1), $i_{\text{op}}(s)$ is given as

$$i_{\text{op}}(s) = Y_{i_{\text{op}}}(s)v^*_{\text{ip}}(s) + Y_{i_{\text{op}}}(s)v_{hp}(s) - \frac{Y_{i_{\text{op}}}(s)}{G_{\text{ol}}(s)}v_{\text{com}}(s) \tag{17}$$

where $Y_{i_{\text{op}}}(s)$ is the open-loop admittance, defined as

$$Y_{i_{\text{op}}}(s) \triangleq i_{\text{op}}(s)/v^*_{\text{ip}}(s) = G_{\text{ol}}/(Z_{\text{ol}} + Z_p). \tag{18}$$

Closing the AD and voltage control loop

$$i_{\text{op}}(s) = \frac{G_{\text{cl}}(s)}{Z_{\text{tp}}(s)}\Delta v_p(s) + \frac{G_{h\_\text{cl}}(s)}{Z_{\text{tp}}(s)}v_{\text{hp}}(s) + \frac{G_{cl}(s)}{Z_{\text{tp}}(s)}v_{\text{syn}}(s) - \frac{v_{\text{com}}(s)}{Z_{\text{tp}}(s)} \tag{19}$$

where

$$Z_{\text{tp}}(s) = Z_{\text{cl}}(s) + Z_p(s) \tag{20}$$

is the equivalent Thevenin impedance viewed from the pth inverter output, toward the common load bus. Close inspection of (19) reveals three useful observations.

The first term can be used to define the plant transfer function for the current sharing loop as

$$Y'_{i_{\text{op}}}(s) \triangleq i_{\text{op}}/\Delta v_p = G_{\text{cl}}(s)/Z_{\text{tp}}(s). \tag{21}$$

The second term represents the low-order harmonic circulating current, excited by the harmonic output voltage v_{hp}. Moreover, Z_{tp} appears in the denominator and since, from Table II

$$|Z_{\text{cl}}(j\omega)| \ll |Z_{\text{ol}}(j\omega)|, \quad \forall\, \omega < \omega_{\text{bw}} \tag{22}$$

the low-order harmonic circulating currents are amplified.

Also, since G_{cl} has unity gain and zero-phase shift at fundamental frequency, the third term in (19) almost cancels with the fundamental component of the fourth term. Consequently, only the harmonic components in the fourth term remain, especially under nonlinear load conditions. The voltages v_{hp} and v_{com} are therefore regarded as disturbance inputs. Hence, minimization of the transfer gains $i_{\text{op}}/v_{\text{hp}}$ and $i_{\text{op}}/v_{\text{com}}$, at fundamental and harmonic frequencies, are additional specifications for the design of H_c.

B. Current Sharing Loop

Closing the current sharing loop gives the load current for pth inverter as

$$i_{\text{op}} = \frac{Y'_{i_{\text{op}}}H_c}{1+Y'_{i_{\text{op}}}H_c}i_{\text{avg}} + \frac{G_{h\_\text{cl}}}{Z_{\text{tp}}(1+Y'_{i_{\text{op}}}H_c)}v_{\text{hp}} + \frac{G_{cl}}{Z_{\text{tp}}(1+Y'_{i_{\text{op}}}H_c)}v_{\text{syn}} - \frac{1}{Z_{\text{tp}}(1+Y'_{i_{\text{op}}}H_c)}v_{\text{com}}. \tag{23}$$

From (23), any design of H_c which satisfies

$$\left|Y'_{i_{\text{op}}}(j\omega)H_c(j\omega)\right| \gg 1, \quad \omega \le \omega'_{\text{bw}} \tag{24}$$

requires maximal bandwidth ω'_{bw} for good reference tracking and disturbance rejection.

Due to efficiency advantages with low inverter switching frequency, a high bandwidth controller designed in the continuous time domain is additionally prone to instability, if the control laws are realized on a digital platform. Since PWM and computation delays crucially affect system stability, a discrete-time model is obtained for better portrayal of system dynamics.

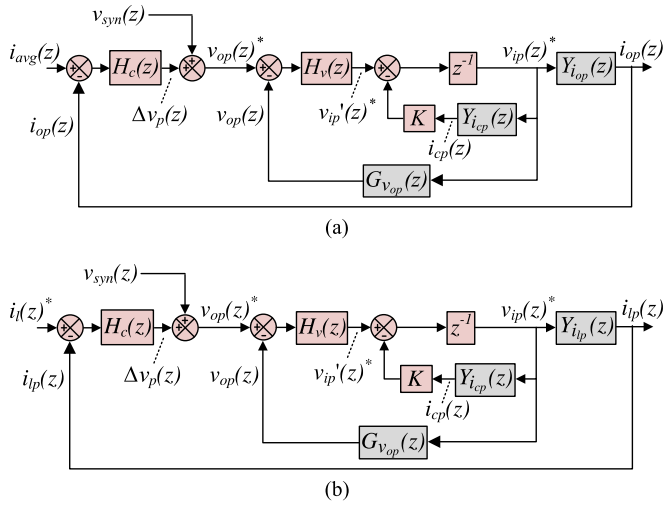

Fig. 6. Discrete-time close-loop schematic. (a) Conventional IACS scheme. (b) Proposed IACS scheme.

VI. Discrete-Time Analysis of Conventional IACS Scheme

From (16) and (17)

$$G_{v_{\text{op}}}(s) \triangleq \frac{v_{\text{op}}(s)}{v_{\text{ip}}^*(s)} = \frac{Z_p(s)G_{\text{ol}}(s)}{Z_{\text{ol}}(s)+Z_p(s)} \tag{25}$$

$$Y_{i_{\text{cp}}}(s) \triangleq i_{\text{cp}}(s)/v_{\text{ip}}^*(s) = sC_f G_{v_{\text{op}}}(s). \tag{26}$$

There are three feedback loops therefore three z-domain transfer function viz. $G_{v_{\text{op}}}(Z)$, $Y_{i_{\text{op}}}(z)$, and $Y_{i_{\text{cp}}}(z)$ are required to obtain the discrete-time model of the Conventional IACS scheme. These are obtained by applying (4)–(18), (25) and (26). Fig. 6(a) shows the close-loop schematic, modeled in the z-domain, from which the plant transfer function is

$$Y'_{i_{\text{op}}}(z) = Y_{i_{\text{op}}}(z)H_v(z)/\{z + KY_{i_{\text{cp}}}(z) + G_{v_{\text{op}}}(z)H_v(z)\} \tag{27}$$

and loop gain for the current sharing loop is expressed as

$$T_{i_{\text{op}}}(z) = H_c(z)Y'_{i_{\text{op}}}(z). \tag{28}$$

Suitability of the conventional IACS is now investigated for multiple UPS units connected to a common ac bus either directly (short cables) or through long cables of unequal length. For even comparison, loop gain frequency response plots, for both applications, are obtained for identical stability margins ($PM \approx 45^\circ$; $GM \approx 6$ dB). Exact expressions are used for arriving at the graphical results, but the analysis includes justified assumptions to enable physical insight.

Length normalized (per unit length) cable resistance and inductance were realistically assumed to be identical but different cable lengths for individual UPS units are considered both in analysis and experimental evaluation. Numerical values of normalized cable parameters are listed in Table I.

A. UPS Paralleled Through Very Short Cables

In practice, all UPS modules are installed in close proximity, implying the impedances of connecting cables to the common ac bus are negligible as compared to the output impedance Z_{cl}. So, plant transfer function for the current sharing loop of the pth inverter is obtained using (20) and (21) and further simplified using Table II as

$$Y'_{i_{\text{op}}}(s) = G'_{\text{ol}}(s)H_v(s)/Z'_{\text{ol}}(s) = H_v(s)/(r_f + sL_f). \tag{29}$$

Retaining $H_v(s)$ as in (3), the plant of (29) has very high gain within the operating bandwidth, which ensures minimal close-loop steady-state error. Furthermore, since $H_v(s)$ approaches k_p in the mid and high-frequency regions, the phase response monotonically converges to -90°. So, even a proportional controller, $H_c(s) = K_c$, is adequate to ensure arbitrary gain cross-over frequency without compromising stability. PWM and computational delay in a digital realization of the same control law however introduce significant additional phase delay around the Nyquist frequency, obviously greater than the close-loop bandwidth. Hence, the phase plot of the loop gain $T_{i_{\text{op}}}(z) = K_c Y'_{i_{\text{op}}}(z)$ converges to -180°, as shown in Fig. 7(a) obtained for cable length L_c of 1 m. Clearly, a bandwidth of 2 kHz is achieved without compromising system stability. Thus, closed-loop bandwidths of similar order as the inverter switching frequency are achievable when cable impedance is negligible.

B. UPS-Paralleled Through Long Cables

Expressing the open-loop admittance function (18) in terms of physical parameters

$$Y_{i_{\text{op}}}(s) = \frac{1}{(r_p + sL_p)\{L_f C_f s^2 + r_f C_f s + 1\} + r_f + sL_f}. \tag{30}$$

The resulting third-order equation does not yield a general solution. So a conservative evaluation (minimal damping) is obtained by considering $r_f = 0$ and then solving for predominantly inductive ($r_p \to 0$) cable impedance. It gives

$$Y_{i_{\text{op}}}(s) = \frac{1}{L_f + L_p}\frac{\omega_1^2}{s(s^2+\omega_1^2)} \tag{31}$$

where ω_1 is the natural frequency of $L_f - C_f - L_p$ resonance and is dependent on cable parameters, as evident from its expression in Table V. Moreover, achieving a high close-loop bandwidth is extremely difficult with the third-order physical system, since at ω_1 its phase plot sharply drops from -90° to -270°, and even further to -360° with digital sampling. This is evident from Fig. 7(b) which shows the frequency response of the loop gain $T_{i_{\text{op}}}(z)$ for 50-m long cable. Clearly, the presence of *LCL* resonance at 3.8 kHz has restricted the close-loop bandwidth and it is reduced by 75% as compared to the ideal situation of zero cable impedance. Similarly Fig. 7(c) shows the loop-gain frequency response for 100-m long cable where slight increment is observed in close-loop bandwidth due to the increased system damping. But it is still well below than ideal case.

VII. Proposed IACS Scheme

As the loop-gain phase plot transits from -90° to -360°, it is an unconditionally unstable situation for all controller gains.

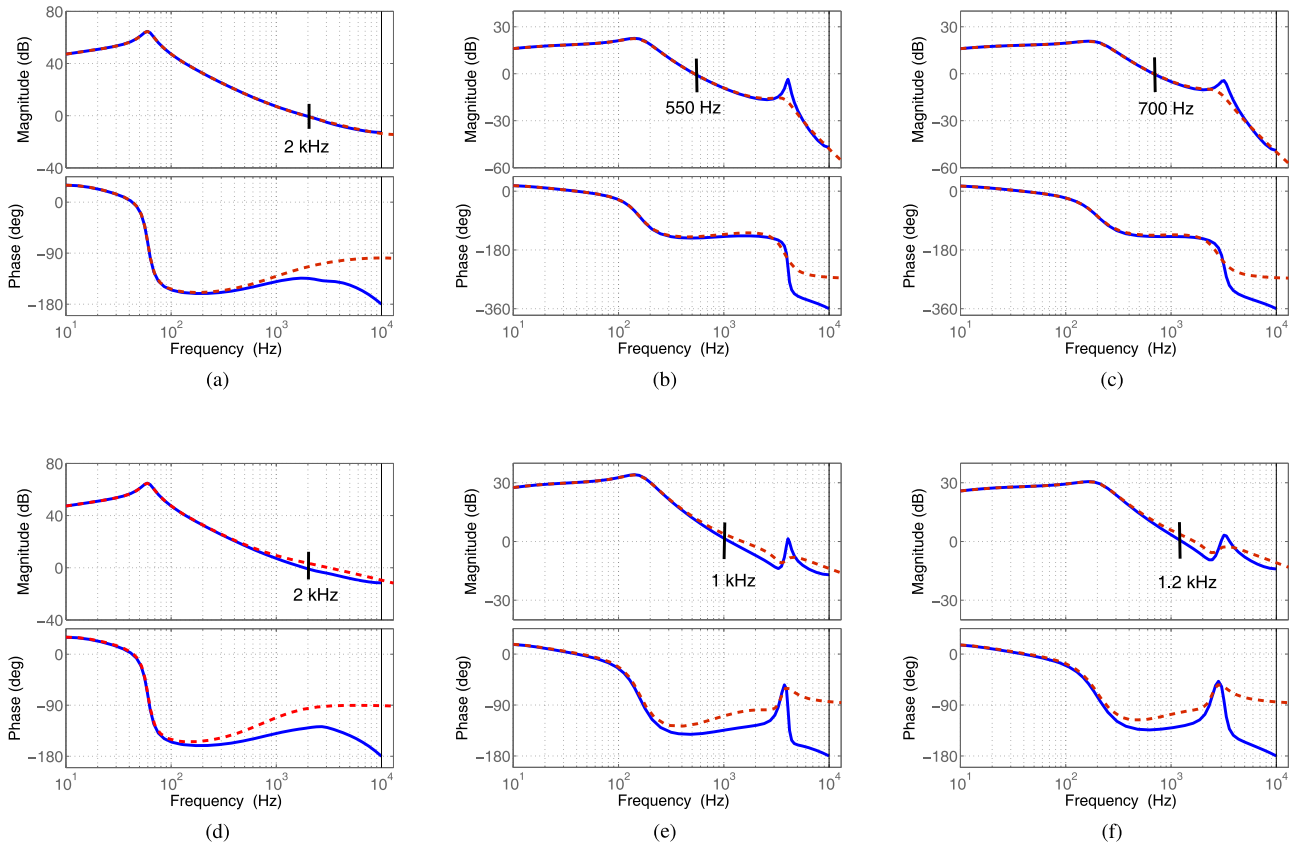

Fig. 7. Frequency response of $T_{i_{op}}$ (a)–(c). Frequency response of $T_{i_{lp}}$ (d)–(f). Continuous-time response: dashed curve, discrete-time response: solid curve. (a) Ideal case $L_c = 1$ m, $H_c = 12$. (b) $L_c = 50$ m, $H_c = 2$. (c) $L_c = 100$ m, $H_c = 3$. (d) Ideal case $L_c = 1$ m, $H_c = 12$. (e) $L_c = 50$ m, $H_c = 7.5$. (f) $L_c = 100$ m, $H_c = 9.5$.

Sharpness of the high-frequency phase roll-off, due to *LCL* resonance and digital sampling, can be softened by increasing the AD coefficient but it is already at its optimal value. Incorporating a lead compensator in $H_c(z)$ gives insufficient phase lead (maximum 90°) while the minimum requirement is 180°. To resolve this problem, this paper modifies the conventional IACS scheme as follows.

Expressing (26) in terms of physical system parameters for the predominating inductive cables as

$$Y_{i_{\rm cp}}(s) = \{L_p C_f \omega_1^2/(L_f + L_p)\} s/(s^2 + \omega_1^2). \tag{32}$$

Using (31), (32) can be expressed as

$$Y_{i_{\rm cp}}(s) = s^2 L_p C_f Y_{i_{\rm op}(s)} \tag{33}$$

rearranging which

$$Y_{i_{\rm cp}}(s) + Y_{i_{\rm op}}(s) \triangleq \frac{i_{\rm lp}(s)}{v^*_{\rm ip}(s)} = (s^2 L_{\rm p} C_f + 1) Y_{i_{\rm op}}(s). \tag{34}$$

Using (31), (34) is expressed as

$$\frac{i_{\rm lp}(s)}{v^*_{\rm ip}(s)} = \frac{\omega_1^2}{\omega_2^2 (L_{\rm p} + L_f)} \frac{s^2 + \omega_2^2}{s(s^2 + \omega_1^2)} \tag{35}$$

where ω_2 is the natural frequency of the $L_p - C_f$ antiresonance and its expression is listed in Table V.

TABLE V
NATURAL FREQUENCIES AND THEIR RELATIONSHIP

ω_1	ω_2	ω_2/ω_1
$\omega_f \sqrt{(L_f + L_p)/L_p}$	$1/\sqrt{(L_p C_f)}$	$\sqrt{L_f/(L_p + L_f)}$

Both (31) and (35) have third-order denominators but (35) has an additional antiresonance term. From the last column of Table V, it is obvious that under all conditions $\omega_2 < \omega_1$, which ensures a phase lead of 180° at the resonance frequency ω_1. This paper exploits this fact to improve the load-current sharing performance when UPS units are paralleled through long cables. Fig. 6(b) shows the discrete-time block diagram schematic of the proposed IACS scheme where filter inductor current $i_{\rm lp}$ feedback has been used instead of the load current feedback. The common current reference i_l^* is obtained by averaging the filter inductor current from all the inverters. The z-domain open-loop plant transfer function is defined as

$$Y_{i_{\rm lp}}(z) \triangleq i_{\rm lp}(z)/v^*_{\rm ip}(z) = Y_{i_{\rm op}}(z) + Y_{i_{\rm cp}}(z) \tag{36}$$

and loop gain

$$T_{i_{\rm lp}}(z) = \frac{Y_{i_{\rm lp}}(z) H_v(z) H_c(z)}{z + K Y_{i_{\rm cp}}(z) + G_{v_{\rm op}}(z) H_v(z)}. \tag{37}$$

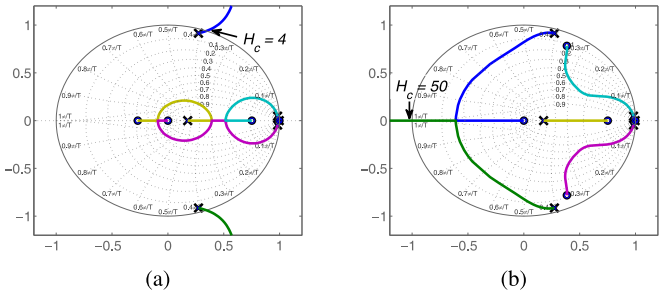

Fig. 8. Root locus of close-loop poles with varying H_c. (a) Conventional IACS. (b) Proposed IACS.

For the ideal situation of UPS units paralleled with negligible cable impedances, both the antiresonance, and hence resonance, frequencies are much higher than the desired close-loop bandwidth. Therefore, plant transfer function for the conventional and proposed scheme are effectively identical, which is reflected in the frequency responses of $T_{i_{\text{op}}}(z)$ and $T_{i_{\text{lp}}}(z)$, shown in Fig. 7. But with long cables, the proposed method gives advantage over the conventional IACS as antiresonance frequency shifts leftward on the frequency response plot and provides phase lead to the loop gain which allows the extension of the gain crossover frequency as shown in Fig. 7(e) and (f). Clearly, the proposed method extends the close-loop bandwidth by almost 50%.

To further explore the effectiveness of the proposed method, root locus of the close-loop poles plotted as the proportional gain H_c is varied. These are shown in Fig. 8(a) and (b) respectively for conventional and proposed IACS scheme for a 50-m long cable. Both have two real poles and two resonant pole pairs, of which one resonant pair always approaches close-loop zero as H_c increases. Hence, this pair does not threaten absolute system stability. The other resonant pole pair however makes the system unstable as it moves out of the unit circle, beyond a critical $\hat{H}_c$. This critical value for conventional IACS is quite low ($\hat{H}_c = 4$) while the proposed method extends this to $\hat{H}_c = 50$, as shown in Fig. 8. Consequently, the proposed system is capable of retaining stability over a much larger range of H_c, which thus allows significant extension in the close-loop bandwidth with adequate stability margins.

VIII. Experimental Results

Experimental verification of the transient and steady-state performances is carried out using two three-phase 415-V 7.5-kVA IGBT-based VSI, which are switched at 10 kHz. Inverters are connected in parallel through interconnecting cables, sharing a common load. System parameters are mentioned in Table I. Fig. 9 shows the experimental setup. All control laws are realized with a 32-bit fixed point DSP (TMS320F2812)-based control platform. The Central control is implemented by having another DSP to receive the output current information from both inverters and then calculate the average current. This signal is then converted back to analog by digital-to-analog converter circuit to send to each inverter.

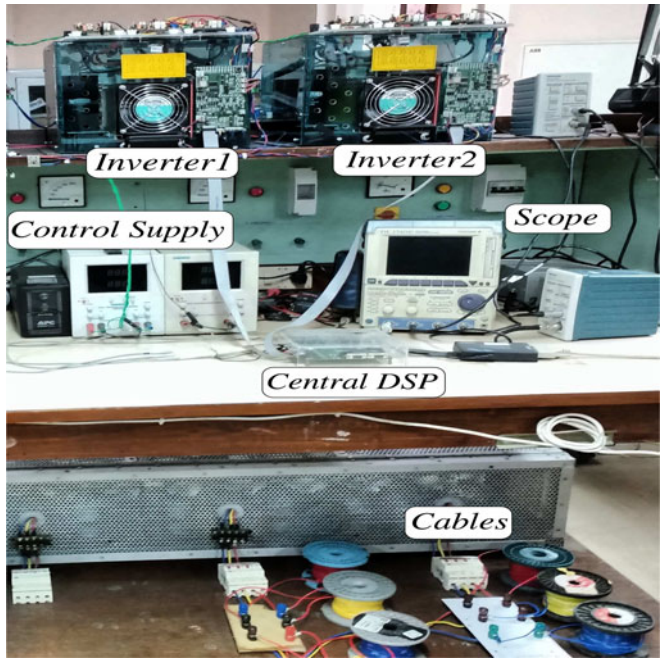

Fig. 9. Experimental setup.

Note that the pth inverter's filter capacitor current i_{cp}, for realizing the AD loop, can be obtained by placing a current sensor in series with the filter capacitor. But this adds to track/lead length which increases undesirable stray inductance in the filter capacitor branch and reduces filtering capacity. Therefore in the experiment, i_{cp} is obtained by taking the difference between filter inductor current i_{lp} and load current i_{op} as shown in Fig. 1. This technique does not increase current sensor count as the one used for i_{lp} sensing is essential for the inverters over current protection and another senses i_{op} instead of i_{cp}.

Experimental results are obtained for both linear and nonlinear loads, the latter comprising a three-phase diode rectifier feeding an *RL* circuit. To validate the feasibility of the proposed controller, cables connecting the inverters and the load are chosen with unequal length (50 and 100 m, respectively, for inverter1 and inverter 2). Fig. 10 demonstrates the operation of current sharing controller with the conventional and proposed IACS schemes, where i_{o1} and i_{o2} are the phase a currents from each inverter while $i_o = (i_{o1} + i_{o2})$ is the total load current in the same phase. Transient performance is investigated by applying a step change in load from no-load to full-load at 30-ms time instant.

Transient and steady-state current sharing performances with the conventional IACS scheme ($H_c = 2$) under linear load condition is shown in Fig. 10(a). It can be seen that currents from inverters are nonsinusoidal while their sum is sinusoidal. It means low-order harmonic current is circulating between the inverters which is not being reduced due to the low close-loop bandwidth. Further, increase in controller gain ($H_c = 3$) as shown in Fig. 10(b) reduces the low-order harmonic circulating current but it makes system less stable as oscillations around the LCL resonance, as predicted by earlier analysis, starts to circulate

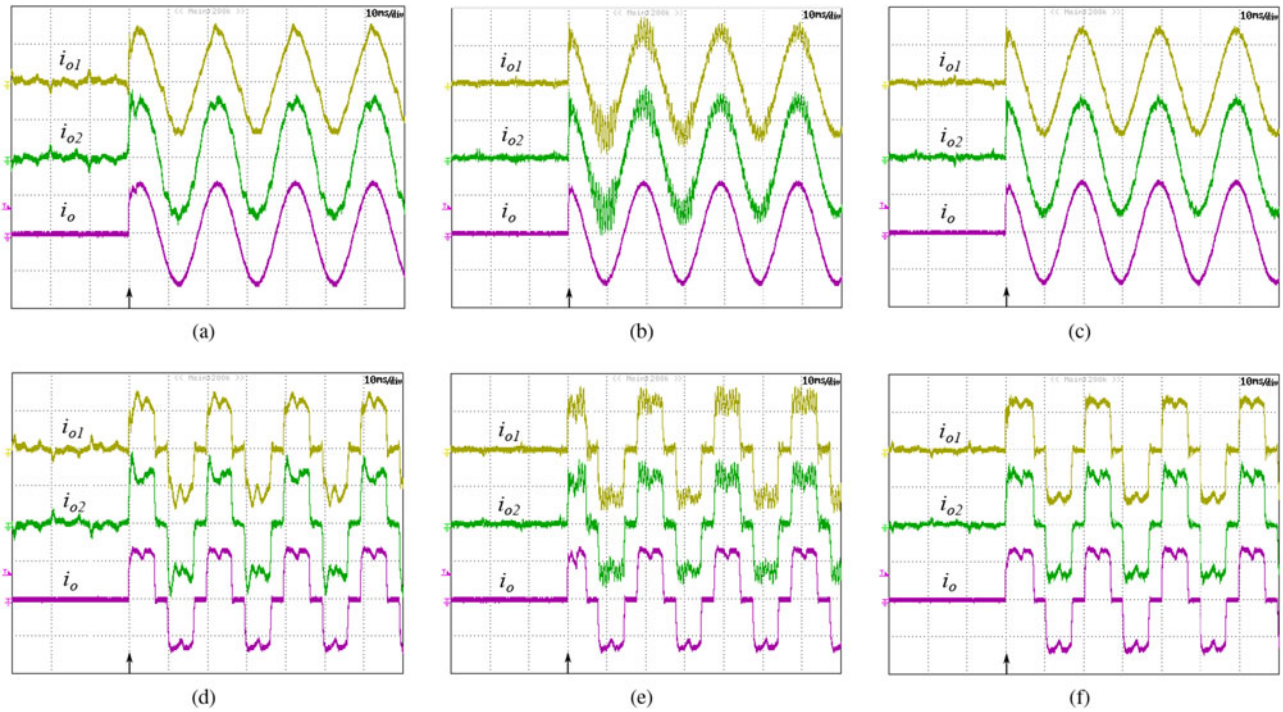

Fig. 10. Load current sharing performance with linear (a)–(c) and nonlinear load (d)–(f). Conventional IACS (a), (b), (d) and (e): (a) $H_c = 2$, (b) $H_c = 3$, (d) $H_c = 2$ and (e) $H_c = 3$. Proposed IACS (c) and (f): $H_c = 10$. Scale: [Time-10 ms/div], [i_{o1}]: and [i_{o2}]: 10 A/div and [i_o]: 20 A/div.

between the inverters. In contrast, a high-bandwidth controller ($H_c = 10$) is feasible with the proposed IACS scheme as shown in Fig. 10(c). Clearly, the steady-state harmonic circulating current is mitigated by the proposed controller. Moreover, the load currents are shared equally even during the no-load to full-load step change which demonstrates the effectiveness of the proposed controller.

Similar results are obtained with the nonlinear load as shown in Fig. 10(d)–(f). Again, the total load is shared accurately using the proposed scheme under transient as well as steady-state condition.

IX. Conclusion

This paper presents the discrete-time analysis of a parallel multi-UPS system based on IACS control scheme. It is analytically shown that the conventional IACS scheme ensures best performance when UPS units are directly connected to the common ac bus. But with long interconnecting cables, the $L_f - C_f - L_p$ resonance restricts the close-loop bandwidth which results in harmonic circulating currents among the inverters. This problem can be solved by extending the $L_f - C_f - L_p$ resonance frequency but it necessitates high switching frequency. In contrast, the proposed IACS extends the close-loop bandwidth due to the presence of inherent L_pC_f antiresonance and ensures proper load sharing even with low switching frequency. Controller designs are validated by experimental results that show excellent transient and steady-state performance.

Appendix

$$\begin{aligned} b_v &= (\omega_r^2 + \omega_c^2)T^2 \\ \Delta(z) &= z^2 - 2e^{-\sigma T}\cos(\omega_d T)z + e^{-2\sigma T} \\ \sigma &= r_f/2L_f \quad \text{and} \quad \omega_d = \sqrt{\omega_f^2 - \sigma^2} \\ a_v &= e^{-\sigma T}\sin(\omega_d T)/\omega_d L_f \\ a_{v0} &= e^{-2\sigma T} - e^{-\sigma T}\cos(\omega_d T) + \sigma a_v L_f \\ a_{v1} &= 1 - e^{-\sigma T}\cos(\omega_d T) - \sigma a_v L_f . \end{aligned} \tag{38}$$

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