

# Direct Sequence Spread Spectrum-Based PWM Strategy for Harmonic Reduction and Communication

Ruichi Wang, *Student Member, IEEE*, Zhengyu Lin, *Senior Member, IEEE*, Jin Du, *Student Member, IEEE*, Jiande Wu, *Member, IEEE*, and Xiangning He, *Fellow, IEEE*

**Abstract**—Switched mode power supplies (SMPSs) are essential components in many applications, and electromagnetic interference is an important consideration in the SMPS design. Spread spectrum-based pulse width modulation (PWM) strategies have been used in SMPS designs to reduce the switching harmonics. This paper proposes a novel method to integrate a communication function into spread spectrum-based PWM strategy without extra hardware costs. Direct sequence spread spectrum (DSSS) and phase shift keying data modulation are employed to the PWM of the SMPS, so that it has reduced switching harmonics and the input and output power line voltage ripples contain data. A data demodulation algorithm has been developed for receivers, and code division multiple access (CDMA) concept is employed as a communication method for a system with multiple SMPSs. The proposed method has been implemented in both Buck and Boost converters. The experimental results validated the proposed DSSS-based PWM strategy for both harmonic reduction and communication.

**Index Terms**—Communication, direct sequence spread spectrum (DSSS), harmonic reduction, pulse width modulation (PWM), switched mode power supply (SMPS).

## I. INTRODUCTION

POWER electronics and communications are subtopics of electrical engineering with different emphasis [1] and both of them are key technologies for smart grids [1], [2] and the Internet of Things (IoT) [3]–[5].

Conventional communication techniques, such as fieldbus and wireless communication, are commonly employed [6]. However, these techniques require extra communication signal generation circuits and associated power supplies. Wired communication methods, such as fieldbus, require dedicated communication cables, which increase system cost, and reduce system flexibility. Wireless communication methods are attractive to eliminate the communication cables, but they are lack of

physical protection, security, and reliability are often doubted, so extra measures are needed for protection.

Power line communication (PLC) technology uses electrical wires for both power and data transmission, and has been widely investigated. PLC has proved a reliable method for communication in many applications, including ac power systems [7], microgrids [8], [9] and IoTs [10]. Many devices (such as remote sensors, LEDs, PV, energy storages, etc.) have power electronics converters. It will be desirable if PLC functions can be integrated into power electronics design, so that via the common dc power line, the remote sensor power supplies can send the measurement to the master controller, energy storage management system can send its state of charge to the master controller, and current demand can be sent to LED drives, etc. However, PLC technology requires independent circuits for injecting, amplifying, and processing the communication signals, the system cost and volume are high.

In recent years, some strategies have been developed to integrate communication techniques into power electronics designs to get better performing power electronic converters [11]–[16].

In communications, spread spectrum techniques are used to establish secure and reliable communication by spreading the transmitted signal over a wide bandwidth. This concept has been applied to power electronics designs to reduce the electromagnetic interference (EMI) emission [14]–[16]. For switched mode power supplies (SMPSs), high switching frequency has the benefits of better output voltage regulation, smaller filter size, and lower system cost [17], but it creates EMI emission problems. The EMI emission may affect the SMPS itself and also interfere with other electronic equipment [18]. Therefore, various electromagnetic compatibility (EMC) standards have been developed to ensure the EMI emission of electrical or electronic equipment does not exceed a level to disturb other equipment. To meet EMC standards, many methods have been proposed to mitigate the EMI emission of SMPS, such as using EMI filters, selecting/designing appropriate components, better physical layout of the circuit, and soft-switch transition techniques [17], etc. For fixed frequency pulse width modulation (PWM) SMPS, the EMI noise peak values are at the harmonics of the switching frequency, making the EMI problem serious. Spread spectrum techniques can spread the spectrum of switching noise and achieve EMI suppression without EMI filters. In [14]–[16], [19]–[23], randomness is introduced to spread the dis-

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R. Wang, J. Du, J. Wu, and X. He are with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China. (e-mail: rui\_chi@163.com; eedujin@zju.edu.cn; eewjd@zju.edu.cn; hxn@zju.edu.cn).

Z. Lin is with the Department of Electrical, Electronic and Power Engineering, Aston University, Birmingham, B4 7ET, U.K. (e-mail: z.lin@ieee.org).

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crete switching harmonic power over a wide frequency band, so that no harmonic of significant magnitude exists. In [15], a pseudorandom sequence is employed in frequency hopping spread spectrum modulation to reduce the spectral power density at the harmonic frequencies. In [24]–[26], triangular and bifrequency periodic modulation techniques are adopted for custom spectral spreading with predictable parameters. In the aforesaid cited papers, spread spectrum techniques are only used for mitigating EMI issues, but not for communications.

For the SMPS, the input and output voltages usually contain ripples, and the voltage ripple fundamental frequency is the same as the switching frequency. For conventional SMPS designs, those voltage ripples are not desired, and many methods are proposed to reduce them. By applying a data modulation strategy in an SMPS, it is possible to use the voltage ripple for PLC communications [6], [12]. Frequency shift keying (FSK) is a common communication method to transmit data through discrete frequency changes of the carrier. In [6] and [12], a common dc bus communication method based on PWM/FSK modulation was proposed, and power converters are able to communicate with each other via the common dc bus. Data modulation is based on changing the converter PWM carrier frequency, so that the dc bus voltage ripple contains the data. Data demodulation is based on analyzing the dc bus voltage harmonic spectrum using discrete Fourier transform (DFT) method. However, EMI filters are not allowed in the system with this communication method because they attenuate the ripple signals. Without EMI filters, the system may not comply EMC standards.

This paper proposes a novel direct sequence spread spectrum (DSSS)-based PWM strategy to integrate some common communication technologies into SMPS design for both harmonic reduction and communication purposes. In the proposed method, power electronics devices with proposed modulation strategy can send data to any devices with proposed demodulation strategy connected to the same dc power line. DSSS is used to the spread data spectrum, and phase shift keying (PSK) is integrated into PWM to modulate both the data and the power. For the SMPS with the proposed PWM strategy, the harmonic spectrum is spread with decreased amplitude, the input and output voltage ripples contain the data, and the data can be transmitted along the dc power line. By introducing the code division multiple access (CDMA) [27], [28] concept, full-duplex multiple access communication among SMPSs can be realized. Compared with other PLC techniques, the proposed modulation strategy integrates communication with the SMPS and no additional signal generation hardware is required. Besides, switching harmonics are reduced [29], [30].

This paper is organized as follows: Data spreading and despreading principle is introduced in Section II, and then the data and power modulation and demodulation are presented in Section III. The proposed DSSS-based PWM strategy has been implemented and experimentally verified. The prototype design and experimental results are shown in Section IV. Finally, conclusions are given in Section V.

## II. DATA SPREADING AND DESPREADING WORKING PRINCIPLE

Fig. 1 shows the block diagram of the proposed DSSS-based PWM strategy for both harmonic reduction and communica-

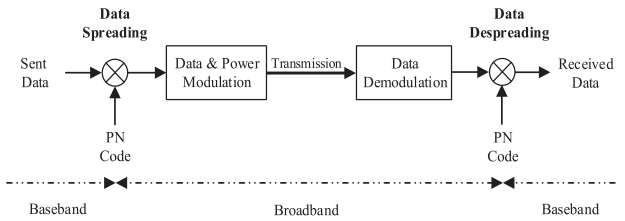


Fig. 1. Block diagram of the proposed DSSS-based PWM strategy.

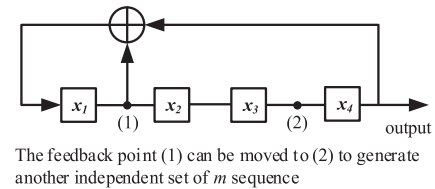


Fig. 2. Generation scheme of four-stage  $m$  sequences.

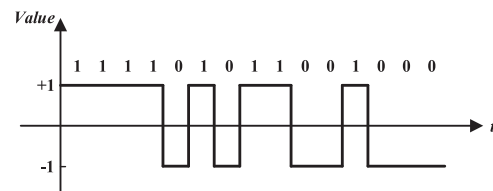


Fig. 3. Waveform of a four-stage  $m$  sequence.

tion. It includes four parts: data spreading, data and power modulation, data demodulation, and data despreading. The data spreading and despreading principle is presented in this section, which is similar to the DSSS method for broadband communication. The data and power modulation and data demodulation will be presented in the next section.

### A. Data Spreading

DSSS is one of the spread spectrum forms, and a pseudorandom (PN) sequence is adopted to represent data. As shown in Fig. 1, to spread the sent data over a broadband, a PN code is employed, which is independent of the data. The PN code is a pseudorandom sequence and has properties similar to white noise.

$m$  sequence (maximum length sequence) is a popular pseudorandom sequence for DSSS.  $m$  sequence is generated by a linear  $a$ -stage shift register ( $a$  is an integer,  $a \geq 2$ ). For a four-stage shift register, it can generate two independent sets of  $m$  sequences, and the generation scheme is shown in Fig. 2. The initial state of  $x_1$  to  $x_4$  can be any combination of 1 and 0, except all 0. The generated sequence repeats itself every 15 elements, and these elements are called “chips.” For a four-stage shift register, two independent  $m$  sequences are 111101011001000 and 100110101111000, or their round-shifts, such as 111010110010001 and 001101011110001. In communication, the waveform of  $m$  sequence is usually bipolar (taking values of +1 or  $-1$ ), as shown in Fig. 3. For higher stage shift registers, more independent sets of longer  $m$  sequence can be generated [20].

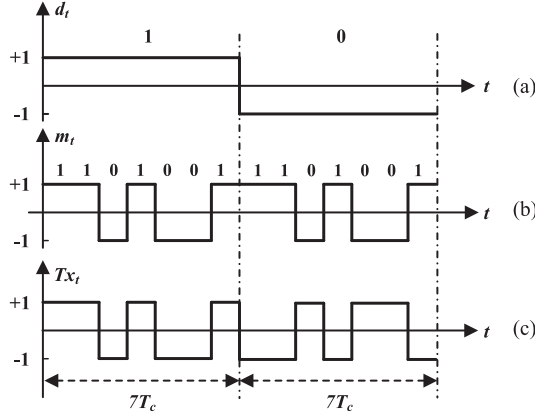


Fig. 4 Waveforms of the DSSS data spreading in the transmitter.

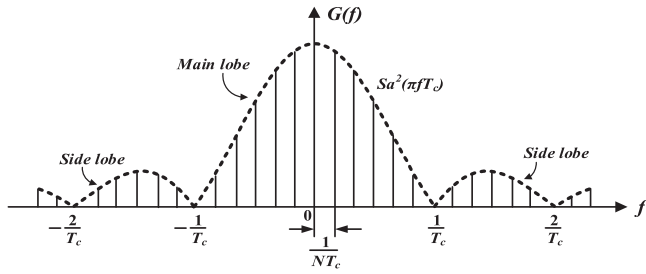
Fig. 5. Power density function  $G(f)$  of  $m$  sequence.

Fig. 4 demonstrates some typical waveforms of the DSSS data spreading in the transmitter. Fig. 4(a) is the sent data  $d_t$ , which is represented with a bipolar waveform. A three-stage  $m$  sequence (the sequence length is 7)  $m_t$  is used for the data spreading, which is shown in Fig. 4(b). The signal after spreading  $Tx_t$  can be calculated as follows:

$$Tx_t = d_t \times m_t. \quad (1)$$

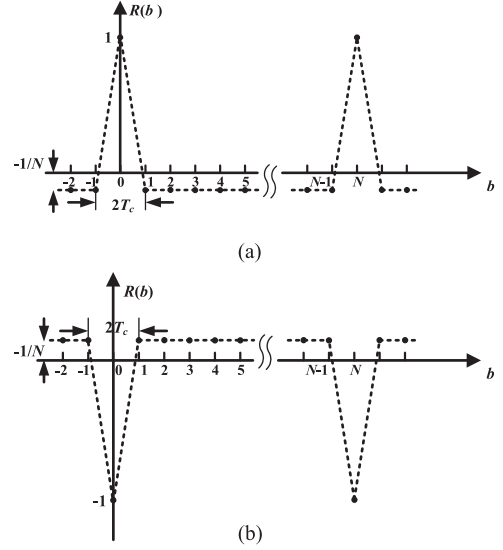
The waveform of  $Tx_t$  is shown in Fig. 4(c).

Equation (2) is the power density function  $G(f)$  of the  $m$  sequence and its graph is shown in Fig. 5, where  $T_c$  is the duration time of a chip [20]. The effect of multiplication of the sent data with an  $m$  sequence is to spread the data to a broad bandwidth of  $2/T_c$

$$G(f) = \frac{1}{K^2} \delta(f) + \frac{K+1}{K^2} \left( \frac{\sin(\pi f T_c)}{\pi f T_c} \right)^2 \times \sum_{\substack{k=-\infty \\ k \neq 0}}^{\infty} \delta\left(f - \frac{k}{KT_c}\right) \quad (2)$$

### B. Data Despreading

To despread the received broadband signal, the receiver needs to know the  $m$  sequence used in the transmitter. One despreading methods is to multiply the received broadband signal with the

Fig. 6. Graph of correlation calculation in the receiver: (a) Autocorrelation calculation of  $m$  sequence and (b) Cross correlation calculation of  $m$  and  $-m$  sequences.

$m$  sequence. This method is based on the highly autocorrelation property of  $m$  sequence, and does not need to synchronize the receiver's  $m$  sequence with the transmitter's.

The autocorrelation function of  $m$  sequence  $R_n$  is defined as (3), where  $x_n$  ( $n = 1, 2, \dots, i$ ) is the  $n$ th chip in the  $m$  sequence and  $K$  is the length of the  $m$  sequence:

$$R(b) = \frac{1}{K} \sum_{n=1}^K x_n x_{n+b} = \begin{cases} 1, & b = 0, K, 2K, \dots \\ -\frac{1}{K}, & b \neq 0, K, 2K, \dots \end{cases} \quad (3)$$

Equation (3) indicates the  $m$  sequence has a highly autocorrelation property. The correlation calculation result is shown in Fig. 6. For data "1", the received signal is the same as the  $m$  sequence, so it will show a high positive autocorrelation peak during despreading, as shown in Fig. 6(a). For data "0", the received signal is opposite to the  $m$  sequence chip by chip (it is a  $-m$  sequence), and therefore, it will show a high negative correlation peak during the despreading, as shown in Fig. 6(b).

## III. DSSS-BASED PWM STRATEGY AND DATA DEMODULATION

### A. Data and Power Modulation

The data and power modulation block diagram for the proposed DSSS-based PWM strategy is shown in Fig. 7. The proposed method can be applied to different synchronous rectification dc-dc converter topologies. The analysis in this section is based on the Buck converter as shown in Fig. 8.

Key waveforms of the proposed DSSS-based PWM strategy are shown in Fig. 9.

Fig. 9(a) shows the spread spectrum signal  $Tx_t$  obtained from the data spreading (as discussed in Section II). Fig. 9(b) shows a triangle carrier for constant frequency PWM. PSK is employed to modulate the data. The phase of the PWM carrier

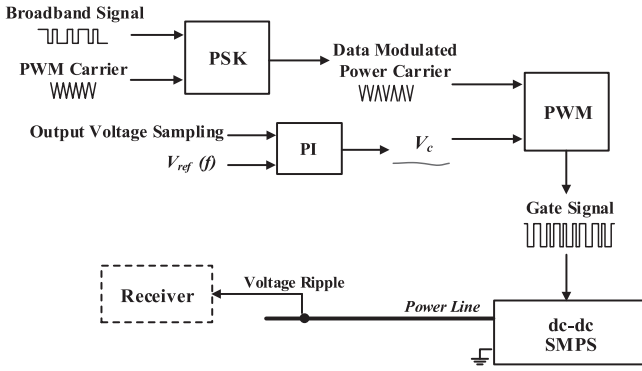


Fig. 7. Block diagram of data and power modulation for the proposed DSSS-based PWM strategy.

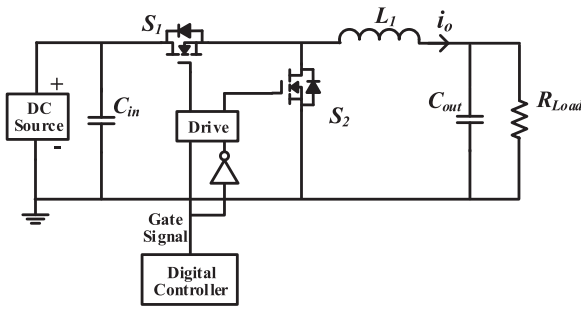


Fig. 8. Block diagram of Buck converter to be analyzed.

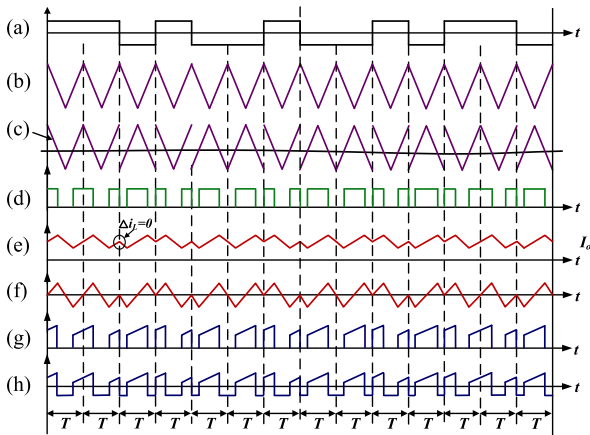


Fig. 9. Key waveforms of the DSSS-based PWM strategy.

will be shifted  $180^\circ$  if  $Tx_t = 0$ , as shown in Fig. 9(c). The PWM reference signal for power modulation is also shown in Fig. 9(c). The PWM signal generated by the reference signal and carrier signal after data modulation is shown in Fig. 9(d).

Using the generated PWM signal as the gate signal of the Buck converter shown in Fig. 8, the resultant inductor current waveform is shown in Fig. 9(e). From Fig. 9(e), the average inductor current does not vary with the PWM carrier phase change. Therefore, the average output voltage does not change, which means data modulation does not affect power modulation.

Considering the equivalent series resistance (ESR) of the output capacitor, the output voltage ripple consists of two parts, the ripple caused by the capacitor  $C$  and the ripple caused by the ESR. The peak-to-peak voltage ripple caused by  $C$  can be approximately calculated as  $\frac{I_{p-p}}{8Cf_{\text{switch}}}$ , where  $I_{p-p}$  is the peak-to-peak inductor current ripple, and  $f_{\text{switch}}$  is the switching frequency. The peak-to-peak voltage ripple caused by ESR can be calculated as  $I_{p-p}R_{\text{ESR,out}}$ , where  $R_{\text{ESR,out}}$  is the ESR of the output capacitor. In this research, an electrolytic capacitor is used as the output capacitor ( $100 \mu\text{F}$ , ESR  $0.13 \Omega$  at  $100 \text{ kHz}$ ). At this condition, the ripple caused by  $C$  is about 10% of the ripple caused by ESR, therefore, the Buck converter output voltage ripple  $V_{\text{ripple,out}}$  can be approximately calculated as follows:

$$V_{\text{ripple,out}} \approx I_{\text{ripple,out}} R_{\text{ESR,out}} \quad (4)$$

where  $I_{\text{ripple,out}}$  is the Buck converter output current ripple, i.e., the inductor current ripple. Thus, the output voltage ripple has the same phase as the inductor current ripple, as shown in Fig. 9(f).

Similarly, the input voltage ripple can be approximately calculated as follows:

$$V_{\text{ripple,in}} \approx I_{\text{ripple,in}} R_{\text{ESR,in}} \quad (5)$$

where  $I_{\text{ripple,in}}$  is the Buck converter input current ripple, and  $R_{\text{ESR,in}}$  is the ESR of the converter input terminals. It should be noted that the aforesaid approximations are less accurate when using low-ESR capacitors or working at lower switching frequency.

Fig. 9(g) shows the Buck converter input current, which is discontinuous. The input voltage ripple is shown in Fig. 9(h).

Fig. 9(f) and (h) show that by shifting the PWM carrier phase angle of  $180^\circ$ , the output/input voltage ripple phase will be shifted  $180^\circ$ . This means that the spread spectrum signal  $Tx_t$  is modulated to the gate signal Fig. 9(d) and then reflected in to the input/output voltage ripple. Therefore, the Buck converter input and output voltage ripples contain the information of the spread spectrum signal  $Tx_t$ .

With triangle PWM carrier, the Buck converter's gate voltage phase angle does not change with the PWM duty-cycle, as shown in Fig. 10(a) and (b), which implies that the input/output voltage ripple phase angle is also constant. The PWM duty-cycle is determined by the power modulation. Therefore, the power modulation does not affect the data modulation.

A sawtooth carrier is not suitable for the proposed DSSS-based PWM strategy. For a Buck converter with a sawtooth PWM carrier, its input/output voltage ripple phase angle is affected by the PWM duty-cycle, as shown in Fig. 10(c) and (d), which indicates that the power modulation will affect the data modulation.

Based on this analysis, for an SMPS with the proposed modulation strategy, data modulation and power modulation are decoupled, the input and output voltage ripple contain information, so that the SMPS can send out data without any additional hardware.

Fig. 11(a) shows the system with  $n$  Buck converters sharing a common output dc power line. In steady state, the input capacitor and switch are equivalent to a pulse voltage source  $v_n$  from

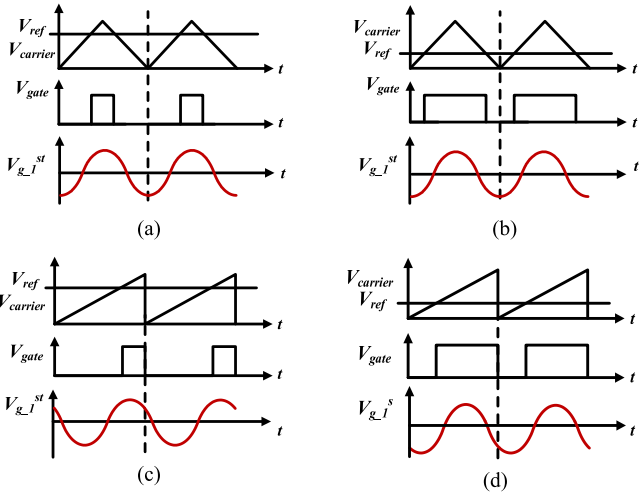


Fig. 10. Influence of duty-cycle to the voltage ripple phase with different PWM carriers: (a) Small duty-cycle with triangle PWM carrier, (b) Large duty-cycle with triangle PWM carrier, (c) Small duty-cycle with sawtooth PWM carrier, and (d) Large duty-cycle with sawtooth PWM carrier.

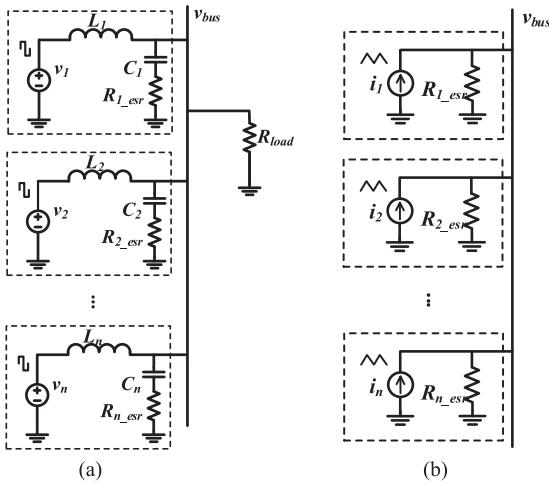


Fig. 11. Signal propagation model. (a) Signal propagation model. (b) Simplified ac equivalent circuit.

the point of view of communication. Ignoring the dc component, the pulse voltage source and the inductor can be replaced by a triangle current source. Since  $V_{\text{ripple.in}} \approx I_{\text{ripple.in}} R_{\text{esr.in}}$ , the diagram can be simplified as Fig. 11(b). Ignoring the resistor in the transmission line for short distance communication applications, the voltage ripple on the power line can be calculated as follows:

$$\tilde{v}_{\text{bus}} = \frac{\sum_{k=1}^n \tilde{i}_k}{\sum_{k=1}^n \frac{1}{R_{k,\text{esr}}}} \quad (6)$$

where  $\tilde{i}_k$  is the current from the equivalent triangle current source.

When several Buck converters are connected to the bus, the waveform on the bus is the linear synthesis of the ripples produced by converters.

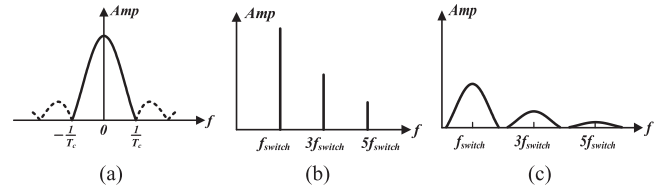


Fig. 12. Harmonic spectrum diagram. (a) Constant frequency PWM signal. (b)  $m$  sequence. (c) Spread spectrum PWM signal.

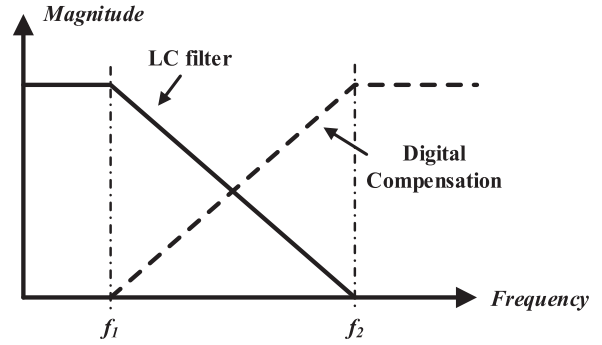


Fig. 13. Bode plot of the LC filter and the digital compensation.

The working principle of harmonic reduction of the proposed PWM modulation is similar to some of existing random PWM strategies [14]–[16]. Fig. 12(a) shows the harmonic spectrum diagram of a conventional constant frequency PWM signal, where the dominate harmonics locate at the fixed frequencies of  $f_{\text{switch}}$ ,  $3f_{\text{switch}}$ ,  $5f_{\text{switch}}$ , and so on. Fig. 12(b) is the power density function of  $m$  sequence. Ignoring the effect of the side lobes, the spectrum diagram of the spread spectrum PWM is approximately a series of main lobes with central frequencies  $f_{\text{switch}}$ ,  $3f_{\text{switch}}$ ,  $5f_{\text{switch}}$ ..., as shown in Fig. 12(c). Compared with Fig. 12(a), the dominate harmonic is spread and distributed to adjacent frequencies and the magnitude of the harmonics are significantly reduced. Therefore, the SMPS with the DSSS-based PWM strategy has reduced harmonics.

The inductor and the output capacitor of the Buck converter form an LC low-pass filter for the output voltage, and its amplitude Bode plot is shown as the solid line in Fig. 13. If the output voltage ripple of the Buck converter acts as the communication signal, the output LC low-pass filter will attenuate the band higher than  $f_1$  in the broadband spectrum. To correct this distortion, a digital compensator is needed before despreading. The bode plot of the digital compensator is shown as the dotted line in Fig. 13, the compensator slope between  $f_1$  and  $f_2$  is opposite to the LC filter, so that the attenuation can be compensated.

## B. Data Demodulation and Despreading

For the receiver, to demodulate the data from the SMPS's input or output voltage ripple, a voltage ripple conditioning circuit [21] is needed to extract the first harmonic of the voltage ripple with correct amplitude.

The amplified voltage ripple is sampled with a high-frequency analog to digital converter (ADC) within the DSP. Based on the

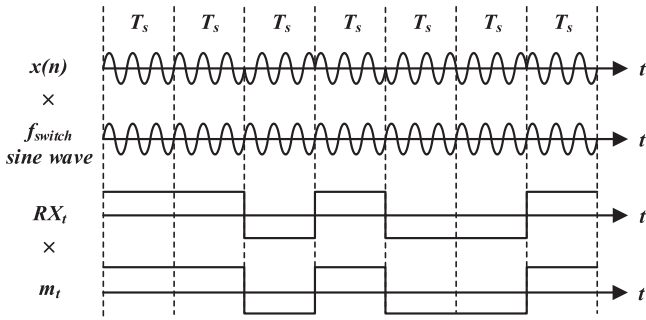


Fig. 14. Process of demodulation and despreading.

Nyquist–Shannon sampling theorem, the ADC sampling rate  $f_{\text{sampling}}$  should be selected as  $N$  times of the PWM carrier frequency ( $N$  is an integer larger than 2).

To detect the phase angle of the voltage ripple at the PWM carrier frequency, DFT is adopted, as shown in

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-jk\Omega_0 n} \quad k = 0, 1, \dots, N-1 \quad (7)$$

where  $\Omega_0$  is the sampling frequency and  $k$  refers to the order of harmonics calculated. In this constant frequency PWM condition, only the phase of the first harmonic of the voltage ripple needs to be analyzed, thus  $k = 1$ . Based on the obtained phase angle, transmission signals can be demodulated into broadband digital signals  $RX_t$ , shown in Fig. 14, for despreading.

With a triangle PWM carrier, the input or output voltage ripples have only sine or cosine components, which means (4) and (5) can be simplified to (8) or (9)

$$X(1) = \sum_{n=0}^{N-1} x(n) \cos(\Omega_0 n) \quad (8)$$

$$X(1) = \sum_{n=0}^{N-1} x(n) \sin(\Omega_0 n). \quad (9)$$

During the demodulation process, in each chip, a sinusoidal wave with frequency  $f_{\text{switch}}$  and the same phase as the ripple (without data modulation) is multiplied by the sampling wave  $x(n)$ , which is essentially a simplified DFT calculation, and then the phase angle can be obtained.

To improve computing efficiency, the demodulation and despreading algorithms can be combined. Thus, a sinusoidal wave of frequency  $f_{\text{switch}}$  is first multiplied by the  $m$  sequence, and then the product is multiplied by the sampling wave  $x(n)$ . The calculation result of the combined “demodulation and despreading” is shown in Fig. 15, which is similar to Fig. 6.

### C. Multiple Access Communication

For a peer-to-peer system with two or more SMPSs, it is necessary to use a DSSS-based PWM strategy for all SMPSs to maintain low system harmonics. CDMA is a communication technology of multiplexing users by distinct PN codes [27]. This paper proposes to apply the CDMA concept in the proposed

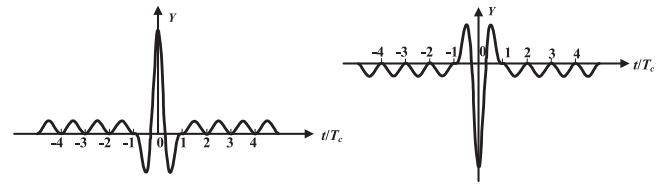


Fig. 15. Calculation result of combined “demodulation and despreading.”

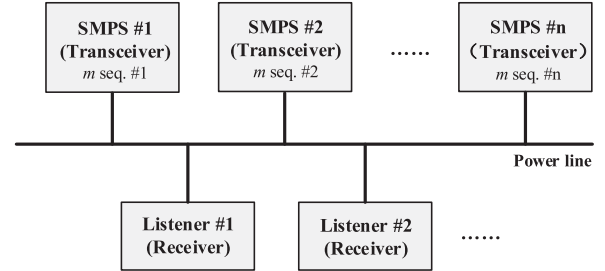


Fig. 16. Block diagram of using CDMA concept for a system with multiple SMPSs.

DSSS-based PWM strategy for multiple access communication. As shown in Fig. 16, a distributed system includes several SMPSs as data transceivers (can both transmit and receive data) and some listeners as data receivers (can only receive data). To avoid signal conflict, each SMPS should employ a unique  $m$  sequence, for example,  $m$  sequence #1 for SMPS #1, and  $m$  sequence #2 for SMPS #2, and so on. The transceiver or receiver can use different  $m$  sequences to receive the data sent by different SMPSs. Other SMPSs produce noise and cause multiple access interference (MAI), which is a factor to limit the number of SMPSs allowed in the system and the reliability of the communication.

## IV. EXPERIMENTAL VERIFICATION

Two experiments have been designed to evaluate the proposed DSSS-based PWM strategy for both harmonic reduction and communication.

### A. Experiment 1

In this experiment, the testing setup includes a Buck converter and a receiver, as shown in Fig. 17, and the experiment parameters are listed in Table I.  $C_{\text{in}}$  and  $C_{\text{out}}$  are voltage ripple filtering capacitors, mainly used to improve the input and output power quality. Via a multiplexer, the receiver can be connected to the input or the output power line. The receiver is composed of a DSP and a signal conditioning circuit. The signal conditioning circuit filters the dc and high-order harmonics and amplifies the first harmonic of the sampled ripple by an active second-order low-pass filter [31]. Both input and output voltage ripples of the Buck converter can be used as a communication carrier. The DSP used for both Buck converter and the receiver is TI’s Piccolo Microcontroller TMS320F28035. This is a low-cost device with a control law accelerator (CLA) [32], which is an independent and

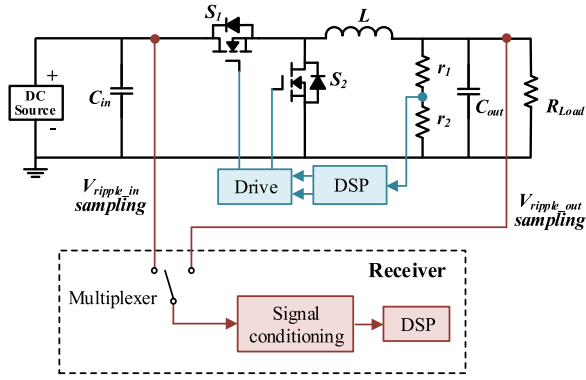


Fig. 17. Block diagram of the prototype in Experiment I.

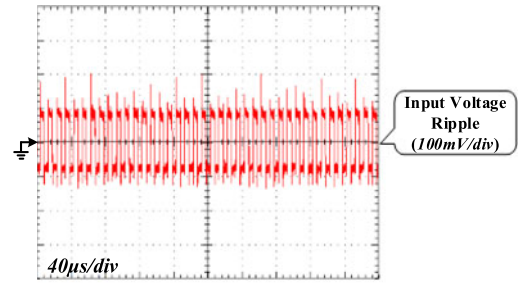
TABLE I  
PARAMETERS OF THE PROTOTYPE IN EXPERIMENT I

Parameters of the Buck converter	Value
$V_{in}$ (Input voltage)	12 V
$V_{out}$ (Output voltage)	5 V
$L$ (Buck inductor)	300 $\mu$ H
$C_{in}$ (Input capacitor)	470 $\mu$ F
$R_{est\_in}$ (Input capacitor ESR in 100 kHz)	0.03 $\Omega$
$C_{out}$ (Output capacitor)	100 $\mu$ F
$R_{est\_in}$ (Output capacitor ESR in 100 kHz)	0.13 $\Omega$
$P_{max}$ (Maximum power)	5 W
Parameters of DSSS modulation	Value
$m$ sequence	1, 1, 1, 1, 0, 1, 0, 1, 1, 0, 0, 1, 0, 0, 0
$f_{switch}$ (Switching frequency)	100 kHz
$T_s$ (Duration time of a chip)	10 $\mu$ s
$f_{sampling}$ (Voltage ripple sampling frequency)	400 kHz
Data rate	6.67 kb/s

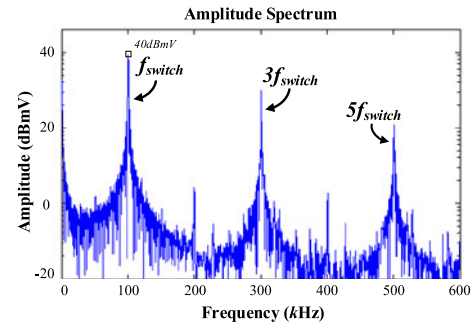
fully programmable 32-bit floating-point math accelerator that runs in parallel with the main CPU. According to the switching frequency (100 kHz), the passband of the signal conditioning circuit and the computing ability of the DSP, the ripple sampling frequency is selected as 400 kHz. The combined “demodulation and spreading” algorithm is implemented in the CLA, and the calculation time is less than 2  $\mu$ s.

Experimental results are shown in Figs. 18–22. Fig. 18 shows the Buck converter input voltage ripple with conventional fixed frequency PWM. Fig. 18(a) shows the input voltage ripple in time domain and Fig. 18(b) shows its spectrum, which is computed from the sampled experimental voltage ripple data points. The dominate harmonics locate at the frequencies of 100 kHz, 300 kHz, 500 kHz, etc.

Fig. 19 shows the Buck converter experimental results with the proposed DSSS-based PWM strategy. The  $m$  sequence used for spectrum spreading is 1, 1, 1, 1, 0, 1, 0, 1, 1, 0, 0, 1, 0, 0, 0. The duration time of a chip is the same as the PWM period, which is 10  $\mu$ s. With DSSS modulation introduced, the dominate harmonic is spread, for example, the dominate harmonic of 100 kHz is spread and distributed to adjacent frequencies between 0–200 kHz, and the magnitude of the harmonic is reduced, as well as the high-order harmonics, which confirms

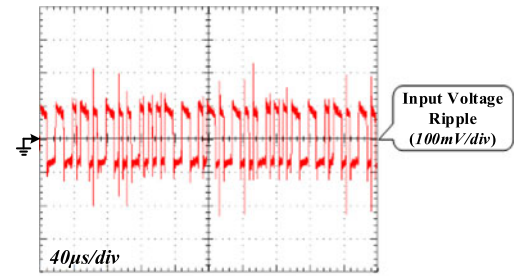


(a)

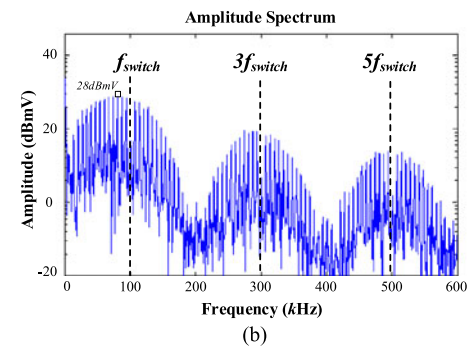


(b)

Fig. 18. Input voltage switching ripples with constant PWM. (a) Input voltage ripple. (b) Spectrum of input voltage ripple.



(a)



(b)

Fig. 19. Input voltage switching ripples with DSSS modulation. (a) Input voltage ripple. (b) Spectrum of input voltage ripple.

the theoretical analysis in Section III. The experimental result shows that the amplitude of the voltage ripple remains the same in time domain but decreases about 12 dB · mV in frequency domain, which implies the significant harmonic reduction for the Buck converter.

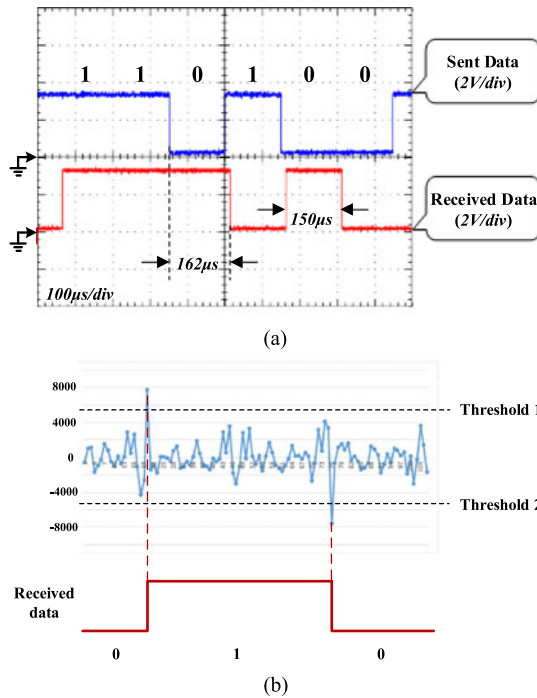


Fig. 20. Communication process in Experiment I. (a) Waveforms of sent data and received data. (b) “Demodulation &and despreading” calculation result within DSP.

The input and output voltage ripples contain the data sent by the Buck converter, and the sent data sequence is shown as the top waveform in Fig. 20(a). In this case, the receiver is connected to the Buck converter input terminals, and the received data after demodulation and despreading are the bottom waveform in Fig. 20(a). The duration time of one data bit is  $150\ \mu\text{s}$ , thus the data rate is  $6.67\ \text{kb/s}$ , while the voltage ripple sampling rate is  $400\ \text{kHz}$ . In the receiver, a correlation peak will appear after receiving a complete data bit, which takes  $150\ \mu\text{s}$ . The combined “demodulation and despreading” algorithm and data determination also takes time. As shown in Fig. 20(a), the total communication delay is about  $162\ \mu\text{s}$ . Fig. 20(b) shows the combined “demodulation and despreading” calculation result within the DSP. For the receiver, when data “1” arrives there appears a positive peak and when data “0” arrives a negative peak appears, as predicted by the theoretical analysis. Two thresholds are set for determining the received data.

Fig. 21(a) shows the Buck converter output voltage with DSSS modulation. Fig. 21(b) shows its spectrum and it indicates that the spectrum is distorted severely, which causes difficulties in data despreading. As analyzed in Section III, this is mainly caused by the  $LC$  low-pass filter on the output port. To correct the spectrum distortion, digital compensation is performed before the “demodulation and despreading” algorithm, as mentioned before. The spectrum after the correction is shown in Fig. 21(c), which is similar to the spectrum shown in Fig. 19(b), and is suitable for demodulation and despreading.

For practical applications, the distance between the SMPS and the receiver cannot be ignored. So the communication per-

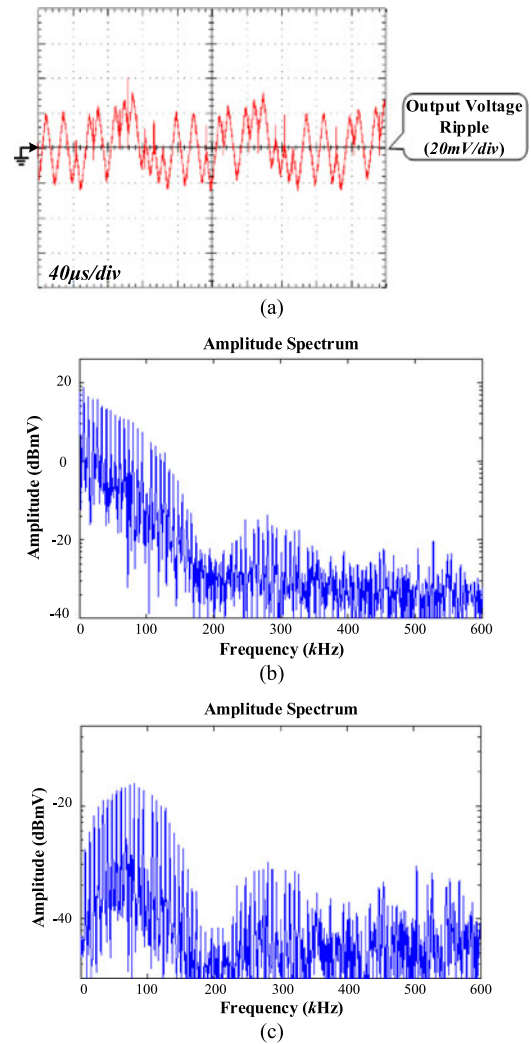


Fig. 21. Output voltage ripples with DSSS modulation. (a) Output voltage ripple. (b) Spectrum of output voltage ripple. (c) Spectrum of output voltage ripple after compensation.

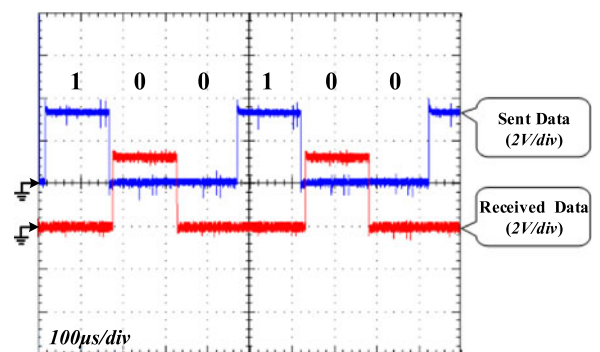


Fig. 22. Waveforms of sent data and received data with 5-m distance.

formance is evaluated when the distance between the Buck converter and the receiver is increased to 5 meters, and connected by a twisted pairs. Fig. 22 shows the experimental results of the sent data and received data waveforms. It shows a reliable

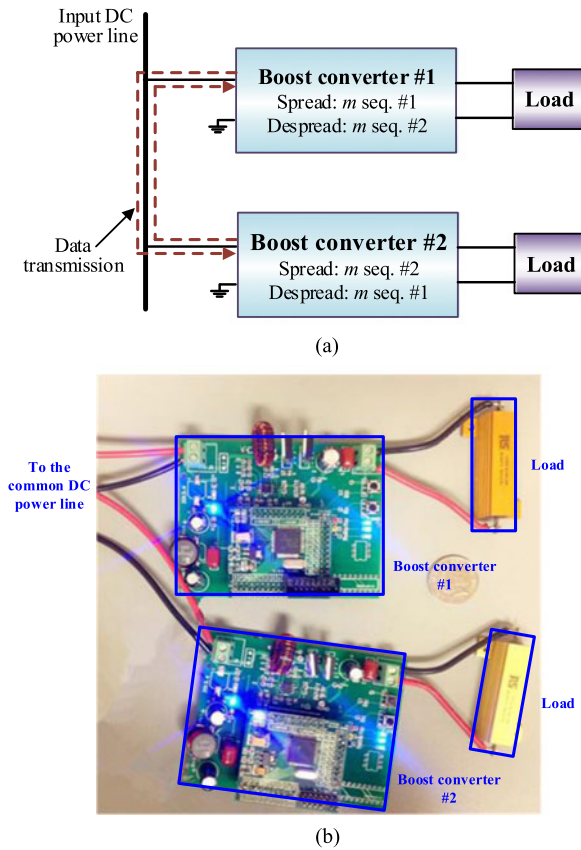


Fig. 23. Prototype in Experiment II. (a) Block diagram of the experiment system setup. (b) Photo of the experiment system setup.

communication is established between the Buck converter and the receiver with 5 m.

### B. Experiment II

In this experiment, the test includes two Boost converters, which act as transceivers. The experimental system setup diagram and photo are shown in Fig. 23. The Boost converter power control, DSSS-based PWM and data “demodulation and despreading” algorithms are implemented in a TMS320F28035 microprocessor. Two Boost converters are connected via a common input dc power line and the system parameters are listed in Table II. Communication parameters remain the same as for Experiment I.

The CDMA concept is employed in this system with multiple SMPSs. Both Boost converters are working at DSSS-based PWM mode to reduce harmonics, but with different independent  $m$  sequences ( $m$  sequence #1 for Boost #1, and  $m$  sequence #2 for Boost #2). Boost #1 (#2) uses  $m$  sequence #2 (#1) to despread the data sent by Boost #2 (#1).

The experimental result is shown in Fig. 24. Fig. 24(a) shows the DSSS-based PWM and the input and output voltage waveforms of the Boost converter. It can be seen that the input voltage is 12V, and the output voltage is 24V, which shows the proper power conversion as designed for PWM duty of 0.5. In Fig. 24(b), data #1 is sent by Boost #1 and received by Boost

TABLE II  
PARAMETERS OF THE PROTOTYPE IN EXPERIMENT II

Parameters of the Boost converter	Value
$V_{in}$ (Input voltage)	12 V
$V_{out}$ (Output voltage)	24 V
$L$ (Boost inductor)	300 $\mu$ H
$C_{in}$ (Input capacitor)	470 $\mu$ F
$R_{esr\_in}$ (Input capacitor ESR in 100 kHz)	0.03 $\Omega$
$C_{out}$ (Output capacitor)	100 $\mu$ F
$R_{esr\_out}$ (Output capacitor ESR in 100 kHz)	0.13 $\Omega$
$P_{max}$ (Maximum power)	5 W
Parameters of DSSS modulation	Value
$m$ sequence #1	1, 1, 1, 1, 0, 1, 0, 1, 1, 0, 0, 1, 0, 0, 0
$m$ sequence #2	1, 0, 0, 1, 1, 0, 1, 0, 1, 1, 1, 1, 0, 0, 0
$f_{switch}$ (Switching frequency)	100 kHz
$T_s$ (Duration time of a chip)	10 $\mu$ s
$f_{sampling}$ (Voltage ripple sampling frequency)	400 kHz
Data rate	6.67 kb/s

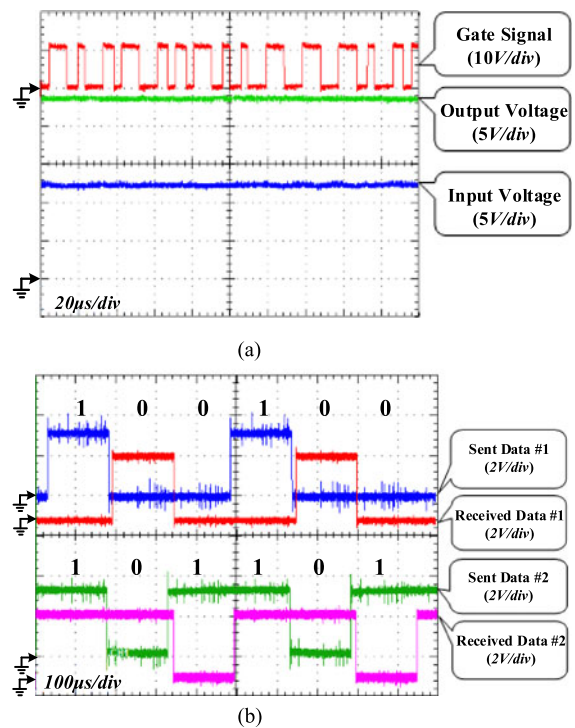


Fig. 24. Experimental waveforms Experiment II. (a) DSSS PWM and input output voltages. (b) Sent data and received data.

#2, and data #2 is sent by Boost #2 and received by Boost #1. It verifies that with CDMA concept introduced, full-duplex multiple access communication is achieved.

As discussed in Section III-C, for a system with multiple SMPSs, MAI is unavoidable, which limits communication reliability. Therefore, PN codes with better cross-correlation characteristics [19], such as 31-chip or longer golden sequences, are needed. To process longer PN codes, more calculation is needed in the receiver. Due to the computational limitation of the low cost DSP (TMS320F28035) used, only two SMPSs with DSSS based PWM can be connected into the system.

## V. CONCLUSION

A novel DSSS-based PWM strategy has been presented for both harmonic reduction and communication purposes. The proposed PWM strategy integrates three communication techniques into the SMPS designs. With the introduction of DSSS, the dominated harmonics of SMPS voltage ripples are spread and distributed to adjacent frequencies. Thus, the amplitude in spectrum is decreased significantly and the switching harmonics of SMPS are reduced. PSK data modulation is combined with PWM power modulation so that input and output voltage ripples of SMPS contain data. CDMA concept is employed for a system with multiple SMPSs. The proposed DSSS-based PWM strategy has been implemented with a low-cost DSP and evaluated experimentally. The experimental results show that the proposed PWM strategy is able to effectively reduce the SMPS's switching harmonics, and communications among SMPSs or between SMPSs and receivers are achieved through the common input or output dc power line. The proposed PWM strategy provides a low-cost communication solution for smart grid and IoT applications. The proposed scheme uses the voltage ripple as the data carrier, whose frequency equals to the switching frequency. As a result, the data rate is limited by the switching frequency. Therefore, it only can provide a noncritical low-bandwidth communication link for the applications. Also, based on (4) and (5), the voltage ripple is proportional to the ESR of the dc bus capacitance. The efficiency of a system with high dc bus ESR is low. Therefore, the proposed scheme is more suitable for low-power rating applications.

The research work presented in this paper established the novel concept of the DSSS-based PWM strategy. Future research will focus on the following two points: first, increase the possible number of SMPSs connected onto the system, where possible solutions are better microprocessors, longer PN codes, and new communication strategy, etc.; and second, to apply and evaluate the proposed method in dc microgrids applications with higher power rating.

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**Ruichi Wang** (S'14) received the B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2013, where she is currently working toward the Ph.D. degree in the College of Electrical Engineering.

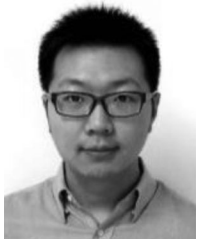
She visited Aston University, Birmingham, U.K., from September 2015 to March 2016. Her current research interests include communication technique applied in power electronics and electromagnetic interference mitigation for SMPS.



**Zhengyu Lin** (S'03–M'05–SM'10) received the B.Sc. and M.Sc. degrees from the College of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1998 and 2001, respectively, and the Ph.D. degree from Heriot-Watt University, Edinburgh, U.K., in 2005.

He is currently a Lecturer in Department of Electrical, Electronic and Power Engineering, Aston University, Birmingham, U.K. He was a Research Associate at the University of Sheffield from 2004 to 2006, an R&D Engineer with Emerson Industrial

Automation, Control Techniques PLC from 2006 to 2011, a Senior Research Scientist with Sharp Laboratories of Europe Ltd. from 2011 to 2012, and a Lecturer in Coventry University from 2013 to 2014. His research interests include power electronics and its applications in renewable energy, energy storage, motor drives, and power systems.



**Jin Du** (S'11) received the B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2011. He is currently working toward the Ph.D. degree in the College of Electrical Engineering, Zhejiang University.

His current research interests include power optimization of renewable generation and communication technique applied in power electronics.



**Jiande Wu** (M'11) was born in Zhejiang, China, in 1973. He received the B.Sc., M.Sc., and Ph.D. degrees from the College of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1994, 1997, and 2012, respectively.

Since 1997, he has been a Faculty Member at Zhejiang University, where he is currently an Associate Professor. From 2013 to 2014, he was an academic visitor at the University of Strathclyde, Glasgow, U.K. His research interests include power electronics control, distributed power electronics system, and fieldbus communication.



**Xiangning He** (M'95–SM'96–F'10) received the B.Sc. and M.Sc. degrees from Nanjing University of Aeronautical and Astronautical, Nanjing, China, in 1982 and 1985, respectively, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 1989.

From 1985 to 1986, he was an Assistant Engineer at the 608 Institute of Aeronautical Industrial General Company, Zhuzhou, China. From 1989 to 1991, he was a Lecturer at Zhejiang University. In 1991, he obtained a Fellowship from the Royal Society of U.K., and conducted a research in the Department of Computing and Electrical Engineering, Heriot-Watt University, Edinburgh, U.K., as a Postdoctoral Research Fellow for two years. In 1994, he joined Zhejiang University as an Associate Professor. Since 1996, he has been a Full Professor in the College of Electrical Engineering, Zhejiang University. He was the Director in the Power Electronics Research Institute and the Head of the Department of Applied Electronics, and he is currently the Vice Dean in the College of Electrical Engineering, Zhejiang University. His research interests are power electronics and their industrial applications. He is the author or co-author of more than 280 papers and one book *Theory and Applications of Multi-level Converters*. He holds 22 patents.

Dr. He received the 1989 Excellent Ph.D. Graduate Award, the 1995 Elite Prize Excellence Award, the 1996 Outstanding Young Staff Member Award, and 2006 Excellent Staff Award from Zhejiang University for his teaching and research contributions. He received seven Scientific and Technological Achievements Awards from Zhejiang Provincial Government and the State Educational Ministry of China in 1998, 2002, 2009, and 2011 respectively, and six Excellent Paper Awards. He is appointed as an IEEE Distinguished Lecturer by the IEEE Power Electronics Society in 2011. He is a Fellow of the Institution of Engineering and Technology (formerly IEE), U.K.