Design and Analysis of a Class of Zero Fundamental Ripple Converters

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***Abstract*—This paper introduces the design procedure for a class of bidirectional zero fundamental ripple or zero first-order ripple (ZFR) dc–dc converters. ZFR topologies eliminate the first-order switching ripples by utilizing a coupled inductor. As a result, these converters require smaller inductive and capacitive filtering elements. After introducing the modes of operation, the average model of a ZFR converter is derived. Using this model, a scheme for optimal design of the damping circuitry is introduced. Also, the overall design procedure for a ZFR converter is introduced using an example. The designed ZFR converter is experimentally evaluated to demonstrate the effectiveness of the design procedure.**

***Index Terms*—Averaging, damping resistor, ripple canceling, stability, super boost, zero ripple, ZFR.**

I. Introduction

CONVENTIONALLY, ripples induced in switching converters are filtered using *LC* or *LCL* filters. Although this method of filtering switching ripples is effective and low cost, it cannot provide ripple-free voltage and current signals. Additionally, if low ripple outputs are of interest, the size of the converter will increase due to the requirements for larger filtering elements. Unlike traditional applications, modern power converters are expected to be small, low cost, and offer lighter weights while maintaining low input/output ripples and high efficiency. Hence, instead of filtering ripples, canceling them at the source is of interest.

Ripple canceling techniques are not new [1]. However, these topologies have not been widely used due to the complexities associated with their design and in particular, their coupled inductors. Ultra low ripple converters which are often known as zero ripple converters utilize coupled inductors to compensate for the switching ripples [1]. The traditional naming of zero ripple converters is not mathematically accurate. Such converters offer zero fundamental ripple or zero first-order ripples (ZFR) but will not eliminate higher order ripples.

Various methods of ripple canceling have been proposed in the literature. For instance, Hosoki and Koizumi[2] investigate ripple canceling in high gain dc–dc converters, and ripple cancellation by interleaving boost converters was investigated in [3]. Recently, ripple canceling interleaved two switch boost topologies were investigated in [4] and [5]. This method was extended to a zero voltage switching approach in [6]. In some ZFR topologies, only current ports are tuned for canceling ripples [7], [8]. However, using the same coupled inductor structure, both current and voltage ripples can be canceled [9]. In [10]–[12], the applications of ripple cancellation for nonisolated and isolated buck topologies were investigated. Lu *et al.* [13] have investigated ZFR boost topologies with their corresponding damping circuitry. Also, coupled inductor ripple cancellation has been integrated with power factor correctors in [14]–[16].

In addition to offering lower ripples and smaller size, ripple canceling topologies eliminate the need for large electrolyte capacitors. Electrolyte capacitors are one of the leading causes of failures in power electronic converters (after connector failures). In addition, in solar applications where the input ripples can significantly reduce the performance of the maximum power point tracking scheme, a ripple canceling methodology such as [17] can improve the performance of the system compared with the traditional filtering techniques. Recently, a multiport ZFR Ćuk for photo-voltaic energy harvesting was introduced in [18] and [19]. The damping circuitry is a critical design aspect of high-order converters which has been studied in [20]–[22]. A new ZFR topology for inverter applications was recently introduced in [23]. This inverter was also utilized for drive applications in [24]. However, details regarding the design and modeling of such topologies were not provided.

In this paper, a general noninterleaved ZFR converter topology is introduced. Also, details on modeling and design of this topology are provided. Contributions of this paper include:

1) development of a design procedure for the class of ZFR converters under study;
2) development of an average model using a proposed dummy state variable to incorporate the true behavior of the coupling transformer;
3) development of an optimization scheme for the selection of damping *C–RC* circuitry to eliminate the inherent modes of oscillation within the converter; and
4) experimental design and development of a 1-kW ZFR converter for the verification of the design procedure.

II. Class of Zero First-Order Ripple Converters

In this section, a class of damped bidirectional zero first-order ripple (ZFR) converters is introduced and modeled. In this paper, first the topology is introduced and modeled.

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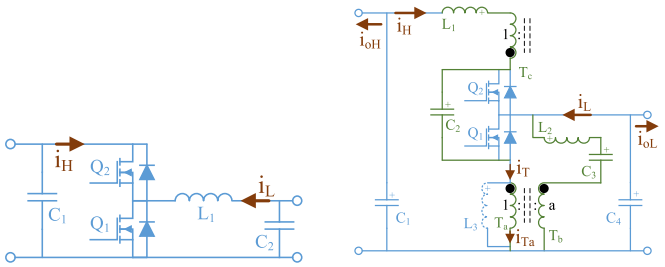

Fig. 1. Bidirectional converter leg: (a) a basic switching converter and (b) a super switching converter with ripple cancellation mechanisms which forms a ZFR topology.

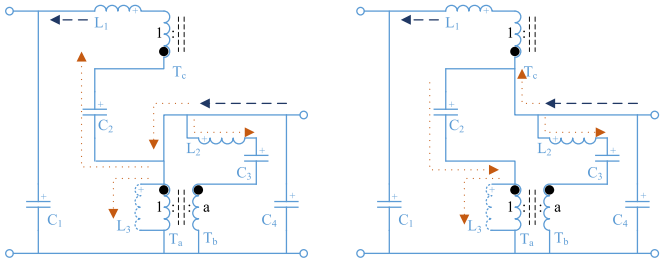

Fig. 2. Modes of operation for a ZFR converter: (a) mode A and (b) mode B.

A. ZFR Converters: A Class of Nearly Zero Ripple Converters

Fig. 1(a) illustrates the widely used converter leg which can operate as a buck or a boost converter to manage the flow of power between a high-voltage side of C_1 and a low-voltage side of C_2. This converter is efficient, small, modular, and has a low cost of manufacturing. However, the most significant drawback of this converter is the requirement for large input and output filtering capacitors. In this converter, i_H is a train of pulses and i_L has triangular ripples. Both of these currents induce voltage ripples on the output and input capacitors, respectively. Traditionally, this issue was resolved by simply selecting large capacitors for C_1 and C_2. However, this solution increases the weight, cost, and volume of the converter.

For this reason, the class of ZFR converters is incorporated to eliminate the requirements for large filtering capacitors. In the first step, the placement of L_1 needs to be changed. This inductor, which is the main energy storage element in a switching converter, is moved in series with the switching unit denoted as L_3 in Fig. 1(b). Then, a coupled inductor is introduced to compensate for the switching ripples as described in the following.

It should be noted that L_3 is in fact not a separate inductor and is the internal magnetizing inductor of the transformer. Hence, similar to a flyback converter, care should be taken in the design of the transformer so that the core provides sufficient energy storage capability (practically, by addition of an air gap). Also, the duty cycle of Q_2 is d and the duty cycle of Q_1 is $d' = 1 - d$. Switching period is $T_{\rm sw} = 1/f_{\rm sw}$.

The two modes of operation for this ZFR converter are illustrated in Fig. 2. These modes are developed with the assumption of continuous conduction mode (CCM) with respect to L_3. It should be noted that some benefits of this converter are lost for the case of discontinuous conduction mode (DCM) and hence, DCM is not considered in this paper.

B. Modes of Operation and Design Requirements

When Q_1 is active, L_3 is connected to the input (i.e., C_4) as shown in Fig. 2(a). Hence, a rise in the current of this inductor is observed such that $L_3 di_{L_3}/dt = v_{\rm in}$. To compensate for this rise, a transformer is utilized to sample the voltage of L_3 and create a voltage equal to $-av_{\rm in}$ across the inductor L_2. During the steady-state operation of the converter, the voltage of C_3 is equal to the input voltage (i.e., $v_{C_4} = v_{C_3} = v_{\rm in}$). As a result, variations in the current of L_2 follows $L_2 di_{L_2}/dt = v_{\rm in} - v_{C_3} - av_{\rm in} \simeq -av_{\rm in}$ (assuming that the changes in the voltage of C_3 are negligible). This current variation goes through the transformer $T_a : T_b$ and appears as $di_{T_a}/dt = -adi_{T_b}/dt = a^2 v_{\rm in}$ on the primary side. Now, one can notice that $i_{\rm in} = i_{L_2} + i_{T_a} + i_{L_3} + i_{L_1}$ with its derivative as $di_{\rm in}/dt = (1/L_3 - a/L_2 + a^2/L_2)v_{\rm in}$ assuming that $di_{L_1}/dt \simeq 0$ as will be shown later. By setting $di_{\rm in}/dt = 0$, one will achieve the fundamental requirement of this topology as $L_2 = a(1-a)L_3$.

This relation will ensure the cancellation of the first-order derivative of the input current. In a practical implementation, the assumption of $v_{C_3} = v_{\rm in}$ cannot be guaranteed. In fact, $C_3 dv_{C_3}/dt = i_{L_2}$. Hence

$$L_2 di_{L_2}/dt\big|_0^{d'T_{\rm sw}} = -av_{\rm in} - \int_0^{d'T_{\rm sw}} i_{L_2}/C_3 \qquad (1)$$

and the variations of the current follows a second-order differential equation. As a result, only the first-order ripples of the input current will be canceled. The above second-order variations are negligible for a properly designed converter. Additionally, i_{L_2} has a zero dc value. Hence, during each period, the above integral is calculated over a signal that is crossing zero which helps to keep the integral negligible. Since only the first derivative is zero, this converter is called a zero first-order ripple or zero fundamental ripple (ZFR) converter.

On the output side, C_2 is being discharged into the output capacitor C_1 at a constant rate of $i_{\rm out} = i_{L_1}$. In the steady-state operation of the converter C_2 has the same voltage as the output capacitor. Hence, when the Q_1 is active, variation of the current of L_1 is defined by $L_1 di_{L_1}/dt = v_{\rm in} + v_{C_2} - v_{T_c} - v_{\rm out}$. The transformer ratio of $1:1$ between T_a and T_c induces the input voltage (i.e., $v_{T_a} = v_{\rm in}$) on T_c. Also, during the steady-state operation, $v_{C_2} \simeq v_{\rm out}$ by neglecting the ripples on C_2. Therefore, the current of L_1 is almost constant considering the fact that $L_1 di_{L_1}/dt = v_{\rm in} + v_{C_2} - v_{T_c} - v_{\rm out} \simeq 0$. Similar to L_2, the accurate current of L_1 follows $L_1 di_{L_1}/dt\big|_0^{d'T_{\rm sw}} = -\int i_{L_1}/C_2$, which is a second-order differential equation with the first-order variations of zero in the vicinity of $t = 0$. Hence, by properly designing the converter with respect to the switching period, the claim of *almost zero ripple* is valid. In conclusion, the larger C_2 and C_3 are selected, the better zero ripple behavior is achieved. But this is gained at a higher cost of manufacturing and a larger real-estate requirements.

In the second mode of operation, Q_2 is active as is illustrated in Fig. 2(b). In this mode $v_{L_3} = v_{\rm in} - v_{C_2} < 0$. This will dis-

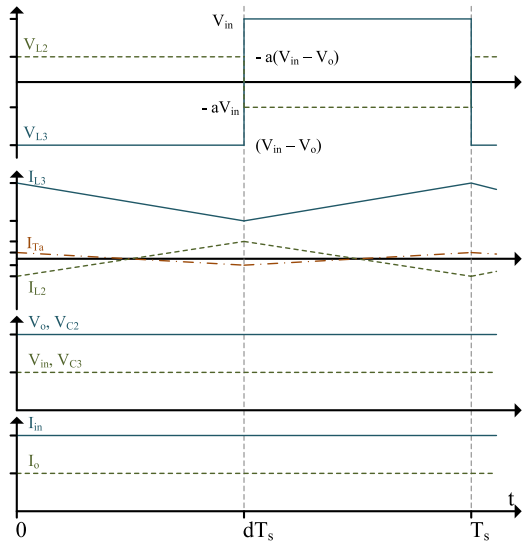

Fig. 3. Waveforms of the ZFR leg shown in Fig. 2.

charge the magnetizing ramp induced by the first mode. The equations proving the almost zero ripples are still valid and hence, the converter will operate with a negligible input or output current ripples. Voltage and current waveforms of the ZFR leg are shown in Fig. 3. This figure is valid under the assumption that the variations in voltages of C_2 and C_3 are negligible. In such conditions, the sum of $i_{L_2} + i_{L_3} + i_{T_a}$ is a dc value and is equal to $i_{\text{in}} - i_{L_1}$. Now that the fundamental requirement for achieving the almost zero behavior was introduced, a complete model of the converter will be derived in the following section.

C. Damping Resistors and Average Model

The proposed converter shown in Fig. 1(b) suffers from low damping factors on the poles generated by L_2–C_3 and L_3–L_1–C_2 resonant tanks. In practice, one can utilize active damping methods to actively oppose the oscillations occurring on these tanks. However, if the tank frequencies are close to the switching frequency, this approach is not effective. A better approach is to add damper resistors to reduce the quality factor of these tanks. However, bypass paths should be considered for the switching harmonics to eliminate loss of power in these added resistors. A common approach to design a damped capacitor bank is through the utilization of a smaller capacitor with low equivalent series resistor (ESR) in parallel with a larger capacitor in series with a resistor. This approach is known as *C–RC* tanks.

The series *RC* path will add a zero and a pole to the original transfer function. For instance, a series *LC* has a current to voltage transfer function of $i_{\text{LC}}/v_{\text{LC}} = Cs/(1 + LCs^2)$. But if the capacitor is broken into a smaller capacitor C_1 and a larger capacitor C_2 in series with a resistor R, the response is $i_{\text{LC}}/v_{\text{LC}} = ((C_1 + C_2)s + C_1C_2Rs^2)/(1 + RC_2s + L(C_1 + C_2)s^2 + LC_1C_2Rs^3)$ which can be effectively damped using R without any significant resistance for frequencies higher than that of $1/\sqrt{L(C_1 + C_2)}$. Therefore, the addition of the two damping circuitry is proposed as shown in Fig. 4. It should be noted that one can design an equivalent damping circuit using an inductive circuit assuming that

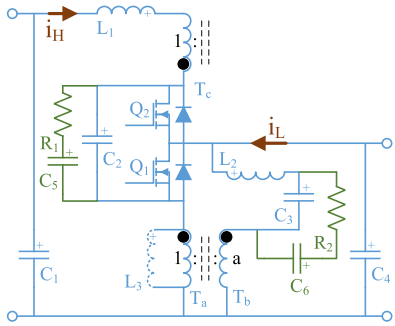

Fig. 4. Placement of damping resistors within a ZFR converter.

the tank frequency is higher than the switching frequency. But that approach is more costly. Here, the selection criteria for the capacitors are to set all of the tank frequencies to a lower frequency than that of the switching frequency as described later in the design procedure.

To design the damping circuits, the average model of the power converter shown in Fig. 4 is derived as (assuming that the duty cycle, d, is fixed) follows:

$$L_1\dot{i}_{L_1} = v_{C_2} - v_{C_1} \tag{2a}$$
$$L_2\dot{i}_{L_2} = (1-a)v_{C_4} - v_{C_3} + dav_{C_2} \tag{2b}$$
$$L_3\dot{i}_{L_3} = v_{C_4} - dv_{C_2} \tag{2c}$$
$$C_2\dot{v}_{C_2} = -d'i_{L_1} - di_{T_a} + (v_{C_5} - v_{C_2})/R_1 + di_{L_3} \tag{2d}$$
$$C_3\dot{v}_{C_3} = i_{L_2} + (v_{C_6} - v_{C_3})/R_2 \tag{2e}$$
$$C_5\dot{v}_{C_5} = (v_{C_2} - v_{C_5})/R_1 \tag{2f}$$
$$C_6\dot{v}_{C_6} = (v_{C_3} - v_{C_6})/R_2 \tag{2g}$$

where $df(t)/dt$ is denoted using $\dot{f}(t)$. If the transformer was ideal, i_{T_a} would be equal to $i_{L_1} + ai_{L_2}$. However, a technical problem is that i_{L_1} has a dc component which will not pass through a practical transformer. Hence, one should implement a practical transformer as a dynamical system with a transfer function of $s/(s + 2\pi b)$, where b defines the passband of the transformer. This transformer introduces a zero on the dc frequency to eliminate any transfer of a dc signal, while the pole at $s = -2\pi b$ cancels this effect at higher frequency. Hence, a high pass system is derived with no gain for dc frequencies and a gain of one for higher frequencies (i.e., $10b \le f$). The pole location b depends on the transformer design parameters. But for simplicity, one can assume that $0.01f_{\text{sw}} \le b \le 0.2f_{\text{sw}}$ as the design of the transformer is for f_{sw}. The core area and the number of turns do not allow for a passband lower than that of the design parameters (i.e., the magnetizing impedance acts like a short circuit for lower frequencies). To achieve this, a dummy state variable of i_{T_a} is introduced as

$$\begin{aligned}\dot{i}_{T_a} &= -2\pi bi_{T_a} + s(i_{L_1}/L_1 + ai_{L_2}/L_2) \\ &= -2\pi bi_{T_a} + (v_{C_2} - v_{C_1})/L_1 \\ &\quad + a((1-a)v_{C_4} - v_{C_3} + dav_{C_2})/L_2\end{aligned} \tag{3}$$

which can emulate the behavior of a practical transformer.

Depending on the mode of operation, the converter can be regulating the voltage of the high side or the voltage of the low side (i.e., C_1 is the input side and C_4 is the output or reverse). In either case, the input is considered as a voltage source and hence no equation will be written for the corresponding capacitor. The output has dynamics described by only one of the following equations depending on the operation mode:

$$\begin{cases} C_1 \dot{v}_{C_1} = i_{L_1} - i_{o_H} \\ C_4 \dot{v}_{C_4} = i_{T_a} - i_{L_1} - i_{L_2} - i_{L_3} - i_{o_L}. \end{cases} \tag{4}$$

To perform stability analysis and to optimally select the damper parameters, the small signal model of the converter is of interest. To derive a small signal model, the converter is considered to be connected to a voltage source on the low-voltage side which will eliminate the capacitor voltage equation for C_4. Hence, in this paper, it is assumed that the converter is operating as a boost regulator. However, based on the above equation, one can derive the following process for a buck regulator. By defining a vector of state variables $x = [i_{L_1}, i_{L_2}, i_{L_3}, v_{C_1}, v_{C_2}, v_{C_3}, v_{C_5}, v_{C_6}, i_{T_a}]^T$ the small signal model can be derived as $x = \bar{x} + \tilde{x}$, where $\bar{x}$ is vector of the state variables at the equilibrium condition and $\tilde{x}$ is the vector of small signal variations of the state variables.

Using this large signal model, the steady-state value of each state variable is calculated for a fixed duty cycle of $\bar{d}$ as

$$\begin{aligned} \bar{x} = \; & [v_{\text{in}}/(\bar{d}R_o), 0, v_{\text{in}}(1-\bar{d})/(\bar{d}^2 R_o), v_{\text{in}}/\bar{d}, \\ & v_{\text{in}}/\bar{d}, v_{\text{in}}, v_{\text{in}}/\bar{d}, v_{\text{in}}, 0] \end{aligned} \tag{5}$$

which can demonstrate the steady-state gain of the converter as $\bar{v}_{\text{out}}/v_{\text{in}} = 1/\bar{d} = 1/(1-\bar{d}')$ which is similar to a standard boost converter. The small signal model of the converter near the above equilibrium point can be derived as $\dot{\tilde{x}} = A\tilde{x} + B\tilde{u}$

$$A = \begin{bmatrix} \mathbf{0}_{3\times3} & A_{\text{LC}} & \mathbf{0}_{3\times2} & \mathbf{0}_{3\times1} \\ A_{\text{CL}} & A_{\text{CC}} & A_{CC_d} & A_{CT_a} \\ \mathbf{0}_{2\times3} & A_{C_dC} & A_{C_dC_d} & \mathbf{0}_{2\times1} \\ \mathbf{0}_{1\times3} & A_{T_aC} & \mathbf{0}_{1\times2} & -2\pi b \end{bmatrix} \tag{6a}$$

$$A_{\text{LC}} = \begin{bmatrix} -1/L_1 & 1/L_1 & 0 \\ 0 & a\bar{d}/L_2 & -1/L_2 \\ 0 & -\bar{d}/L_3 & 0 \end{bmatrix} \tag{6b}$$

$$A_{\text{CL}} = \begin{bmatrix} 1/C_1 & 0 & 0 \\ -\bar{d}'/C_2 & 0 & \bar{d}/C_2 \\ 0 & 1/C_3 & 0 \end{bmatrix} \tag{6c}$$

$$A_{\text{CC}} = -\begin{bmatrix} 1/(C_1R_o) & 0 & 0 \\ 0 & 1/(C_2R_1) & 0 \\ 0 & 0 & 1/(C_3R_2) \end{bmatrix} \tag{6d}$$

$$A_{CC_d} = \begin{bmatrix} 0 & 0 \\ 1/(C_2R_1) & 0 \\ 0 & 1/(C_3R_2) \end{bmatrix} \tag{6e}$$

$$A_{CT_a} = \begin{bmatrix} 0 \\ -\bar{d}/C_2 \\ 0 \end{bmatrix} \tag{6f}$$

$$A_{C_dC} = \begin{bmatrix} 0 & 1/(C_5R_1) & 0 \\ 0 & 0 & 1/(C_6R_2) \end{bmatrix} \tag{6g}$$

$$A_{C_dC_d} = \begin{bmatrix} -1/(C_5R_1) & 0 \\ 0 & -1/(C_6R_2) \end{bmatrix} \tag{6h}$$

$$A_{T_aC} = \begin{bmatrix} -1/L_1 & (1/L_1 + a^2\bar{d}/L_2) & -a/L_2 \end{bmatrix} \tag{6i}$$

where R_o is the output resistor connected to the high-voltage side (i.e., C_1). $\mathbf{0}$ is a matrix of zeros with an appropriate size. $\bar{d}' = 1 - \bar{d}$ is the steady-state duty cycle of the Q_1. The vector of inputs is $\tilde{u} = [\tilde{v}_{\text{in}}, \tilde{d}]^T$ and

$$B = \begin{bmatrix} 0 & 0 \\ (1-a)/L_2 & a\bar{v}_{C_2}/L_2 \\ 1/L_3 & -\bar{v}_{C_2}/L_3 \\ 0 & 0 \\ 0 & (\bar{i}_{L_3} + \bar{i}_{L_1} - \bar{i}_{T_a})/C_2 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ a(1-a)/L_2 & a^2\bar{v}_{C_2}/L_2 \end{bmatrix}. \tag{7}$$

Using this model, an optimization framework for designing the damping capacitors is introduced as follows.

From Fig. 4, one can notice that if the damping resistors go toward infinity, the damping circuits are disconnected. Similarly, if the damping resistors go toward zero, both capacitors are added together to form a larger capacitor and hence, the damping circuitry will vanish. Hence, there is an optimal value for the damping resistors to maximize the damping performance. To start, the ratio between the capacitors is defined as $k_1 = C_5/C_2 > 1$ as well as $k_2 = C_6/C_3 > 1$. C_2 and C_3 are selected based on other criteria which are introduced in the next section. However, k_1 and k_2 are parameters that have to be optimally selected using the proposed framework. To optimally select the set of $\mathcal{D} = \{R_1, R_2, k_1, k_2\}$, one needs to perform a multiobjective optimization over the feasible range of these parameters. The proposed optimization is

$$\max_{\mathcal{D}} \;\; O_1 + \gamma_1 O_2 + \gamma_2 O_3 \tag{8a}$$

$$\text{s.t. } \nu = [\nu_i] = [\lambda \mid |A(\mathcal{D}) - \lambda I| = 0] \tag{8b}$$

$$1 \le k_1, \; k_2 \tag{8c}$$

$$O_1 = -\max(\Re(\nu)) \tag{8d}$$

$$O_2 = \min(-\text{diag}(|\nu|)^{-1}\Re(\nu)) \tag{8e}$$

$$O_3 = -(k_1 + k_2) \tag{8f}$$

where $\Re(\cdot)$ is the vector of the real parts of its argument, $\text{diag}(\cdot)$ generates a diagonal matrix from its input vector, and ν is the vector of eigenvalues λ_i, which is defined using (8b). It should be noted that the matrix A in (6) is a function of $\mathcal{D}$ and has to be dynamically recalculated during the optimization to be used as the constraint (8b). γ_1 and γ_2 form a linear combination between

the objectives. O_1 maximizes the absolute value of the real part of the slowest pole of the system to achieve a faster settling time. O_2 maximizes the lowest damping factor of the poles (O_2 will find the lowest damping factor, and the optimization will then maximize the lowest damping factor). By maximizing the lowest damping factor, the circuit will be damped as much as possible to minimize the oscillations caused by the complex pole pairs. A simple definition for the damping factor ζ can be proposes as

$$\zeta \simeq -\Re(\lambda)/|\lambda| \tag{9}$$

which defines the damping factor as the ratio between the real part of the pole and its absolute value. If the pole is imaginary, this value is zero and if the pole is real, this value is one. Therefore by maximizing this parameter, one can reduce the impacts of the sinusoidal terms (i.e., imaginary components) in the time-domain response of the pole. Finally, the third objective minimizes the sum of k_1 and k_2. The larger this sum is, the larger capacitors are required. Hence, the third objective aims at finding a compromise between the first two performance objectives and the cost of the converter.

Additionally, a constraint on the value of the resistors is required to reduce the passage of the switching currents through the resistors. If the resistors are too small, the main switching current will pass through the series *RC* paths and will reduce the efficiency of the converter. Consider the block C_3–C_6–R_2. At the switching frequency, the impedance of C_3 is $|Z_{C_3}| = 1/(2\pi f_{\rm sw} C_3)$ while the impedance of C_6–R_2 is $|Z_{C_6R_2}| = \sqrt{1+4\pi^2 f_{\rm sw}^2 k_2^2 C_3^2 R_2^2}/(2\pi f_{\rm sw} k_2 C_3)$. If $\kappa = |Z_{C_6R_2}|/|Z_{C_3}|$, then it is desired to have M times higher impedance for C_6–R_2 compared with the C_3 path at this frequency to ensure passage of the switching ripples from the C_3 path (i.e., $\kappa \geq M \geq 1$). Hence, a lower boundary for R_2 is derived as

$$\left(\sqrt{M^2 k_2^2 - 1}\right)/(2\pi f_{\rm sw} k C_3) \leq R_2 \tag{10}$$

where $M^2 k_2^2$ is always greater than one since both k_2 and M are greater than one. A similar boundary for R_1 is $(\sqrt{M^2 k_1^2 - 1})/(2\pi f_{\rm sw} k C_2) \leq R_1$. Using these final constraints, the optimization can be solved to find the optimal values for the set $\mathcal{D}$.

The above optimization problem is nonconvex and is NP-hard (the values of k_i and R_i are not continuous and depend on the availability of the components). One can solve this optimization using a heuristic method such as the particle swarm optimization or differential evolution. It should be noted that this is a design optimization and does not have to be solved very often. Hence, improving the speed of the optimization is not necessary.

III. Design Procedure for a ZFR DC–DC Converter

In this section, the design procedure for a ZFR boost converter is introduced along with a design example of a 1-kW 50–100 V ZFR boost converter operating at a switching frequency of 200 kHz which is experimentally evaluated in the results section. This section is introduced with respect to parameters defined in Fig. 4. Based on the model developed earlier, the steady-state ratings of each element is calculated.

A. Power Stage Design

The first step in designing a ZFR converter starts with the selection of a nominal current ripple on the magnetizing inductance of the transformer L_3. This approach is similar to the design procedure for a boost or a fly back converter. In practice, a current ripple of 25% can lead to satisfactory results. It should be noted that although the input current has no ripples, the magnetizing current of the transformer has ripples and these ripples define the CCM range for the converter. Using the up ramp in the current of the inductor, one can derive

$$L_3 = v_{\rm in} d' T_{\rm sw}/(2k\bar{i}_{L_3}) \tag{11}$$

where k is the desired ratio between the amplitude of the current ripple to the nominal average current. For the 1 kW converter under study, $k = 25\%$ and hence, L_3 is 25 μH which is set to 28 μH (due to the quantization effect while wrapping the coil in the experimental section). This value is the magnetizing inductance of the transformer seen from T_a.

The next step is to design the input ripple canceling circuit. The ratio of the transformer for $T_a : T_c$ is $1:1$. However, the selection of $T_a : T_b$ is a design choice. For the proper operation of the circuit, $L_2 = a(1-a)L_3$. Hence, $0 < a < 1$ is a boundary for selecting a. To optimally select a, one should note that the voltage applied L_2 is $av_{\rm in}$ and hence, the current of this inductor is proportional to a/L_2. Also, the total energy stored in this inductor is proportional to $L_2 i_{L_2}^2$ and so to a^2/L_2. However, $L_2 = a(1-a)L_3$. Therefore, the energy stored in this inductor which is directly responsible for the size and volume of this inductor is proportional to $a/(1-a)$. As a result, naturally, one tries to minimize this value on the range of $0 < a < 1$. It should be noted that L_2 is the sum of the leakage inductance of T_b and an added inductance of L_2'. Hence, there is another minimum boundary induced by the leakage inductance of T_b as $L_{l-T_b} \leq a(1-a)L_3$ (i.e., the added inductance of L_2' cannot be a negative value). Therefore, the optimal value for a is in fact the ratio between the leakage inductance of L_{l-T_b} and the magnetizing inductance, L_3. However, to enforce the placement of the main magnetizing behavior on T_a, a small added inductance, L_2', in series with T_b is recommended. In this paper, it is suggested that $a = 0.25$. Hence, for the 1-kW example under study, $L_2 = L_{l-T_b} + L_2' = 5.2\,\mu$H (in the practical example, the leakage inductance of T_b is measured at $4.2\,\mu$H and hence, $L_2' = 1\,\mu$H).

The selection of C_3 is a tradeoff between the cost and the performance. Higher capacitance values will allow for better ripple cancellation but at a higher cost. The lowest value that can be selected is limited by the resonance frequency of L_2–(C_3–C_6). To have a good ripple cancellation, the voltage ripples of this capacitor are limited to a factor of $k = 1\%$ to 10%. Voltage of this capacitor varies as a result of i_{L_2}. Hence, assuming a linear ramp for the current of L_2, the current of i_{L_2} by the end of $d'T_{\rm sw}$ is $i_{L_2} = av_{\rm in} d' T_{\rm sw}/2L_2$. Current of L_2 is roughly triangular. To get a simple model for the current of C_3, it is

assumed that the average of this current is passing through the capacitor (i.e., the triangle is represented by its dc average). Hence, as an approximation, to get $k\%$ ripple on v_{C_3}, one can derive

$$C_3 = ad'T_{\rm sw}^2/(8L_2k) \tag{12}$$

and with $k = 2\%$, $C_3 \simeq 4\,\mu$F. But to ensure stable operation of the converter and for proper selection of the damping resistors, one should care to set the tank frequency of C_3–L_2 to at least 0.5–2 decades below the switching frequency (otherwise, either the circuit is not properly damped or the efficiency is reduced as the main switching ripples will pass through the damping resistors). In this example, $f_{L_2C_3} \simeq 25\,$kHz which is 0.85 decade below the switching frequency. Hence, C_3 is increased to $8\,\mu$F to achieve the 1 decade separation. This approach will slightly increase the cost of the converter while improving its efficiency (this separation allow for proper design of the damping resistor and to prevent any switching ripples passing through the damping resistor). For a practical implementation, one needs a capacitor with the selected value and with a current tolerance of $i_{C_3}^{\rm RMS} = av_{\rm in}d'T_{\rm sw}/(2\sqrt{(}3)L_2)$. In this example, this value is 2A.

The next step is to select L_1. L_1 is the total inductance of the leakage inductance of T_c and an external inductor L_1' as $L_1 = L_{l-T_c} + L_1'$. This inductor is to prohibit variations of current on the T_c side. Hence, by selecting a sufficiently large inductor, L_1 can regulate the current of its path and prevent variations in the current of T_c. The minimum value for this inductance is the leakage inductance of T_c itself. However, it is recommended to add a series inductance L_1' so that the total inductance in this path is twice as large as L_3 to ensure that the magnetizing behavior appears on T_a. In the example under study, an external inductor of $L_1' = 25\,\mu$H is added to the leakage inductance of L_{l-T_c} which is measured at $28\,\mu$H.

C_2 can be selected by assuming a nominal voltage ripple as well. The voltage ripple of this capacitor is almost canceled by the voltage induced on T_c and will not directly propagate to the output (unlink conventional converters, in this converter the ripple is passed as a second-order differential equation which relaxes the requirements for larger capacitance values). In this paper, a nominal ripple of $k = 2.5\%$ is considered. Therefore,

$$C_2 = d'T_{\rm sw}/(kR_o) \tag{13}$$

and hence, $C_2 = 10\,\mu$F for the example under study. After selection of this capacitor, the resonant tank frequency of L_3–L_1–C_2 has to be checked to ensure sufficient separation from the switching frequency. In this case, $f_{L_1L_3C_2} \simeq 5\,$kHz. For a practical implementation, one needs a capacitor with the selected capacitance and a current ripple tolerance of $i_{C_2}^{\rm RMS} \simeq i_{\rm out} = v_{\rm in}/(dR_o)$. In this example, this value is 10 A and hence, a high current, low ESR metalized polypropylene film capacitor will be selected.

The output capacitor does not have any specific requirements as the ripples on this capacitor are theoretically negligible. One can design this capacitor based on the full load step considering the bandwidth of the converter. If the converter has a full step response time of $T_{\rm settle}$, then the output capacitor should tolerate the full load from the time of the load step t to $t + T_{\rm settle}$ with a maximum drop of $k\%$. Hence, $T_{\rm settle}/(kR_o) \le C_1$. In this example, $C_1 = 7.5\ \mu$F.

Finally, to optimally find the damping parameters, the circuit parameters of $C_1 = 7.5\,\mu$F, $C_2 = 10\,\mu$F, $C_3 = 8\,\mu$F, $L_1 = 25\,\mu$H, $L_2 = 5.2\,\mu$H, and $L_3 = 28\,\mu$H are placed in (6) to derive the state matrix A. This matrix is a 9×9 matrix with four unknown parameters of C_5, C_6, R_1, and R_2. To perform the optimization (8), $C_5 = k_1C_2$ and $C_6 = k_2C_3$ and the optimization is performed on k_1 and k_2 instead as described before. Also, k_1 and k_2 have to be larger than one to provide the desired damping behavior. Larger values of k_1 and k_2 will add to the cost and real-estate requirements of the design. Hence, as a rule of thumb, many industries use a k value of 2 or 3 to design a *C–RC* damping scheme. Also, k_1 and k_2 are selected as fractional numbers based on the availability of capacitors. In this example, k_1 and k_2 are selected from the set $\{1.5,\ 2,\ 2.5,\ 3\}$. Constraints on R_1 and R_2 are defined using (10). In (10), M is selected as $M = 5$ to guarantee the *RC*-path impedance of at least five times higher than the *C* path at the frequency of switching. This will improve the efficiency of the converter by reducing the flow of the switching current through the *RC* path. Based on this *M* and using the largest *k*'s, the constraints are derived as $0.4\Omega \le R_1$ and $0.49\Omega \le R_2$. Also, the values of these resistors are restricted to the standard 1% resistor table. The objective of the optimization is

$$\min[\max(\Re(\nu)) + \max(\mathrm{diag}(|\nu|)^{-1}\Re(\nu)) + \gamma K] \tag{14}$$

where $K = k_1 + k_2$. By solving this optimization problem using PSO, $R_1 = 1.2\Omega$, $R_2 = 1.3\Omega$, $k_1 = 2$, and $k_2 = 2$.

B. Controller Design

In this paper, PI controllers are considered for the current and voltage regulators. Although more advanced type of controllers are applicable, majority of the industries prefer simple analog controllers to achieve cost effectiveness. To design the PI controllers, two approaches can be taken. In the first approach, the linearized model of the system can be reduced in order. It has been shown that a reduced order model can improve the performance of the controllers designed based on the analytical methods. In the second approach, the order of the model is not reduced and the controller parameters are numerically optimized to achieve the desired performance indices. The second method requires numerical optimization but will deliver the optimal compensator coefficients. In this paper, PI parameters are optimized using the full small signal model of the system in Matlab. In the first step, the current controller has to be designed.

The ZFR converter under study has multiple current paths that can be regulated. The magnetizing current of the converter i_{L_3} defines the power flowing through the converter and can be considered as the main current to be regulated. However, L_3 is an imaginary inductor and the current of this inductor is not measurable. The current of the primary side of the transformer can be written as $i_{L_3} - i_{T_a} = i_{L_3} - \tilde{i}_{L_1} - ai_{L_2}$. This current is measurable and contains information regarding the current

ripples which can be used for fault circuitry and peak current control.

In the example under study, the input current is of interest. Input current can be described as $i_{\rm in} = i_{L_1} + i_{L_2} + i_{L_3} - i_{T_a} = (i_{L_1} - \tilde{i}_{L_1}) + (1-a)i_{L_2} + i_{L_3}$ which does not contain the first-order switching ripples and has a steady-state value of $v_{\rm in}/(d^2 R_o)$. Due to lower ripple contents, this current allows for a better PI controller design with reduced ripple pass-through challenges in analog implementation of proportional controllers. Based on the model developed before, a selection matrix of C = [1, 1,1, 0, 0, 0, 0, 0, -1] can extract the input current as $\tilde{i}_{\rm in}(s)/\tilde{d}(s) = C\tilde{x}(s) = C(s\mathbf{I} - A)^{-1}B[0,1]^T$, where $[0,1]^T$ selects the duty cycle as the input. During the controller design, one should note that the model is derived based on the duty cycle of Q_2. However, the converter is operating in the boost mode. Hence, the controller requires to have one additional negative sign for stability since $\tilde{i}_{\rm in}(s)/\tilde{d}(s)|_{s\to 0} < 0$. This PI controller will regulate the current passing through the converter. Knowing the duty cycle, one can directly control the magnetizing current of the converter using this PI controller and without adding a separate current sensor on T_a.

By robust tuning of PI parameters using Matlab, an optimized PI controller for this design is derived as $k_{p_i}(1 + k_{i_i}/s)$ with $k_{p_i} = 0.00092$ and $k_{i_i} = 14\,000$. This PI controller generates the small signal variations of $\tilde{d}$ as a function of the current feedback. Meanwhile, the large signal duty cycle, $\bar{d}$ can be calculated as $\bar{d} = v_{\rm in}/v^*_{C_1}$. Therefore, the combined feedforward and feedback controllers is $d = v^*_{C_1}/(R_o i^*_{\rm in}) - k_{p_i}(1 + k_{i_i}/s)(i^*_{\rm in} - i_{\rm in})$ which can be written as $d = v_{\rm in}/v^*_{C_1} - k_{p_i}(1 + k_{i_i}/s)(i^*_{\rm in} - i_{\rm in})$ to eliminate the dependence on R_o (the superscript $*$ denotes the reference parameter).

Next, by combining the current controller and the small signal of the system in Matlab, a voltage controller is designed for the closed-loop current-controlled example as $k_{p_v}(1 + k_{i_v})$, where $k_{p_v} = 0.23$ and $k_{i_v} = 14\,000$. Now, the voltage and current controllers are designed and can be implemented as well as the hardware.

IV. Converter Development and Experimental Results

In this section, the 1-kW 50–100 V converter designed in this paper will be developed and evaluated.

A. Coupled Inductor Development

It should be noted that the total $N \times I$ in the magnetic core of the coupled inductor is $N_a i_T + a^2 N_a i_{L_2} + N_a i_{L_1}$, where N_a is the number of turns for T_a [see Fig. 1(b)]. Based on the equilibrium point derived in (5), the dc magnetizing term of the core is $N_a v_{\rm in}/\bar{d}^2 R_o$ which will be added by the ripple terms including the major ripples of L_3 as $v_{\rm in}(1-d)T_{\rm sw}/2L_3$. Hence, as the gain of the converter is increased, the magnetizing current increases by a square factor. This is a significant drawback for this converter. However, as long as a reasonable gain is demanded, the total magnetic core required will be smaller than that of a traditional topology offering the same input/output ripples.

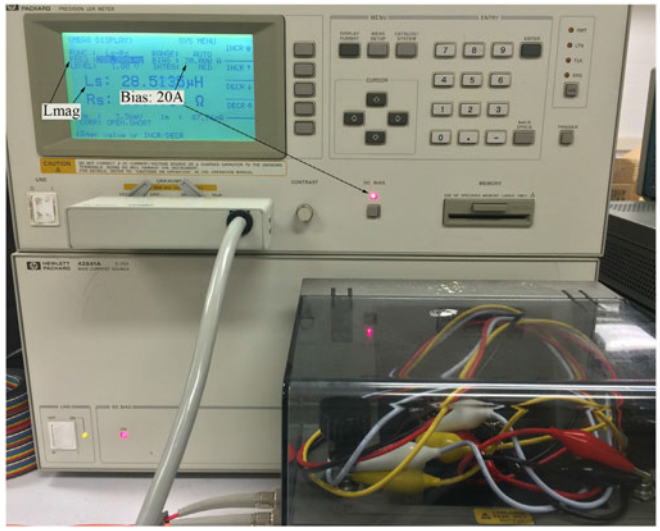

Fig. 5. Testing of the inductor under a bias of $v_{\rm in}/\bar{d}^2 R_o = 20$ A.

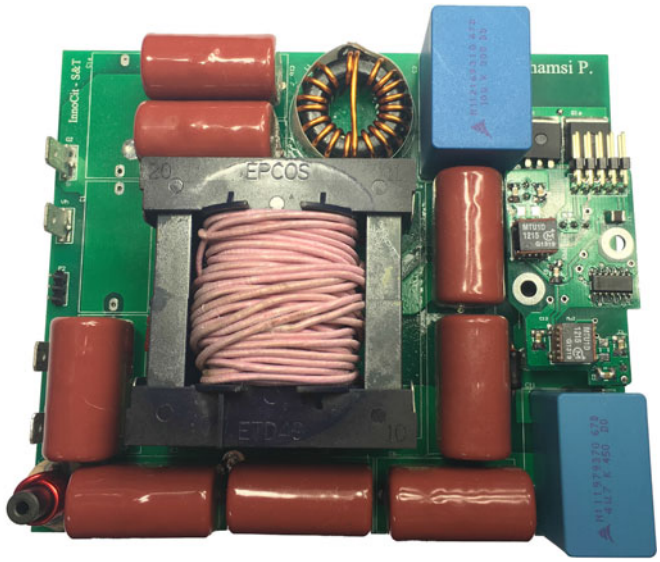

Fig. 6. Designed 1-kW 50–100 V bidirectional ZFR boost converter.

In this example, the gain of the converter is set to 2. Hence, the inductor will have to handle slightly more than 20 A without entering saturation. To implement this inductor, an ETD core is wrapped with 12 turns of four parallel Litz wires to construct T_a, 12 turns of four parallel Litz wires for T_c, and 4 turns of the same Litz wire for T_b (the wire used are rated for 2.5 A). This inductor was tested under a 20 A dc bias to ensure its performance and maintaining its inductance at the maximum load. This test is shown in Fig. 5.

B. Experimental Results

The final converter is developed and is depicted in Fig. 6. In this section, different sets of loads are applied to this converter. First, the converter is loaded at 25% of its nominal rating. Results are plotted in Fig. 7. It can be observed that the output voltage

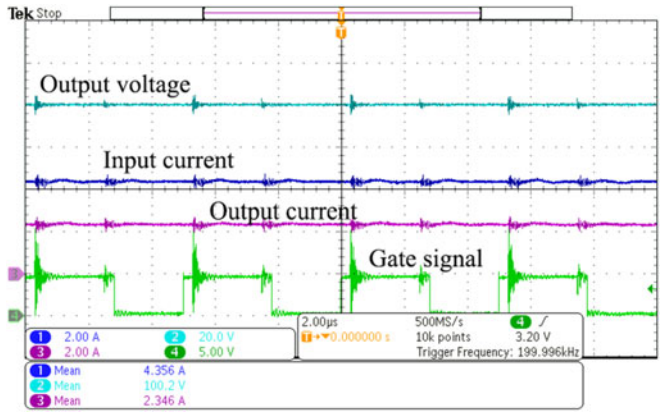

Fig. 7. Input/output signals measured during a 25% loading.

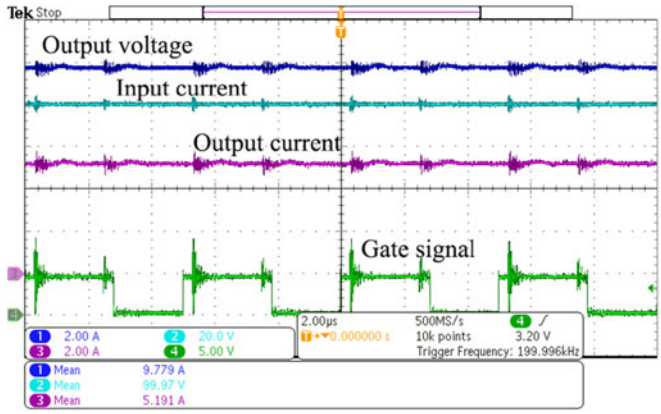

Fig. 8. Input/output signals measured during a 50% loading.

and current are almost flat. This is achieved with about 20 μF of total output capacitance. The reason for the slight deviation on the current measurements is the electromagnetic interference (EMI) induced on the current probes due to their close proximity to the magnetic core. The output of the converter is connected to a resistive load and hence, in reality, the output current is as flat as the output voltage.

The input current has a slightly higher ripples. The main reason for such ripples is the nonideal ripple cancellation due to the practical development of the circuit. The perfect cancellation can be achieved only if $L_2 = a(1-a)L_3$. However, in a real-world development of the converter, exact matching of the inductors cannot be achieved. Considering the utilization of only 4.7 μF input capacitor, this converter offers a much lower input ripples compared with a traditional topology.

Now, the load is increased to 500 W. This scenario is illustrated in Fig. 8. It can be observed that the signals are still satisfactory. However, the effects of EMI are impacting the measurements more than the previous case. In the last case, the converter is fully loaded and the signals are illustrated in Fig. 9. It can be observed that the input current is smoother in the 50% and 100% tests. This is due to the variations of the inductors as a function of current. The testing of the inductors was performed at the full load. Hence, the accuracy of $L_2 = a(1-a)L_3$ is

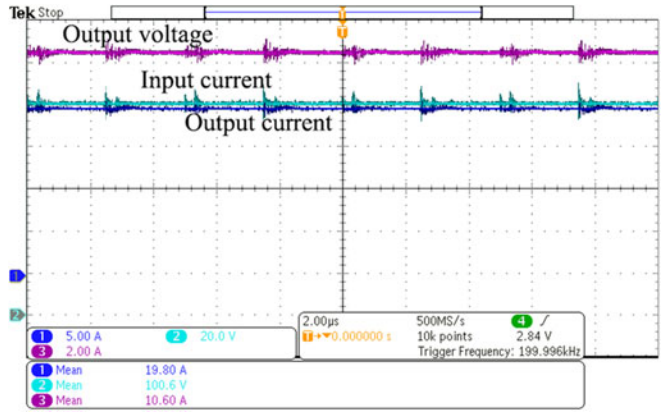

Fig. 9. Input/output signals measured during a 100% loading.

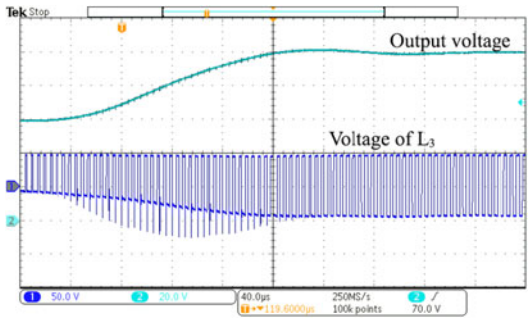

Fig. 10. Step response of the designed ZFR boost.

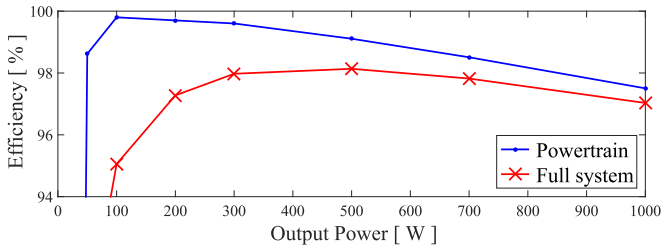

Fig. 11. Efficiency of the ZFR boost.

higher near the full load. Fig. 9 illustrates a very flat input and output currents, which demonstrate the effectiveness of the proposed bidirectional topology and the design process.

A step-up response of the ZFR boost is plotted in Fig. 10. The initial reference voltage of the converter is set to the minimum voltage that will maintain the CCM with the nominal load. This voltage is 60 V. The step response is applied by setting the reference to the nominal value of 100 V. Results are plotted in Fig. 10. It can be observed that the settling time is close to 160 μs. Also, the voltage of L_3 is swinging between v_{in} and $-(v_o - v_{\text{iv}})$ which is initially equal to +50 V and -10 V and has gradually increased to +50 V and -50 V.

The measured efficiency plot of the designed ZFR converter is shown in Fig. 11. In this figure, the power train plot illustrates the input–output efficiency of the ZFR boost without including the power required to run the controller and the gate drivers. The full

TABLE I
COMPARISON BETWEEN A ZFR AND A TRADITIONAL 1-KW BIDIRECTIONAL BOOST CONVERTERS OFFERING THE SAME INPUT AND OUTPUT RIPPLES

Parameter	ZFR	Traditional
Inductor		
- Total Inductance	60 μH	420 μH
- Weight	120 g	900 g
- Volume	50 cm^3	600 cm^3
Capacitors		
- Total Capacitance	$\simeq$ 55 μF	4700 μF
- Weight	60 g	700 g
- Volume	42 cm^3	820 cm^3

system plot illustrates the efficiency of the system, including the controllers, gate drivers, and auxiliary power supplies. It can be observed that the efficiency of the converter has its maximum at 100 W output power. The reason for this behavior is the structure of the coupled inductor. The coupled inductor has a dc current bias of $Ni_{\rm in}$. This bias current does not contribute to the ripple canceling behavior. However, it will shift the magnetic flux of the coupled inductor toward 0.25 T causing higher magnetic losses for the high-frequency components of the current. The Ferrite core used in this design is recommended to be operated at under 0.1 T at 200 kHz. Hence, as the output power increases, the magnetic losses in the inductor will increase exponentially.

The comparison between the proposed ZFR boost and a traditional boost offering the same input and output ripples is shown in Table I. The switching frequency for the traditional boost converter is the same as the ZFR boost. Since the traditional boost does not demonstrate ripple canceling behavior, a larger inductor is required to filter the input current. Additionally, the output current of a traditional boost converter is not continuous. Hence, a very large capacitor is needed to achieve the same level of output ripples as a ZFR boost. In particular, the efficiency of a traditional converter offering the same input and output ripples is lower than a ZFR boost. Between the two converters, the losses on the switches are the same as the switches will observe the same current and voltage stresses. However, if a same magnetic material is used, to achieve the required 420 μH filtering inductor, the volume of the magnetic material has to be seven times larger (under the same flux density). And since the losses in the magnetic material are proportional to the volume, the magnetic losses of the traditional boost will be higher. At the same time, the higher number of turns used to achieve 420 μH will lead to higher copper losses. In addition, the capacitors in the traditional boost are electrolytic. Electrolytic capacitors have higher ESRs and generate more losses.

V. CONCLUSION

This paper introduced a class of bidirectional ZFR legs. An average model for such legs was developed for both buck and boost modes of operation. A design procedure for the proposed ZFR legs was introduced. Later, the small signal model of the converter was developed and a procedure to optimally design the damping circuitry was provided. Finally, experimental measurements from a 1-kW ZFR boost were illustrated and the effectiveness of the ZFR topology in providing low ripple input/output currents was demonstrated.

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