Analysis and Compensation of Inverter Nonlinearity for Three-Level T-Type Inverters

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***Abstract*—This paper addresses the inverter nonlinearity of a three-level T-type inverter. The main causes of the nonlinearity are pulse shaping, pulse skipping due to narrow pulses for the dead time, and voltage drop of the switching devices. Although the same causes have existed in two-level inverters, the pulse skipping phenomenon and results are quite different in the case of the three-level T-type inverter. The effects of pulse shaping and skipping have been investigated and discussed. In addition, the voltage drop of the switching devices has been considered in conjunction with the conduction path of the T-type inverter. Compensation methods based on the pulse width modulation (PWM) of T-type inverter to alleviate the inverter nonlinearity have been proposed from research results. The proposed methods could be easily implemented by adding appropriate offset voltages to the voltage references of the inverter in PWM. Furthermore, a neutral voltage balancing method of a three-level T-type inverter has been proposed in conjunction with the proposed PWM methods using offset voltage. Through extensive experimental tests, the fifth- and seventh-harmonic components of the current are conspicuously reduced along with the even harmonics. The neutral voltage of the inverter can be balanced effectively with the proposed offset voltage adjustments as well.**

***Index Terms*—Even-order harmonics, inverter nonlinearity, narrow pulse, neutral point (NP) voltage control, offset voltage, pulse shaping and skipping, three-level topology, T-type inverter.**

I. Introduction

MULTILEVEL pulse-width modulation (PWM) voltage-source inverters (VSIs) have received much attention thanks to their advantages over two-level VSIs, such as better harmonic characteristics, smaller *dv/dt*, and higher efficiency. Among many multilevel inverters, three-level inverters, such as neutral point clamped (NPC) topology and T-type topology, have been widely used due to their relatively simple control and technical maturity. T-type topology is preferred over NPC topology in low-voltage applications where the conduction losses could be minimized due to the reduced number of switching semiconductors [1].

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However, due to the increased number of switching states, the inverter nonlinearity resulting in output voltage distortion on the three-level topology is more complicated than that in the two-level topology. The inverter nonlinearity effects from the dead time, parasitic capacitors, and voltage drop across the switching devices distort the output voltage of the inverter and degrade overall performances of the variable-speed electric machine drive system fed by a three-level T-type inverter.

There has been lots of research conducted on the inverter nonlinearity compensation for two-level inverters [2]–[9]. Some previous literature [2]–[5] proposed inverter nonlinearity compensation methods by adding a compensation voltage to voltage references [2], [3] or adjusting the length of gating pulses [4], [5]. The effect of parasitic capacitances [5]–[7] and voltage drops across the switching devices [2], [7] were considered to improve compensation accuracy. Moreover, the inverter nonlinearity in multilevel inverters and its compensation were addressed in several papers [10]–[16].

However, the majority of literature did not cover output voltage distortion induced by so-called narrow pulses resulting in pulse skipping during the dead time [8], [9] that occurs when pole voltage references are near the PWM carrier edges. The problem should be considered since it becomes more severe for multilevel inverters. In [12] and [13], the pulse skipping problem in the overmodulation region was considered on the basis of space vector PWM (SVPWM). Nevertheless, SVPWM had complications accommodating the compensation algorithm against the problem, because the on-time of each switch of the inverter was geometrically computed. Non-nearest three vectors SVPWM were proposed to avoid the narrow pulses [14], but causes considerable voltage harmonics compared to the conventional SVPWM.

It has been known that the carrier-based PWM methods are equivalent to SVPWM, but simpler to implement. In [15] and [16], techniques to prevent the narrow pulses in three-level VSI drives based on zero-sequence voltage injection were proposed. However, they did not consider other factors like sideband harmonics at the carrier frequency and neutral point (NP) voltage balancing issues. A repetition algorithm was presented to resolve the narrow pulse problem and enable the NP balancing [16]. However, it asked for online computation that could be a burden to low-cost digital signal processors (DSP). Moreover, the effects of parasitic capacitors were disregarded in aforementioned compensation methods [11]–[16] against the narrow pulse problem. Even-order harmonics from the T-type inverter

TABLE I
FEATURES OF CONVENTIONAL METHODS

Control issues	Zhou and Rouaud [10]	Minshull *et al.* [11]	Li *et al.* [12]	Jin and Zhong [13]	Liu and Cho [14]	Zheng [15]	Guan and Wang [16]
Parasitic capacitors	O	X	X	X	X	X	X
Narrow pulse problem	X	X	O	O	O	O	O
Neutral voltage balancing	X	X	X	X	X	O	O
Even-order harmonics	X	X	X	X	X	X	X

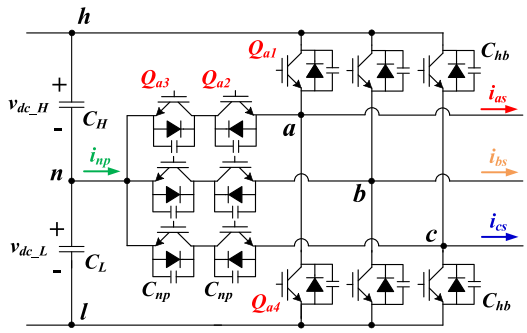

Fig. 1. Circuit diagram of a three-level T-type inverter.

nonlinearity have not been fully covered, although they cause considerable distortion of the inverter output voltage. Features of aforementioned algorithms [10]–[16] can be summarized as in Table I. In the table, "O" and "X" indicate whether each issue is considered or not. It can be seen that none of them fully considered the inverter nonlinearity issues in T-type inverters.

In this paper, the inverter nonlinearity effects that result in the output voltage distortion of the three-level T-type inverter are addressed in detail. Based on the analysis, a carrier-based PWM technique as well as a compensation method to alleviate the inverter nonlinearity effects is proposed. In the proposed PWM methods, the controllability of NP voltage and output voltage linearity is considered. By adjusting the offset voltage to solve aforementioned nonlinearity issues by the proposed PWM methods, the NP balancing could be realized simultaneously. The experimental results are provided to verify the validity of the proposed methods. In addition to the previous version of this research [17], a comparative study on the inverter nonlinearity effects and experiments on the dynamic performances of the proposed NP balancing controllers are included in this paper.

II. ANALYSIS OF INVERTER NONLINEARITY EFFECTS IN THREE-LEVEL T-TYPE INVERTERS

Fig. 1 shows the configuration of a three-level T-type inverter. Due to the junction capacitance of the semiconductor switches, there are naturally parasitic capacitors connected in parallel with the half-bridge switches ($C_{\rm hb}$) and bidirectional switches ($C_{\rm np}$). For the output pole voltage, $v_{\rm xn}$ where x denotes an arbitrary phase among a, b, and c, three switching states can be defined as follows: "H" state when phase current, $i_{\rm xs}$, flows through the upper switch, "M" state through the bidirectional switches, and "L" state through the lower switch.

There are two main causes for an output voltage error, $\delta v_{\rm xn}$, which is defined as

$$\delta v_{\rm xn} = v^*_{\rm xn} - v_{\rm xn} \tag{1}$$

where $v^*_{\rm xn}$ stands for a pole voltage reference and $v_{\rm xn}$ for an actual pole voltage. Note that all the variables in (1) are per-switching-cycle average quantities.

A. Pulse Shaping and Skipping due to the Dead Time

The voltage distortion from the narrow pulse issue is depicted in Fig. 2 where the dead time is set as T^*_d. Fig. 2 shows the x-phase pole voltage generation in a three-level inverter based on level-shifted carrier waves while considering the effect from the dead time when the polarity of $i_{\rm xs}$ is positive. In this figure, the values with subscript "*pwm*" indicate instantaneous quantities and $V_{\rm DT}$ is defined as $V_{\rm DT} = T^*_d / T_{\rm sw} \cdot V_{\rm dc}$, where $V_{\rm dc} = v_{\rm dc\_H} + v_{\rm dc\_L}$. To simplify the analysis, each dc-link voltage, $v_{\rm dc\_H}$ and $v_{\rm dc\_L}$ defined in Fig. 1, is assumed to be equally balanced (i.e., $v_{\rm dc\_H} = v_{\rm dc\_L} = 0.5V_{\rm dc}$). If $v^*_{\rm xn}$ is between $V_{\rm DT}$ and $0.5V_{\rm dc} - V_{\rm DT}$ as shown in Fig. 2(a), the dead time effect in three-level inverters is very similar to that in two-level inverters. At on-sequence, where the switches are turning on, the output voltage is simply delayed by T^*_d, which leads to volt–sec loss in the inverter output. At off-sequence, where the switches are turning off, the pulses from the inverter are shaped, because the output voltage does not fall instantly after the gating signal is turned off. In this condition, the falling rate is determined by the parasitic capacitances and the current during the dead time and leads to volt–sec gain in the inverter output. When $v^*_{\rm xn}$ is set between $0.5V_{\rm DT}$ and $V_{\rm DT}$, as shown in Fig. 2(b), the dead time at on-sequence affects the output voltage at off-sequence. The dead time effect in this case is the same as that in the previous case for a switching period in the average manner. However, if $v^*_{\rm xn}$ is between 0 V and $0.5V_{\rm DT}$, as shown in Fig. 2(c), the actual pole voltage $v_{\rm xn\_pwm}$ is clamped to 0 V since the two dead time durations at on and off sequences are overlapped and the turn-on signal for the switch is cut off. The pulses are skipped in this case and the phenomenon is called the narrow pulse problem [8]. If $v^*_{\rm xn}$ is negative and gets closer to the carrier peak, a larger distortion occurs in the output voltage, as shown in Fig. 2(d).

Fig. 3 shows the distortion of the output voltage assuming that parasitic capacitors do not exist. In this figure, $V_{\rm DZ} = 0.5V_{\rm DT}$ and four regions, denoted as DZ1-DZ4 and whose widths are determined by $V_{\rm DZ}$, indicate dead zones where the output voltage cannot be synthesized properly. DZ1 and DZ3 arise with the positive phase current, while DZ2 and DZ4 arise with the negative phase current. This narrow pulse problem has already been investigated for two-level inverters [8], [9]. However, this problem occurs in two-level inverters only under high modulation index (MI) operations where $v^*_{\rm xn}$ goes near the peak or valley of the carrier wave (e.g., near or at overmodulation range). In

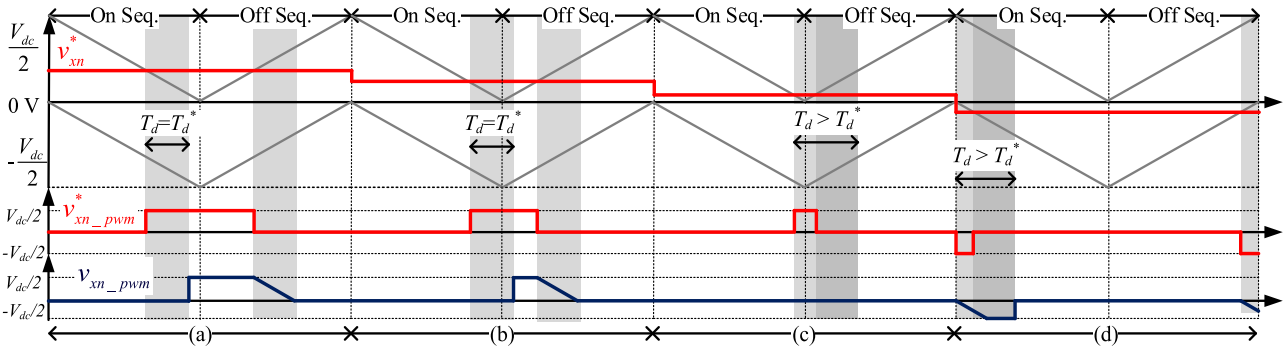

Fig. 2. Dead time effect due to narrow pulses when $i_{\rm xs} > 0$. (a) $V_{\rm DT} \le v^*_{\rm xn} < 0.5V_{\rm dc} - V_{\rm DT}$. (b) $0.5V_{\rm DT} \le v^*_{\rm xn} < V_{\rm DT}$. (c) $0\,{\rm V} \le v^*_{\rm xn} < 0.5V_{\rm DT}$. (d) $-0.5V_{\rm DT} \le v^*_{\rm xn} < 0\,{\rm V}$.

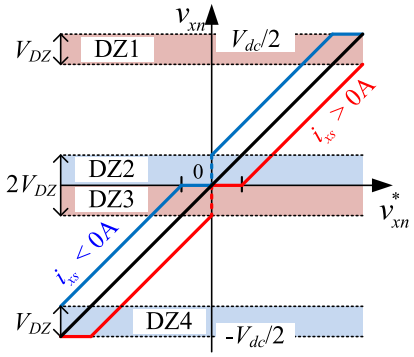

Fig. 3. Relationship between $v^*_{\rm xn}$ and $i_{\rm xs}$ while disregarding parasitic capacitors.

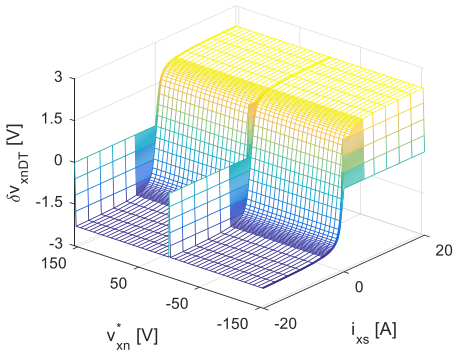

Fig. 4. $\delta v_{\rm xn\_DT}$ according to $i_{\rm xs}$ and $v^*_{\rm xn}$.

three-level inverters, such a problem could occur even under low MI operations since DZ2 and DZ3 are located at zero voltage, which has not been sufficiently covered in the previous literature. Here, MI is defined as the ratio between the fundamental component of the phase voltage, V_{s1}, and a half of dc-link voltage such as

$$\text{MI} = \frac{V_{s1}}{0.5V_{\rm dc}}. \tag{2}$$

Considering all the aforementioned behaviors, the voltage error induced by the dead time, $\delta v_{\rm xn\_DT}$, can be derived from the difference between $v^*_{\rm xn\_pwm}$ and $v_{\rm xn\_pwm}$ within a switching period. $\delta v_{\rm xn\_DT}$ outside the dead zones can be expressed as

$$\delta v_{xn\_DT} = \begin{cases} -\frac{1}{8}\frac{C_{\rm eff}V_{\rm dc}^2}{T_{\rm sw}}\frac{1}{i_{\rm xs}} - \frac{T_d}{T_{\rm sw}}\frac{V_{\rm dc}}{2}, & (i_{\rm xs} < -I_{\rm crit}) \\ \frac{T_d}{T_{\rm sw}}\frac{T_d}{2C_{\rm eff}}i_{\rm xs}, & (-I_{\rm crit} \le i_{\rm xs} < I_{\rm crit}) \\ -\frac{1}{8}\frac{C_{\rm eff}V_{\rm dc}^2}{T_{\rm sw}}\frac{1}{i_{\rm xs}} + \frac{T_d}{T_{\rm sw}}\frac{V_{\rm dc}}{2}, & (I_{\rm crit} \le i_{\rm xs}) \end{cases} \tag{3}$$

where $C_{\rm eff}$ is an effective parasitic capacitance defined as

$$C_{\rm eff} = 2C_{\rm hb} + C_{\rm np}. \tag{4}$$

Note that $\delta v_{\rm xn\_DT}$ in (3) is an averaged value in a switching period. $\delta v_{\rm xn\_DT}$ according to $i_{\rm xs}$ and $v^*_{\rm xn}$ with $f_{\rm sw} = 10$ kHz, $T^*_d = 1.5\,\mu$s, and $V_{\rm dc} = 310$ V is illustrated in Fig. 4. $\delta v_{\rm xn\_DT}$ is not only a function of the current, but also affected by the voltage reference itself.

B. Voltage Drop of Switching Devices

In T-type inverters, the pole voltage error induced by the voltage drop of the switching devices, $\delta v_{\rm xn\_SW}$, depends on the switching state. As shown in Fig. 1, the current should flow through the two switches, Q_{x2} and Q_{x3}, in the "M" state and only through one switch in the current conduction path in the "H" and "L" states. For this reason, $\delta v_{\rm xn\_SW}$ in the "M" state is distinctively large compared to that in other states. Considering the duty ratio, the per-switching-cycle average value of $\delta v_{\rm xn\_SW}$ can be modeled as

$$\delta v_{xn\_SW} = \begin{cases} \left(1 - \frac{|v^*_{\rm xn}|}{0.5V_{\rm dc}}\right)(\delta v_{Q_{x2}}(i_{\rm xs}) + \delta v_{Q_{x3}}(i_{\rm xs})) \\ \quad + \frac{|v^*_{\rm xn}|}{0.5V_{\rm dc}}\delta v_{Q_{x4}}(i_{\rm xs}), \quad (v^*_{\rm xn} \le 0) \\ \left(1 - \frac{|v^*_{\rm xn}|}{0.5V_{\rm dc}}\right)(\delta v_{Q_{x2}}(i_{\rm xs}) + \delta v_{Q_{x3}}(i_{\rm xs})) \\ \quad + \frac{|v^*_{\rm xn}|}{0.5V_{\rm dc}}\delta v_{Q_{x1}}(i_{\rm xs}), \quad (v^*_{\rm xn} > 0) \end{cases} \tag{5}$$

where $\delta v_{\rm Qxi}(i_{\rm xs})$ represents the voltage drop of each switching device $Q_{\rm xi}$. Subscript "i" denotes an arbitrary number from 1 to 4. Each $\delta v_{\rm Qxi}(i_{\rm xs})$ is taken from the datasheets of the switching devices as a function of $i_{\rm xs}$. Fig. 5 shows $\delta v_{\rm xn\_SW}$ according to

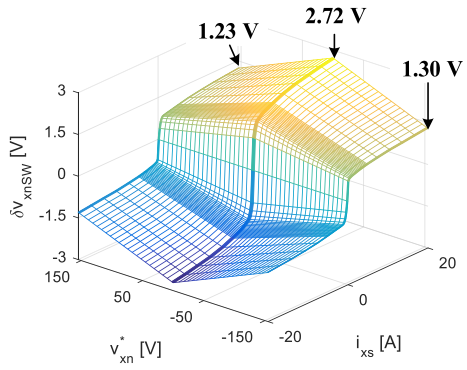

Fig. 5. $\delta v_{\mathrm{xn\_SW}}$ according to i_{xs} and v^*_{xn}.

i_{xs} and v^*_{xn} in the case of a 1200-V 80-A T-type IGBT module (VINCOTECH 10-FZ12NMA080SH01-M260F), which is used in the experiments. In this figure, the voltage error increases as the magnitude of v^*_{xn} decreases since the duty ratio of the bidirectional switch increases as the magnitude of v^*_{xn} decreases to zero.

The total voltage error is simply a sum of $\delta v_{\mathrm{xn\_DT}}$ and $\delta v_{\mathrm{xn\_SW}}$ (i.e., $\delta v_{\mathrm{xn}} = \delta v_{\mathrm{xn\_DT}} + \delta v_{\mathrm{xn\_SW}}$). Compared to the case of two-level inverters, $\delta v_{\mathrm{xn\_SW}}$ takes up a relatively larger portion of δv_{xn} in three-level T-type inverters. That is, $\delta v_{\mathrm{xn\_SW}}/\delta v_{\mathrm{xn}}$ in three-level T-type inverters is larger than that in two-level inverters. This is because dc-link voltage is divided in half by two dc-link capacitors and there are two switches in the current conduction path in the "M" state in three-level T-type inverters. Therefore, the dependence of $\delta v_{\mathrm{xn\_SW}}$ on v^*_{xn} as well as that on i_{xs} should be considered carefully for three-level T-type inverters.

III. Proposed Scheme

As described in Figs. 3 and 4, it is physically impossible to synthesize v_{xn} in the dead zones because of the pulse skipping. For a proper synthesis of the output voltage, pole voltage references, $\mathbf{v^*_{abcn}} \equiv [\, v^*_{\mathrm{an}} \; v^*_{\mathrm{bn}} \; v^*_{\mathrm{cn}} \,]^T$, should be located outside the dead zones. In the carrier-based PWM method, this can be implemented by adding an offset voltage, which is also called zero-sequence voltage, v^*_{sn}, to phase voltage references, $\mathbf{v^*_{abcs}} \equiv [\, v^*_{\mathrm{as}} \; v^*_{\mathrm{bs}} \; v^*_{\mathrm{cs}} \,]^T$. This operation can be presented as follows:

$$v^*_{\mathrm{xn}} = v^*_{\mathrm{xs}} + v^*_{\mathrm{sn}}. \tag{6}$$

In the proposed scheme, the PWM method is switched between two methods: optimal margin PWM (OMPWM) and alternating offset voltage PWM (AOVPWM). This avoids the dead zones according to $v_{\mathrm{max}-}v_{\mathrm{min}}$, as shown in Fig. 6, where v_{max} and v_{min} are defined as

$$\begin{aligned} v_{\mathrm{max}} &= \max(\mathbf{v^*_{abcs}}) \\ v_{\mathrm{min}} &= \min(\mathbf{v^*_{abcs}}). \end{aligned} \tag{7}$$

For a stable transition, a hysteresis band is implemented in the transition function. Working under the assumption that $\mathbf{v^*_{abcn}}$ are properly located off the dead zones, the inverter nonlinearity

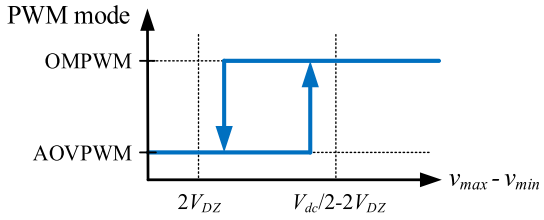

Fig. 6. Transition of PWM mode.

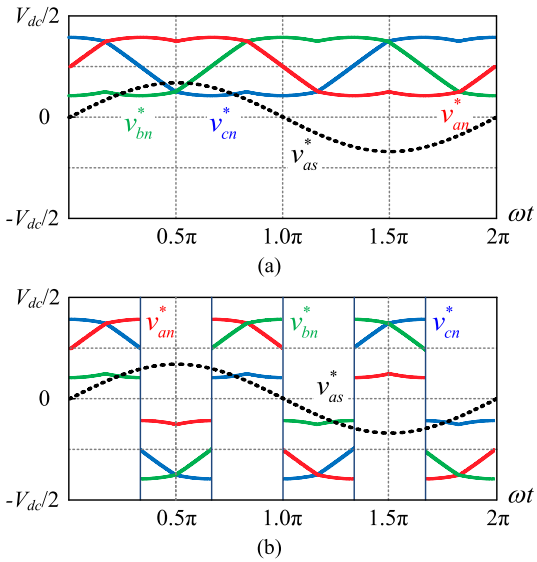

Fig. 7. Waveform of $\mathbf{v^*_{abcn}}$ at low MI. (a) $\mathbf{v^*_{abcn}}$ using (9). (b) $\mathbf{v^*_{abcn}}$ using AOVPWM.

due to the pulse skipping can be compensated using a compensation function from i_{xs} and v^*_{xn}. When $v_{\mathrm{max}-}v_{\mathrm{min}}$ gets closer to the physical voltage limit, V_{dc}, $\mathbf{v^*_{abcn}}$ cannot be located off the dead zones by adjusting offset voltage. That is the physical limit of the PWM. In the proposed scheme, to avoid undesired inverter output saturation, MI is limited under 1.097 for 5% voltage margin in the linear modulation range of SVPWM [18]. The operation principles of two PWM methods are described as follows.

A. Technique to Avoid Dead Zones Using AOVPWM

When $\mathbf{v^*_{abcs}}$ are small in low MI operations, shifting all $\mathbf{v^*_{abcs}}$ to the middle of a carrier is the only way to avoid the dead zones. By doing so, the output voltage can be generated by only two switching states; either "H" and "M" states or "M" and "L" states. By excluding one switching state, three-level inverters can operate as if they are two-level inverters in low MI operations. One of the most popular offset voltage settings for two-level VSIs can be expressed as (8), which is known to be equivalent to three-phase symmetry SVPWM [19]:

$$v^*_{\mathrm{sn}} = -\frac{v_{\mathrm{max}} + v_{\mathrm{min}}}{2}. \tag{8}$$

This method is called as symmetrical continuous PWM (SCPWM) hereafter. Since $\mathbf{v^*_{abcn}}$ generated by (8) with low MI might be placed in the dead zones for PWM of three-level

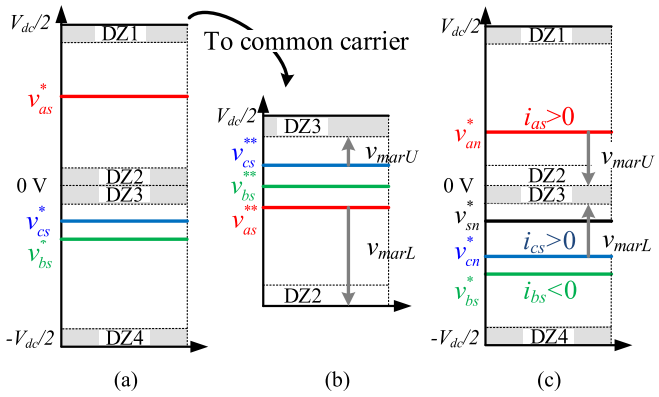

Fig. 8. Step-by-step procedure of $\mathbf{v}^*_{\mathbf{abcn}}$ calculation for OMPWM. (a) Step 1, (b) step 2, and (c) step 3.

inverters, $v^*_{\rm sn}$ can be modified as (9), (10) to let $\mathbf{v}^*_{\mathbf{abcn}}$ be all positive or all negative where the modified voltages may be out of the dead zones

$$v^*_{\rm sn} = -\frac{v_{\rm max}+v_{\rm min}}{2} + \frac{v_{\rm dc\_H}}{2} \tag{9}$$

$$v^*_{\rm sn} = -\frac{v_{\rm max}+v_{\rm min}}{2} - \frac{v_{\rm dc\_L}}{2}. \tag{10}$$

Fig. 7(a) shows $\mathbf{v}^*_{\mathbf{abcn}}$ waveforms using (9). Applying either (9) or (10), the redundant switching vectors, (0 0 0) and (1 1 1) vectors, are split equally and placed at the beginning and end in an on/off sequence. While $v^*_{\rm sn}$ in [20] only achieves the optimal switching sequence, $v^*_{\rm sn}$ in (9) and (10) not only guarantees the optimal switching sequence but also keeps $\mathbf{v}^*_{\mathbf{abcn}}$ out of the dead zone so as to minimize sideband harmonics at the carrier frequency and avoid the narrow pulse problem.

However, applying either (9) or (10) provokes even-order harmonics in the output voltage. Even-order harmonics come up due to the asymmetry of $\delta v_{\rm xn\_SW}$ shown in Fig. 5. Since $\delta v_{\rm xn\_SW}$ increases as $v^*_{\rm xn}$ is closer to zero, $v^*_{\rm xn}$ in Fig. 7(a) suffers larger voltage error at the valley than at the peak, which breaks the half-wave symmetry of the voltage error (i.e., $\delta v_{\rm xn}(\theta) \neq -\delta v_{\rm xn}(\theta - 180^\circ)$). To satisfy $\delta v_{\rm xn}(\theta) = -\delta v_{\rm xn}(\theta - 180^\circ)$, $v^*_{\rm sn}$ can be changed between (9) and (10) alternately with 120° period as depicted in Fig. 7(b). Using this method, namely AOVPWM, even-order harmonics in the output voltage can be successfully diminished. Considering the computation burden, compared with SCPWM implemented by (8), AOVPWM requires two more operations: "+"/"−" operation to move $\mathbf{v}^*_{\mathbf{abcn}}$ to the upper/lower carrier region and one "if" statement to decide when the offset voltage should vary.

B. Technique to Avoid Dead Zones Using OMPWM

Over a certain MI, $\mathbf{v}^*_{\mathbf{abcn}}$ are placed in the dead zones even though AOVPWM is applied. In this case, one or two of $\mathbf{v}^*_{\mathbf{abcn}}$ have to be located in the upper carrier region and the other has to be located in the lower carrier region, which is called OMPWM.

As a basic principle, OMPWM optimizes the voltage margin between $\mathbf{v}^*_{\mathbf{abcn}}$ and the dead zones. The margin could be exploited simultaneously for balancing NP voltages of three-level inverters. Fig. 8 shows the setting $\mathbf{v}^*_{\mathbf{abcn}}$ in OMPWM. If $\mathbf{v}^*_{\mathbf{abcs}}$

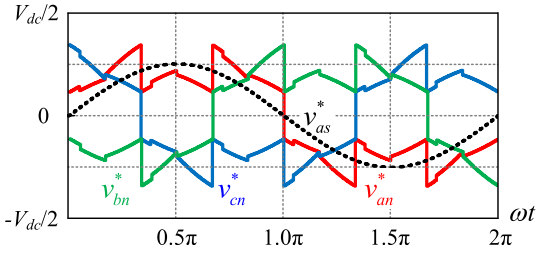

Fig. 9. Waveform of $\mathbf{v}^*_{\mathbf{abcn}}$ using OMPWM under MI = 0.5 and PF = 0.5.

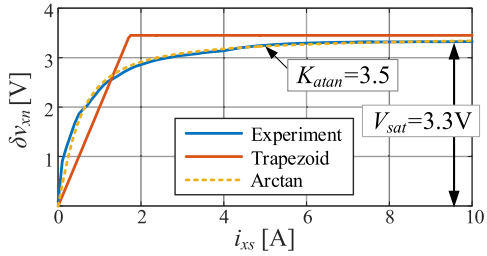

Fig. 10. Experimentally measured $\delta v_{\rm xn}$ according to $i_{\rm xs}$ and compensation functions.

are given as in Fig. 8(a), negative phase voltages are shifted to the upper carrier region by applying (11), as shown in Fig. 8(b):

$$v^{**}_{\rm xs} = v^*_{\rm xs} + 0.5V_{\rm dc}. \tag{11}$$

In Fig. 8(b), $v_{\rm marU}$ and $v_{\rm marL}$ indicate upper and lower voltage margins, respectively. The dead zones are affected by the current polarity. For example, if $i_{\rm as} > 0$ and $i_{\rm cs} > 0$ in Fig. 8(b), DZ3 is effective but DZ2 is not. In this case, $v_{\rm marU}$ and $v_{\rm marL}$ can be computed as

$$\begin{aligned} v_{\rm marU} &= 0.5V_{\rm dc} - V_{\rm DZ} - v^{**}_{\rm cs} \\ v_{\rm marL} &= 0\,{\rm V} - v^{**}_{\rm as}. \end{aligned} \tag{12}$$

In order to avoid the pulse skipping due to the dead zones and to secure maximum voltage margins, it is appropriate to set $|v_{\rm marU}| = |v_{\rm marL}|$. For maximum voltage margins, the offset voltage can be set as

$$v^*_{\rm sn} = \frac{v_{\rm marU}+v_{\rm marL}}{2}. \tag{13}$$

Fig. 8(c) shows $\mathbf{v}^*_{\mathbf{abcn}}$ after applying (13). The magnitudes of $v_{\rm marU}$ and $v_{\rm marL}$ become the same in the figure. The computation burden of OMPWM is slightly larger than that of optimal switching sequence [20] due to the voltage margin calculation considering the current polarity in (12). The proposed PWM methods would not induce excessive computation burden.

Fig. 9 shows pole voltage waveforms using OMPWM under MI = 0.5 and PF = 0.5 which matches to the experimental condition of Fig. 17(b). All of $\mathbf{v}^*_{\mathbf{abcn}}$ can be out of the dead zones over an electrical rotating period when OMPWM is applied as shown in Fig. 9. When $V_{\rm DZ}$ is much smaller than $V_{\rm dc}$, $v^*_{\rm sn}$ defined as (13) is equivalent to that with the optimal switching sequence [20].

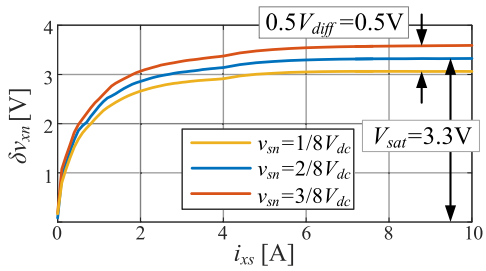

Fig. 11. Experimentally measured $\delta v_{\rm xn}$ according to $i_{\rm xs}$ with variation of $v_{\rm sn}$.

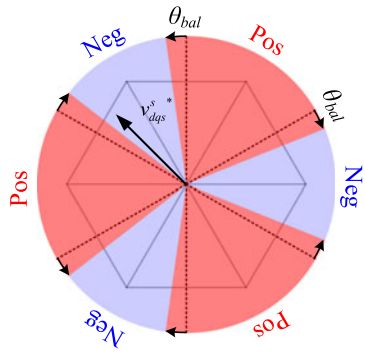

Fig. 12. Principle of NP balancing for AOVPWM.

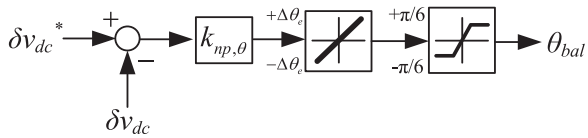

Fig. 13. Block diagram of NP balancing controller for AOVPWM.

C. Compensation of Inverter Nonlinearity due to Pulse Shaping and Voltage Drop of Switching Devices

Fig. 10 shows experimentally measured $\delta v_{\rm xn}$ according to $i_{\rm xs}$, with $v_{\rm sn}$ set as (9) to locate $\mathbf{v}^*_{\mathbf{abcn}}$ off the dead zones; hence, the pulse skipping could be avoided. However, due to the pulse shaping and voltage drop of the switching devices, there are output voltage errors $\delta v_{\rm xn}$. The error can be compensated by a compensation function $v_{\rm xn\_Comp}$. Several functions, namely a step function, a trapezoidal voltage, and an arctangent function, could be considered for the compensation function. In this paper, the arctangent function is utilized as the compensation function since it exhibits great agreement with the actual $\delta v_{\rm xn}$, as shown in Fig. 10.

$v_{\rm xn\_Comp1}$ defined as (14) is suitable for the conventional NPC topology, because the difference of $\delta v_{\rm xn\_SW}$ between switching states would be negligible.

$$v_{\rm xn\_Comp1} = V_{\rm sat} \cdot \frac{2}{\pi} \arctan\left(K_{\rm atan} \cdot i_{\rm xs}\right). \tag{14}$$

In a T-type inverter, $\delta v_{\rm xn\_SW}$ is not only a function of the current, but also affected by pole voltage references. To consider the asymmetric behavior of $\delta v_{\rm xn\_SW}$, the compensation function is modified as

$$v_{\rm xn\_Comp2} = \left(V_{\rm sat} + V_{\rm diff}\left(\frac{|v^*_{\rm xn}|}{0.5V_{\rm dc}} - 0.5\right)\right) \cdot \frac{2}{\pi} \arctan\left(K_{\rm atan} \cdot i_{\rm xs}\right) \tag{15}$$

where $V_{\rm diff}$ refers to the difference between $\delta v_{\rm xn}$ in the "M" state and that in the "H" or "L" state. To get $V_{\rm diff}$ experimentally, $\delta v_{\rm xn}$ should be extracted with various $v_{\rm sn}$ outside the dead zones. Fig. 11 shows experimentally measured $\delta v_{\rm xn}$ according to $i_{\rm xs}$ with different values of $v_{\rm sn}$. The resistance of the switching devices is excluded when $\delta v_{\rm xn}$ is extracted, because it cannot be distinguished from that of load connected to the inverter [2].

IV. Voltage Balancing Control of the Proposed Scheme

For three-level inverters, the NP current causes a voltage difference between capacitors in the dc link. The NP balancing algorithms have been widely discussed in the previous literature [21]–[25], but none have dealt with the compensation of inverter nonlinearity effects since the offset voltage selection has been optimized only for the NP balancing objective. In other words, $v^*_{\rm xn}$ determined by conventional NP balancing algorithms could be located in the dead zones where the pulse skipping occurs. Therefore, the inverter nonlinearity effects should be taken into consideration in the NP balancing control to minimize the output voltage distortion.

Conventional NP balancing methods would not be compatible with the proposed PWM methods, because both algorithms use the offset voltage for different purposes. This problem is not crucial for three-level converters with active front ends like a boost PWM converter where either the offset voltage of the PWM converter or that of the PWM inverter could be used to balance the NP potential. Yet considering passive front ends, such as the diode rectifier, voltage balancing control methods should be incorporated into the proposed PWM methods of the T-type inverter to keep the voltage balance at NP.

Two NP balancing controllers optimized for each PWM method are proposed in this paper. They are easy to implement and do not degrade the performances of the proposed PWM algorithms to prevent the pulse skipping. It is confirmed through experimental comparisons that the proposed NP controllers have better THD performance over other NP balancing algorithms.

A. Analysis of NP Current According to Offset Voltage

The NP current averaged over a switching period, $i_{\rm np}$ shown in Fig. 1, can be analytically calculated [21], [22]. Measured dc-link voltages, $v_{\rm dc\_H}$ and $v_{\rm dc\_L}$, are used to synthesize proper $v^*_{\rm xn}$ even when the difference between high- and low-side dc-link voltages, $\delta v_{\rm dc} \equiv v_{\rm dc\_H} - v_{\rm dc\_L}$, exists. $i_{\rm np}$ can be calculated in a three-phase system as

$$i_{\rm np} = D_{\rm an} i_a + D_{\rm bn} i_b + D_{\rm cn} i_c. \tag{16}$$

$D_{\rm xn}$ in (16) denotes the duty ratio of the NP at "x" phase as

$$D_{\rm xn} = \left\{ \begin{matrix} 1 + v_{\rm xn}/v_{\rm dc\_L}, & (v_{\rm xn} < 0) \\ 1 - v_{\rm xn}/v_{\rm dc\_H}, & (v_{\rm xn} \geq 0) \end{matrix} \right\}. \tag{17}$$

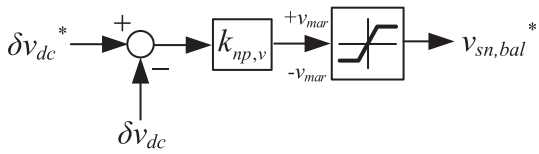

Fig. 14. Block diagram of NP balancing controller for OMPWM.

Since $i_{\rm np}$ varies according to $v_{\rm sn}$, adding a proper offset voltage is key to minimize $\delta v_{\rm dc}$. The relationship between $i_{\rm np}$ and $v_{\rm sn}$ can be derived as

$$i_{\rm np}=\begin{cases}-\dfrac{P_{\rm out}}{v_{\rm dc\_H}},\ (v_{\rm sn}\geq -v_{\rm min})\\ -\dfrac{P_{\rm out}}{v_{\rm dc\_H}}+\left(\dfrac{1}{v_{\rm dc\_H}}+\dfrac{1}{v_{\rm dc\_L}}\right)(v_{\rm min}+v_{\rm sn})i_{\rm min},\\ \quad(-v_{\rm mid}\leq v_{\rm sn}<-v_{\rm min})\\ \dfrac{P_{\rm out}}{v_{\rm dc\_L}}-\left(\dfrac{1}{v_{\rm dc\_H}}+\dfrac{1}{v_{\rm dc\_L}}\right)(v_{\rm max}+v_{\rm sn})i_{\rm max},\\ \quad(-v_{\rm max}\leq v_{\rm sn}<-v_{\rm mid})\\ \dfrac{P_{\rm out}}{v_{\rm dc\_L}},\ (v_{\rm sn}<-v_{\rm max})\end{cases}\tag{18}$$

where $P_{\rm out}$ is the output power defined as

$$P_{\rm out}=v_{\rm max}i_{\rm max}+v_{\rm mid}i_{\rm mid}+v_{\rm min}i_{\rm min}\tag{19}$$

$v_{\rm max}$, $v_{\rm mid}$, and $v_{\rm min}$ are defined as the maximum, medium, and minimum pole voltages, respectively. $i_{\rm max}$, $i_{\rm mid}$, and $i_{\rm min}$ are the currents of corresponding phases to $v_{\rm max}$, $v_{\rm mid}$, and $v_{\rm min}$, respectively. To simplify the analysis, $P_{\rm out}$ is assumed to be constant over an electrical rotating period.

B. NP Controller for AOVPWM

All pole voltages are shifted to one of the carrier regions for AOVPWM. When the positive offset voltage expressed in (9) is applied, all pole voltages become positive (i.e., $v_{\rm sn}\geq -v_{\rm min}$). When the negative offset voltage expressed in (10) is applied, all pole voltages become negative (i.e., $v_{\rm sn}<-v_{\rm max}$). In either condition, $i_{\rm np}$ cannot be changed by shifting $v_{\rm sn}$. However, (18) shows that the polarity of $i_{\rm np}$ changes with the offset voltage settings in (9) and (10). Additionally, the NP balancing can be achieved by adjusting the ratio between durations of the two offset voltages in (9) and (10).

Fig. 12 shows the principle of the NP balancing for AOVPWM. The NP current averaged over an electrical rotating period $\bar{i}_{\rm np}$ can be adjusted by the balancing angle $\theta_{\rm bal}$. $\bar{i}_{\rm np}$ can be expressed as a linear function of $\theta_{\rm bal}$ as

$$\begin{aligned}\bar{i}_{\rm np}&=\frac{1}{2\pi}\int_0^{2\pi}i_{\rm np}(\theta)d\theta\\&=\frac{P_{\rm out}}{2}\left(\frac{1}{v_{\rm dc\_L}}-\frac{1}{v_{\rm dc\_H}}\right)-\frac{3P_{\rm out}}{\pi}\left(\frac{1}{v_{\rm dc\_L}}+\frac{1}{v_{\rm dc\_H}}\right)\theta_{\rm bal}.\end{aligned}\tag{20}$$

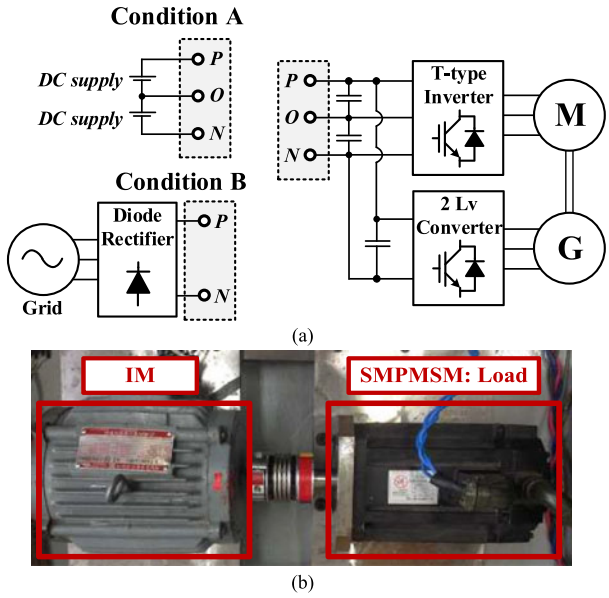

Fig. 15. Experimental setup. (a) Hardware configuration. (b) Motor-generator set.

TABLE II
PARAMETERS OF INDUCTION MOTOR

Parameter	Value
Rated Power	3.7 kW
Pole number	4
R_s/R_r	0.22/0.3 Ω
$L_{\rm m}$	63.62 mH
$L_{\rm ls}/L_{\rm lr}$	2.44/2.44 mH
Rated torque	11.5 N·m

The NP controller for AOVPWM, or the $\theta_{\rm bal}$ controller, consists of proportional gain, rate limiter, and output limiter, as shown in Fig. 13. The rate limiter is chosen to suppress the rapid variation of offset voltage in low rotating speeds and the reference $\delta v_{\rm dc}^*$ is normally set to zero. If the proportional gain is set as (21) where $\omega_{\rm vc}$ is the bandwidth of NP control loop, the transfer function from $\delta v_{\rm dc}^*$ to $\delta v_{\rm dc}$ can be deduced as (22), assuming that $\delta v_{\rm dc}$ is small.

$$k_{np,\theta}=-\frac{\pi}{12}C_{\rm dc}V_{\rm dc}\frac{\omega_{\rm vc}}{P_{\rm out}}\tag{21}$$

$$\delta v_{\rm dc}=\frac{\omega_{\rm vc}}{s+\omega_{\rm vc}}\delta v_{\rm dc}{}^*.\tag{22}$$

Since the period of $v_{\rm sn}^*$ in AOVPWM gets longer at low speeds, third-harmonic ripple of $\delta v_{\rm dc}$ increases. In order to reduce the ripple of $\delta v_{\rm dc}$, the period of $v_{\rm sn}^*$ which is originally set as 120° as shown in Fig. 12 can be divided by a divider $n_{\rm div}$, a natural number, i.e., $120^\circ/n_{\rm div}$. The larger the $n_{\rm div}$ is, the smaller the ripple of $\delta v_{\rm dc}$ becomes. Since the half-wave symmetry still holds even though the period is divided by $n_{\rm div}$, the even-order harmonic currents are not induced.

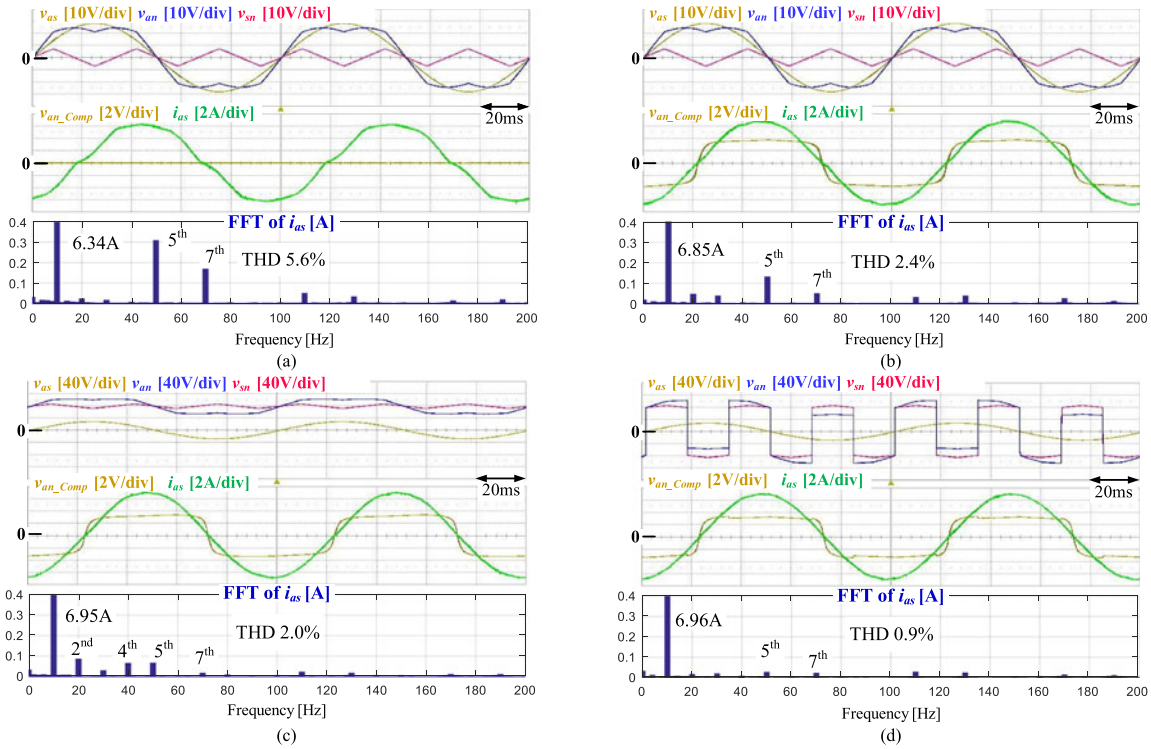

Fig. 16. Experiment 1: Waveforms and harmonic spectra of $i_{\rm as}$ under no load at 10-Hz frequency. (a) SCPWM without compensation. (b) SCPWM with the proposed compensation based on (15). (c) $v_{\rm sn}^*$ in (9) with the proposed compensation based on (15). (d) AOVPWM with the proposed compensation based on (15).

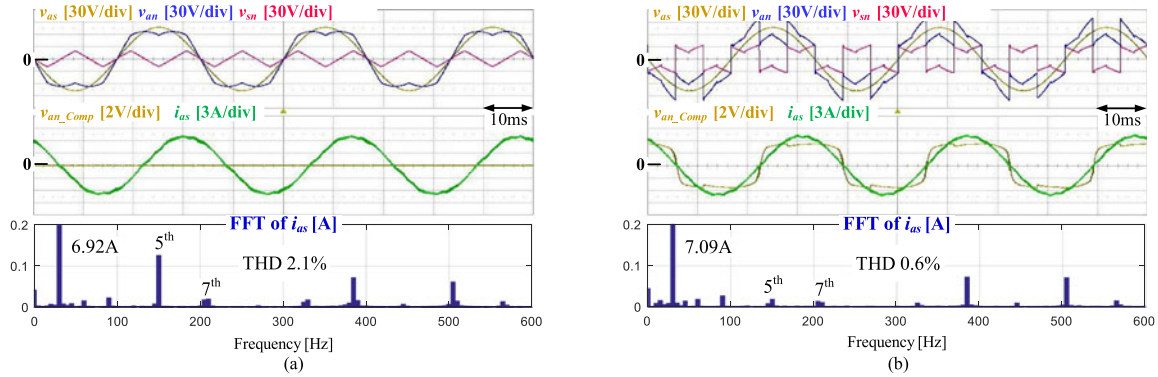

Fig. 17. Experiment 2: Waveforms and harmonic spectra of $i_{\rm as}$ under 25% load at 30-Hz frequency. (a) SCPWM without compensation. (b) OMPWM with the proposed compensation based on (15).

C. NP Controller for AOVPWM

There can be only one or two positive pole voltages in OMPWM since $v_{\rm sn}$ is limited to $-v_{\rm max} \le v_{\rm sn} < -v_{\rm min}$. In this $v_{\rm sn}$ range, $i_{\rm np}$ can be changed by adjusting $v_{\rm sn}$. Fig. 14 shows the block diagram of the NP controller for OMPWM. Balancing offset voltage, $v_{\rm sn,bal}^*$, is determined by a proportional controller with limiter and $v_{\rm sn,bal}^*$ is added to offset voltage defined by (13). The proposed NP controller has a similar structure with the dc common-mode voltage injection algorithm [23]. However, the limiter is added to keep $\mathbf{v}_{\mathbf{abcn}}^*$ out of the dead zones. The proportional gain, $k_{\rm np,v}$, can be set by considering the performance of the NP balancing and current harmonics.

Proposed NP controllers can bet utilized for motoring as well as for regenerating operations by changing the signs of output variables $\theta_{\rm bal}$ and $v_{\rm sn,bal}$.

V. Experimental Results

The experimental setup for the verification of the proposed scheme is depicted in Fig. 15. An induction machine is driven by a three-level T-type inverter and the parameters of the induction machine are shown in Table II. The machine is simply driven by *Vlf* control. A two-level converter controls the SMPMSM load machine to emulate loading conditions to the induction machine. Two dc supplies or a three-phase diode rectifier supplies the dc-link depending on experimental conditions. All control algorithms are implemented digitally in a DSP board. Each value of

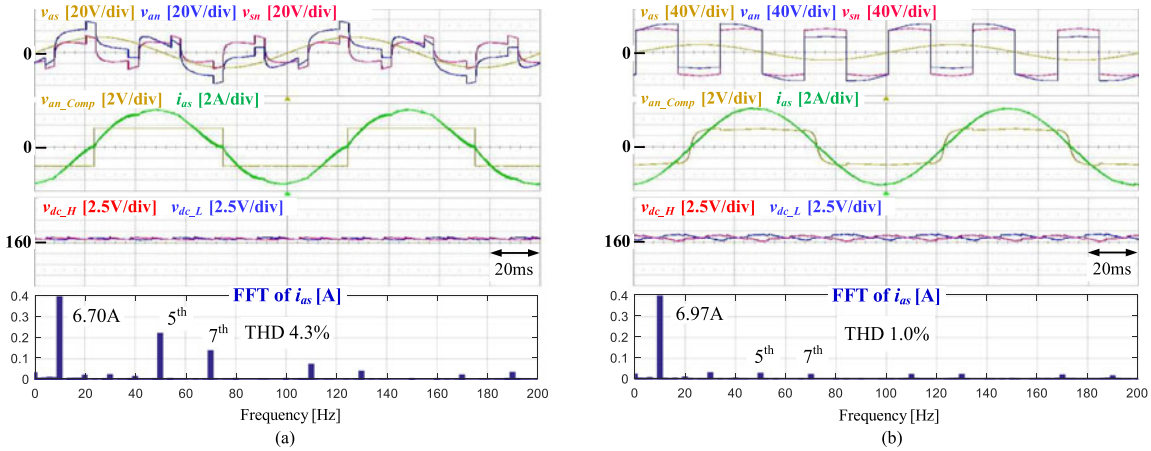

Fig. 18. Experiment 3: Waveforms and harmonic spectra of $i_{\rm as}$ with NP control under no load at 10-Hz operating frequency. (a) Conventional method [16] with step function compensation. (c) AOVPWM with the proposed compensation based on (15).

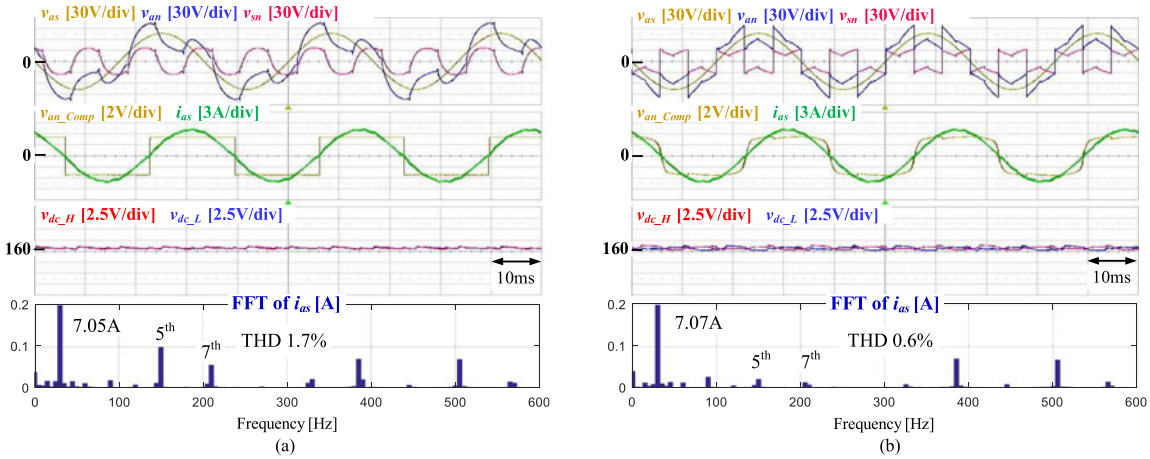

Fig. 19. Experiment 4: Waveforms and harmonic spectra of $i_{\rm as}$ with NP control under 25% load at 30-Hz operating frequency. (a) Conventional method [16] with step function compensation. (b) OMPWM with the proposed compensation based on (15).

dc-link capacitances, switching frequency, and preset dead time are 4000 μF, 10 kHz, and 1.5 μs, respectively. Furthermore, the sampling frequency is set to 20 kHz.

A. *Performance of Inverter Nonlinearity Compensation*

To show the performance of the proposed PWM methods without the NP balancing control, each dc-link voltage was fixed to 155 V by two dc supplies, as shown in Fig. 15(a) with condition A. Fig. 16 shows waveforms and harmonic spectra of $i_{\rm as}$ according to the PWM methods under no load at 10-Hz operating frequency. In Fig. 16(a), where no compensation is applied, $i_{\rm as}$ is severely distorted due to the inverter nonlinearity. Even after applying the compensation method shown in Fig. 16(b), the fifth and seventh harmonics in $i_{\rm as}$ are not eliminated since $\mathbf{v}^*_{\mathbf{abcn}}$ can cross the dead zones at zero voltage and the voltage disturbance induced by the pulse skipping cannot be compensated. Applying $v^*_{\rm sn}$ in (9) to move $\mathbf{v}^*_{\mathbf{abcn}}$ to the upper carrier region, the fifth and seventh harmonics of the current are conspicuously reduced, as shown in Fig. 16(c). However, additional even-order harmonics arise in $i_{\rm as}$ due to the voltage disturbance induced by the aforementioned asymmetric $\delta v_{\rm xn\_SW}$. Due to alternatively shifted pole voltages in AOVPWM, even-order harmonics of the current are eliminated, as shown in Fig. 16(d). Fig. 17 shows waveforms and harmonic spectra of $i_{\rm as}$ according to the PWM methods under 25% load at 30-Hz operating frequency under condition A in Fig. 15(a). In Fig. 17(a), where SCPWM is applied without any compensation of the inverter nonlinearity, the fifth and seventh harmonics arise in $i_{\rm as}$ because of the inverter nonlinearity. The fifth- and seventh-harmonic components of $i_{\rm as}$ are conspicuously reduced when OMPWM is applied with the compensation method in (15). Similar to AOVPWM under a low MI operation, $\mathbf{v}^*_{\mathbf{abcn}}$ can avoid the dead zones under a high MI operation applying OMPWM.

B. *Effectiveness of NP Balancing Control*

The dc-link capacitors are connected to the output of a three-phase rectifier converting line-to-line 220–$V_{\rm rms}$ 60-Hz grid voltage to 311-V dc voltage, as shown in Fig. 15(a) with condition B. As shown in the figure, the NP between the capacitors is floating and requires the NP balancing control. The proposed NP controllers control the NP current. NP controller gains, $\omega_{\rm vc}$ and $k_{\rm np,v}$, are set to 2π rad/s and -0.5, respectively. The pro-

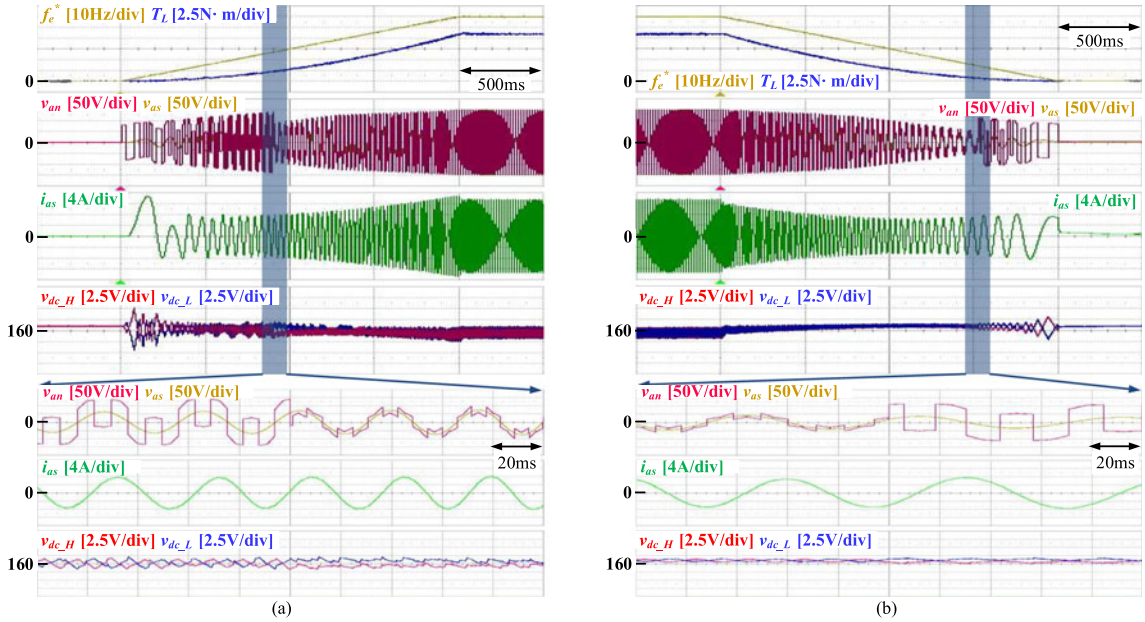

Fig. 20. Experiment 5: Waveforms with the proposed PWM methods under *V/f* operation in (a) accelerating and (b) decelerating conditions.

posed method is compared with the conventional method [16] which considers both the narrow pulse problem and neutral voltage balancing as summarized in Table I. Since Guan and Wang [16] does not consider parasitic capacitors ($C_{\text{eff}} \asymp 0$), a step function which is a particular case of (14) with $K_{\text{atan}} = \infty$ is adopted as the compensation function for the conventional method [16].

Fig. 18 shows the effectiveness of AOVPWM with the NP balancing control under no load at 10-Hz operating frequency. In Fig. 18(a), where conventional method [16] is applied with the step function compensation, the dc-link voltages are well balanced. However, the fifth and seventh harmonics in i_{as} still remain because the compensation function does not reflect the effects of parasitic capacitors and asymmetric $\delta v_{\text{xn\_SW}}$. Applying AOVPWM and the compensation method, the fifth and seventh harmonics of i_{as} are conspicuously reduced without losing the voltage balancing control performance shown in Fig. 18(b).

Fig. 19 shows the effectiveness of OMPWM with the NP balancing control under 25% load torque at 30-Hz operating frequency. Comparing Fig. 19(a) and (b), it can be seen that the fifth- and seventh-harmonic components of i_{as} are remarkably reduced using the proposed scheme while maintaining the voltage balancing control performance.

Fig. 20 shows the transition between the two proposed PWM methods. The load torque is set to be proportional to the square of the rotational speed to emulate fan or pump load. During acceleration, the PWM method is switched from AOVPWM to OMPWM when $v_{\max} - v_{\min} = 0.5\,\text{V}_{\text{dc}} - 4V_{\text{DZ}}$, as shown in Fig. 20(a). Fig. 20(b) shows that the PWM method is switched from OMPWM to AOVPWM when $v_{\max} - v_{\min} = 6V_{\text{DZ}}$. Applying the hysteresis band for stable transition between two PWM methods, the transition points are set differently during acceleration and deceleration. It can be confirmed from the time-magnified plot that the current is kept sinusoidal without distortion even at the transition point. Furthermore, the dc-link voltages are well balanced regardless of these transient operations. Large fluctuation of δv_{dc} is observed at the beginning of acceleration in Fig. 20(a) and at the end of deceleration in Fig. 20(b). This comes from the nature that third-harmonic ripple of δv_{dc} increases using AOVPWM as aforementioned. In the experiment, $n_{\text{div}} = 2$ is used below $f_e^* = 5$ Hz and $n_{\text{div}} = 1$ otherwise to limit δv_{dc} under 10 V at low speeds.

VI. Conclusion

In this paper, the inverter nonlinearity effects in three-level T-type inverters have been analyzed. Though the inverter nonlinearity in two-level inverters has been presented and discussed for the past 40 years, the phenomena are different in three-level T-type inverters. It has been discussed that the inverter nonlinearity effects in three-level T-type inverters mainly come from the pulse shaping and skipping due to the narrow pulses from the dead time. Furthermore, the voltage distortion due to the asymmetric voltage drop of the switching devices has been studied. The inverter nonlinearity due to the pulse skipping has been avoided by the proposed PWM methods called OMPWM and AOVPWM. The PWM method is switched between the two proposed methods according to MI. The distortion due to the pulse shaping and switching devices has been solved by a compensation function based on the arctangent function. Moreover, NP controllers cooperating with the proposed PWM methods to keep the voltage balancing of dc link have been devised. The effectiveness of the proposed scheme has been verified by extensive experimental results. Using the proposed AOVPWM and OMPWM, even-order harmonics as well as the fifth and seventh harmonics of the current have been remarkably reduced. The NP voltage balancing performances in the transient and steady states have been also verified. The proposed scheme could be extended not only to NPC topology, but also to multilevel and multileg topologies.

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