An Optimized Hybrid SVPWM Strategy Based on Multiple Division of Active Vector Time (MDAVT)

Jayanta Biswas, *Member, IEEE*, Meenu D Nair, *Student Member, IEEE*, Vivek Gopinath, *Student Member, IEEE*, and Mukti Barai, *Member, IEEE*

***Abstract*—This paper presents a new advanced bus-clamped space vector pulsewidth modulation (SVPWM) technique to reduce line current harmonic distortion as well as switching loss. The proposed sequence introduces multiple division of active vector time (MDAVT) in a subcycle. An analysis of optimal subdivision of active vector dwell time is presented. Existing bus-clamping pulsewidth modulation techniques use double-switching clamping sequences, which use only one zero state and apply an active vector twice in a subcycle. The proposed MDAVT-based SVPWM technique presents a hybrid SVPWM technique. The additional switching is added when the fundamental voltage crosses zero. The switching patterns for the other two phases are not changed. The harmonic performance and switching loss characteristics of the proposed hybrid SVPWM techniques over the existing SVPWM is verified with experimental results on a 415-V, 2.2-kW induction motor drive.**

***Index Terms*—Harmonic distortion, induction motor drives pulsewidth modulation (PWM), space vector, switching loss.**

I. Introduction

SEVERAL pulsewidth modulation (PWM) techniques have been reported for the voltage source inverter (VSI)-fed motor drives. There are two real-time PWM methods to generate pulses for VSIs. One is sine PWM (SPWM) and another is space vector PWM (SVPWM). The line current distortion and switching loss are considered as the principal performance indices for evaluating various PWM techniques. An equivalent quantity, which is independent of the motor parameters, is the weighted total harmonic distortion (THD) of the line voltage waveform[1]. To minimize line current THD, root mean square (rms) current ripple in every subcycle should be reduced. For the conventional PWM, the THD of the output current is inversely proportional to the switching frequency [13]–[21]. In order to reduce harmonic currents, the switching frequency can be increased. However, higher switching frequency leads to higher switching loss, and in the case of high-power converters, it may not even be possible due to device limitations. The switching loss for a subcycle depends on the number of switching per subcycle, the phase current and the dc bus voltage. SVPWM and third harmonic injection PWM have higher dc bus utilization compared toSPWM.

The SVPWM technique has eight switching states, six active vector, and two zero vector states. The flexibility in the placement of zero space vector results in either continuous or discontinuous SVPWM (bus-clamped SVPWM). The switching losses , waveform quality, and voltage linearity characteristics are different in each discontinuous method. The discontinuous techniques can be effectively used for reducing switching loss and harmonics. With the lower switching frequency, the bus-clamped PWM strategy provides reduction in switching losses when compared to the continuous SVPWM (CSVPWM). The combined objective of maximum dc bus utilization, minimizing THD, and switching loss is achieved by a different advanced bus-clamped SVPWM technique [2]–[16]. The choice of the clamped leg and the duration of clamping depend on the orientation of the desired reference voltage. A detailed review and analysis of different advanced SVPWM techniques are presented in [22]–[25].

This paper introduces a novel hybrid advanced SVPWM technique that uses the best clamping sequences to achieve minimum error voltage. To minimize the current ripple as well as the switching loss in every subcycle, an optimized subdivision of active vector dwell time is analyzed. Section II of this paper presents the proposed hybrid SVPWM techniques to reduce harmonic distortion and switching loss. Section III analyzes the optimal subdivision of active vector dwell time. Results and performance evaluation of proposed hybrid SVPWM techniques are presented in Section IV. Section V concludes this paper.

II. Proposed Hybrid SVPWM Technique for Reduced THD and Switching Loss

The dynamic model of the three-phase induction motor is derived by transforming the three phase quantities into two phase quantities. The two phase quantities are placed on two axes, which are called the direct, or d-axis and the quadrature or q-axis. The two axes are 90^0 apart from each other. The d–q transformation can be thought of in geometric terms as the projection of the three separate sinusoidal phase quantities onto two axes rotating with the same angular velocity as the sinusoidal phase quantities. The stator flux ($\vec{\psi}$) of the induction motor can be defined by the time integral value of the applied supply voltage ($\vec{V_s}$) . Therefore, the stator flux equation in stationary reference frame can be expressed as follows, while neglecting the stator

Manuscript received November 4, 2015; revised February 9, 2016 and May 29, 2016; accepted July 21, 2016. Date of publication August 2, 2016; date of current version February 11, 2017. Recommended for publication by Associate Editor A. M. Trzynadlowski.

J. Biswas is currently working as freelancer researcher working at home, Kozhikode, Kerala (e-mail: jayantab2002@gmail.com).

M. D Nair, V. Gopinath, and M. Barai are with the Department of Electrical Engineering National Institute of Technology Calicut, Kozhikode 673601, India (e-mail: meenudnair@gmail.com; gvivek1988@gmail.com; muktib@nitc.ac.in).

Digital Object Identifier 10.1109/TPEL.2016.2597247

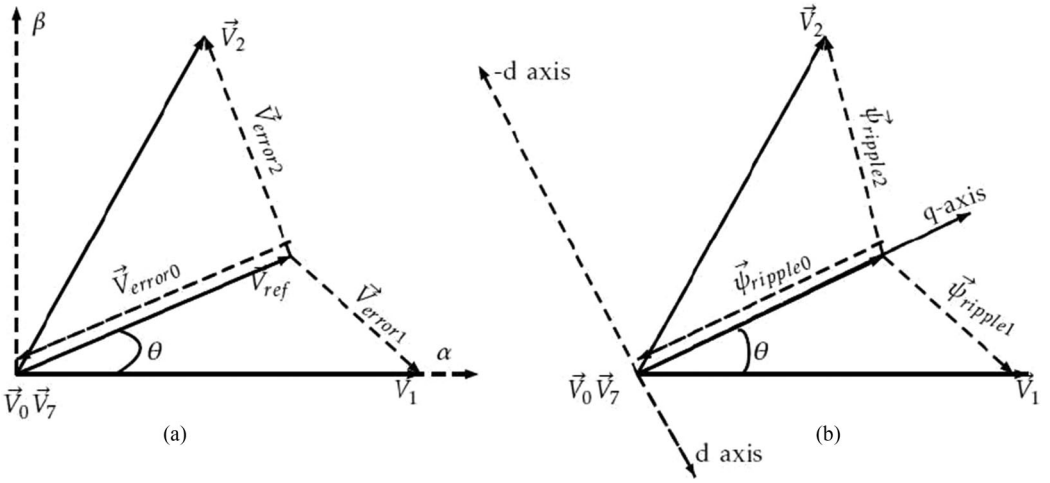

Fig. 1. Representation of (a) error voltages (b) flux ripple corresponding to V_{ref} in sector I.

resistance drop:

$$\vec{\psi} = \int \vec{V}_s dt. \tag{1}$$

In the space vector PWM approach, the applied voltage equals the reference voltage only in an average sense over the given sampling interval, and not in an instantaneous fashion. The difference between applied voltage ($\vec{V}$) and reference voltage ($\vec{V}_{\text{ref}}$) is defined as the error voltage ($\vec{V}_{\text{error}}$). The instantaneous error voltages in the $\alpha - \beta$ plane can be expressed by the following expressions when $\vec{V}_{\text{ref}}$ is at sector I.

$$\begin{aligned} \vec{V}_{\text{error1}} &= \vec{V}_1 - \vec{V}_{\text{ref}} \\ \vec{V}_{\text{error2}} &= \vec{V}_2 - \vec{V}_{\text{ref}} \\ \vec{V}_{\text{error0}} &= -\vec{V}_{\text{ref}} \end{aligned} \tag{2}$$

where $\vec{V}_{\text{error1}}$ and $\vec{V}_{\text{error2}}$ are the error voltage vectors corresponding to active vectors $\vec{V}_1$ and $\vec{V}_2$, respectively. The error voltage $\vec{V}_{\text{error0}}$ corresponds to zero voltage vectors $\vec{V}_0$ or $\vec{V}_7$. The instantaneous error voltage causes the ripple in flux linkage ($\vec{\psi}_{\text{ripple}}$) in the machine. Hence, the ripple in flux linkage can be defined as the time integral of the error voltage applied to the machine by the PWM inverter.

$$\vec{\psi}_{\text{ripple}} = \int \vec{V}_{\text{error}} dt. \tag{3}$$

This definition can also be written in differential form as

$$\frac{d(\vec{\psi}_{\text{ripple}})}{dt} = \vec{V}_{\text{error}}. \tag{4}$$

For convenience, the ripple in flux linkage is termed as rms flux ripple here after.

The instantaneous error voltage and corresponding flux ripple are presented in Fig. 1. The stationary reference frame $\alpha - \beta$ for the stator flux is converted into synchronously revolving magnetic field reference *d–q*. The corresponding rms flux ripple in the *d–q* plane is given by the following equations:

$$\begin{aligned} \psi_{\text{qripple0}} &= \vec{\psi}_{\text{ripple0}} = \vec{V}_{\text{error0}} * T_0 \\ \psi_{\text{qripple1}} + j\psi_{\text{dripple1}} &= \vec{\psi}_{\text{ripple1}} = \vec{V}_{\text{error1}} * T_1 \\ \psi_{\text{qripple2}} - j\psi_{\text{dripple2}} &= \vec{\psi}_{\text{ripple2}} = \vec{V}_{\text{error2}} * T_2. \end{aligned} \tag{5}$$

It is observed that the flux ripple results in flux variation both in the d and q-axis components. The rms ripple of the motor line current is equally affected by the error voltage and causes the distortion in the line current waveform. To reduce variation in flux and distortion in line current, the error voltage should be less. Therefore, switching can be selectively added to reduce current ripple only in regions, where the voltage errors are large. The limited additional switching can keep the switching loss in a permissible limit. In this paper, a hybrid SVPWM strategy is proposed to obtain an optimum switching sequence to reduce the instantaneous voltage error.

The design of a hybrid SVPWM technique involves two steps, mainly 1) selection of a set of switching sequences and 2) determination of boundaries of the various subsectors [2]. In sector I, the reference vector $\vec{V}_{\text{ref}}$ is made of by the nearby two active vectors $\vec{V}_1$ and $\vec{V}_2$ and zero vectors $\vec{V}_0$ and $\vec{V}_7$. The variations of the rms flux ripple of different switching sequences (0127 , 012, 0121, 01212) with respect to the reference angle for different modulation indices (mi $= 0.55$, mi $= 0.65$, mi $= 0.75$, and mi $=$ 0.866) are plotted in Fig. 2(a)–(d), respectively. It is seen that the conventional sequences perform better in the lower modulation index (upto mi $= 0.65$). It is observed that the sequence 01212 has the lowest rms flux ripple over the region $(10^0 - 50^0)$ in sector I for higher modulation index (0.7–0.866). rms flux ripple produced by sequences 0121 and 01212 are comparable at lower modulation index region. Therefore, the introduction of multiple division of active vector dwell time (MDAVT) sequences further reduce the rms flux ripple. It is also observed that rms flux ripple produced by 012, 0121, and 01212 are comparable over the region $(0^0 - 10^0)$. Hence, 012 sequence is used for $(0^0 - 10^0)$ and 721 is used for $(50^0 - 60^0)$to reduce the pulse number of

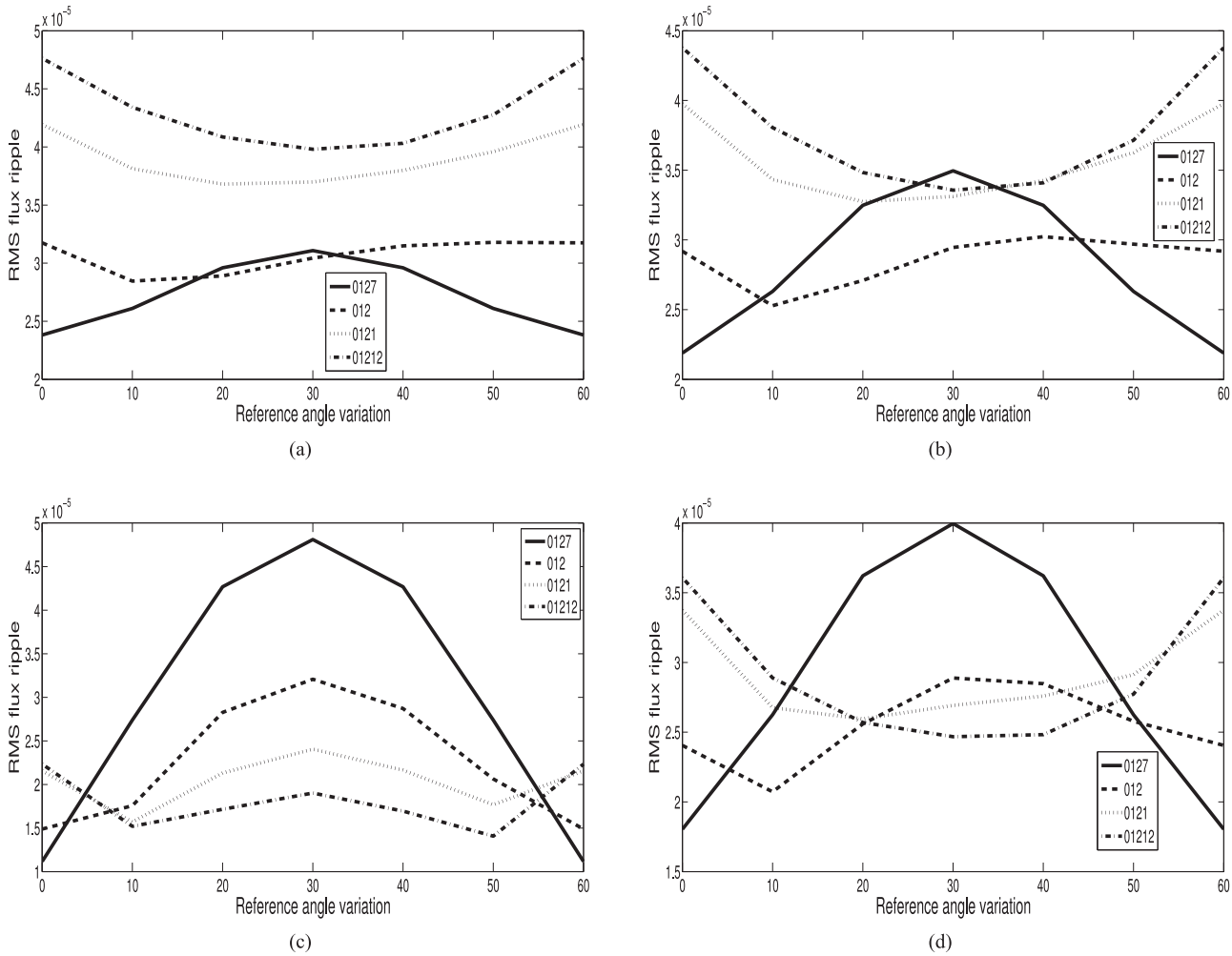

Fig. 2. rms ripple variation of switching sequence with reference vector angle α. (a) mi $= 0.55$, (b) mi $= 0.65$, (c) mi $= 0.75$, (d) mi$= 0.866$.

the proposed hybrid strategy. The additional switchings are added when the fundamental voltage crosses zero.

The proposed hybrid SVPWM considers sequences 0127, 01212, and 012 in the first half $(0^0 - 30^0)$ of the sector I. Sequences 721 and 72121 are used in conjunction with 7210 in the second half $(30^0 - 60^0)$ of the sector I. The proposed MDAVT sequences are used in the range of $10^0 - 50^0$ in sector I. Sequences 012 and 721 are used for the boundary regions $(0^0 - 10^0)$ and $(50^0 - 60^0)$, respectively . The zero vector changing sequence 0127 is used exactly at 30^0 for odd number of samples. The clamping sequence 012 and 127 are used for even number of samples in the middle of the sector to maintain symmetry. In this case, samples need not be placed at 30^0. Zero vector $\vec{V}_0$ is used in the first half of the sector and zero vector $\vec{V}_7$ is used at the second half of the sector. This switching sequence results in 30^0 clamping of a phase. The application of zero vector $\vec{V}_7$ in the first half and zero vector $\vec{V}_0$ in the second half of the sector I result in 60^0 clamping of a phase to either positive or negative dc rail.

Table I gives the complete details of the proposed strategy in the form of number of samples, position of samples, sequences used, pulse number, and clamping position in sector I. This approach maintains all the symmetries in the three-phase waveform and reduces the harmonic contents. Sequences pertaining to all the sectors are listed in Table II.

The active vectors are not applied continuously in the proposed MDAVT sequence. The duration for $\vec{V}_1$ and $\vec{V}_2$ are equally divided as $\frac{T_1}{2}$ and $\frac{T_2}{2}$ in the double switching sequence in the literature [6]–[9]. For the MDAVT sequence, the dwell time T_1 of $\vec{V}_1$ is subdivided into two parts: T_{11} and T_{12} and the dwell time T_2 of $\vec{V}_2$ is also subdivided into two parts: T_{21} and T_{22}. where

$$T_{11} + T_{12} = T_1$$
$$T_{21} + T_{22} = T_2$$

this can be written as

$$\frac{T_{11}}{T_1} + \frac{T_{12}}{T_1} = 1$$
$$\frac{T_{21}}{T_2} + \frac{T_{22}}{T_2} = 1. \quad (6)$$

TABLE I
SPACE-VECTOR-BASED PROPOSED HYBRID SVPWM STRATEGIES

No. of Sample	Position of Samples in Sector I	Sequence Used in Sector I	Pulse Number	Clamp Type
4	$7.5^0, 22.5^0, 37.5^0, 52.5^0$	127-72121-01212-210	12	60^0
5	$6^0, 18^0, 30^0, 42^0, 54^0$	012-21210-0127-72121-127	15	30^0
5	$6^0, 18^0, 30^0, 42^0, 54^0$	721-12127-7210-01212-210	15	60^0
6	$5^0, 15^0, 25^0, 35^0, 45^0, 55^0$	012-21210-012-127-72121-127	17	30^0
6	$5^0, 15^0, 25^0, 35^0, 45^0, 55^0$	721-12127-721-210-01212-210	17	60^0
7	$4.3^0, 12.9^0, 21.4^0, 30^0, 38.6^0, 47.1^0, 55.7^0$	127-72121-12127-7210-01212-21210-012	23	60^0
8	$3.75^0, 11.25^0, 18.75^0, 26.25^0, 33.75^0, 41.25^0, 48.75^0, 56.25^0$	127-72121-12127-721-012-21210-01212-210	25	60^0
9	$3.3^0, 10^0, 16.7^0, 23.3^0, 30^0, 36.7^0, 43.3^0, 50^0, 56.7^0$	012-210-01212-21210-0127-72121-12127-721-127	27	30^0
9	$3.3^0, 10^0, 16.7^0, 23.3^0, 30^0, 36.7^0, 43.3^0, 50^0, 56.7^0$	721-127-72121-12127-7210-01212-21210-012-210	27	60^0
10	$3^0, 9^0, 15^0, 21^0, 27^0, 33^0, 39^0, 45^0, 51^0, 57^0$	012-210-01212-21210-012-127-72121-12127-721-127	29	30^0
10	$3^0, 9^0, 15^0, 21^0, 27^0, 33^0, 39^0, 45^0, 51^0, 57^0$	721-127-72121-12127-721-210-01212-21210-012-210	29	60^0

TABLE II
SVPWM SWITCHING SEQUENCES IN SIX SECTORS OF THE HEXAGON

Sector	Zero Vector Changing Sample Sequence (30^0)	Sequences Used in the Boundary Sample ($0^0 - 10^0, 50^0 - 60^0$)	Sequence Used in the Middle Sample Sample ($10^0 - 50^0$)
I	0127 - 7210	012, 127	01212 - 72121
II	7230 - 0327	723, 032	72323 - 03232
III	0347 - 7430	034, 743	03434 - 74343
IV	7450 - 0547	745, 054	74545 - 05454
V	0567 - 7650	056, 765	05656 - 76565
VI	7610 - 0167	761, 016	76161 - 01616

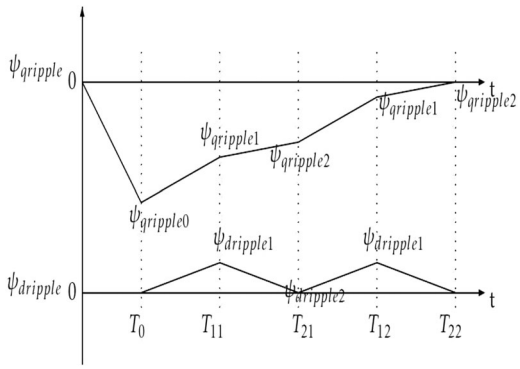

Fig. 3. Variation of stator flux ripple based on MDAVT in *d–q* plane over a subcycle.

To describe the process of swapping parts of $\vec{V}_1$ and $\vec{V}_2$, two variables *x* and *y* are defined as

$$x = \frac{T_{11}}{T_1}$$

$$y = \frac{T_{21}}{T_2}$$

$$x + y = \frac{T_{11}}{T_1} + \frac{T_{21}}{T_2}. \tag{7}$$

By using symmetry property, it is obtained as follows:

$$\frac{T_{11}}{T_1} + \frac{T_{21}}{T_2} = \frac{T_{12}}{T_1} + \frac{T_{22}}{T_2} = 1. \tag{8}$$

The distribution of flux ripple along *d* and *q*-axis with MDAVT sequence is shown in Fig. 3. To obtain minimum THD, the flux ripple should be minimum. For minimum flux ripple, voltage error should be minimum. A mathematical analysis is presented in the following section to obtain minimum voltage error for an optimum value of *x* and *y*.

III. ANALYSIS OF OPTIMAL SUBDIVISION OF ACTIVE VECTOR DWELL TIME

A unique solution is presented to obtain the optimal subdivision of active vectors and the objective function is chosen with respect to rms error. The rms voltage error is taken into consideration for the analysis of the clamped sequence. The optimal value corresponding to the minimum rms ripple also satisfies the absolute minimum area criteria. Therefore, minimum absolute area is taken for the analysis of the proposed sequence. The subdivision criteria to corresponding sequence 0121 and 7212 are same to keep the symmetry in the waveform. Similarly subdivision of sequence and corresponding optimized value for 01212 and 72121 are also same. The optimization criteria remains valid when the rms error maps to the absolute area of the triangle. The small angle approximation is useful simplification of the basic trigonometric functions which is approximately true in the limit where the angle approaches zero. Linear approximation of a 2-D digital curve is often a compact and effective representation of the curve for shape analysis and pattern classification. Approximation of functions by linear functions are widely used in many hardware and software design applications. The standard methodologies consist in the piecewise linear approximation of such functions. The optimization criteria is to minimize the maximum absolute error over the range. Two approximation models are studied to obtain the optimum subdivision of the

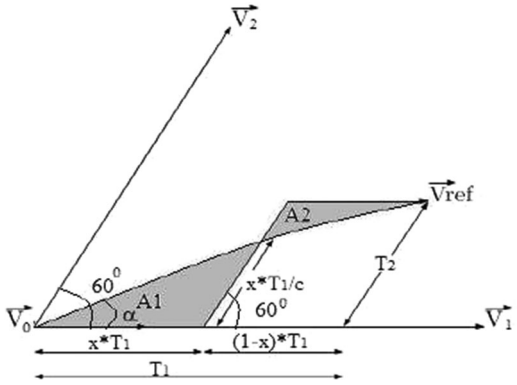

Fig. 4. Linear approximation of the sine model of Sequence 0121.

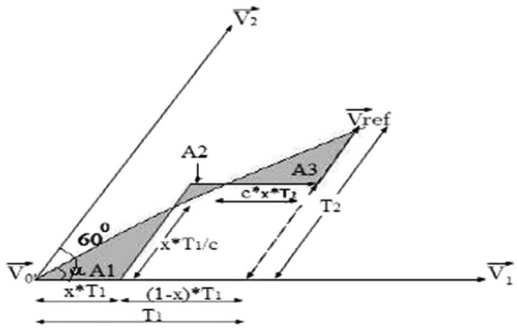

Fig. 5. Linear approximation of sine model of sequence 01212.

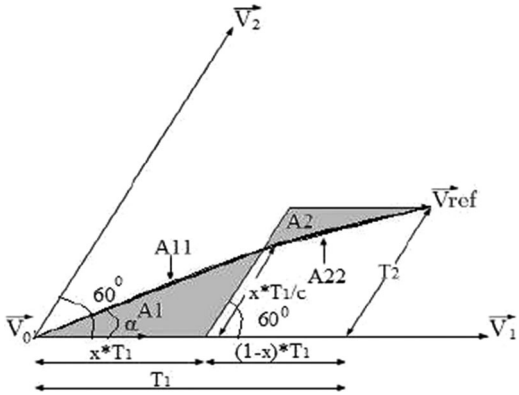

Fig. 6. Sine approximation model of sequence 0121.

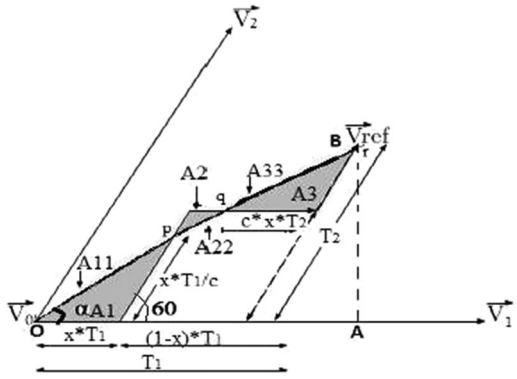

Fig. 7. Sine approximation model of sequence 01212.

active vector dwell time. They are linear approximation of sine model and sine approximation model. The derived values obtained from sine approximation model are found to be the best optimum solution.

A. Linear Approximation of Sine Model

The slope of a sine curve between two sample location at $\theta 1$ and $\theta 2$ is defined as $\frac{\sin(\theta 2)-\sin(\theta 1)}{(\theta 2)-(\theta 1)}$.

The value of $\theta 2 - \theta 1$ is limited by 60^0 within a sector and

$$\frac{\sin(\theta 2)-\sin(\theta 1)}{(\theta 2)-(\theta 1)} <= 1. \tag{9}$$

If $\vec{V}_{\text{ref}}$ is applied at an angle α w.r.t $\vec{V}_1$, then

$$\tan\alpha = \frac{T_2 \sin 60}{T_1 + T_2 \cos 60} <= 1 \tag{10}$$

$$\frac{T_2 \sin 60}{T_1 + T_2 \cos 60} = \frac{1}{k1} T_1 = \left(\frac{\sqrt{3}k1 - 1}{2}\right) T_2$$

$$T_1 = c * T_2 \tag{11}$$

where $k1 > 1$ and $c = (\frac{\sqrt{3}k1-1}{2})$, $c < 1$ is a positive quantity.

Linear approximation of the sine model is considered by joining two points on the actual sine curve. The area of $\triangle A1$ and $\triangle A2$ in Fig. 4 represent the rms voltage error corresponding to sequence 0121. The linear approximated absolute area of the two triangles A1 and A2 of switching sequence 0121 are calculated as follows.

Area of first triangle

$$A1 = \frac{1}{2} * x * T_1 * T_1 * \frac{x}{c} * \sin 60 = \frac{1}{2} * T_1^2 * \frac{x^2}{c} * \sin 60. \tag{12}$$

Area of second triangle

$$A2 = \frac{1}{2} * T_1^2 * ((1-x)^2/c) * \sin 60. \tag{13}$$

The total absolute area of the sequence is optimized by $\frac{dA}{dx} = 0$, where A = A1 + A2

$$4x - 2 = 0. \tag{14}$$

The optimum value of x obtained is 0.5.

The rms voltage error of sequence 01212 is shown in Fig. 5. The total absolute area of triangles represents the total rms error.

Area of first triangle

$$A1 = \frac{1}{2} * x * T_1 * T_1 * \frac{x}{c} * \sin 60 = \frac{1}{2} * T_1^2 * \frac{x^2}{c} * \sin 60. \tag{15}$$

Area of second triangle

$$A2 = \frac{1}{2} * T_1 * T_1 * (1 - 2\,x) * \frac{1 - 2\,x}{c} * \sin 60 = \frac{1}{2} * T_1^2 * \frac{(1-2\,x)^2}{c} * \sin 60. \tag{16}$$

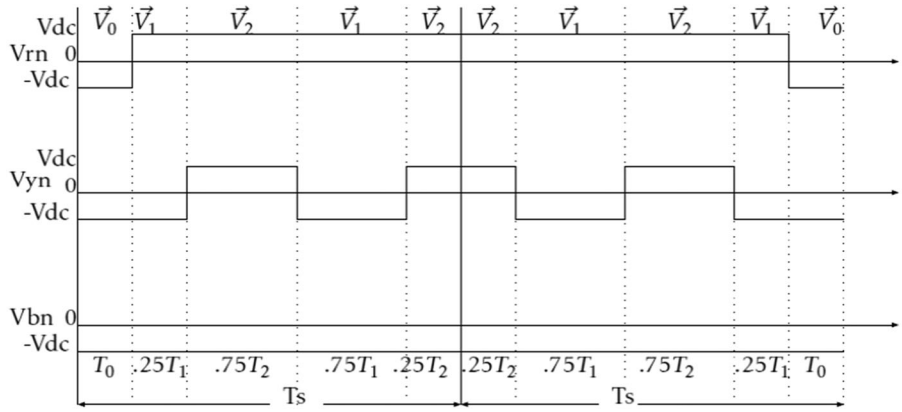

Fig. 8. Optimum dwell time application of active vectors in sequence 01212.

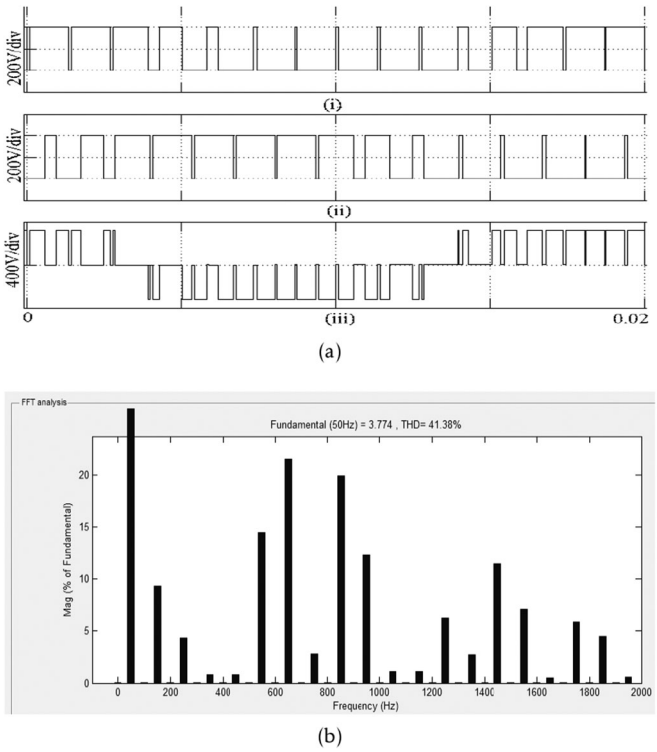

Fig. 9. (a) Pole voltages and line voltage (i) V_{RN}, (ii) V_{YN}, and (iii) V_{RY} (x-axis = 5 ms/div). (b) FFT spectrum of the line voltage of CSVPWM.

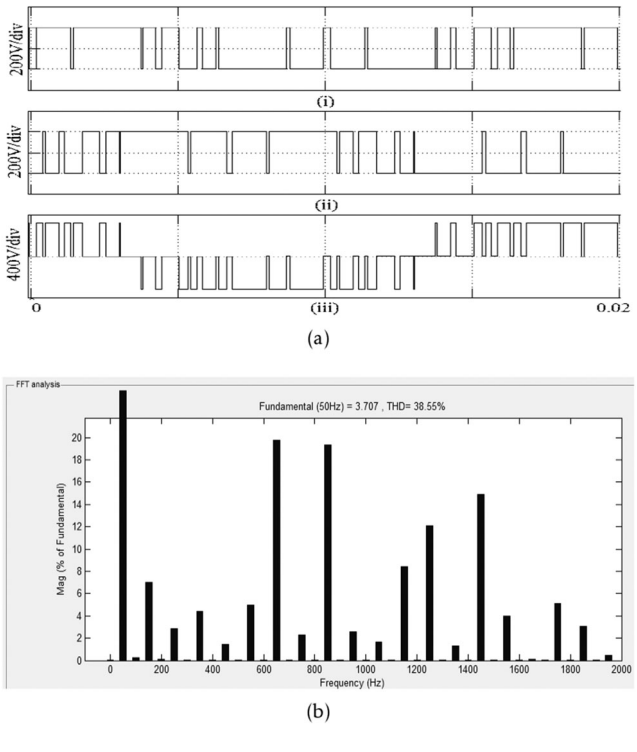

Fig. 10. (a) Pole voltages and line voltage (i) V_{RN}, (ii) V_{YN}, and (iii)V_{RY} (x-axis = 5 ms/div). (b) FFT spectrum of the line voltage of ASCPWM.

Area of third triangle

$$A3 = \frac{1}{2} * T_1^2 * \frac{x^2}{c} * \sin 60. \tag{17}$$

The total approximated absolute area of three triangles are

$$\begin{aligned} A &= A1 + A2 + A3 \\ &= \frac{1}{2} * T_1^2 * \sin 60 * \left[\frac{x^2}{c} + \frac{(1-2\,x)^2}{c} + \frac{x^2}{c} \right] \\ &= \frac{1}{2 * c} * T_1^2 * \sin 60 * (6\,x^2 - 4\,x + 1). \end{aligned} \tag{18}$$

By optimum area criteria

$$\begin{aligned} \frac{dA}{dx} &= 0 \\ 12\,x - 4 &= 0. \end{aligned} \tag{19}$$

The optimum value of x is 0.333 and y is 0.6667 .

B. Sine Approximation Model

The shaded portion of Fig. 6 shows that the adjusted absolute area (denoted by A11 and A22) of the sine approximation model of sequence 0121 . A small area is adjusted to the absolute area of the linear portion (denoted by A1 and A2) of the sine model to obtain a closer approximated sine model. A small area is added

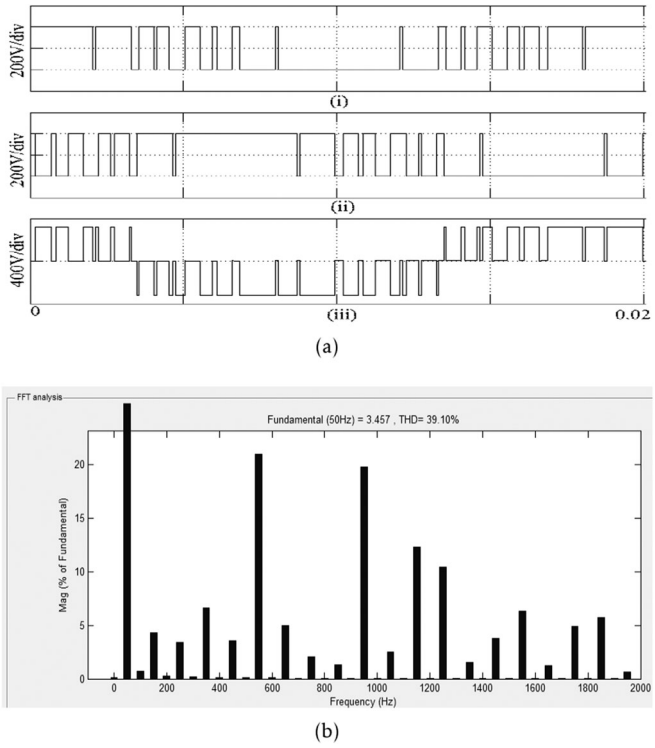

Fig. 11. (a) Pole voltages and line voltage (i) V_{RN}, (ii) V_{YN}, and (iii) V_{RY} (x-axis = 5 ms/div). (b) FFT spectrum of the line voltage of ACCPWM.

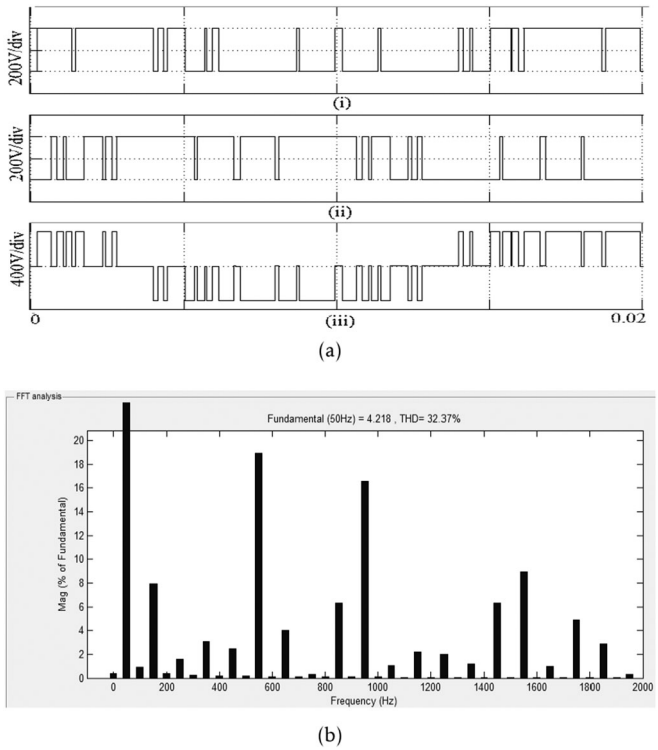

Fig. 12. (a) Pole voltages and line voltage (i) V_{RN}, (ii) V_{YN}, and (iii) V_{RY} (x-axis = 5 ms/div). (b) FFT spectrum of the line voltage of the proposed hybrid SVPWM.

to the first triangle A1 and a small area is excluded from the second triangle A2. If the value of x is optimum, the included area in the first triangle should be equal to the excluded area of the second triangle. Hence, the value of x and y are 0.5 to keep symmetry of the switching sequence.

In Fig. 7, the points o, p, q, and r are on the actual sine curve. The approximated adjusted area (A11, A22, and A33) of the sine approximation model of sequence 01212 is shown in Fig. 7. A small area A11 is added to the first triangle A1 and a small area A22 is excluded from the second triangle A2 and small area A33 is added to the third triangle A3 of linear sine approximated absolute area to keep the objective function as an approximated sine. We may consider that the adjusted absolute area is a small rectangular strip, whose width is proportional to k and length is the length of the hypotenuse of the triangle. Therefore, the adjusted absolute area under the sine curve is equal to k*(length of the hypotenuse of the triangle).

The hypotenuse of the large triangle $\triangle OAB$ (see Fig. 7) is taken by the Pythagoras theorem as

$$\begin{aligned}(OB)^2 &= \left(T_1+\frac{T_2}{2}\right)^2+\left(\frac{\sqrt{3}T_2}{2}\right)^2\\ &= \left(c*T_2+\frac{T_2}{2}\right)^2+\frac{3}{4}(T_2)^2=(c^2+c+1)T_2^2\\ &= \left(1+\frac{1}{c}+\frac{1}{c^2}\right)*T_1^2\\ OB &= k2*T_1 \end{aligned} \tag{20}$$

where $k2=\sqrt{(1+\frac{1}{c}+\frac{1}{c^2})}$, $k2>1$. The base of the triangle A1, A2, and A3 is x, x–y, and $1-y$, respectively. The approximated adjusted area of the three strips are

$$\begin{aligned}A11 &= k*(x*OB)=k*(x*k2*T_1)\\ A22 &= k*((x-y)*OB)=k*((x-y)*k2*T_1)\\ &= k*((1-2\,x)*k2*T_1)\\ A33 &= k*((1-y)*OB)=k*((1-y)*k2*T_1)\\ &= k*(x*k2*T_1). \end{aligned} \tag{21}$$

When the value of x and y are optimum, the adjusted absolute area of the triangle ($\triangle OAB$) is

$$Area_{\text{adjusted absolute area}} = Area_{\text{added}} - Area_{\text{excluded}}. \tag{22}$$

The adjusted area that is taken in consideration of the sine approximation method is

$$\begin{aligned}Area_{\text{adjusted absolute area}} &= A11-A22+A33\\ &= k*[(k2*x*T_1+k2*x*T_1)\\ &\quad -k2*(T_1-2*T_1*x)]\\ &= k*k2*T_1*[4x-1]. \end{aligned} \tag{23}$$

By using the optimum area criteria, the adjusted absolute area should be minimum.

$$\frac{d}{dx}(Area_{\text{adjusted absolute area}})=0 \tag{24}$$

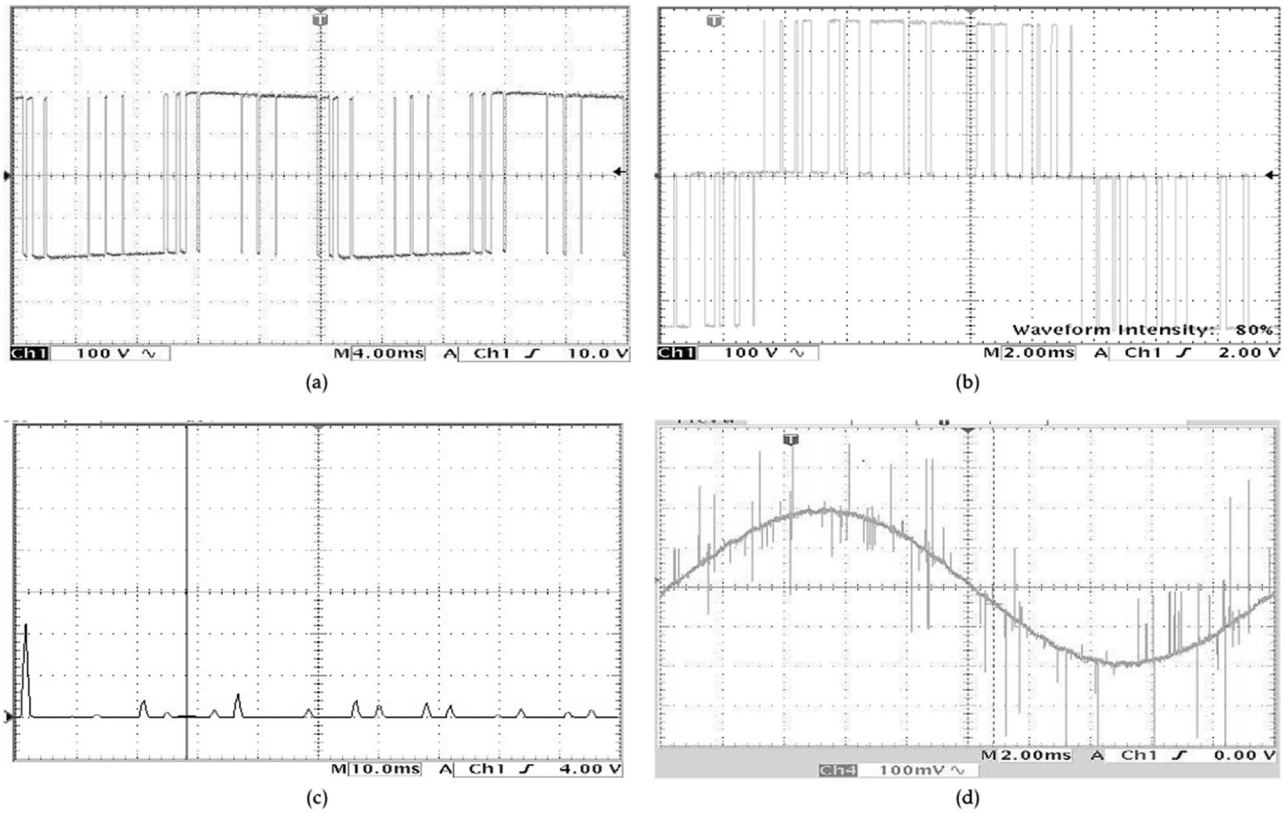

Fig. 13. (a) Pole voltage waveform. (b) Line voltage waveform. (c) FFT spectrum. (d) Line current of the proposed hybrid SVPWM (30^0 clamping).

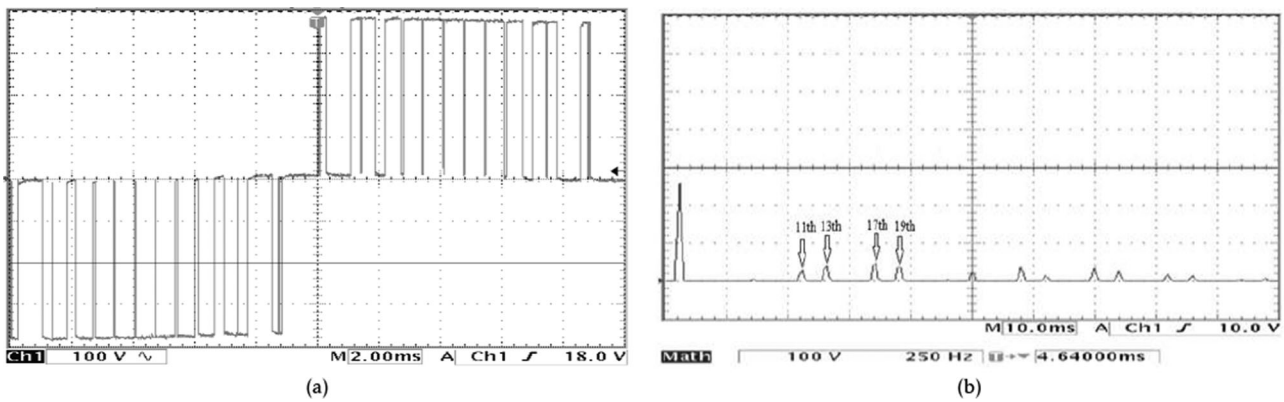

Fig. 14. (a) Line voltage waveform. (b) FFT spectrum of CSVPWM (switching frequency = 750 Hz).

which gives

$$k * k2 * [4x - 1] = 0 \tag{25}$$

i.e., $x = 0.25$. In the sine approximation model, adjusted absolute area is added to the approximated absolute area of linear approximation of sine model. When $x = 0.25$, the approximated adjusted area of A11 and A33 is equal to A22. Therefore, the effect of approximated adjusted area is minimum only at $x = 0.25$.

The generalized equation for resultant absolute area of triangle ($\triangle OAB$) is

$$\begin{aligned} Absolute\ Area = {} & \frac{1}{2} * T_1 * T_2 * \sin 60 * [x^2 + (1 - 2x)^2 + x^2] \\ & + k * [(k2 * x * T_1 + k2 * x * T_1) \\ & - k2 * (T_1 - 2 * T_1 * x)]. \end{aligned} \tag{26}$$

From (26), approximated absolute area in linear portion of sine approximation method is proportional to $T_1^2 (T_1 * T_2)$ and adjusted absolute area in the sine approximation method is pro-

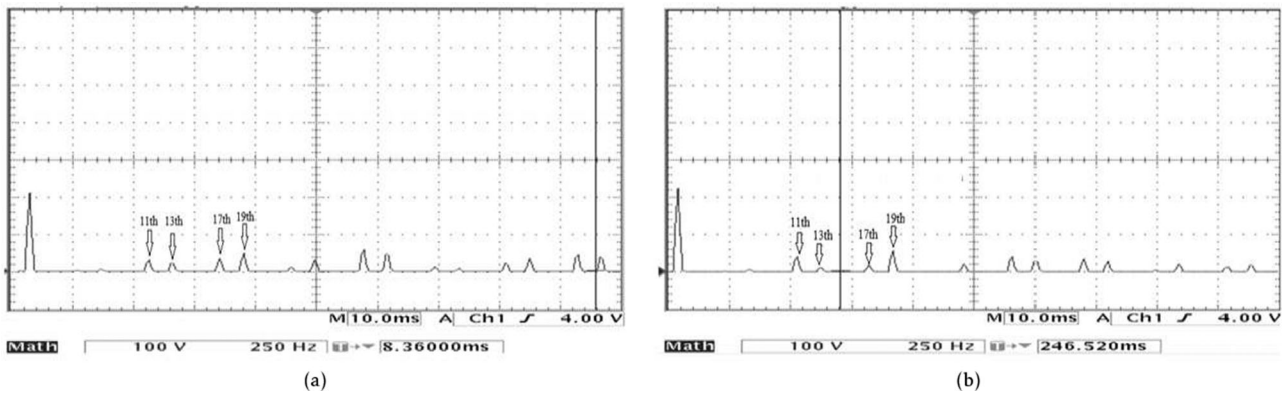

Fig. 15. FFT spectrum of the line voltage (a) ASCPWM and (b) proposed hybrid SVPWM (30^0 clamping) (switching frequency = 750 Hz).

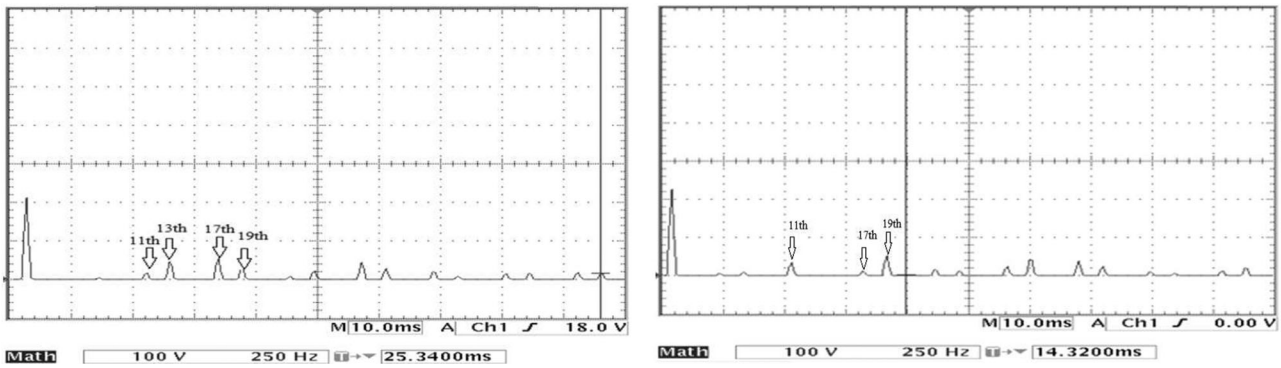

Fig. 16. FFT spectrum of the line voltage (a) ACCPWM and (b) proposed hybrid SVPWM (60^0 clamping) (switching frequency = 750 Hz).

portional to T_1. If $0 < T_1 < 1$, the resultant area of linear sine approximation method is less effective than adjusted absolute area in the sine approximation method in determining the optimum value of x and y.

At $x = 0.25$, the adjusted absolute area corresponding to sine approximation model is zero and the approximated absolute area of the linear approximation of the sine model is deteriorated by 12.5% than at $x = 0.333$. Hence, the sine approximation method is considered to be the best and optimal value of x and y are taken as 0.25 and 0.75, respectively. The corresponding timing diagram for the optimum MDAVT sequence is shown in Fig. 8.

The durations and positions of the additional pulses are controlled by selecting x and y (8). The optimization of the active vector dwell time in the proposed hybrid SVPWM ensures that the waveform of the output voltage retains half-wave symmetry. The performance evaluation of the proposed hybrid SVPWM with optimal subdivision of active vectors is presented with simulation and experimental results in the next section.

IV. Results and Performance Evaluation of Proposed Hybrid SVPWM Techniques

A. Simulation Results

The proposed optimized modulation strategy is implemented in MATLAB—SIMULINK. The specifications of motor drive used in simulation are 4 kW, 400 V, 50 Hz, 1430 r/min, $Rs = 1.405\ \Omega$, $Ls = 0.005839$ H, $Rr = 1.395\ \Omega$, $Lr = 0.00589$ H, $Lm = 0.1722$ H, and pole pair = 2. All the double switching SVPWM techniques existing in the literature have been implemented based on the constant fundamental frequency.

The simulation results of CSVPWM, ASCPWM, and ACCPWM and the proposed hybrid SVPWM are shown in Figs. 9–12, respectively. Fig. 9(a) and (b) represents pole and line voltage waveforms and FFT spectrum, respectively, of CSVPWM. Similarly Figs. 10–12 present pole and line voltage waveforms and FFT spectrum corresponding to ASCPWM, ACCPWM, and the proposed hybrid SVPWM with optimal ratio of (0.25, 0.75), respectively. From the spectrum, it can be observed that the proposed hybrid SVPWM with optimal division (0.25, 0.75) of active vectors achieves the lowest THD. The proposed work has been experimentally verified on a 415-V, 2.2-kW, three-phase induction motor and demonstrated with the experimental results in next subsection.

B. Experimental Results

An IGBT-based VSI with a dc bus voltage of 400 V, 2 kV·A is developed. The proposed hybrid SVPWM strategy is implemented with an 8-bit microcontroller (PIC18f452). The work has been experimentally verified on the 415-V, 2.2-kW, three-phase induction motor.

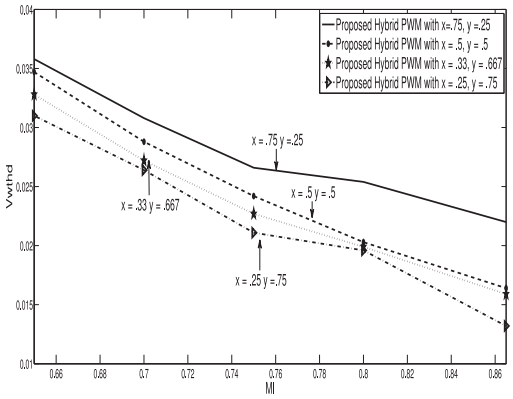

Fig. 17. V_{wthd} performance of proposed switching clamping strategies with different x and y.

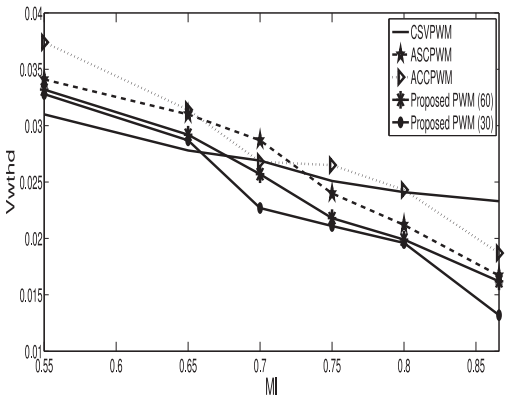

Fig. 18. V_{wthd} performance of proposed hybrid SVPWM with CSVPWM and existing advanced SVPWM techniques at no load (pulse no. = 15).

TABLE III
SVPWM SWITCHING SEQUENCES IN SECTOR I WITH SAMPLE NO = 5 AND PULSE NO = 15

SVPWM Technique	Sequences Used in Sector I
CSVPWM	0127, 7210, 0127, 7210, 0127
ASCPWM	0121, 1210, 0127, 7212, 2127
ACCPWM	7212, 2127, 7210, 0121, 1210
Proposed hybrid PWM (60^0)	721, 12127, 7210, 01212, 210
Proposed hybrid PWM (30^0)	012, 21210, 0127, 72121, 127

The pole voltage, line voltage, FFT spectrum of line voltage, and line current obtained from the experiment are shown in Fig. 13(a)–(d), respectively.

Harmonic spectra of the proposed SVPWM technique is presented by the FFT of the inverter output voltage (Vdc = 400 V, MI = 0.8). The THD of inverter output fed to the motor drive is computed from the oscilloscope frequency spectrum. Fig. 14(a) and (b) presents the line voltage waveform and oscilloscope frequency spectrum for CSVPWM. The line-voltage FFT spectrum of ASCPWM, proposed hybrid SVPWM (30^0 clamping), ACCPWM, and proposed hybrid SVPWM (60^0 clamping) are presented in Figs. 15(a), 15(b), 16(a), and 16(b), respectively. The computed values of weighted voltage THD

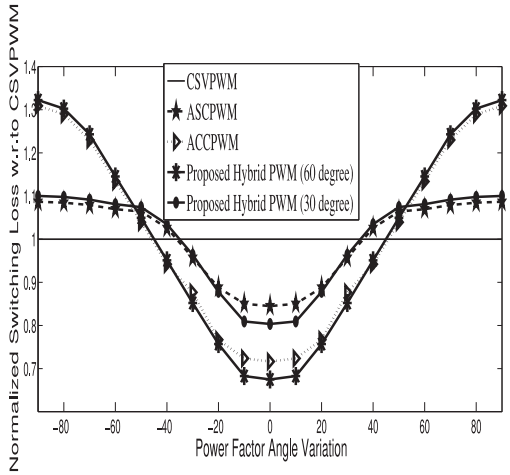

Fig. 19. Normalized switching loss characteristics of different SVPWM techniques.

(V_{wthd}) are obtained as 2.41%, 2.1%, 1.96%, 2.4%, and 2% for CSVPWM, ASCPWM, proposed hybrid SVPWM (30^0 clamping), ACCPWM, and the proposed hybrid SVPWM (60^0 clamping), respectively. It can be observed from Fig. 14(b), the side band components of switching frequency (750 Hz) are 11th, 13th, 17th, and 19th are present in considerable amount for CSVPWM. The respective harmonic components in the proposed hybrid SVPWM technique have been reduced drastically.

The optimal subdivision of MDAVT as explained in Section III is incorporated in the proposed hybrid SVPWM technique. The value of x and y are also verified experimentally in different combination. The results obtained are shown in Fig. 17. It is observed that the optimal value of x= 0.25 and y = 0.75 gives the minimum THD.

In the present implementation the fundamental frequency (50 Hz) is fixed with respect to various sample number. The subcycle time is determined with respect to total number of samples and fundamental frequency. Subcycle time remains fixed irrespective of number of switchings present in the sample. The samples are uniformly placed in the sector and we do not enforce average time between two switchings to be equal. Hence, the proposed technique provides fixed frequency behavior in an average sense with respect to various pulse number. Pulse number denotes the number of switching pulses present in one half cycle corresponding to the fundamental frequency. For a pulse number of 15, the switching frequency of the SVPWM technique is 750 Hz. All the strategies (CSVPWM, ASCPWM, ACCPWM) including the proposed strategy are compared with respect to same pulse number. Hence, the performance of the proposed SVPWM strategy is not affected by the increased number of switching in a sequence.

The THD obtained from the experimental results are shown in Fig. 18. It shows that the proposed hybrid SVPWM strategy with MDAVT has the lowest THD in linear modulation index region compared to advanced existing SVPWM techniques [6]. The switching sequences used in different SVPWM techniques for sector I are summarized in Table III. The zero vector changing sample of ASCPWM and ACCPWM strategies is located at 30^0.

TABLE IV
SWITCHINGLOSS CHARACTERISTICS OF THE PROPOSED HYBRID SVPWM WITH EXISTING ADVANCED SVPWM

Power factor (MI = 0.8)	ACCPWM (60^0)	Proposed Hybrid SVPWM (60^0)	ASCPWM (30^0)	Proposed Hybrid SVPWM (30^0)
$0^0 - 30^0$	72%	67%	85%	80%
$30^0 - 45^0$	85%	85%	95%	96%
$45^0 - 60^0$	106%	105%	105%	106%
$60^0 - 90^0$	130%	131%	109%	110%

The normalized switching loss characteristics of the proposed and existing SVPWM techniques compared to CSVPWM is shown in Fig. 19.

The switching loss is less compared to CSVPWM (-30^0 to $+30^0$) and comparable to the existing advanced SVPWM techniques. From Table I, it is clear that all the multiple switching sequence is located near to the middle (10^0–50^0) of the sector. Sequence 01212 results in single switching in R-phase, three switchings in Y-phase and zero switching in B-phase. The strategy keeps B-phase clamped to either positive or negative dc rail. Y-phase passes through zero crossing (unity power factor angle) point at 30^0 in sector I. Therefore, the additional switching in Y-phase does not increase the switching loss level. The proposed strategy produce very good THD performance over the range of modulation index from 0.7 to 0.866. Fig. 19 demonstrates that the proposed strategy (30^0 clamping) outperforms ASCPWM for the power factor angle over the range of $+30^0 - -30^0$ with respect to switching loss. Outside the mentioned range the normalized performance of the proposed strategy with respect to CSVPWM deteriorates with in a limit of 1%, which is comparable with the existing strategies. Similarly the proposed strategy (60^0 clamping) outperforms ACCPWM for the power factor angle over the range of $+40^0 - -40^0$. The proposed strategy deteriorates by 1% outside the mentioned range.

Comparison of performance index switching loss of the proposed hybrid SVPWM technique with advanced SVPWM [2]–[10] over the conventional SVPWM is given in Table IV. The average percentage of reduction in switching loss of ACCPWM, ASCPWM compared to CSVPWM are 28% and 15%, whereas the corresponding reductions in switching loss by the proposed hybrid SVPWM techniques are 33% and 20%, respectively, for unity power factor operation. Therefore, the proposed hybrid SVPWM with optimum MDAVT performs better than existing advanced SVPWM techniques.

V. CONCLUSION

This paper introduces a new hybrid SVPWM switching strategy based on MDAVT to reduce rms flux ripple. The rms error voltage is taken into consideration for the analysis of the clamped sequence. The optimal value corresponding to the minimum rms ripple also satisfies the absolute minimum area criteria. To minimize the voltage error and the corresponding flux ripple an optimal subdivision of the active vector dwell time is presented by theoretical analysis and verified by experimental results. The proposed hybrid SVPWM strategy provides less THD compared to existing advanced SVPWM techniques. The switching loss is less in the higher power factor region compared to existing advanced SVPWM techniques.

REFERENCES

[1] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converter: Principle and Practice*. New York, NY, USA: Wiley, 2003.

[2] G. Narayanan and V. T. Ranganathan, "Synchronized PWM strategies based on space vector approach. Part 1: Principles of waveform generation," *Proc. IEE*, vol. 146, no. 3, pp. 267–275, May 1999.

[3] G. Narayanan and V. T. Ranganathan, "Synchronized PWM strategies based on space vector approach. Part 2: Performance assessment and application to V/f drives," *Proc. IEE*, vol. 146, no. 3, pp. 267–275, May 1999.

[4] G. Narayanan, and V. T. Ranganathan, "Triangle comparison approach and space vector approach to pulsewidth modulation in inverter fed drives," *J. Indian Inst. Sci.*, vol. 80, pp. 409–427, Oct. 2000.

[5] G. Narayanan, and V. T. Ranganathan, "Two novel synchronized bus-clamping PWM strategies based on space vector approach for high power drives," *IEEE Trans. Power Electron.*, vol. 17, no. 1, pp. 84–93, Jan. 2002.

[6] G. Narayanan, H. K. Krishnamurthy, D. Zhao, R. Ayyanar, "Advanced bus-clamping PWM techniques based on space vector approach," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 974–984, Jul. 2006.

[7] G. Narayanan, D. Zhao, H. K. Krishnamurthy, R. Ayyanar, V. T. Ranganathan, "Space vector based hybrid PWM technique for reduced current ripple," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1614–1627, Apr. 2008.

[8] Di Zhao, V. S. S. Pavan Kumar Hari, G. Narayanan, Rajapandian Ayyanar, "Space-vector-based hybrid pulsewidth modulation techniques for reduced harmonic distortion and switching loss," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 760–774, Mar. 2010.

[9] T. Bhavsar, G. Narayanan, "Harmonic analysis of advanced bus-clamping PWM techniques," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2347–2352, Oct. 2009.

[10] G. Narayanan, J. S. Siva Prasad, H. K. Krishnamurthy, R. Ayyanar, "Reduction in torque ripple in induction motor drives using an advanced hybrid PWM technique," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2085–2091, Jun. 2010.

[11] V. Blasko, "Analysis of a hybrid PWM based on modified space vector and triangle comparison methods," *IEEE Trans. Ind. Appl.*, vol. 33, no. 3, pp. 756–764, Jun. 1997.

[12] K. Taniguchi and Y. Ogino, "PWM technique for power MOSFET inverter," *IEEE Trans. Power Electron.*, vol. 3, no. 3, pp. 328–334, Jul. 1988.

[13] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "Simple analytical and graphical methods for carrier-based PWM-VSI drives," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 49–61, Jan. 1999.

[14] S. Bernet, R. Teichmann, A. Zuckerberger, and P. K. Steimer, "Comparison of high-power IGBT's and hard-driven GTO's for high-power inverters," *IEEE Trans. Ind. Appl.*, vol. 35, no. 2, pp. 487–495, Mar./Apr. 1999.

[15] K. Gopakumar, V. T. Ranganathan, and S. R. Bhat, "Split phase induction motor operation from PWM voltage source inverter," *IEEE Trans. Ind. Appl.*, vol. 29, pp. 927–932, Sep./Oct. 1993.

[16] J. W. Kolar, H. Ertl, and F. C. Zach, "Minimizing the current harmonic rms value of three-phase PWM converter system by optimal and suboptimal transition between continuous and discontinuous modulation," in *Proc. IEEE Power Electron. Spec. Conf.*, Cambridge, MA, USA, Jun. 1991, pp. 372–381.

[17] P. G. Handley and J. T. Boys, "Practical real-time PWM modulators–An assessment," *Proc. IEE*, vol. 139, no. 2, pp. 96–102, 1992.

[18] Y. Iwaji *et al.*, "A new PWM method to reduce beat phenomenon in large–capacity inverters with low switching frequency," *IEEE Trans. Ind. Appl.*, vol. 35, no. 3, pp. 606–612, May/Jun. 1999.
[19] D. G. Holmes, "The significance of zero space vector placement for carrier-based PWM schemes," *IEEE Trans. Ind. Appl.*, vol. 32, pp. 1122–1129, Sep./Oct. 1996.
[20] S. R. Bowes and A. Midoun, "Suboptimal switching strategies for microprocessor- controlled PWM inverter drives," *Proc. IEE*, vol. 132, no. 3, pp. 133–148, 1985.
[21] J. Holtz, W. Lotzkat, and A. Khambadkone, "On continuous control of PWM inverters in the overmodulation range including the six-step mode," *IEEE Trans. Power Electon.*, vol. 8, no. 4, pp. 546–553, Jul. 1993.
[22] S.-L. An, X.-D. Sun, Q. Zhang, Y.-R. Zhong, and B.-Y. Ren, "Study on the novel generalized discontinuous SVPWM strategies for three-phase voltage source inverters," *IEEE Trans. Ind. Informat.*, vol. 9, no. 2, pp. 781–789, May 2013.
[23] M. D. Nair, G. Vivek, K. Anjana, and M. Barai, "A comparative investigation of various advanced bus clamped space vector pulse width modulation (SVPWM) techniques," in *Proc. IEEE Energy Convers. Congr. Expo.*, Pittsburgh, PA, USA. pp. 5458–5465, 2014.
[24] M. D. Nair, G. Vivek, and M. Barai, "Performance study of advanced discontinuous SVPWM methods with zero changing angle variation," in *Proc. IEEE Signal Process., Informat., Commun. Energy Syst.*, Calicut, India, 2015, pp. 1–5.
[25] M. D. Nair, G. Vivek, M. Barai "Performance evaluation of clamping position variation on advanced bus clamping strategies: Experimental verification," in *Proc. IEEE Power Electron. Drive Syst.*, Sydney, Australia, 2015, pp. 1156–1161.

Jayanta Biswas (M'09) received the B.E. degree in computer science from Bengal Engineering College, Howrah, India, in 1993, and the M.E. degree in system science and automation and the Ph.D. degree in multicasting over wireless networks for entertainment applications from the Indian Institute of Science, Bengaluru, India, in 1995 and 2006, respectively.

From January 1995 to 1998, he was with NCR Corporation, Columbia, SC, USA. From January 1999 to November 2002, he was with Alcatel Internetworking, Calabasas, CA, USA, where from May 2000 to November 2002, he was the Project Manager at Alcatel Internetworking ATM (core and edge) switch software development effort, and he was also leading ten Gigabit software development effort. He worked at CEM solutions, Bangalore, India, leading embedded product development and research activity as the Technical Director. He worked and taught as Assistant Professor at the International Institute of Information Technology, Bangalore, in Embedded systems and VLSI group. His current research interests include digital controller architecture for power management application ICs and modulation techniques for multilevel power electronics converter. He is currently working as a freelancer researcher working at home.

Meenu D Nair (S'16) received the B.Tech.degree in electrical and electronics engineering from the Rajiv Gandhi Institute of Technology, Kottayam, India, in 2009, the M.Tech. degree in power electronics from Shanmugha Arts, Science, Technology & Research Academy, Tanjavur, India, in 2011. She is currently working toward the Ph.D. degree in Department of Electrical Engineering, National Institute of Technology Calicut, Kozhikode, India.

Her research interests include multilevel inverters and pulsewidth modulation techniques for drives.

Vivek Gopinath (S'16) Received the B.Tech degree in electrical and electronics engineering from the University of Calicut, Malappuram, India, in 2009, the Master of Engineering degree in power electronics and drives from Anna University, Chennai, India, in 2011. He is currently working toward the Ph.D. degree in the Department of Electrical Engineering, National Institute of Technology Calicut, Kozhikode, India.

His research interests include pulsewidth modulation control in multilevel inverters.

Mukti Barai (M'09) received the B.E. degree in electrical engineering from Bengal Engineering College, Howrah, India, in 1992, and the M.Tech. and Ph.D. degrees in machine drives and power electronics from the Indian Institute of Technology, Kharagpur, India, in 1994 and 2009, respectively.

From 1994 to 2000, she was a Senior Engineer (Design and Development) in the Electronics Division, Bharat Heavy Electricals Limited, Bangalore, India. From 2000 to 2002, she was a Principal Software Development Engineer at Alcatel Internetworking, Inc. From 2003 to 2004, she was at ST Microelectronics Research Laboratory, Indian Institute of Science, Bangalore. She is currently working as an Assistant Professor at the National Institute of Technology Calicut, Kozhikode, India. Her research interests include modulation techniques for multilevel power electronics converter and digital controller architecture for power management application ICs.