A New Topology of Multilevel VSC Converter for a Hybrid HVDC Transmission System

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***Abstract*—This paper introduces a new multilevel converter topology for a hybrid HVDC system comprising line-commutated converter (LCC) and voltage source converter (VSC). Among the existing modular multilevel converter (MMC) topologies for the hybrid HVDC, a mixed MMC structure with half-bridge submodules (HBSMs) and full-bridge submodules (FBSMs) has characteristics of reduced system cost, low operation loss, but still keeping capability to cope with dc short-circuit fault. However, it is very difficult for the conventional hybrid MMC structure to balance the submodule capacitor voltages under dc-bus voltage sliding since each MMC arm is a mixture of HBSMs and FBSMs. To solve the defect of the conventional hybrid MMC structure, an asymmetric mixed MMC, in which one arm is made of series-connected HBSMs and other arm is made of FBSMs, is devised. The proposed asymmetric MMC can regulate the dc-bus voltage freely without uncontrollable submodule capacitor voltages. The problems of the conventional MMC structure and the validity of asymmetric MMC are verified by both computer simulation and experimental results.**

***Index Terms*—DC short-circuit fault, hybrid HVDC transmission system, hybrid modular multilevel converter (MMC), line-commutated converter (LCC), MMC.**

I. Introduction

FOR decades, a line-commutated converter (LCC) based HVDC has been developed and applied to most HVDC transmission systems. Nowadays, most HVDC systems in commercial operation employ LCCs due to higher reliability, higher power capability, excellent overload capability, and higher efficiency. However, it presents some drawbacks such as strong ac grid requirements, larger system size for harmonic and reactive filters, and lack of black starting capability [1]. The IGBT-based voltage source converter (VSC) has been developed recently to solve the disadvantages of LCC schemes. Among the VSC technologies, the modular multilevel converter (MMC) is a promising and competitive technology over two- or three-level VSC topologies [1]–[3]. MMC presents many advantages, such as very low harmonics, low *dv*/*dt*, modularity, simple scaling, high reliability and low switching loss, no need for series connection of power semiconductors, dc-bus capacitor elimination, etc. [4]–[8], [24]. Two submodule types could be used in the MMC: a half-bridge chopper module and a full-bridge inverter module. The half-bridge submodule (HBSM) has been used widely to reduce the number of switching devices in a module and conduction loss. The output voltage of HBSM is confined to two levels, namely, null and dc-link voltage of each module. A full-bridge submodule (FBSM) includes negative of the dc-link voltage, and the FBSM can synthesize ac output voltage even in the case that dc transmission voltage drops down to null due to dc short-circuit faults, etc. Fault ride through against the dc short-circuit fault is one of main concerns of an HVDC transmission system, especially in the case that the overhead line is used for VSC−HVDC transmission. Therefore, several topologies have been devised to ensure the safety of the MMCs against the dc short-circuit faults [9]–[11], [19].

In some applications, considerable electricity may be transmitted from a strong ac grid, which consists of several large power plants, to several distributed power loads. In this case, the compactness and black starting capability of the sending side may not be a crucial concern due to inherent large power plants at the HVDC converter site. Furthermore, the LCC-type HVDC converter would be the best option at the sending side because of its technical maturity and higher operating efficiency. On the receiving side, the compact structure and black starting capability cannot be traded if the distributed loads are at the city centers or offshore platforms. In such an application, a hybrid HVDC structure with high power LCC−HVDC converter at the source side and several medium-power VSC−HVDC converters in distributed load sides would be a promising solution. Therefore, various studies have been conducted to accommodate LCC and VSC simultaneously in an HVDC transmission system, which is called a hybrid HVDC transmission system [12]–[18], [31]. In recent years, a hybrid HVDC transmission system with LCC and MMC has become the most compatible candidate for future flexible dc transmission systems. Since this configuration would combine the merits of the LCC as a single end in a large site and MMCs as distributed ends with a compact structure, MMC could be installed in the distributed wind farms or offshore oil platforms, forming a multiterminal system [16]–[18], [31].

Several existing MMC topologies introduced in literature [17]–[21], [25]–[26] can be candidates as the VSC topology for hybrid HVDC transmission system. This paper discusses

Manuscript received February 4, 2016; revised June 16, 2016; accepted July 25, 2016. Date of publication August 5, 2016; date of current version February 11, 2017. The original version of this paper will be presented at the *IEEE Applied Power Electronics Conference and Exposition 2016*, Long Beach, CA, USA. Recommended for publication by Associate Editor J. Clare.

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Digital Object Identifier 10.1109/TPEL.2016.2598368

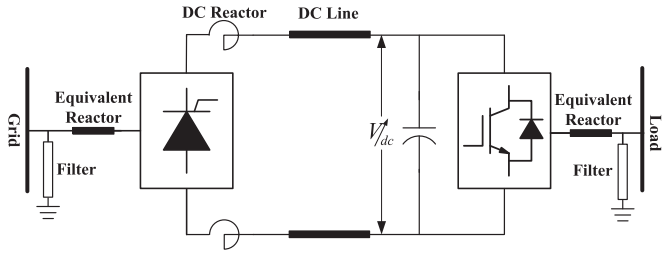

Fig. 1. Configuration diagram of a point-to-point hybrid HVDC.

the weakness of the conventional hybrid MMC structure, in which each MMC arm is a mixture of HBSM and FBSM, in balancing the submodule capacitor voltages under dc-bus voltage sliding [19]–[21], [25]. Based on the review results, a new MMC topology for point-to-point hybrid HVDC transmission system is proposed due to the cost saving, low loss, and free and quick dc-bus voltage regulation to adjust the dc transmission power in hybrid HVDC systems. In addition, it can deal with the black starting and dc fault ride through. Finally, the fully scaled computer simulation studies and experimental results with a scaled version of the proposed MMC topology in laboratory are provided to support the validity of the proposed topology.

II. Hybrid HVDC Configuration and Fundamental Principles

The basic structure of a point-to-point hybrid HVDC is shown in Fig. 1. The sending end is the conventional LCC-based HVDC system, while the receiving end is a VSC-based HVDC system. In this paper, it is assumed that the LCC−HVDC system sets the dc current as constant and the VSC−HVDC system controls the dc-bus voltage for varying and adjusting dc transmission power. The VSC on the receiving end has the turn-off capability and can maintain the voltage and frequency stability independently on the ac grid. The active and reactive power may be controlled independently by VSC. The VSC not only requires no reactive power from the ac grid but can also operate as STATCOM to compensate the reactive power dynamically. If VSC has enough capacity, the hybrid HVDC can supply active power and reactive power to improve the voltage and power angle stability when a fault occurs. On the other hand, the sending converter of the hybrid HVDC transmission system adopts the conventional current source converter based on the HVDC rectifier system with mature technology and relatively low cost. Therefore, the hybrid HVDC transmission system features both the well-developed technology and lower cost of LCC−HVDC with the desired regulating characteristics of VSC−HVDC. The VSC−HVDC system candidates can be MMCs, and several modified modular structure-based VSC high-power converters.

The conventional HBSM−MMC could not ride through the dc short-circuit fault without introducing ac or dc breakers. The solid state based dc breaker can achieve excellent dynamics with fast interruption time, but it has several disadvantages, such as high installation cost and considerable conduction loss in normal operation [27]–[30]. FBSM−MMC can make the dc-side voltage change from −1 to +1 p.u. by modulating the output voltage of the FBSM without any restrictions. Hence, it is very easy for FBSM−MMC to deal with the black starting, power flow variation, and dc short-circuit fault ride through. When dc short fault occurs, each submodule operates like a normal full-bridge and the dc-bus voltage is synthesized to zero in order to clear the short-circuit current of the dc transmission line. Since a full-bridge inverter can output bipolar voltage, the converter can generate back-EMF to regulate the ac-side current during the fault. Even though a full-bridge inverter can be modulated in the bipolar or unipolar mode, one of the lower switches should be kept normally ON and the other corresponding complementary switch kept OFF during normal operations to minimize switching loss. During normal operation, the full-bridge-inverter-based MMC operates like a conventional half-bridge-chopper-based MMC and the FBSM−MMC also causes extra loss in the normal operation mode for most of its life span.

Fig. 2(a) describes the circuit configuration of mixed HBSM and FBSM-based MMC [19]–[21]. When the MMC operates in the normal mode, the dc-bus voltage is commonly synthesized as +Vdc. When a dc short-circuit fault occurs, the dc-bus voltage should be synthesized as 0. Consequently, half of the dc-bus voltage output capability is redundant. However, it should be noted that the FBSM-based MMC can output back-EMF to regulate the ac-side current while the dc bus is synthesized from –Vdc (−1 p.u.) to +Vdc (+1 p.u.). Meanwhile, for hybrid HVDC transmission systems, the FBSM−MMC can utilize power flow reversal. In conventional and practical hybrid HVDC transmission system operation, the power flow is unidirectional from the LCC−HVDC to VSC−HVDC system. Therefore, a mixed HBSM and FBSM structure can take full advantage of the converter output voltage capability in the hybrid HVDC transmission system. During normal operating conditions, the symmetric mixed converter operates like a conventional HBSM−MMC. During dc short-circuit fault, the half-bridge choppers are bypassed and the converter operates like a full-bridge-based MMC to ride through the fault. For the hybrid HVDC transmission system, the amount of dc transmission power can be regulated and varied by controlling the dc-bus voltage from 0 to +Vdc (+1 p.u.). Contrary to the existing structure where an equal number of HBSMs and FBSMs are used in an arm of each MMC leg, a circuit shown in Fig. 2(b) can be considered as another option where one arm in a leg is consisted of fully HBSMs and the other of fully FBSMs. Based on the MMC leg configuration, the former can be called a symmetric mixed MMC and the latter an asymmetric mixed MMC. In Fig. 2(b), the upper arm is a series connection of HBSMs while the lower arm is a series connection of FBSMs as a case of two possible compositions of asymmetric mixed MMC. The number of HBSMs and FBSMs are the same in both mixed MMCs, as described in Fig. 2(a) and (b). In the proposed asymmetric mixed MMC shown in Fig. 2(b), the upper arm is composed of HBSMs and operates like as normal HBSM−MMC mode in both normal operation and fault operation. The lower arm, which is composed of FBSMs, operates like HBSM−MMC in normal mode and operates like FBSM−MMC in fault mode and also in the low power transmission mode, which have lower amount of dc power than 1 p.u. Like the symmetric mixed MMC in Fig. 2(a), the dc transmission power can be regulated and varied by controlling

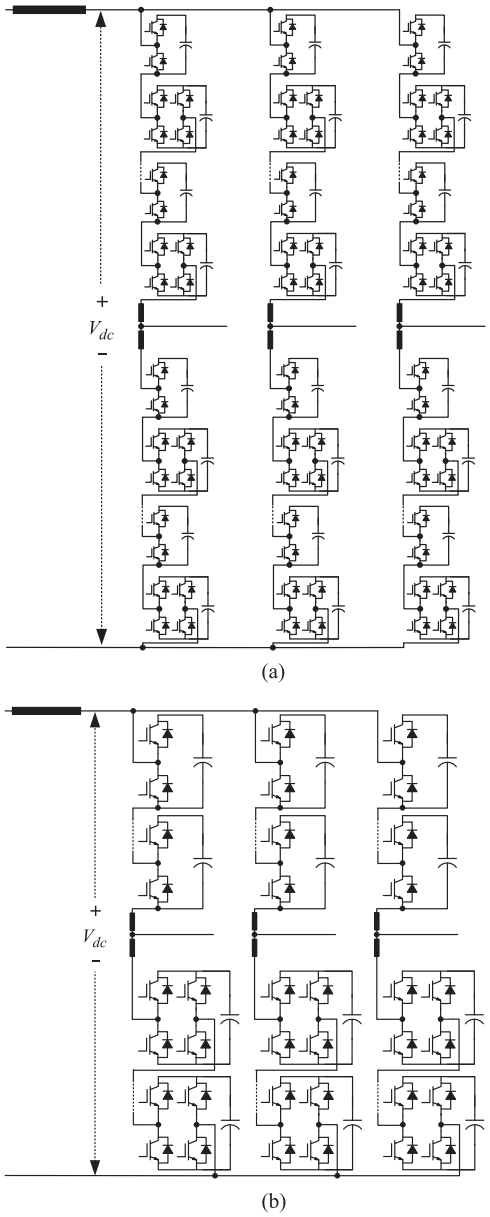

Fig. 2. Circuit diagrams of modified modular multilevel VSC converter topologies for hybrid HVDC transmission system: (a) symmetric mixed MMC and (b) proposed asymmetric mixed MMC.

the dc-bus voltage from 0 to +Vdc (+1 p.u.). The advantages and characteristics of asymmetric mixed MMC is described in subsequent sections in comparison to symmetric mixed MMC.

III. Comparisons of Symmetric and Asymmetric Mixed MMC in Hybrid HVDC Transmission System

A. Operation Principles of the Symmetric Mixed MMC

The symmetric mixed MMC modeling with the closed-loop indirect modulation [22]–[24] is shown in Fig. 3(a). The reference voltages (v^*_{xu}, v^*_{xl}) of upper and lower arms are derived by (1) and (2), respectively, where V^*_{dc} is dc-bus voltage reference, v^*_{xs} is the phase voltage reference, and *x* denotes a phase among *u*, *v*, and *w*. The leg internal voltage (v^*_{xo}) is associated with the

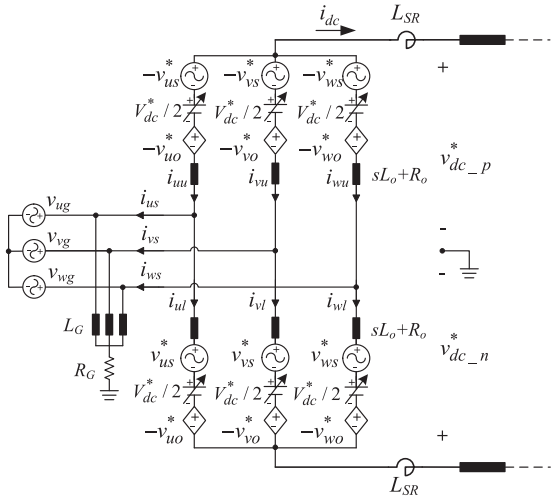

Fig. 3. Modeling of the symmetric mixed MMC.

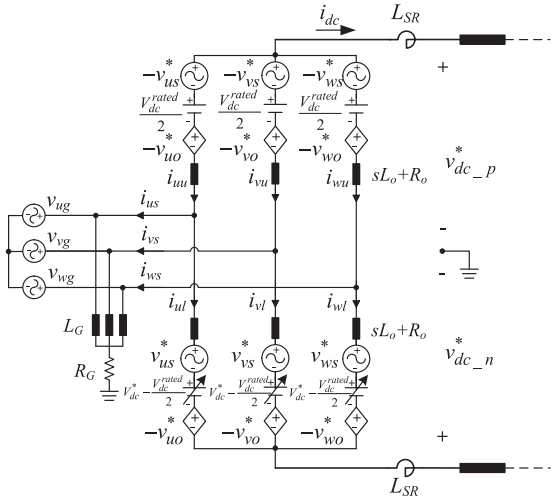

Fig. 4. Modeling of the asymmetric mixed MMC.

circulating current to balance the system [11]. The leg internal voltage can be omitted for simplification due to its negligible magnitude when compared dc-bus voltage magnitude and phase voltage reference

$$v^*_{\mathrm{xu}} = \frac{V^*_{\mathrm{dc}}}{2} - v^*_{\mathrm{xs}} - v^*_{\mathrm{xo}} \tag{1}$$

$$v^*_{\mathrm{xl}} = \frac{V^*_{\mathrm{dc}}}{2} + v^*_{\mathrm{xs}} - v^*_{\mathrm{xo}}. \tag{2}$$

Under the assumption that the number of submodules in one arm is *N*, each arm is composed of *N*/2 HBSMs and *N*/2 FBSMs. The controllable range of an arm output voltage is $-NV_{\mathrm{cap}}/2$ to NV_{cap}, assuming that the capacitor voltages of all submodule are the same as V_{cap}.

B. Operating Principles of the Asymmetric Mixed MMC

MMC modeling with the indirect modulation is shown in Fig. 4. In modeling the asymmetric mixed MMC of Fig. 4, the arm voltage references are given by (3) and (4), where $V^{\mathrm{rated}}_{\mathrm{dc}}$

means the rated dc-bus voltage in rated power transmission conditions

$$v_{xP}^{*} = \frac{V_{\mathrm{dc}}^{\mathrm{rated}}}{2} - v_{\mathrm{xs}}^{*} - v_{\mathrm{xo}}^{*} \tag{3}$$

$$v_{xN}^{*} = \left(V_{\mathrm{dc}}^{*} - \frac{V_{\mathrm{dc}}^{\mathrm{rated}}}{2}\right) + v_{\mathrm{xs}}^{*} - v_{\mathrm{xo}}^{*}. \tag{4}$$

In Figs. 2(d) and 4, the upper arm consists of N HBSMs while the lower arm is composed of N FBSMs. The capable range of an upper arm output voltage is from 0 to NV_{cap} and that of a lower arm output voltage is from $-NV_{\mathrm{cap}}$ to NV_{cap}. In addition, the upper arm voltage is always positive while the lower arm voltage can be negative as well as positive.

C. Definitions of Currents in Symmetric and Asymmetric Mixed MMC

The asymmetric MMC modeling with the closed-loop indirect modulation is shown in Fig. 4. The leg current i_{xo} is defined as the average value of the upper and lower arm currents as in (5). A circulating current of x-phase $i_{\mathrm{xo,cir}}$ is defined as (6), which is the difference between the leg current i_{xo} and the average value of the dc-bus current that equally flows into each phase. The circulating current flows only inside the converter and can transfer energy between arms without affecting ac grid current and dc-bus current when using the closed-loop indirect modulation [7], [8], [20], [22]

$$i_{\mathrm{xo}} = (i_{\mathrm{xu}} + i_{\mathrm{xl}})/2 \tag{5}$$

$$i_{\mathrm{xo,cir}} = i_{\mathrm{xo}} - i_{\mathrm{dc}}/3\cdot \tag{6}$$

The upper and lower arm currents can be deduced by (7) and (8), respectively, from using i_{xo} and $i_{\mathrm{xo,cir}}$ defined by (5) and (6) and the output phase current of i_{xs}

$$i_{\mathrm{xu}} = i_{\mathrm{xo}} + \frac{1}{2}i_{\mathrm{xs}} = \frac{1}{3}i_{\mathrm{dc}} + \frac{1}{2}i_{\mathrm{xs}} + i_{xo,\,\mathrm{cir}} \tag{7}$$

$$i_{\mathrm{xl}} = i_{\mathrm{xo}} - \frac{1}{2}i_{\mathrm{xs}} = \frac{1}{3}i_{\mathrm{dc}} - \frac{1}{2}i_{\mathrm{xs}} + i_{xo,\,\mathrm{cir}}\cdot \tag{8}$$

D. Characteristics of the Symmetric and Asymmetric Mixed MMC in DC Transmission Power Variation Mode in Hybrid HVDC System

In the conventional hybrid HVDC system, the LCC-based HVDC system is the sending end operating in the rectifier mode while the VSC-based HVDC system is the receiving end which operates as inverter mode [1], [2]. The VSC-based HVDC system controls the dc-bus voltage in the point-to-point hybrid HVDC transmission system. The system operates as the dc-bus voltage regulation mode and can be named the voltage regulator. In conventional point-to-point hybrid HVDC systems, the LCC−HVDC sets the dc-bus current as constant and VSC−HVDC determines the quantity of the dc transmission power by controlling the dc-bus voltage. Therefore, to control the dc-bus voltage, the MMC-HVDC system should have the ability to change the dc-bus voltage.

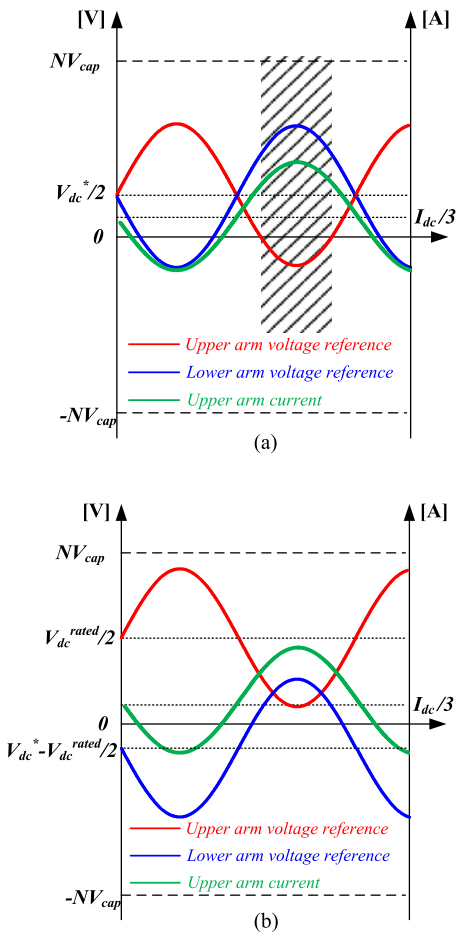

Fig. 5. Arm voltage references and arm current of (a) symmetric mixed MMC and (b) asymmetric mixed MMC when the dc-bus voltage is lower than $V_{\mathrm{dc}}^{\mathrm{rated}}$ (+1 p.u.). For example, in this figure, $V_{\mathrm{dc}}^{*} = V_{\mathrm{dc}}^{\mathrm{rated}}/2$.

The arm voltage references and the arm current of the symmetric mixed MMC while the dc voltage is lower than the rated dc-bus voltage are depicted in Fig. 5(a). In this figure, for example, $V_{\mathrm{dc}}^{*} = V_{\mathrm{dc}}^{\mathrm{rated}}/2$. Because the dc-bus voltage is lower than the rated voltage, the arm voltage references have a negative value within the region marked in Fig. 5(a). If the upper arm voltage is positive, all submodules operate like the half-bridge chopper cells by unipolar FBSMs mode. While the upper arm voltage is negative as in the marked section of Fig. 5(a), all HBSMs of the upper arm are bypassed. The FBSMs in the upper arm operate in bipolar mode and make a negative arm voltage. Assuming that the power factor is unity, the arm voltage is negative and the arm current is positive, as shown in Fig. 5(a); the capacitor voltages of upper arm FBSMs decrease, because the positive arm current and the negative arm voltage generate negative power to make capacitor voltages in FBSMs discharged. In the other hand, those of upper arm HBSMs are unchanged, because all HBSMs are bypassed. Therefore, the voltage difference between FBSMs and HBSMs in the upper arm becomes larger in the marked section. The same difference may also happen in the lower arm when the arm voltage is negative and the arm current is positive. In this case, the capacitor voltages of the lower arm FBSMs decrease, whereas those of the lower

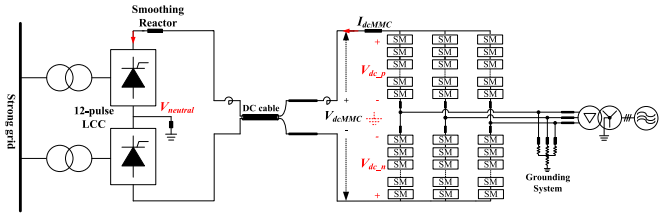

Fig. 6. Schematic diagram of the simulated hybrid HVDC transmission system with symmetric and asymmetric mixed MMCs.

arm HBSMs are unchanged. On the other hand, the voltage difference between FBSMs and HBSMs becomes smaller in the region where the arm voltage is positive, because FBSMs operate like half-bridge chopper modules and the cell balancing algorithm applies equally to all submodules. However, as the interval of negative arm voltage becomes larger and the arm current becomes larger, the imbalance of the symmetric mixed MMC in each arm becomes worse and the system finally stalls. Voltage ripple and capacitance of the submodule cells are a significant factor for MMC systems [25]. The capacitance of the FBSM cells should be larger for reducing voltage ripple, and thus it increases the cost and size of MMC. And, the exact cell capacitance design for minimizing the cost is not a simple task.

The arm voltage references and arm current in the asymmetric mixed MMC system when the dc voltage is lower than the rated dc-bus voltage can be depicted as in Fig. 5(b). In this figure, for example, $V_{\rm dc}^{*} = V_{\rm dc}^{\rm rated}/2$. As shown in (3) and (4), the dc component of the upper arm voltage reference is fixed as half of the rated dc-bus voltage. While the lower arm voltage reference determines the dc-bus voltage, the dc component of the lower arm voltage reference can vary between $-V_{\rm dc}^{\rm rated}/2$ and $V_{\rm dc}^{\rm rated}/2$. The cell-balancing algorithm applies equally to HBSMs in the upper arm and FBSMs in the lower arm. Hence, the voltage imbalance between submodules cannot occur. The comparison and verification by simulation and experimental results between the symmetric and asymmetric mixed MMC are described in Sections IV and V.

IV. Full-Scaled Simulation Results

A 400 MVA MMC model has been established by using full-scale computer simulations based on PSIM software. The schematic of the simulated system is illustrated in Fig. 6. The number of submodules per arm is 216, the rated dc-bus voltage is 400 kV, and the rated submodule capacitor voltage is 2200 V. The detailed parameters for the simulation are available in Table I.

Fig. 7 shows the simulation results of the symmetric mixed MMC when the dc-bus voltage decreases from 400 kV (1 p.u.) to 140 kV (0.35 p.u.) in 1.5 s. Furthermore, the dc current is regulated to be constant at -1500 A. Because the voltage at ac side is constant, the magnitudes of ac-side currents in the third trace of Fig. 7 are decreased after 1.5 s in proportion to reducing the dc transmission power. As shown in the fourth trace of Fig. 7, the dc components of the upper and lower arm voltage references change from 200 to 70 kV and their ac components remain unchanged due to constant ac-side voltage, which is in accordance

TABLE I
Parameters of the Simulated System

Quantity	Values
Grid line-to-line voltage (LCC side)	144 kV
Leakage inductance of transformers (LCC)	13.8 mH (0.15 p.u)
Inductance of smoothing reactor (LCC)	150 mH
Transmission line inductance	20 mH
Number of submodules per arm	216
Rated dc-bus voltage	400 kV
Rated dc-bus current	1500 A
Rated module capacitor voltage	2.2 kV
Capacitance of module capacitor	4.5 mF
Inductance of arm inductor	15.0 mH
Resistance of arm inductor	367.0 mΩ
Sampling frequency (MMC)	10.0 kHz
Rated MMC output voltage	180.5 kV

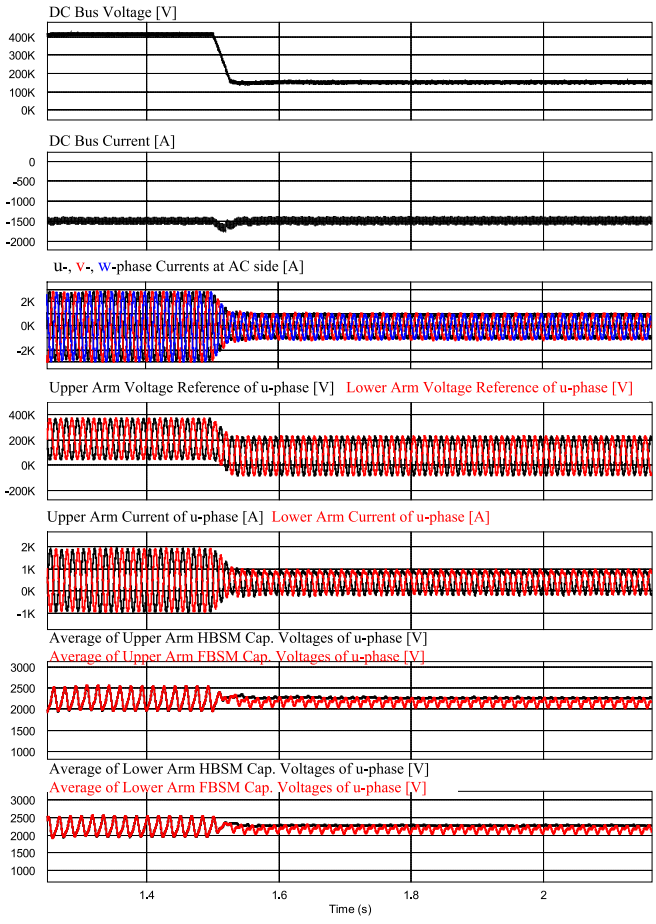

Fig. 7. Simulation results of the symmetric mixed MMC when the dc transmission power decreases from 1 to 0.35 p.u. by regulating the dc-bus voltage.

with the arm voltage references in (1) and (2). The sixth and seventh traces of Fig. 7 show the upper and lower arm HBSMs and FBSMs capacitor voltage averages of u-phase, respectively. When the dc-bus voltage is rated 400 kV, all cell voltages are well balanced. However, when the dc-bus voltage is reduced down to 140 kV, the cell voltages between HBSMs and FBSMs are unbalanced. Fig. 8 shows the magnified waveforms of the section between 1.6 and 1.7 s to confirm the disadvantages of

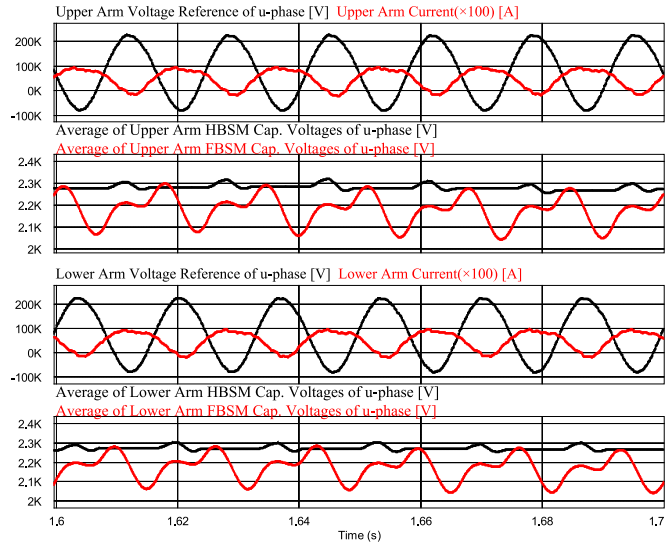

Fig. 8. Magnified waveform sections of Fig. 6 between 1.6 and 1.7 s.

the conventional symmetric mixed MMC. From the moment that arm voltage reference becomes negative, the difference between HBSM and FBSM capacitor voltages starts to increase. Because the arm current is positive when the arm voltage is negative, the capacitor voltages in FBSMs are discharged due to the negative power produced by the positive current and negative voltage. When the arm voltage is positive, the cell-balancing algorithm applies equally to all submodules because all the submodules operate like half-bridge chopper modules. Hence, the difference between HBSM and FBSM voltages decreases and the imbalance is resolved finally within one period.

Fig. 9 shows the simulation results when the dc transmission power decreases from 1 to 0.25 p.u. Because the dc-bus voltage is set down to 100 kV, the region where the arm voltage is negative is enlarged. The imbalance becomes more severe and is not resolved even in the positive arm voltage region. In other words, the discharged energy in FBSMs is larger than the charged energy during one fundamental period. Hence, the energy in FBSMs is depleted and the system is diverged. As shown in results of Fig. 9, it may have a severe effect on the stability and result in control and capacitor sizing issues of converter systems.

On the other hand, the simulation results of the asymmetric MMC system are shown in Fig. 10. Because the upper and lower arm voltage references follow (3) and (4), the upper arm voltage reference is always positive while the lower arm regulates the dc component for producing the exact dc-bus voltage reference shown by the fourth trace of the figure. From the sixth trace of Fig. 10, the submodule capacitor voltages in both upper and lower arms are well regulated below the allowable bound.

Fig. 11 shows the simulation results of upper and lower arm voltage references, upper and lower dc-bus voltages, and the neutral voltage of the pole-to-pole hybrid HVDC system, as depicted in Fig. 6, when the dc transmission power varies from 1.0 to 0.5 p.u. by controlling the dc-bus voltage as shown in first trace of Fig. 11. In the third trace of the waveform, the

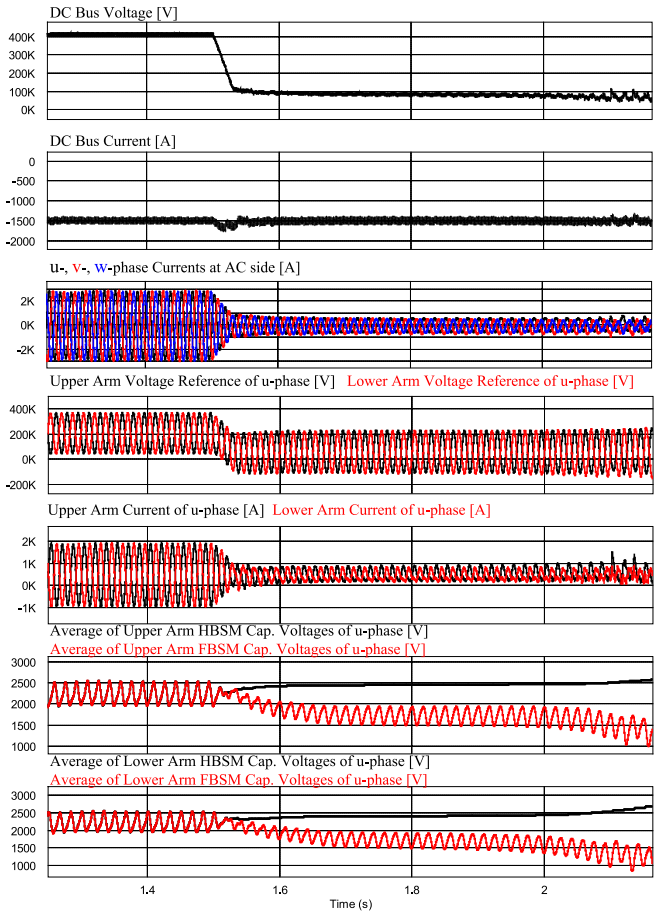

Fig. 9. Simulation results of the symmetric mixed MMC when the dc transmission power decreases from 1 to 0.25 p.u. by regulating the dc-bus voltage.

magnitudes of the potentials of upper and lower dc voltage (V_{dc_p}, V_{dc_n}) differ from each other. Because the upper and lower arm voltage references follow (3) and (4), as shown in second trace of the figure, the potential of upper dc voltage is always a constant rated value of $V_{\mathrm{dc}}^{\mathrm{rated}}/2$ while the potential of the lower dc voltage is modulated to produce the exact dc-bus voltage ($V_{\mathrm{dc\,MMC}}$) shown by the third trace of the figure. Because the potentials of upper and lower dc voltages at the LCC side follow those at the MMC side in a transmission system, the neutral voltage does not have a dc component as in the fourth trace of the figure. Therefore, it does not induce any problems such as dc bias to the grounding system or earth.

V. Experimental Results

The comparison of the symmetric and asymmetric mixed MMC and the validity of the asymmetric mixed MMC are verified by a 9 kVA reduced scale prototype hybrid HVDC system, as shown in Fig. 12(a). The number of cells in each arm N is 6, and there are a total of 36 cells used for the three-phase system. The parameters for the test setup are given in Table II. And the LCC is emulated by the full-bridge chopper in the dc link of a two-level converter, as shown in Fig. 12(b). The full-bridge chopper controls and regulates the dc-bus current to be constant for emulating the LCC system.

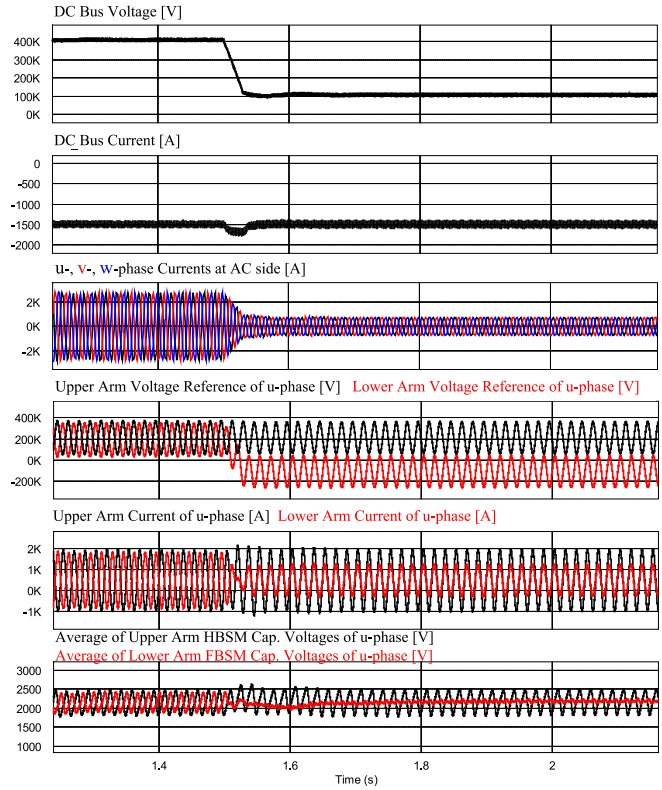

Fig. 10. Simulation results of the asymmetric mixed MMC when the dc transmission power decreases from 1 to 0.25 p.u. by regulating the dc-bus voltage.

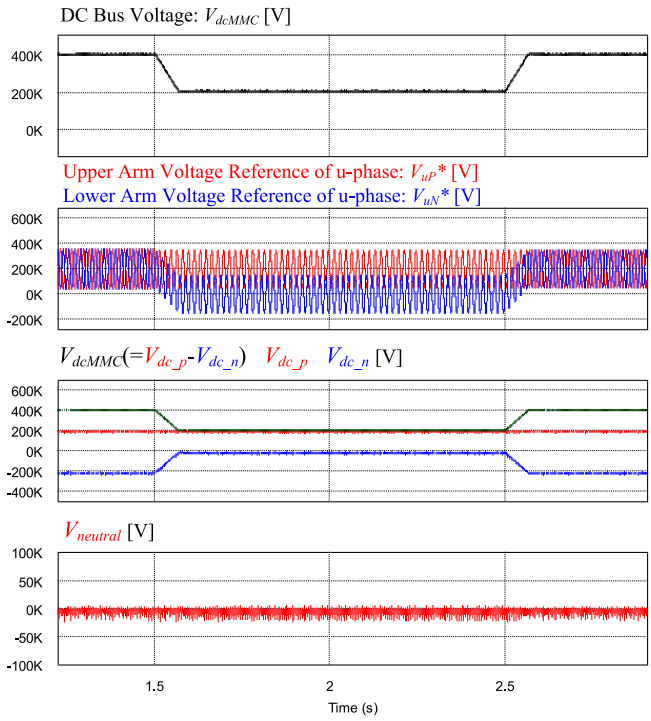

Fig. 11. Simulation results of arm voltage references, dc-bus voltages in upper and lower sides, and neutral voltage while dc transmission power varies from 1.0 to 0.5p.u.

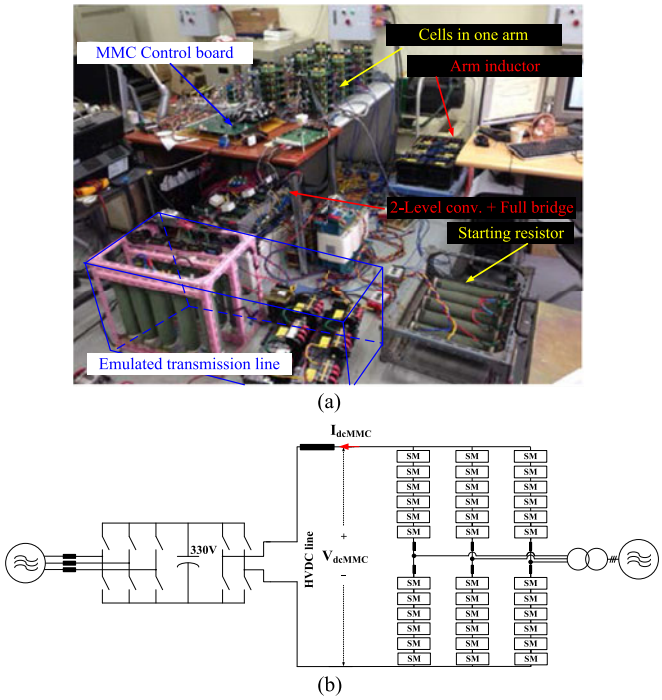

Fig. 12. Experimental setup: (a) a downscaled prototype hybrid HVDC system and (b) schematic diagram of experimental setup.

TABLE II
PARAMETERS OF PROTOTYPE HYBRID HVDC SYSTEM

Quantity	Values
Transmission line inductance	8 mH
Transmission line resistance	0.5 Ω
Number of full-bridge modules per arm	6
Rated dc-bus voltage	300 V
Rated dc-bus current	30 A
Rated module capacitor voltage	50 V
Capacitance of module capacitor	5.4 mF
Inductance of arm inductor	4 mH
Resistance of arm inductor	5 mΩ
Sampling frequency (MMC)	10.0 kHz
Rated MMC output voltage (line-to-line rms)	140 V

A. Experimental Comparisons Between the Symmetric and Asymmetric Mixed MMC

Fig. 13 shows the experimental results of the symmetric mixed MMC when the dc-bus voltage decreases from 300 V (1 p.u.) to 150 V (0.5 p.u.) and further down to 75 V (0.25 p.u.) to confirm the drawbacks of the conventional symmetric mixed MMC. The dc-bus current is set constant at −10 A. As shown in the upper and lower arm voltage references in Fig. 13, the dc components of the arm voltage references change from 150 to 75 V and further down to 37.5 V, as mentioned previously in (1) and (2). When the dc-bus voltage is the rated 300 V, all cell voltages are well balanced because both upper and lower arm voltage references are always positive, as shown in Zoom-in I of the figure. However, when the dc-bus voltages are 150 and 75 V, the cell voltages between HBSMs and FBSMs are unbalanced. From the moment when the arm voltage reference is negative,

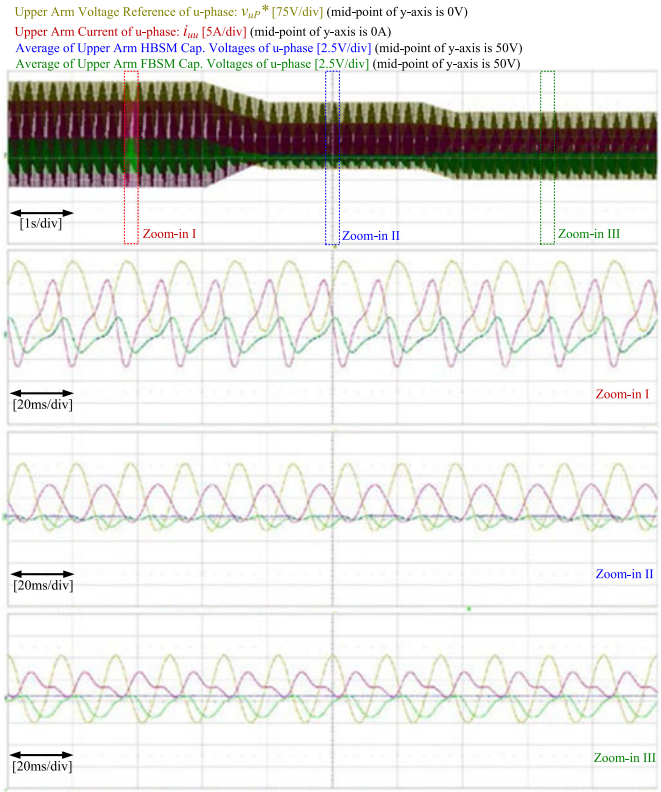

Fig. 13. Experimental results of the symmetric mixed MMC when the dc-bus voltage decreases from 300 V (1 p.u.) to 150 V (0.5 p.u.) and further to 75 V (0.25 p.u.). The dc-bus current is set constant at −10 A.

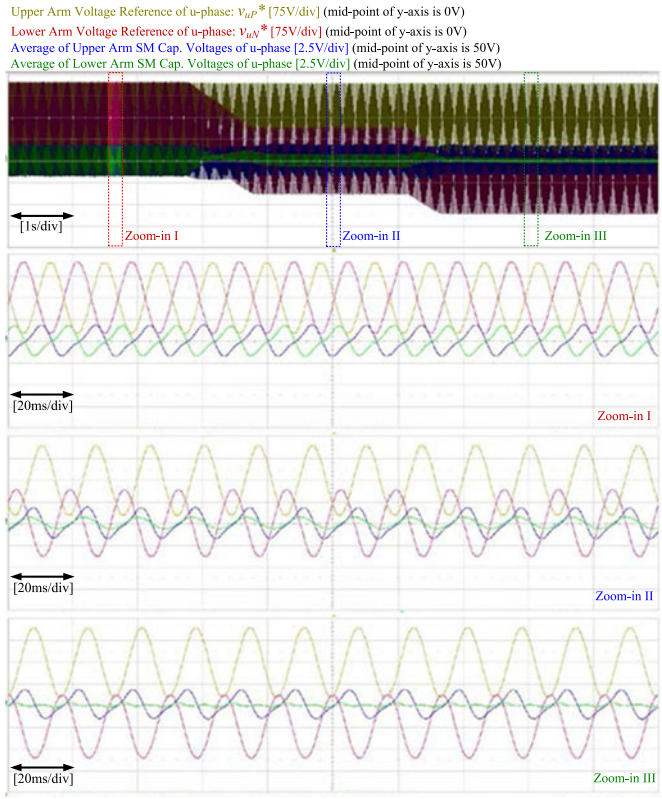

Fig. 14. Experimental results of the asymmetric mixed MMC when the dc-bus voltage transfers from 300 V (1 p.u.) to 150 V (0.5 p.u.), then down to 75 V (0.25 p.u.). The dc-bus current is set constant at −10 A.

the difference between the HBSM and FBSM capacitor voltages begins to increase. Because the arm current is positive when the arm voltage is negative, as shown in Zoom-in II of Fig. 13, the capacitor voltages in FBSMs are discharged due to the negative power produced by the positive current and negative voltage. When the dc voltage is 75 V, as shown in Zoom-in III, the imbalance is more conspicuous as the interval of negative arm voltage becomes larger.

Fig. 14 shows the experimental results of the asymmetric mixed MMC when the dc-bus voltage decreases from 300 to 150 V and further down to 75 V and the dc-bus current is set constant at −10 A, with same conditions of the experimental results of the symmetric mixed MMC. As the upper and lower arm voltage references follow (3) and (4), the upper arm voltage is modulated as positive while the lower arm voltage is modulated to produce the exact dc-bus voltage. As shown in Fig. 14, the submodule capacitor voltages in both upper and lower arms are well controlled within allowable bounds, and the results of this experiment are in agreement with the simulation results.

Figs. 15 and 16 show the experimental results when the dc-bus voltage reference of the emulated LCC system changes from 300 to 75 V and the dc current is set constant at −15 A. In Fig. 15, after the dc-bus voltage drops, the symmetric mixed MMC system becomes unstable, and the system eventually stalls. The capacitor voltages in FBSMs could not follow the reference value 50 V and the FBSM energy exhausts. However, the asymmetric mixed MMC system is stable even

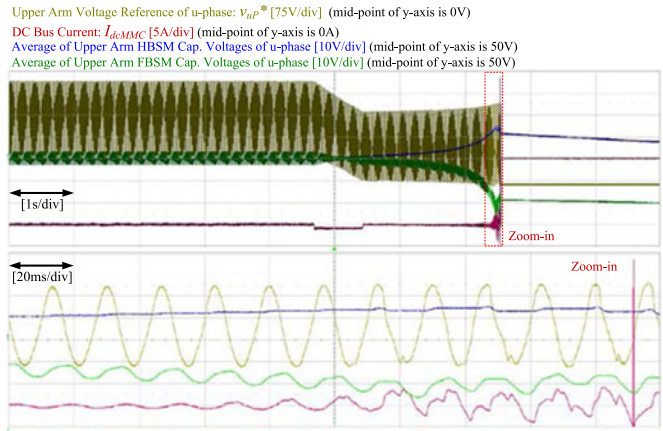

Fig. 15. Experimental results of the symmetric mixed MMC when the dc-bus voltage is changed from 300 V (1.0 p.u.) to 75 V (0.25 p.u.). The dc current is set constant at −15 A.

after dc-bus voltage changes from 300 to 75 V, as shown in Fig. 16. The reduced scale experimental results also support the validity of the asymmetric mixed MMC topology in the LCC-VSC hybrid HVDC transmission system.

B. DC Short-Circuit FRT Capability of the Asymmetric Mixed MMC

To verify the dc short-circuit FRT capability of the proposed topology, a downscaled fault experiment has been performed.

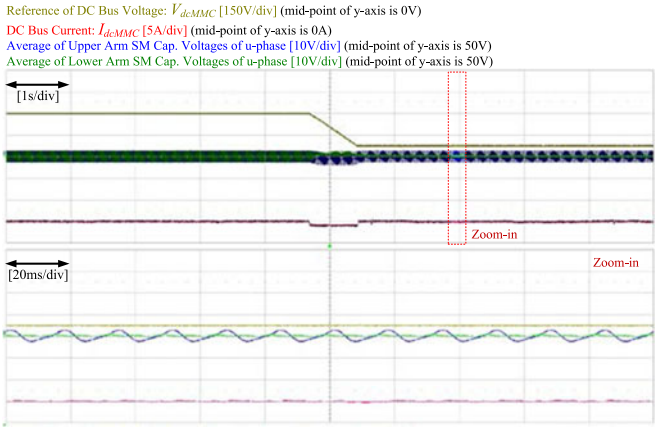

Fig. 16. Experimental results of the asymmetric mixed MMC when the dc-bus voltage is changed from 300V (1.0 p.u.) to 75V (0.25 p.u.). The dc current is set constant at −15 A.

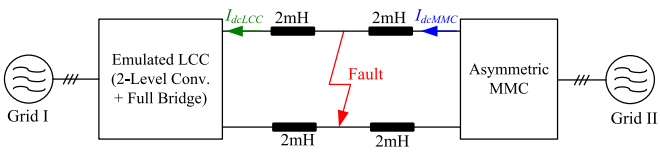

Fig. 17. Schematic diagram of the experimental setup for emulating the dc short-circuit fault.

The schematic diagram of the experimental setup for emulating the dc short-circuit fault is illustrated in Fig. 17, which is a simplified diagram of the experimental setup in Fig. 12. The parameters of the system are the same as in Table II. The fault is a dc pole-to-pole bolted short circuit, and the fault detection is conducted only by monitoring the dc-bus current. The dc short-circuit fault accident is simply identified by measuring the dc-bus current magnitude at the MMC side. The threshold of the current for detecting the fault is set to 13 A.

Figs. 18 and 19 show the experimental results of the pole-to-pole short-circuit FRT. In the prefault condition (before time point t_0), the emulated LCC transfers 3 kW of active power from Grid I to Grid II while the asymmetric MMC controls the dc-bus voltage at a constant 300 V. The pole-to-pole dc short-circuit fault occurs at time point t_0 and the dc fault accident is detected by measuring the dc fault current exceeding the threshold, 13 A. After detection, the MMC produces the appropriate dc-bus voltage regulating the dc fault current. In addition, the dc-bus voltage of the MMC is synthesized as null as soon as the fault is detected in order to extinguish the fault current, as shown in Fig. 18. In the dc fault mode, the dc component of the lower arm voltage reference is synthesized as $-V_{\mathrm{dc}}^{\mathrm{rated}}/2$, because the dc-bus voltage reference (V_{dc}^{*}) should be zero, as denoted in (4). Fig. 18 shows the upper and lower arm voltage references under the dc short-circuit fault. The dc component of the upper arm voltage reference is constant at 150 V and that of the lower arm voltage reference is −150 V, which produces the dc-bus voltage as null, as shown in Fig. 18. The fault current at the MMC side is cleared completely at t_1 through the fault current suppression mode while the emulated LCC normally controls the dc-bus current at a constant −10 A. The dc short-circuit fault

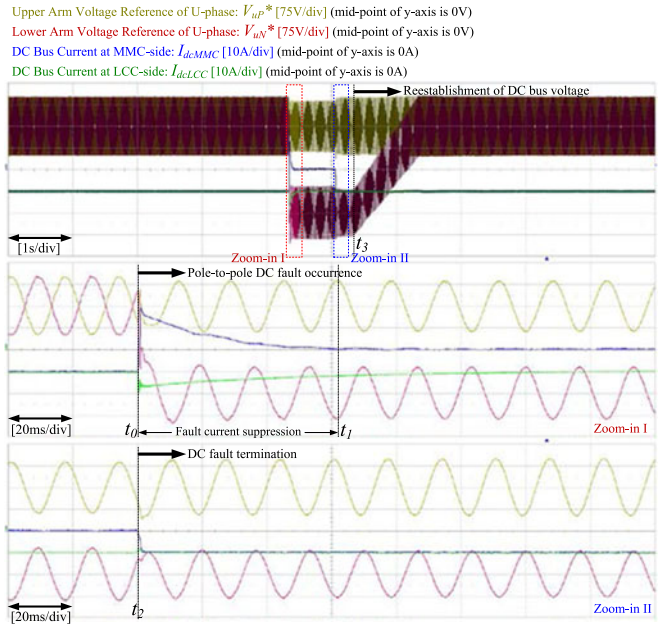

Fig. 18. Experimental results of FRT against the pole-to-pole short circuit: the synthesis of the upper and lower arm references in u-phase under dc short-circuit fault, dc-bus current at the MMC side, and dc-bus current at the LCC side.

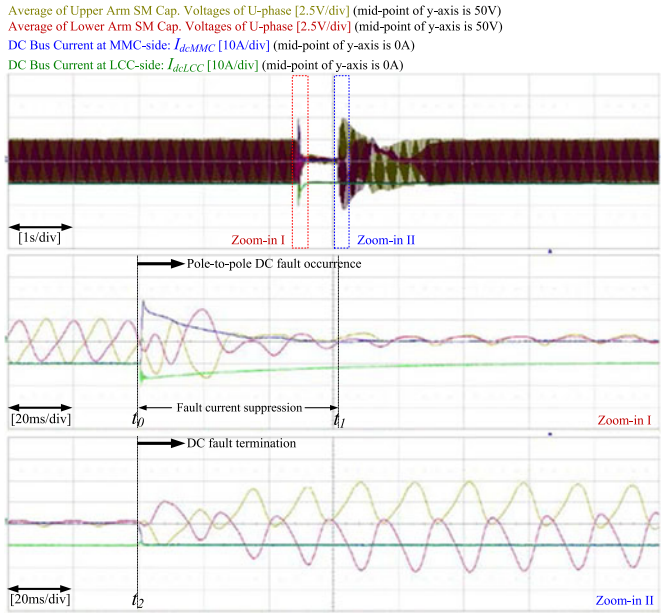

Fig. 19. Experimental results of FRT against the pole-to-pole short circuit: average values of upper and lower arm submodule capacitor voltages of u-phase, dc-bus current at the MMC side, and dc-bus current at the LCC side.

is terminated, and the transmission line is restored to normal at time point t_2. Additionally, after dc fault termination, the dc-bus current flows from the LCC side to the MMC side, as shown in the third trace of Fig. 18. Because the MMC produces the dc-bus voltage as null, the transmitted power between Grid I and Grid II is zero. To resume the normal power transmission operation, the dc-bus voltage is recovered and reestablished to the rated value after t_3 in the first trace of Fig. 18.

Fig. 19 shows the average values of upper and lower arm submodule capacitor voltages of u-phase. After the dc fault, the

inrush current flows to the MMC abruptly and the submodule capacitor voltages fluctuate, as shown in the second trace of Fig. 19. The dc-bus current at the MMC side is cleared through the fault current suppression mode while the submodule capacitor voltages have little or no fluctuated component. After the dc fault finishes at t_2, the dc current from the LCC side begins to flow into the MMC system. As shown in the third trace of Fig. 19, the pulsations of the capacitor voltages increased instantaneously after t_2. However, the maximum amplitude of the capacitor voltage ripple is around 5 V, or 10% of its rated value, 50 V. Therefore, the submodule capacitor voltage is successfully regulated within allowable bounds during the FRT period.

The experimental results demonstrated the dc short-circuit FRT capability of the asymmetric mixed MMC topology. Although the asymmetric MMC is subjected to one of the most severe types of dc short-circuit faults, it does not suffer from overcurrent and overvoltage and can be restored to normal conditions by its FRT capability.

VI. Conclusion

In this paper, an asymmetric mixed MMC topology has been introduced with characteristics like reduced system cost, reduced operational loss, and FRT capability against dc short-circuit fault, which is the same as conventional symmetric mixed MMC. In contrast to the conventional symmetric mixed MMC, the asymmetric mixed MMC for hybrid HVDC transmission system can regulate the dc-bus voltage freely without uncontrollable submodule capacitor voltages. The drawbacks of the conventional symmetric mixed MMC for hybrid HVDC have been identified. In addition, the validity of the asymmetric MMC system under dc-bus voltage sliding and dc short-circuit FRT capability have been verified by simulation studies with a 600 MVA full-scale model and experimental results with a 9 kVA downscaled version.

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