A Matrix-Based Nonisolated Three-Phase AC–DC Rectifier With Large Step-Down Voltage Gain

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***Abstract*—This paper presents a matrix-based nonisolated three-phase ac–dc converter with a current-doubler rectifier (CDR) circuit. Buck-type rectifiers are normally used for step-down ac-to-dc conversion. However, for three-phase buck rectifiers, the lower bound of rectified dc voltage is limited as the converter is severely underutilized by operating at lower modulation index. Moreover, at lower modulation index, the rms values of current increases contributing to higher conduction losses. However, by using a matrix (3×1) topology followed by a CDR, the desired dc output voltage can be reduced by half. The matrix topology directly converts three-phase line frequency ac voltages into intermediate high-frequency ac voltage which is subsequently, rectified using a CDR to obtain the required output dc voltage. A modified space vector modulation based modulation scheme especially suited for the proposed converter is presented for superior input power quality with reduced power loss. Comprehensive analysis and design of the proposed converter is carried out followed by simulation and laboratory-based experimental tests. Subsequently, the loss analysis of the proposed converter is carried out and a comparative evaluation of the proposed converter with the traditional six-switch buck rectifier is provided to demonstrate the suitability of the proposed converter for large step-down voltage gain. Digital implementation of the proposed modulation scheme is carried out at 40-kHz switching frequency. A hardware prototype of 500 W is developed to validate the theoretical and simulation results.**

***Index Terms*—AC–DC converter, aircraft systems, buck rectifiers, matrix converter, rectifier, space vector modulation (SVM), total harmonic distortion (THD).**

I. Introduction

In industries, ac–dc rectifiers are widely used as front-end converters. There are various applications including telecommunication, electrical-vehicle, and aircraft systems, etc., where high-performance ac–dc rectifiers are essential to meet the ever increasing demand of power-weight ratio [1]–[4]. Moreover, stringent requirements of total harmonic distortion (THD) and power factor (PF) for certain applications such as aircraft system emphasize the design of ac–dc rectifier with high input power quality [5], [6].

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Basically, two types of topologies are possible for ac–dc conversion, a boost-type rectifier and a buck-type rectifier. For applications, where lower output dc voltage is required, buck type of rectifiers are used as the boost-type structure has limitation over minimum output dc voltage. Moreover, buck-type topologies have other benefits over boost type including direct startup and the overcurrent protection in case of an output short circuit [7]. Therefore, the buck-type rectifiers are of high interest for applications such as telecommunication, power supplies for process technology, and More Electric Aircraft systems [8].

The three-phase buck rectifier with six switches is a conventional topology and has been widely discussed in the literature [9]–[13]. In [14], an ac/dc matrix converter with an optimized modulation strategy is presented for vehicle-to-grid application. A three-phase discontinuous mode buck rectifier has been presented in [15], where input power quality is improved by modifying the traditional control algorithm and modulation scheme.The comprehensive design of a thee-phase three-switch buck-type pulse width modulation (PWM) rectifier is carried out in [7].

The zero-current-switched buck rectifier circuits are presented in [16] and [17], which use an axillary circuit to achieve zero-voltage switching (ZVS) with unity PF. The output of the buck rectifier is controlled by varying the modulation index, m (also known as modulation depth) which essentially controls the pulse width of the gating signal to the switching devices. In theory, the output voltage of a buck rectifier can be varied from $\frac{3}{2}V_m$ to 0 by varying the modulation index, m from 1 to 0 where, V_m is the peak value of input phase voltage. However, if the desired regulated output dc voltage is lower than $\frac{3}{4}V_m$, the converter always has to operate at the modulation index, $m \leq 0.5$ which underutilizes the converter capability. Moreover, operation of the converter at lower value of m increases the THD of input phase currents and the switch rms current contributing to reduced input power quality and increased switch conduction loss, respectively.

For large step-down voltage gain, the matrix-based ac–dc converter with an isolation transformer can be used [18]–[20]. By changing the turns-ratio of the transformer, the desired output dc voltage can be obtained. However, the applications where electrical isolation is not mandatory, the use of transformer reduces the power density with additional power loss. Moreover, the leakage inductance of the transformer presents additional current commutation problems resulting in increased switch voltage stress and duty cycle loss [19], [20].

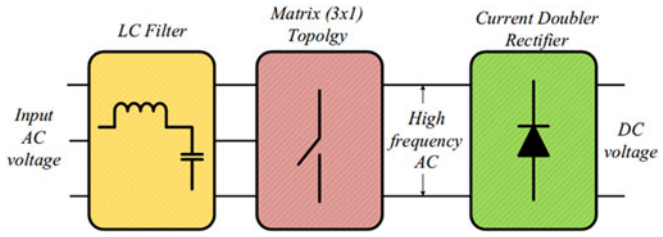

Fig. 1. Block diagram of the proposed matrix-based ac–dc converter.

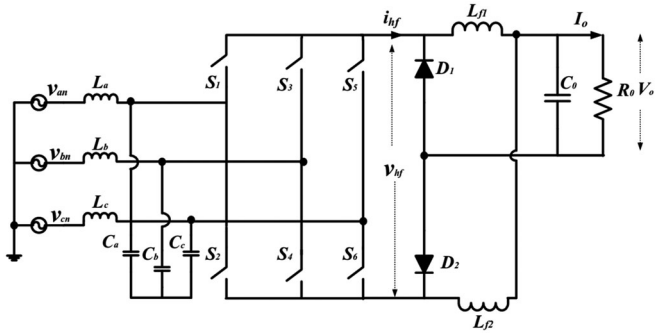

Fig. 2. Circuit schematic of the proposed three-phase ac–dc rectifier. Each matrix switch is formed by connecting two back-to-back MOSFETs.

The current-doubler rectifier (CDR) circuits [21], [22] are antithesis of the voltage-doubler rectifier (VDR) circuits. Unlike VDR, the CDR reduces the rectified output dc voltage by half. By removing the transformer from the traditional matrix-based three-phase ac–dc converter and replacing the diode bridge rectifier using a CDR, a three-phase nonisolated buck rectifier with twice step-down voltage gain can be realized. Since this converter does not have issues of the leakage inductance due to the absence of high-frequency transformer, the traditional switching scheme based on SVM can be modified to reduce switching complexity and to improve power conversion efficiency. Moreover, there are several other benefits of combining the matrix topology with the CDR such as reduction in switch rms current, which has never been presented in the literature.

Therefore, in this paper a nonisolated matrix-based three-phase ac–dc rectifier is proposed, which provides half of the voltage gain achieved by the conventional three-phase buck-type rectifiers without compromising the input power quality and power conversion efficiency. The block diagram of the proposed converter is shown in Fig. 1. The input three-phase voltage is first filtered using an input LC filter followed by a matrix (3×1) topology. The matrix topology converts the three-phase line frequency ac voltages into an intermediate high-frequency ac voltage. The high-frequency ac voltage is then fed to a CDR circuit which in turn, rectifies it to the output dc voltage. The intermediate high-frequency ac voltage generated by the matrix topology allows the use of CDR circuit which essentially reduces the output dc voltage by half. Moreover, the high-frequency ac voltage reduces the passive filter elements of (L and C) of the current doubler. A SVM-based modulation scheme is proposed for the matrix converter for improved input power quality.

In summary, the novelty and contributions of this paper are as follows.

1) An idea of combining the matrix (3×1) with a CDR circuit for large step-down nonisolated buck rectification is proposed. Subsequently, a modified-SVM-based modulation scheme is presented which provides simpler implementation and improves overall power conversion efficiency.
2) The proposed SVM-based modulation scheme requires single control for each of the matrix switches unlike the proposed two independent control for each matrix switch in [23] and therefore, does not need switch body diode conduction and therefore, facilitates reduced number of isolated gate drivers (six for six matrix switches), and no body diode loss (conduction loss and reverse recovery loss). Moreover, the switching sequence is arranged symmetrically to provide symmetrical bipolar high-frequency ac voltage at the matrix output unlike [20].
3) Comprehensive steady-state analysis and design equations are presented based on the modes of operation which are further validated using both simulation and experimental tests.
4) The comprehensive loss analysis of the proposed converter is carried out which is subsequently verified by experimental test results.
5) A comparative evaluation of the proposed converter with the traditional six-switch buck rectifier [24] is presented to demonstrate the benefits of the proposed converter.

The paper is organized as follows. Section II provides the details of the proposed topology, the proposed modulation scheme, and the modes of operation. In Section III, steady-state analysis and design of the converter is carried out. In Section IV, the validity of theoretical analysis and design is proven through digital simulation. In Section V, the loss analysis of the proposed converter is carried out. Subsequently, a comparative evaluation of the proposed converter with the traditional six-switch buck rectifier is presented. Section VI presents experimental results of the developed hardware prototype. Section VII provides the conclusion.

II. Topology, Modulation Scheme, and Principle of Operation

In this section, the topology of matrix-based nonisolated converter is discussed. Subsequently, the modulation scheme for the proposed converter is derived based on SVM. The different modes of operation of the converter is discussed in details which is used for analysis and designed in Section III. Fig. 2 shows the circuit schematic of the proposed matrix-based three-phase ac–dc converter. It consists of a three-phase ac input ($v_{\rm an}$, v_{bn}, v_{cn}), an input filter with inductors (L_a, L_b, L_c) and a capacitor (C_a, C_b, C_c), six bidirectional switches (S_1–S_6), two diodes D_1 and D_2, two output filter inductors L_{f1} and L_{f2}, output capacitor C_o, and a load resistor R_o.

A. Assumptions

The following assumptions have been taken for deriving the switching scheme of the proposed ac–dc converter.

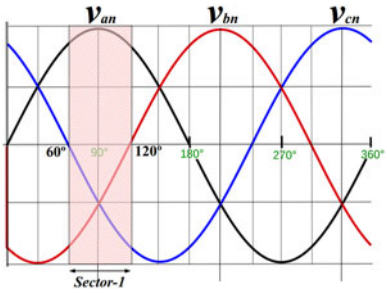

Fig. 3. Operation of the converter is divided into six similar sectors. Sector-1 ranges from $\theta = \frac{\pi}{3}$ to $\frac{2\pi}{3}$.

1) The filter capacitor voltages are of purely sinusoidal in shape and in phase with the three-phase input ac voltages which are given by

$$v_{\rm an} = V_m \sin(\theta); v_{bn} = V_m \sin\left(\theta - \frac{2\pi}{3}\right); \quad v_{cn} = V_m \sin\left(\theta + \frac{2\pi}{3}\right) \qquad (1)$$

where V_m is the peak of the three-phase input voltages and θ is in radians.
2) The reactive current due to the filter capacitors are neglected.
3) The output dc current I_o is assumed to be constant and ripple free. Consequently, the current in each of the filter inductors, L_{f1} and L_{f2} is assumed to be $\frac{I_0}{2}$.
4) The dead time, t_d between the two adjacent matrix switches which is required to avoid short circuiting of the input filter capacitors is assumed to be zero.

B. Modulation Scheme

To derive the switching signals for the matrix converter, the three-phase input ac voltages are divided into six equal sectors. During each sector, the current vector, $I_{\rm ref}$ can be synthesized by the SVM method. For sector-1, $I_{\rm ref}$ can be written as

$$I_{\rm ref} T_s = i_{ab} t_\alpha + i_{\rm ac} t_\beta \qquad (2)$$

where t_α and t_β are the time for which i_{ab} and $i_{\rm ac}$ flow through the circuit, respectively, for one switching cycle. If T_s is the time period of one switching cycle, then the duration t_α and t_β are derived as

$$t_\alpha = mT_s \sin\left(\frac{\pi}{3} - \theta\right) \qquad (3)$$

$$t_\beta = mT_s \sin(\theta) \qquad (4)$$

$$t_0 = T_s - t_\alpha - t_\beta. \qquad (5)$$

For sector-1, θ varies from $\frac{\pi}{3}$ radian to $\frac{2\pi}{3}$ radian as shown in Fig. 6. The time interval, t_o represents the zero period for the matrix converter. During this interval, the output voltage of the matrix converter remains zero. Once the duration, t_α, t_β, and t_o are calculated, the next step is to arrange the time durations in a particular sequence to generate symmetrical bipolar high-frequency ac output voltage. In the proposed modulation scheme, the switching period, T_s is divided into two equal parts. In the first half, the positive voltage is generated whereas in the second half, the negative voltage is generated. However, the sum of the each time duration, t_α, t_β, and t_0 are distributed in such a way that they remain unchanged and satisfy (2).

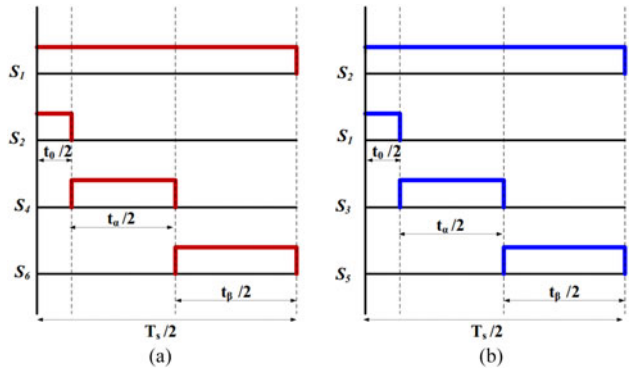

Fig. 4. Proposed modulation scheme. (a) Switching signal during positive half cycle. (b) Switching signal during negative half cycle.

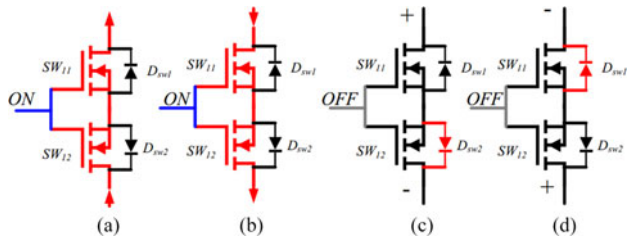

Fig. 5. Different states of the matrix switch, S_1. (a) Switch S_1 is ON and current is flowing in the +ve direction. (b) Switch S_1 is ON and current is flowing in the − ve direction. (c) Switch S_1 is OFF and +ve voltage appears across the switch. (d) Switch S_1 is OFF and − ve voltage appears across the switch.

Fig. 4 shows the operation of the proposed modulation scheme. The switching cycle, T_s is divided into two equal parts. In the first half, the states of the matrix switches are shown in Fig. 4(a). During zero period, switch S_1 and S_2 are ON whereas, switches S_1 and S_4 are ON for $\frac{t_\alpha}{2}$ duration. In the end, switches S_1 and S_6 are ON for $\frac{t_\beta}{2}$ duration. Similarly, the switch states in the next half of the cycle are shown in Fig. 4(b).

Each of the matrix switches, S_1–S_6 is realized by connecting two back-to-back MOSFETs. This particular arrangement of the MOSFETs in the matrix switch facilitates four quadrant operation. In the proposed modulation scheme, the two back-to-back connected MOSFETs are controlled with a single control signal which is different from the traditional SVM-based modulation scheme where both MOSFETs are independently controlled. The single control for each of the matrix switch requires only six isolated gate drivers for the matrix operation. When control signal is ON, both of the MOSFETs are ON and therefore, the current always flow through the MOSFET's channel whereas when control signal is OFF, both of the MOSFETs are in OFF state and no current flows through the matrix switch. The four state of the switch in the proposed switching scheme is shown in Fig. 5.

Fig. 5(a) and (b) shows the state of the matrix switch S_1 when it is in ON state. The current flows through the channel of the MOSFETs in both conditions. Fig. 5(c) and (d) shows the state of the matrix switch when it is in OFF state. No current flows through the switch S_1. However, one of the body diodes of the

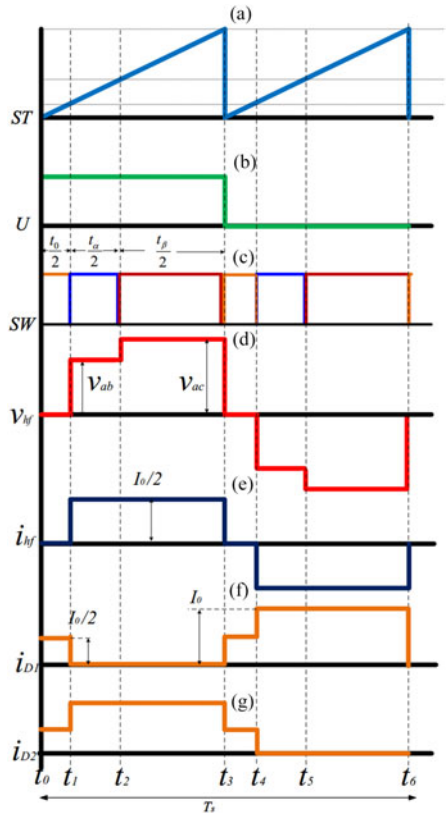

Fig. 6. Theoretical modes of operation of the proposed ac–dc converter.

MOSFETs is forward biased due to the voltage across the switch S_1. As shown in Fig. 5(c), the body diode D_{sw2} is forward biased whereas in Fig. 5(d), the body diode D_{sw1} is forward biased.

It is worth mentioning that there is no state of the matrix switch where body diodes of the MOSFETs conduct. Therefore, in the proposed modulation scheme, losses due to body diodes are eliminated. Moreover, as one of the body diodes of the matrix switch remains forward biased in OFF state, it turns ON with zero voltage resulting in ZVS of the MOSFET. For example, in Fig. 5(c), the MOSFET, SW_{12} turns ON with ZVS. Therefore, the proposed switching scheme reduces both the switch conduction loss and the switching loss.

C. Modes of Operation

The complete modes of operation of the proposed converter can be divided into six modes. For the first 3 modes (mode-1 to mode-3), the inversion signal $U = 1$, whereas for next 3 modes (mode-4 to mode-6), the inversion signal $U = 0$.

Mode-1 ($t_0 \leq t \leq t_1$): During this mode of operation, switches S_1 and S_2 are ON resulting in zero output voltage ($v_{hf} = 0$) of the matrix converter. No power transfer happens during this mode of the operation. The diodes D_1 and D_2 conduct during this mode of operation. The output current I_o is shared equally in both diodes, D_1 and D_2 during this mode of operation. The governing equation during this mode of operation is given as

$$\begin{aligned} v_{hf}(t-t_o) &= 0; i_{hf}(t-t_o) = 0; i_{D1}(t-t_o) \\ &= i_{D2}(t-t_o) = \frac{I_o}{2}. \end{aligned} \tag{6}$$

Mode-2 ($t_1 \leq t \leq t_2$): During this mode of operation, switches S_1 and S_4 are turned ON resulting in v_{ab} at the matrix output. The diodes D_1 remains OFF during this mode. The diode D_2 shares all the output current. The governing equation during this mode of operation is given as

$$\begin{aligned} v_{hf}(t-t_1) &= v_{ab}; i_{hf}(t-t_1) = \frac{I_o}{2}; i_{D1}(t-t_1) \\ &= 0; i_{D2}(t-t_1) = I_o. \end{aligned} \tag{7}$$

Mode-3 ($t_2 \leq t \leq t_3$): During this mode of operation, switches S_1 and S_6 are turned ON resulting in $v_{\rm ac}$ at the matrix output. The diodes D_1 remains OFF during this mode. The diode D_2 shares all the output current. The governing equation during this mode of operation is given as

$$\begin{aligned} v_{hf}(t-t_2) &= v_{\rm ac}; i_{hf}(t-t_2) = \frac{I_o}{2}; i_{D1}(t-t_2) \\ &= 0; i_{D2}(t-t_2) = I_o. \end{aligned} \tag{8}$$

Mode-4 ($t_3 \leq t \leq t_4$): This mode is exactly similar to mode-1. During this mode of operation, switches S_1 and S_2 are ON resulting in zero output voltage ($v_{hf} = 0$) of the matrix converter. No power transfer happens from source to load during this mode of the operation. The output current I_o is shared equally in both diodes D_1 and D_2. The governing equation during this mode of operation is given as

$$\begin{aligned} v_{hf}(t-t_3) &= 0; i_{hf}(t-t_3) = 0; i_{D1}(t-t_3) \\ &= i_{D2}(t-t_3) = \frac{I_o}{2}. \end{aligned} \tag{9}$$

Mode-5 ($t_4 \leq t \leq t_5$): During this mode of operation, switches S_2 and S_3 are turned ON resulting in $-v_{ab}$ at the matrix output. The diodes D_2 remains OFF during this mode. The diode D_1 shares all the output current. The governing equation during this mode of operation is given as

$$\begin{aligned} v_{hf}(t-t_4) &= -v_{ab}; i_{hf}(t-t_4) = \frac{I_o}{2}; i_{D1}(t-t_4) \\ &= I_o; i_{D2}(t-t_4) = 0. \end{aligned} \tag{10}$$

Mode-6 ($t_5 \leq t \leq t_6$): During this mode of operation, switches S_2 and S_5 are turned ON resulting in $-v_{\rm ac}$ at the matrix output. The diodes D_2 remains OFF during this mode. The diode D_1 shares all the output current. The governing equation during this mode of operation is given as

$$\begin{aligned} v_{hf}(t-t_5) &= -v_{\rm ac}; i_{hf}(t-t_5) = \frac{I_o}{2}; i_{D1}(t-t_5) \\ &= I_o; i_{D2}(t-t_5) = I_o. \end{aligned} \tag{11}$$

The end of mode-6 completes the one switching cycle. Mode similar to mode-1 starts after the end of mode-6 and hence, generates symmetrical bipolar high-frequency ac at the matrix output.

TABLE I
VOLTAGE ACROSS CDR INDUCTOR, L_{f1} DURING ONE SWITCHING CYCLE, Ts

Duration	Voltage across inductor, L_{f1}
t_0–t_1	$-V_o$
t_1–t_2	$v_{ab}-V_o$
t_2–t_3	$v_{\rm ac}-V_o$
t_3–t_4	$-V_o$
t_4–t_5	$-V_o$
t_5–t_6	$-V_o$

TABLE II
CURRENT IN CDR DIODE, D_2 DURING ONE SWITCHING CYCLE, T_s

Duration	Current in diode, D_1, D_2
t_0–t_1	$\frac{I_o}{2}$
t_1–t_2	I_o
t_2–t_3	I_o
t_3–t_4	$\frac{I_o}{2}$
t_4–t_5	0
t_5–t_6	0

III. STEADY-STATE ANALYSIS AND DESIGN

In this section, the steady-state analysis of the converter is carried out based on the modes of operation as described in Section II. Subsequently, design equations such as voltage and current stresses are derived for the proposed converter.

A. Voltage Gain of the Converter

The derivation of voltage gain is based on the assumption that output current, I_o is constant and ripple free throughout the switching cycle (T_s). By volt–time balance across one of the filter inductors, voltage gain of the converter can be derived. Based on the modes of operation shown in Fig. 6, the voltage across inductor is shown in Table I.

The volt–time balance across inductor L_{f1} results in

$$-V_o\frac{t_o}{2}+(v_{ab}-V_o)\frac{t_\alpha}{2}+(v_{\rm ac}-V_o)\frac{t_\beta}{2}-V_o\left(\frac{T_s}{2}\right)=0 \tag{12}$$

where T_s is defined as

$$T_s=t_o+t_\alpha+t_\beta. \tag{13}$$

Simplifying (15) and (16) result in

$$2V_oT_s=v_{ab}t_\alpha+v_{\rm ac}t_\beta. \tag{14}$$

From (1) to (7), the above equation can be further simplified to

$$V_o=\frac{3}{4}mV_m \tag{15}$$

where V_m is the peak voltage of the input ac phase voltage. By controlling the value of the modulation index m the output voltage, V_o is controlled.

B. Voltage Stresses

In this section, the voltage stresses on the active and passive devices are determined. The maximum line-to-line input voltage $V_{ll,\max}$ is

$$V_{ll,\max}=\sqrt{3}V_m. \tag{16}$$

Each of the matrix switches is realized by connecting two MOSFETs back-to-back as shown in Fig. 4. It is to be noted that maximum voltage across each of the switches is $\sqrt{3}V_m$. The voltage across one of the two switches of the matrix switch is zero as it is forward biased.

Similarly, the maximum voltage stress across diodes D_1 and D_2 is the maximum value of high-frequency ac output of the matrix converter, v_{hf} which is $\sqrt{3}V_m$. During mode-1 and mode-4, the voltage across both the diodes is zero (assuming zero forward voltage drop across diodes).

The filter inductors L_{f1} and L_{f2} and filter capacitor C_o are selected for output voltage V_o. A sufficient amount of margin should be considered while selecting the active and passive devices.

C. Current Stresses

The calculation of current stress is based on the assumption that load current I_o is constant and ripple free and switching frequency f_s is much higher than the input voltage frequency f_i. The current stress in each of the semiconductor devices is evaluated.

1) Current Stresses in the Matrix Switches: The average and rms values of current in the matrix switch are calculated which are critical for selecting the suitable switch for a given specification. Both average and rms values are calculated for half of the mains period ($\theta=0^\circ$ to 180°). For a given load current I_o the amplitude of current in the matrix switches is $\frac{I_o}{2}$. The average current in the switches is given by

$$i_{SW,\rm avg}=\frac{mI_o}{4\pi}\int_0^{\frac{\pi}{3}}\sin(\theta)d\theta+\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}}\left(\sin\left(\frac{2\pi}{3}-\theta\right)+\sin\left(\theta+\frac{\pi}{3}\right)\right)d\theta+\int_{\frac{2\pi}{3}}^{\pi}\sin(\pi-\theta)d\theta \tag{17}$$

which is simplified to

$$i_{SW,\rm avg}=\frac{I_o}{2\pi}m. \tag{18}$$

Similarly, the rms current in the switches can be calculated which is given by

$$i_{SW,\rm rms}=\sqrt{\frac{1}{\pi}\frac{mI_o^2}{8}\left(\int_0^{\frac{\pi}{3}}\sin(\theta)d\theta+\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}}\sin\left(\frac{2\pi}{3}-\theta\right)+H\right)} \tag{19}$$

where $H=\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}}\sin(\theta-\frac{\pi}{3})d\theta+\int_{\frac{2\pi}{3}}^{\pi}\sin(\pi-\theta)d\theta$.

Simplifying the (22) results in

$$i_{SW,\rm rms}=\frac{I_o}{2}\sqrt{\frac{m}{\pi}}. \tag{20}$$

It is important to note here that the use of CDR circuit in the output side reduces the current amplitude in the switches by half. As conduction loss in the switches is directly proportional to the

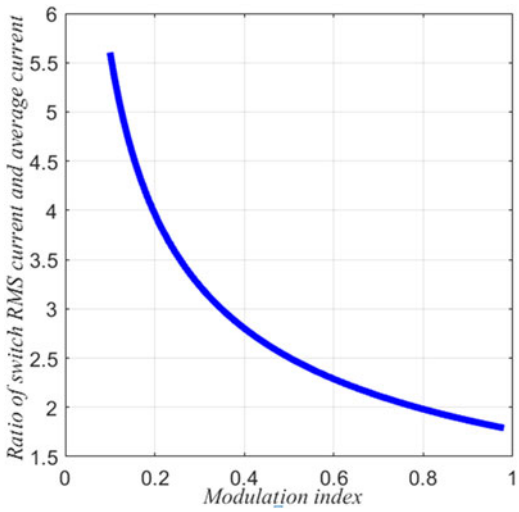

Fig. 7. Form factor of the matrix switch current.

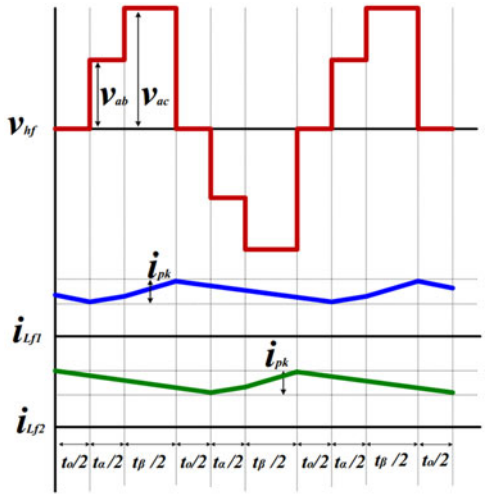

Fig. 8. Output inductor current ripple, i_{Lf1} and i_{Lf2}.

TABLE III
SPECIFICATION OF THE EXAMPLE CONVERTER

Parameters	Values
Input Voltage, v_{abc}	115 V_{ac} (rms)
Output Voltage, V_o	90 Vdc
Switching Frequency, f_s	40 kHz
Output Power, P_o	500 W

switch rms current, there is significant reduction in conduction loss for the matrix switches.

2) Form Factor of Matrix Switch Current: The form factor is defined as the ratio of rms current and average current. The lower form factor of current indicated lower loss for a given output power. The form factor, k_f for the matrix switch current is given by

$$k_f = \sqrt{\frac{\pi}{m}}. \tag{21}$$

Fig. 7 shows that for a given average current, switch rms current increases with lower modulation index which contributes to more switch losses. Therefore, it is not preferred to design the operating point of the converter at low modulation index.

3) Current Stress in the Diodes: The current stress in the current double diodes is calculated based on the modes of operation as shown in Fig. 4. Table II shows the current in diode during one switching cycle.

The average current, $i_{D_1,\text{avg}}$ is calculated for the complete switching cycle and is found to be $\frac{I_o}{2}$. Similarly the rms value, $i_{D_1,\text{rms}}$ is calculated as

$$i_{D_1,\text{avg}} = \frac{I_o}{2} \tag{22}$$

$$i_{D_1,\text{rms}} = \frac{I_o}{\sqrt{2}}. \tag{23}$$

Similarly, avg and rms currents in diode D_2 can be evaluated which is the same as diode D_1. It is to be noted that both diodes share half of the load current I_o.

D. Filter Design

In this section, the design of filter is carried out. There are two type of filters, an input LC filter and an output LC filter required in the proposed converter. The design of L and C components is carried out as follows.

1) Output Filter Design: In the output of the proposed converter, a current doubler circuit is used which consists of two equal inductors, L_{f1} and L_{f2} and an output capacitor, C_o. The design of inductors, L_{f1} and L_{f2} is carried out in such a manner that the peak-to-peak value of the dc output inductor current ripple, $\Delta i_{L1,pp,\text{max}}$ is limited to a given value. The peak-to-peak value of the inductor current ripple can be calculated via

$$\Delta i_{L1,pp} = \frac{V_o}{L_{f1}}\left(\frac{T_s + t_o}{2}\right) \tag{24}$$

which can be further simplified to

$$\Delta i_{L1,pp} = \frac{V_o T_s}{L_{f1}}\left(1 - \frac{m}{2}\right). \tag{25}$$

With this, the output inductor can be selected according to

$$L_{f1} \geq \frac{V_o}{\Delta i_{L1,pp,\text{max}}}\left(\frac{1 - \frac{m_{\text{min}}}{2}}{f_s}\right) \tag{26}$$

where m_{min} is the minimum modulation index and f_s is the switching frequency of the converter. The output current is sum of the current in inductor L_{f1} and L_{f2}. The two inductor behaves like interleaved inductors and essentially, reduces the peak-to-peak current ripple in the output current, I_o. Fig. 8 shows the ripple currents, i_{Lf1} and i_{Lf2}. The ripple frequency of output current becomes twice the switching frequency, f_s contributing in reducing the size of output capacitor. The output capacitor, C_o is selected in order to limit the peak-to-peak value of the

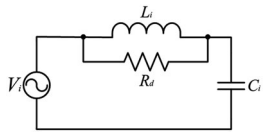

Fig. 9. Configuration of damped input filter for the proposed converter.

output voltage ripple $\Delta v_{C_o,pp,\max}$ to a given value

$$\Delta v_{C_o,pp} = \frac{V_o}{16 C_o L_{f1} f_s^2}(1-m). \tag{27}$$

The output capacitor value is given by

$$C_o \geq \frac{V_o}{16 \Delta v_{C_o,pp,\max} L_{f1} f_s^2}(1-m_{\min}). \tag{28}$$

2) Input Filter Design: Unlike PWM boost kind of rectifiers, the input filter of the proposed converter is an *LC* filter. For getting smooth sinusoidal current, high quality capacitors with low equivalent series resistance, equivalent series inductance, and high current ratings are required. However, a large value of input capacitor results in capacitive reactive power leading to low PF particularly in low power conditions. The reactive power supplied to the capacitor is given by

$$Q_m = 3\omega_i C_i V_i^2 \tag{29}$$

where $\omega_i = 2\pi f_i$. It is desirable that even at low load, the displacement PF does not go below a certain value. Based on this specification, the upper limit of input filter capacitance can be calculated.

After the selection of capacitor value, the inductor value is chosen. Typically the resonant frequency is kept higher than 20 times the supply frequency and lower than one-third the PWM frequency [25]. Based on [25], the damping resistor for the filter is selected. For the input filter configuration shown in Fig. 9, the resonant frequency, $\omega_{r,i}$ and damping factor, ξ are given as

$$\omega_{r,i} = \frac{1}{\sqrt{L_i C_i}} \tag{30}$$

$$\xi = \frac{1}{2R_d}\sqrt{\frac{L_i}{C_i}}. \tag{31}$$

The higher the damping factor, poorer is the high-frequency attenuation. Therefore, a compromise is needed between the damping factor and the filtering performance.

E. Effect of Modulation Index (m) on the THD of the Input Line Current

In this section, the effect of modulation index, m on the THD of the input line current is analyzed mathematically. At lower modulation index, pulse width of the unfiltered input current becomes narrower and therefore, the THD of the current increases. In this section, the THD of the unfiltered input current shown in Fig. 10 is derived mathematically and its variation is analyzed at different modulation index, m. The analysis is subjected to the assumption that the phase voltages (which are also the voltages across the input filter capacitors) are perfectly sinusoidal.

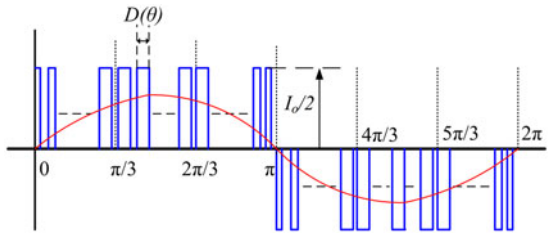

Fig. 10. Unfiltered input current and fundamental input current of the proposed converter.

The THD of the unfiltered input current is defined by

$$\text{THD} = \frac{\sqrt{I_{\text{rms}}^2 - I_{1,\text{rms}}^2}}{I_{1,\text{rms}}} \tag{32}$$

where I_{rms} is the rms value of unfiltered input current and $I_{1,\text{rms}}$ is the rms value of the fundamental of the unfiltered input current. The rms value of the unfiltered input current, I_{rms} is calculated in two steps. In the first step, the rms value of the current for a switching period, T_s is calculated. If the rms value of the current for a switching cycle is given by $I_{\text{rms},\theta}$ then

$$I_{\text{rms},\theta} = \sqrt{\left(\frac{I_o}{2}\right)^2 D(\theta)} \tag{33}$$

where $D(\theta)$ is the duty cycle of the pulsed current at angle, θ. In the second step, the rms value of the current is calculated for 2π duration as

$$I_{\text{rms}} = \sqrt{\frac{1}{2\pi}\left(\int_0^{2\pi} I_{\text{rms},\theta}^2 d\theta\right)}. \tag{34}$$

Simplifying the equation using (19) results in

$$I_{\text{rms}} = \frac{I_o}{\sqrt{2}}\sqrt{\frac{m}{\pi}}. \tag{35}$$

To calculate the rms value of the fundamental current, the Fourier analysis of the unfiltered input current shown in Fig. 10 is carried out. The analytical harmonic solution of the unfiltered input current is given by

$$\begin{aligned} i_a(t) &= \frac{\sqrt{3}}{4} I_o m \sin(\omega_o t) \\ &+ \frac{2I_o}{\pi}\sum_{k=1}^{\infty}\sum_{l=-\infty}^{\infty}\frac{1}{k}J_n\left(k\frac{\pi}{2}m\right)\sin\left([k+l]\frac{\pi}{2}\right) \\ &\times \sin l\frac{\pi}{3}\sin\left(k\omega_s t + l\omega_o t\right) \end{aligned} \tag{36}$$

where ω_s and ω_o are the switching frequency and the line frequency of the proposed converter, respectively. From (36), the rms value of the fundamental current, $I_{\text{in,rms}}$ is derived as

$$I_{\text{in,rms}} = \frac{\sqrt{3}}{4\sqrt{2}} m I_o. \tag{37}$$

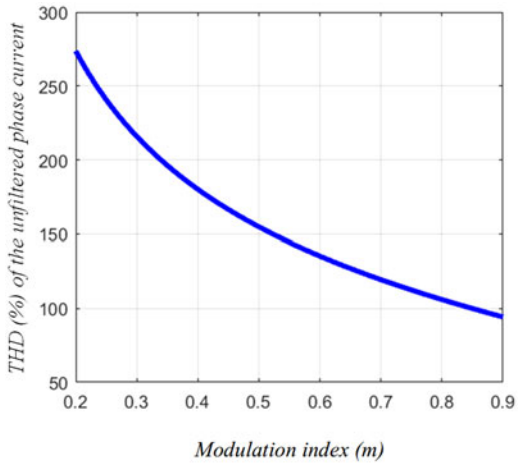

Fig. 11. Variation of the THD with modulation index, m.

TABLE IV
COMPARISON OF RESULTS OBTAINED BY ANALYTIC SOLUTION AND DIGITAL SIMULATION

	Parameters	Analytic Solution	Digital Simulation
1)	Voltage gain (m)	0.7	0.72
2)	Switch current (Avg)	0.62 A	0.7 A
3)	Switch current (rms)	1.31 A	1.46 A
4)	Diode current (Avg)	2.78 A	2.89 A
5)	Diode current (rms)	3.93 A	3.76 A
6)	Current ripple ($pk-pk$)	1.28 A	1.15 A
7)	Voltage ripple ($pk-pk$)	0.00109 V	0.00147 V

The THD of the unfiltered input current is calculated using (32), (35), and (37)

$$\text{THD} = \sqrt{\frac{16}{3m\pi} - 1}. \tag{38}$$

Fig. 11 shows the variation of THD with modulation index m. It is worth noticing that the lower modulation index, the THD of unfiltered input current increases and therefore, the converter should not be operated at lower modulation index.

IV. SIMULATION OF THE PROPOSED CONVERTER

In this section, the digital simulation of the proposed converter for the given specification in Table I is carried out. Based on the steady-state analysis, the different parameters of the converter are designed. Furthermore, the current stresses in passive and active devices and voltage and current ripple are evaluated for the proposed converter using both digital simulation and analytical calculation.

The switching frequency of $f_s = 40$ kHz is selected in order to achieve a good compromise between high power conversion efficiency and high power density. The specification of an example converter suitable for aircraft system is provided in Table III.

With switching frequency, $f_s = 40$ kHz the value of passive components are selected as $L_{f1} = L_{f2} = 1.2$ mH, $C_o = 800$ μF, filter inductor ($L_a = L_b = L_c$) $= 200$ μH, filter capacitor ($C_a = C_b = C_c$) $= 1.2$ μF following the design rules given in Sections III-C and III-D.

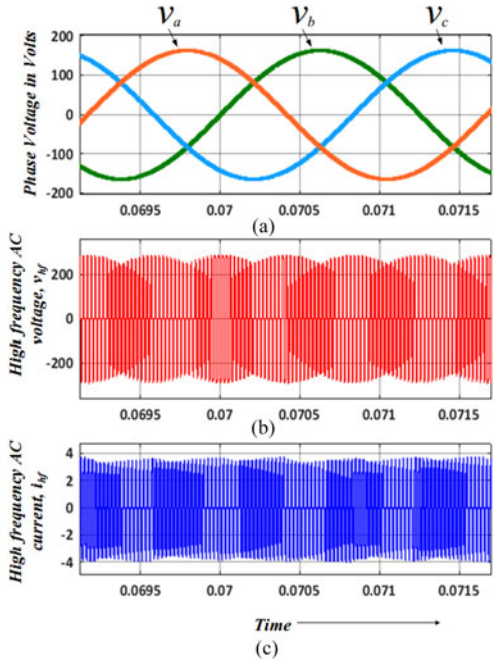

Fig. 12. (a) Three-phase input ac voltage v_a, v_b, v_c. (b) High-frequency ac voltage v_{hf}. (c) High-frequency ac current i_{hf}.

Based on the designed parameters of the converter, the converter is simulated in MATLAB 2015a for full load. The current stresses of active/passive devices as well as voltage and current ripple are evaluated which are compared with analytical solutions found by the following Sections III-C and III-D. Table II shows the comparison of the results obtained using analytic calculation and digital simulation. The digital simulation validates the analysis of the proposed converter.

The proposed matrix converter directly converts three-phase line frequency ac into single-phase high frequency. Fig. 12(a) shows the input three-phase ac, v_{an}, v_{bn}, v_{cn}. Fig. 12(b) shows the high-frequency ac output, v_{hf} of the matrix converter. Fig. 12.(c) shows the corresponding high-frequency ac current, i_{hf}.

The frequency of the v_{hf} depends on the switching frequency, f_s. The switching frequency, f_s of the converter is selected as 40 kHz. Fig. 13 shows the zoomed picture of v_{hf} and i_{hf}. A symmetrical bipolar high-frequency ac of frequency $= 40$ kHz is generated using matrix topology. A dead time is introduced to avoid short circuiting of the input filter capacitor.

The proposed modulation scheme is based on SVM modulation scheme and it provides superior input power quality. Fig. 14 shows the three-phase input current for full load (500 W). The THD of the current is estimated and found to be 3.25% as shown in Fig. 15. Fig. 16 shows the input phase voltage, v_{an} and phase current, i_a for full load. The displacement PF is found to be almost unity. The high-frequency ac output of the matrix converter is processed using current doubler. Fig. 17(a) shows the output dc voltage, V_o. Fig. 17(b) and (c) shows the inductor current, i_{Lf1} and i_{Lf2}, respectively. The output current I_o is the sum of two currents.

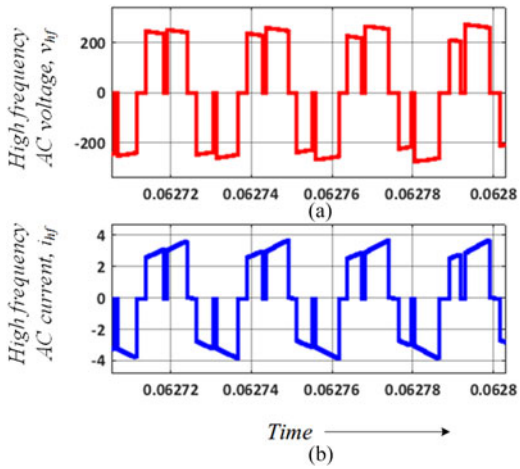

Fig. 13. (a) High-frequency ac voltage v_{hf}. (b) High-frequency ac current i_{hf}.

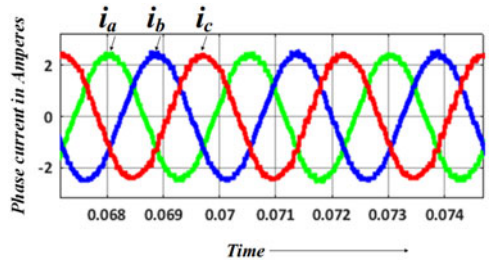

Fig. 14. Three-phase input ac current i_a, i_b, i_c. The simulated THD of current is found to be 3%.

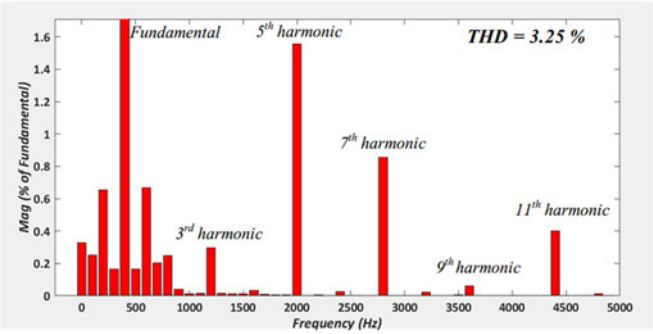

Fig. 15. Fast Fourier transform spectrum of input phase-a current. The fundamental frequency is 400 Hz. The other frequencies which have relatively larger percentage are 5th, 7th, and 11th harmonics of the fundamental frequency.

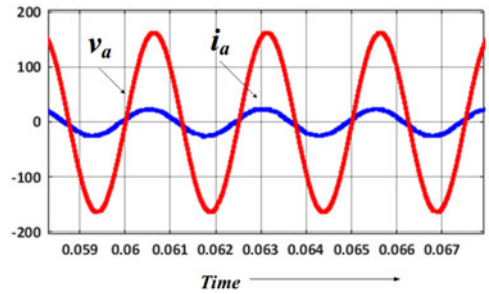

Fig. 16. Input phase-a current i_a and input phase-a voltage v_a. The displacement power factor of the converter is almost found to be unity.

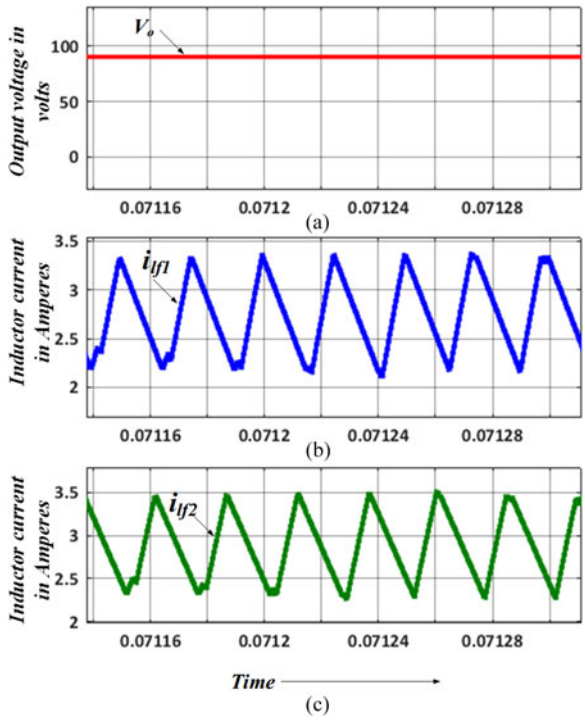

Fig. 17. (a) Output dc voltage V_o. (b) Output filter inductor current i_{Lf1}. (c) Output filter inductor current, i_{Lf2}.

V. Comparative Loss Evaluation of the Proposed Converter

In this section, the loss analysis of the proposed converter is carried out. This section is divided further into three sections. In the first section, the semiconductor losses of the proposed converter are carried out. In the second section, the semiconductor losses in the traditional six-switch buck rectifier based on [24] are carried out. Subsequently, the semiconductor losses of these two converters are compared in the third section at different switching frequency and at different output power. It is to be noted that since the input and output filter of the two converters are almost identical, the loss comparison is carried out based on only total semiconductor losses.

A. Semiconductor Losses in the Proposed Converter

The semiconductor losses in the proposed converter are divided into two parts: conduction loss and switching loss. These two losses are calculated for the proposed converter as follows.

1) Conduction Loss: In the proposed modulation scheme, the body diodes of the MOSFETs in the matrix switches do not conduct and therefore, the switch conduction losses is only due to the ON resistance of the MOSFETs. The switch rms current is given by (19).

The total conduction loss in the matrix switches, $P_{c,\text{Matrix}}$ is given by

$$P_{c,\text{Matrix}} = 12 i_{SW,\text{rms}}^2 R_{ds,\text{ON}} \tag{39}$$

where $R_{ds,\text{ON}}$ is the ON resistance of the MOSFETs used to implement matrix switch.

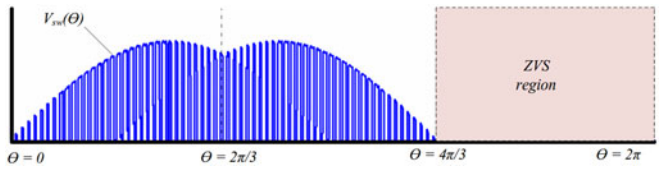

Fig. 18. Voltage across on of the MOSFETs of the matrix switch for a line cycle ($T_i = \frac{1}{f_i}$).

Similarly, the conduction loss in the CDR diodes is calculated based on average and rms current calculated in (22) and (23). The total conduction loss in the CDR diodes, $P_{c,\text{CDR}}$ is given by

$$P_{c,\text{CDR}} = 2\left(i^2_{D,\text{rms}} R_D + i_{D,\text{avg}} V_f\right) \tag{40}$$

where R_D and V_f are the ON resistance and forward voltage drop of the CDR diodes, respectively.

2) Switching Loss: The switching losses in the proposed converter are divided into three parts. The first part is due to the overlapping of voltage and current during MOSFET turn ON and turn OFF. The second part is due to the charging and discharging of the parasitic capacitance of the MOSFETs and the CDR diodes. The third part is the gate driving loss. To calculate the total switching loss of the proposed converter, all these three losses are taken into consideration. As SiC diodes are used in both proposed and traditional, the reverse recovery losses have not been considered for switching loss calculation in diodes.

Taking $V_{DS,\text{ON}}$ as drain–source voltage prior to turn ON of the MOSFET and I_{ON} as the drain–source current after turn ON, the power loss during turn ON, $P_{sw,\text{ON}}$ can be approximated by the following:

$$P_{sw,\text{ON}} = \frac{V_{\text{DS,ON}} I_{\text{ON}}}{2} t_r f_s \tag{41}$$

where t_r is the overlapping period during the turn ON of the MOSFET of the matrix switch.

The drain–source voltage $V_{\text{DS,ON}}$ varies throughout the line period $T_i = \frac{1}{f_i}$ and thus, the average value of $V_{\text{DS,ON}}$ is taken for calculating turn ON loss using (43). The current I_{ON} remains constant and its value is given by $\frac{I_o}{2}$, where I_o is the output current of the converter.

Fig. 18 shows the voltage variation $v_{sw}(\theta)$ across one of the MOSFETs of the matrix switch. During the one third of the line period, ($\theta = \frac{4\pi}{3}$ to 2π) the voltage across the MOSFET is zero which results in ZVS in this region. The average voltage across the MOSFET is thus calculated by integrating the switch voltage v_{sw} from $\theta = 0$ to $\theta = 2\pi$.

If the average value of the drain–source voltage is represented by $< V_{\text{DS,ON}} >$, then

$$< V_{\text{DS,ON}} > = \frac{1}{2\pi}\int_o^{2\pi} v_{sw}(\theta) d\theta = \frac{3\sqrt{3}}{\pi} V_m. \tag{42}$$

The total turn ON power loss $P_{sw,\text{ON, total}}$ for the matrix switches is given by the following:

$$P_{sw,\text{ON, total}} = \frac{9\sqrt{3}}{4\pi} V_m I_o t_r f_s. \tag{43}$$

During the turn OFF the matrix switch, the voltage across the two back-to-back connected MOSFETs are different. One of the MOSFETs is charged to $V_{\text{DS,ON}}$ whereas other MOSFET is charged to the forward voltage drop of the diode, V_f. As V_f is too small in comparison to $V_{DS,\text{ON}}$, the turn OFF loss due to one MOSFET is only taken into consideration. With this, the total turn OFF loss of the matrix switch is given by

$$P_{sw,\text{OFF,total}} = \frac{9\sqrt{3}}{4\pi} V_m I_o t_f f_s \tag{44}$$

where t_f is the overlapping period during the turn OFF of the MOSFET.

The switching loss due to charging and discharging of the output capacitor in each of the MOSFETs of the matrix switch is derived as

$$P_{sw,\text{Matrix}} = \frac{C_{\text{oss}} f_s}{2\pi}\int_0^{2\pi} v^2_{sw}(\theta) d\theta \tag{45}$$

where C_{oss} is the output capacitance of the MOSFET of the matrix switch.

The output capacitance of the diodes of the CDR circuit, $C_{\text{oss},D}$ also charges and discharges resulting in additional switching loss which is given by

$$P_{sw,\text{CDR}} = C_{\text{oss},D} V_m^2 \left(\frac{1}{6} + \frac{\sqrt{3}}{8\pi}\right) f_s \tag{46}$$

where $C_{\text{oss},D}$ is the output capacitance of the diode of the CDR circuit. As there are 12 MOSFETs and two CDR diodes in the proposed converter, the total switching loss due to charging and discharging of the MOSFETs capacitance and the CDR diodes is given by

$$P_{sw,C,\text{total}} = \frac{12\left(\pi + \frac{3\sqrt{3}}{8}\right)}{\pi} C_{\text{oss}} V_m^2 f_s + 2C_{\text{oss},D} V_m^2 \left(\frac{1}{6} + \frac{\sqrt{3}}{8\pi}\right) f_s \tag{47}$$

where C_{oss} is the output capacitance of each of the MOSFETs. Similarly, the total gate drive loss of the proposed converter is given by

$$P_{sw,G,\text{total}} = 12 C_{iss} V_g^2 f_s \tag{48}$$

where C_{iss} is the input capacitance of each of the MOSFETs.

3) Total Loss: Taking all losses into consideration, the total semiconductor loss, $P_{\text{total, proposed}}$ of the matrix switcher under the proposed modulation scheme is given by the following:

$$P_{\text{total, proposed}} = \underbrace{\frac{3mI_o^2 R_{ds,\text{ON}}}{\pi} + I_o^2 R_D + I_o V_f}_{\text{conduction loss}} + P_{\text{switching loss, proposed}} \tag{49}$$

where

$$P_{\text{switching loss, proposed}} = \frac{9\sqrt{3}}{4\pi} V_m I_o f_s (t_r + t_f) + \frac{12\left(\pi + \frac{3\sqrt{3}}{8}\right)}{\pi} C_{\text{oss}} V_m^2 f_s + 12 C_{iss} V_g^2 f_s + 2 C_{\text{oss},D} V_m^2 \left(\frac{1}{6} + \frac{\sqrt{3}}{8\pi}\right) f_s. \quad (50)$$

B. Semiconductor Losses in the Traditional Six-Switch Buck Rectifier

The comprehensive loss analysis of the traditional six-switch buck rectifier is presented in [24]. The rms and avg current of the semiconductor devices are derived based on [24]. It should be noted that in the traditional buck rectifier, the amplitude of the switch current is equal to the load current, I_o unlike the proposed converter where the amplitude of the switch current is half of the load current. This not only reduces the switch rms current but also reduces the switching loss almost by half in the proposed converter. Assuming all the semiconductor devices of the traditional converter are identical to the proposed converter, the total loss of the traditional six-switch buck rectifier is given by the following:

$$P_{\text{total, traditional}} = \underbrace{\frac{6}{\pi} M R_{ds,\text{ON}} I_o^2}_{\text{Mosfet conduction loss}} + \underbrace{\frac{6}{\pi} M (I_o^2 R_D + I_o V_f)}_{\text{Switch diode conduction loss}} + \underbrace{\left(1 - \frac{3M}{\pi}\right)(I_o^2 R_f + I_o V_f)}_{\text{Output diode conduction loss}} + P_{\text{switching loss, traditional}} \quad (51)$$

$$P_{\text{switching loss, traditional}} = \frac{3\sqrt{3}}{\pi} V_m I_o t_r f_{st} + \frac{12\left(\frac{7\pi}{16} - \frac{9\sqrt{3}}{32}\right)}{\pi} \left(\frac{C_{\text{oss}} + 3C_{\text{oss},D}}{2}\right) V_m^2 f_{st} + 6 C_{iss} V_g^2 f_{st} \quad (52)$$

where M and f_{st} are the modulation index and the switching frequency of the traditional converter, respectively. It is worth noticing that all the diodes of the traditional converter are assumed to be identical.

It is important to note here that the value of modulation index is not same in both the proposed and traditional converter. For the same input and output specification, the modulation indexes and the switching frequencies of the proposed and traditional converter are related by

$$m = 2M; f_{st} = 2 f_s. \quad (53)$$

The proposed converter generates bipolar symmetrical high-frequency ac of 40 kHz frequency which is equivalent to 80 kHz output, if rectified. As buck converter generates unipolar high-frequency output at its output, the matrix switching frequency f_s and the buck rectifier switching frequency, f_{st} are related as shown in (53).

TABLE V
ACTIVE AND PASSIVE COMPONENTS SELECTED FOR THE EXPERIMENTAL VALIDATION OF THE PROPOSED MATRIX-BASED THREE-PHASE AC–DC CONVERTER

	Component	Specification
1	MOSFET, S_1–S_6	FCA16N60N, 600 V, 16 A
2	Diode D_1, D_2	C3D10060A-ND, 600 V 14.5 A
3	Input filter inductors, L_a, L_b, L_c	513-1660-ND, 200 μH 7A
4	Input filter capacitor, C_a, C_b, C_c	PCF1569-N, 1.2 μF 630 Vdc
5	Output Inductor, L_{f1}, L_{F2}	513-1654-ND, 1.2 mH 4.7 A
6	Output capacitor, C_o	Electrolytic capacitor 400 μF, 400 V
7	FPGA controller board	ALTERA QUARTUS II
8	Microcontroller board	TMDSCN28335

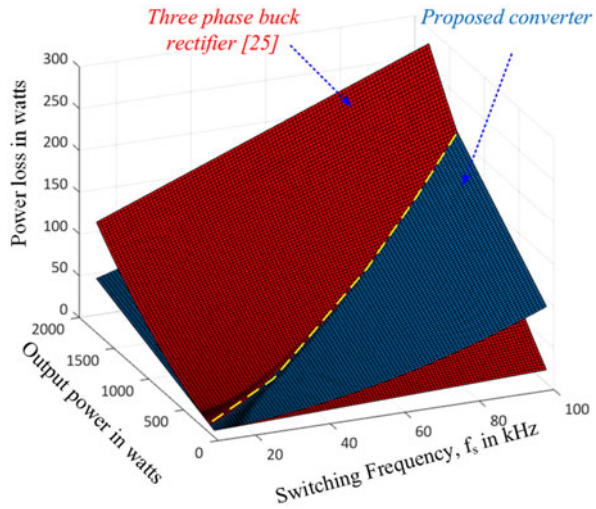

Fig. 19. Total semiconductor power loss versus output power P_o and switching frequency f_s.

C. Comparison of the Semiconductor Losses in the Proposed and the Traditional Six-Switch Buck Rectifier

For comparing the losses of the proposed and the traditional converter, identical semiconductor devices have been chosen. Based on the selected semiconductor devices given in Table III, the various parameters of the two converters are as follows. $R_{ds,\text{ON}} = 200$ mΩ, $R_D = 50$ mΩ, $V_f = 1.8$ V, $t_r = 200$ nS, $m = 2M = 0.7$, $C_{\text{oss}} = 70$ pF, $C_{iss} = 2170$ pF, $C_{\text{oss},D} = 200$ pF.

Assuming the device parameters to be same for 100–2000 W, the total semiconductor losses of the two converters are calculated for varying switching frequency, f_s (20–100 kHz) evaluated. The results are illustrated through a three-dimensional plot in Fig. 19. The followings observation are made through the loss analysis of the proposed and the traditional buck converter [24].

1) The proposed converter provides lower semiconductor loss compared to the three-phase buck rectifier for the same input–output specifications at relatively lower switching frequency and higher output power.
2) For a given output power, the semiconductor losses of both—the traditional and the proposed converter becomes

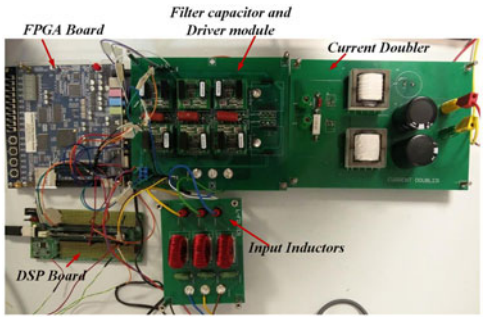

Fig. 20. Hardware prototype of the proposed matrix-based ac–dc converter.

equal at certain switching frequency. For example, at f_s = 40 kHz, the losses of these two converters are almost equal at 500 W output power. However, increasing the output power at this switching frequency results in lower semiconductor losses in the proposed converter than the three-phase buck rectifier as shown in Fig. 19.

3) As shown in Fig. 19, by increasing the output power, the yellow line shifts at higher switching frequencies which shows that with the increase in the output power, the proposed converter can be operated at higher switching frequency with overall lower semiconductor loss than the traditional three-phase six-switch buck rectifier.

VI. Experimental Verification

A. Prototype and Structure

Fig. 20 shows the prototype of the proposed matrix-based nonisolated ac–dc rectifier. The converter is divided into four modules. The first module consists of a filter inductor and a damping resistor. The second module consists of power devices, gate drivers, and input filter capacitor. The output of second module is processed using a current doubler (third module) to provide the rectified dc output voltage. The fourth module consists of voltage/current sensors, DSP board, and field programmable gate array board. The matrix switches are formed using two discreet MOSFETs by connecting them back-to-back as shown in Fig. 5. The three-phase input voltage is sensed and given to the DSP board to generate PWM signals which are further processed using the Field Programmable Gate Array (FPGA) board to generate switching signal for gate drivers [26]. The active and passive components selected for the experimental validation of the proposed converter are given in Table V.

B. Controller

The controller hardware for the proposed converter includes a DSP board and a Field Programmable Gate Array (FPGA) board. The DSP board used is the TI TMDSCNF28335 evaluation board whereas the Field Programmable Gate Array (FPGA) board used is ALTERA QUARTUS II board. The three-phase input ac voltage is sensed and given to the DSP board which in turn, generates PWM signal. A abc-dq based phase-locked loop is implemented inside DSP for calculating the phase angle, θ. Based on θ and modulation index, m the DSP generates PWM signals. The PWM signals are further processed using Field Programmable Gate Array (FPGA) board based on the sector information and thus, final switching signals are generated which are given to the gate drivers [27].

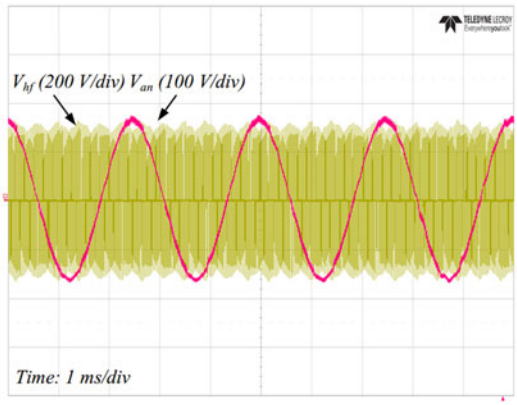

Fig. 21. Input phase voltage v_{an} and high-frequency ac output v_{hf}.

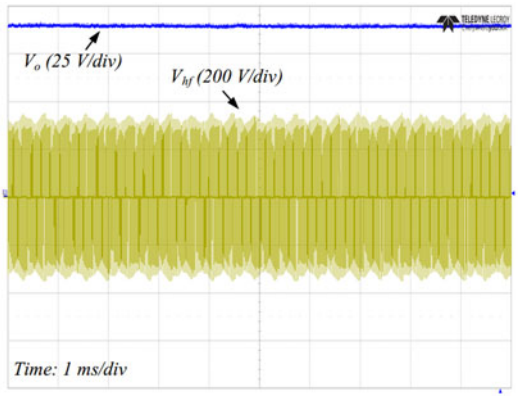

Fig. 22. Output dc voltage V_o and high-frequency ac output v_{hf}.

C. Experimental Results

1) Key Experimental Results: The proposed matrix-based ac–dc rectifier is tested with a resistor load and the three-phase input voltage of 115 V(rms), ac at 400 Hz. The power devices are mounted with heat sinks and an additional fan cooling is provided for the converter to test at full load. Fig. 21 shows input phase-a voltage, v_{an} and high-frequency ac, v_{hf}. The proposed matrix topology converts three-phase line frequency ac directly into single-phase high-frequency ac. Subsequently, the high-frequency ac output is processed using CDR to provide the required dc output voltage. Fig. 22 shows the rectified output dc voltage V_o, and high-frequency ac output v_{hf} of the matrix converter.

Fig. 23 shows the high-frequency ac output of the converter. It is evident that the output is symmetrical and bipolar. The small zero period between the adjacent voltage is due to the presence of dead time t_d which is required to avoid the short circuit of input filter capacitor during switch transition.

Fig. 24 shows the high-frequency ac output v_{hf} and the high-frequency ac current i_{hf} at full load. A small *RC* snubber is kept across the input of current doubler to reduce the voltage spikes.

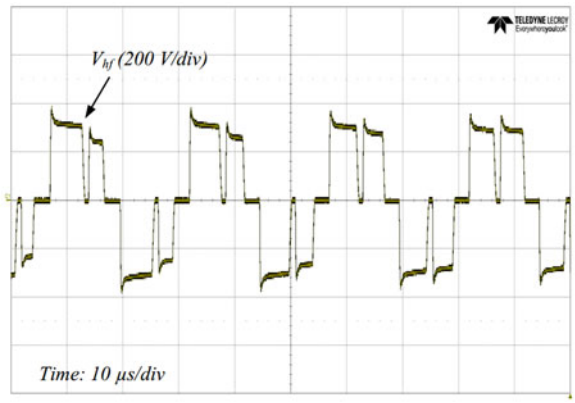

Fig. 23. High-frequency ac output, v_{hf} of the matrix converter.

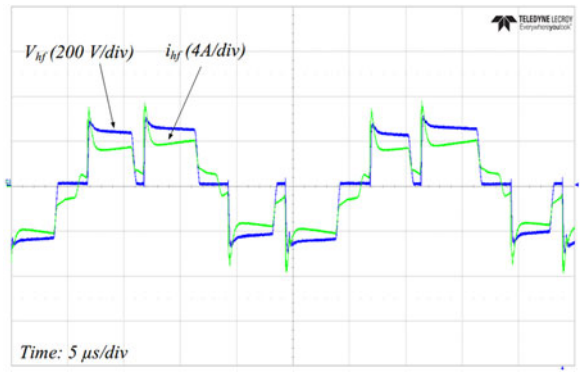

Fig. 24. High-frequency ac output v_{hf} and high-frequency ac current i_{hf} of the matrix converter at full load.

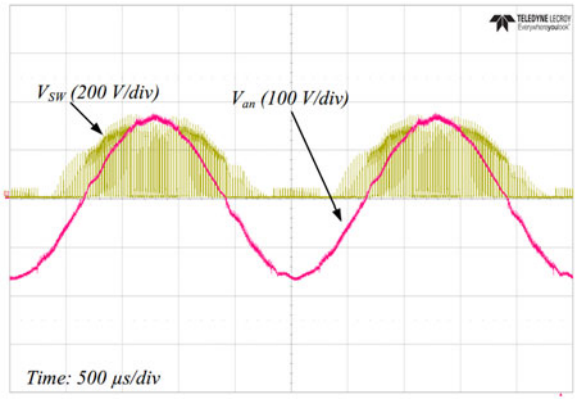

Fig. 25. Input phase-a voltage $v_{\rm an}$ and switch SW_{11} voltage.

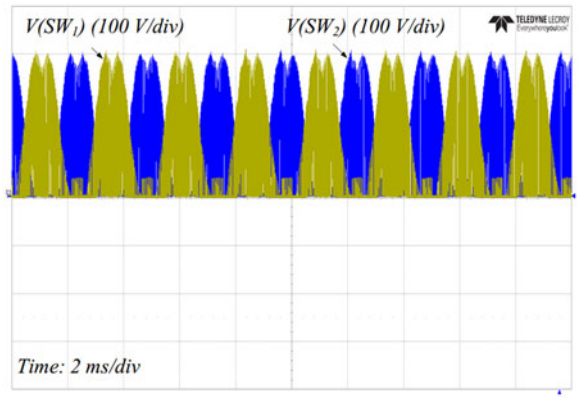

Fig. 26. Voltage across switch SW_{11} and SW_{12}.

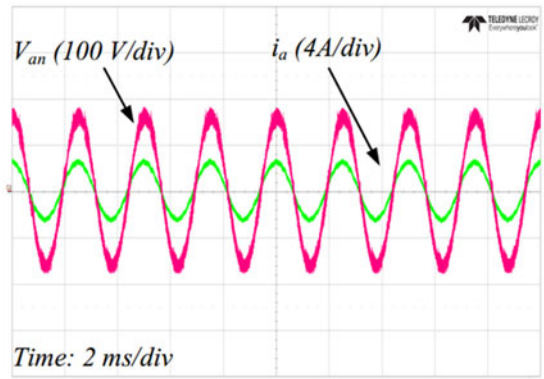

Fig. 27. Input phase-a voltage $v_{\rm an}$ and phase current i_a. The displacement power factor is close to unity.

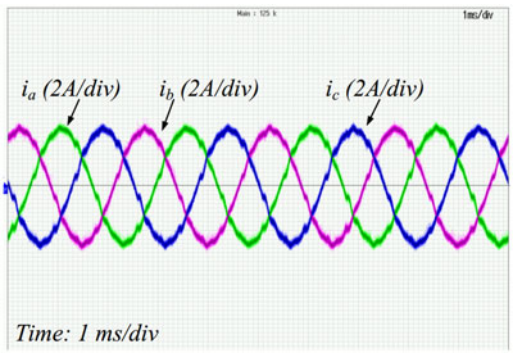

Fig. 28. Three phase input current i_a, i_b, i_c. Total harmonic distortion (THD) of the current is found to be 3.7%.

Because of parasitic capacitance of current doubler diodes, the high-frequency ac is having some spikes which has further scope of improvement by the proper design of printed circuit board layout. Fig. 25 shows the input phase voltage $V_{\rm an}$ and the voltage across switch SW_{11}. The switch voltage rises from zero become maximum and then falls to zero. For a 60° time interval, the voltage across the switch remains zero. Fig. 26 shows the voltage across switches SW_{11} and SW_{12}. Both switches SW_{11} and SW_{12} forms S_1 as shown in Fig. 5. Each of the two switches are ON for 60^{ω} time interval. It is because of the forward biasing of the switch diode. Consequently, it gives rises to zero switching loss during this particular interval and therefore, improves power conversion efficiency. Therefore, even though the proposed matrix converter has 12 switches, half of the switches will not contribute to the switching loss because of the zero voltage across them. Fig. 27 shows the phase-a voltage $v_{\rm an}$ and phase current i_a at full load. The displacement PF of the converter is close to unity. Fig. 28 shows the three-phase input current. The currents are balanced and symmetrical. The THD of the current is estimated for full load and 50% of the full load. It is found to be 3.7% and 4.19%. Fig. 29 shows the voltage across current doubler diodes D_1 and D_2. Each of the diodes remains ON for less than half of the switching cycle. During the mode when

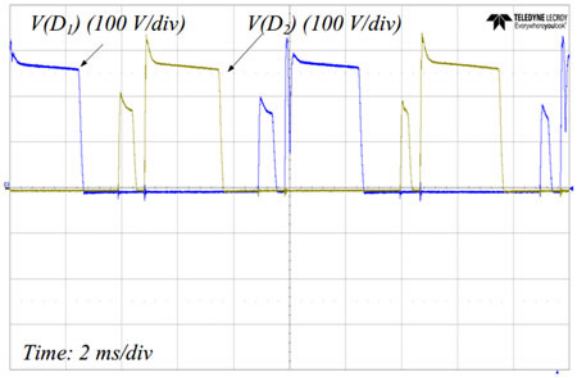

Fig. 29. Voltage across the diodes, D_1 and D_2.

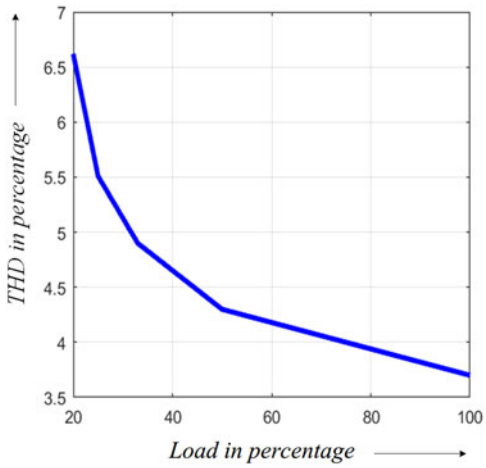

Fig. 30. Experimental THD at different output load.

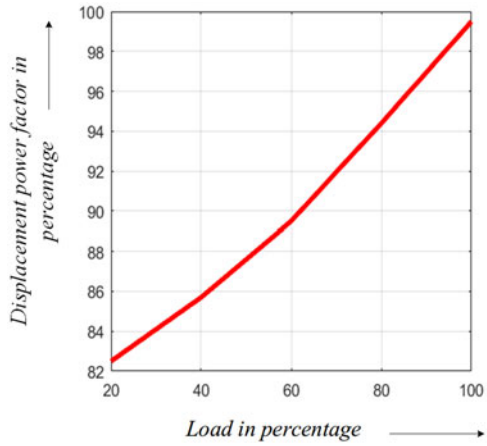

Fig. 31. Displacement power factor at different output load.

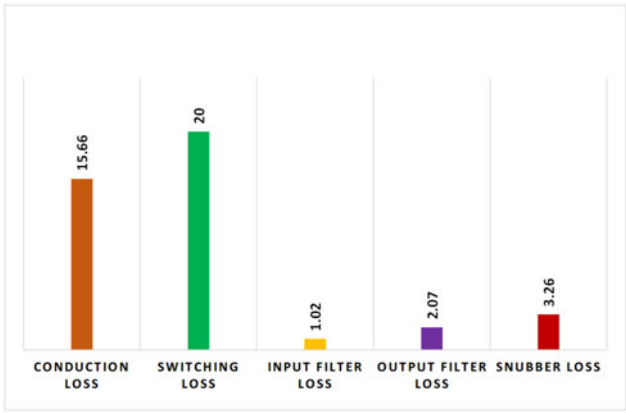

Fig. 32. Theoretical distribution of the power loss in the proposed converter. The total power loss is 42.01 W.

power is not delivered from source to load, both of the diodes D_1 and D_2 conducts and zero voltage appears across the input of current doubler circuit.

2) Discussion on the Power Quality of the Proposed Converter: The proposed power converter provides superior input power quality. Fig. 30 shows the THD variation of input current at different load. Even at 20% of the full load, THD is better than 7%. The THD at the full load is found to be 3.7%. The THD of the converter can be further improved by increasing the input filter capacitor. However, the maximum value of the input filter capacitor is limited by displacement PF. The proposed converter is tested at 500 W power with 3.7% of THD and almost unity PF that demonstrates the performance of the converter in terms of the input power quality. Fig. 31 shows the variation of displacement PF with the output load. The displacement PF is almost unity at 100% of the load. It reduces with reduction in the output load. However, even at 50% of the full load, the displacement PF is more than 90%.

3) Discussion on the Power Conversion Efficiency of the Proposed Converter: The proposed converter is tested with resistive load and programmable three-phase power supply. As shown in the modes of operation, there is no switch diode conduction which contributes in reducing conduction losses of the switches. Moreover, the use of current doubler reduces switch rms current by half which further reduces the switch conduction loss. To realize the matrix topology, each matrix switch is realized by two back-to-back connected switches. During the switching process, one of the two switches undergoes natural ZVS as it remain forward biased which contributes in reducing the switching loss. The total semiconductor losses have been calculated in Section V for the proposed converter. The input and output filter losses are calculated according to their datasheet. The effect of ripple voltage and ripple current is ignored in the total loss calculation of the proposed converter. A *RC* snubber of 50 Ω and 1.5 nF has been added across all the switches of the matrix converter to reduce the voltage spikes due to the parasitic effects. The theoretical loss distribution of the proposed converter is shown in Fig. 32. The total estimated loss of the converter at 500 kW output power is 42.01 W and therefore, the theoretical full-load efficiency of the proposed converter is found to be 91.6%.

The experimental full-load efficiency of the prototype was found be 91% which is very close to the theoretical efficiency of the converter. The difference in theoretical and experimental efficiency is due to the parasitic elements, and voltage and current ripple which have been ignored in the calculation. The operation of the proposed converter at high switching frequency ($\geq$ 40 kHz) requires proper layout design for reducing the parasitic effects. There is further scope of optimizing the power

conversion efficiency by selecting semiconductor devices and Printed Circuit Board (PCB) layout design. However, the main focus of this paper is the topology, modulation techniques, and its experimental validation; the optimization of efficiency is not carried out.

VII. Conclusion

In this paper, a matrix-based nonisolated three-phase ac–dc converter suitable for aircraft system was presented. The use of matrix converter allows the use of current doubler and therefore, it can reduce the output voltage further by a factor of two for the same modulation index. For lower output voltage, a conventional three-phase buck rectifier must be operated at lower modulation index which in turn increases the switch rms current and reduces the power conversion efficiency. The proposed topology is very suitable for the applications where lower voltage gain ($\frac{V_o}{V_{\text{in}(\text{rms})}}$) is required. The proposed SVM-based modulation scheme is digitally implemented using DSP and Field Programmable Gate Array (FPGA). As the converter is operating at high switching frequency and discreet semiconductor switches are used to realize matrix switches, the Printed Circuit Board (PCB) layout design is very important for reducing the parasitic effects. The proposed converter provides superior input power quality. With small input filter and output filter, the proposed topology has potential to provide high power density. The use of current doubler in the output side reduces the output current ripple by interleaving the output inductors. Comprehensive simulation followed by hardware experiments on a 500 W prototype validates the feasibility and suitability of the proposed converter.

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