A High Power Density Series-Stacked Energy Buffer for Power Pulsation Decoupling in Single-Phase Converters

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***Abstract*—A high-efficiency, high-power-density buffer architecture is proposed for power pulsation decoupling in power conversion between dc and single-phase ac. We present an active decoupling solution that yields improved efficiency and reduced circuit complexity compared to existing solutions. In the proposed architecture, the main energy storage capacitor is connected in series with an active buffer converter across the dc bus. The series-stacked capacitor blocks the majority of the dc bus voltage to reduce the voltage stress on the buffer converter, such that fast, low-voltage transistors can be employed for the buffer converter. Moreover, the series capacitor provides the majority of the power pulsation decoupling through a wide voltage swing, and the buffer converter only needs to process a small fraction of the total power of the entire architecture, allowing a very small active circuit volume and very high system efficiency. The circuit operation and design constraints are analyzed in detail. In the proposed buffer architecture, the series stacking of a nearly lossless capacitor and a lossy converter presents a challenge of capacitor voltage balancing and power loss compensation. We propose a control scheme exploiting the small ripple in the bus voltage and dc input current to compensate for the power loss in the buffer converter while maintaining the voltage balance. Light-load techniques are also introduced to ensure that the buffer architecture meets strict ripple requirements while providing sufficient loss compensation. A 2-kW hardware prototype based on low-voltage GaN switches has been built to demonstrate the performance of the proposed solution. A power density of 25 W/cm^3 (410 W/in^3) by rectangular box volume and an efficiency above 98.9% across a wide load range has been experimentally verified.**

***Index Terms*—Active filters, circuit topology, digital control, DC-AC power converters, power smoothing.**

I. Introduction

POWER converters interfacing dc and high power factor single-phase ac (inverters or rectifiers) typically require an energy buffer to handle the twice-line-frequency power ripple. As shown in Fig. 1, the power of 60-Hz single-phase ac with unity power factor takes a shifted 120-Hz sinusoidal waveform (twice-line-frequency power pulsation). While the cycle average equals the dc power, there exists a mismatch between the instantaneous values. An energy buffer is, therefore, required to compensate the energy difference within a cycle such that the dc power can be decoupled from the ac power pulsation.

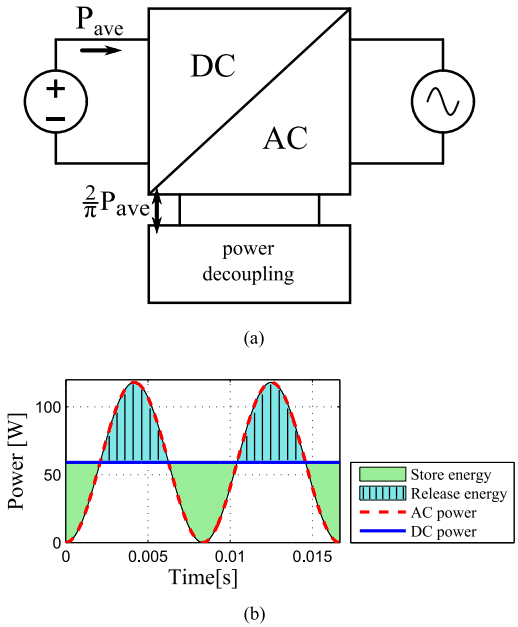

Fig. 1. Power conversion between dc and single-phase ac. (a)High-level schematic. (b) Instantaneous power plot.

Capacitors are often used for energy storage in power pulsation decoupling applications, owing to their superior energy density compared to inductors [1]. The simplest and most widely used solution in practice is a dc bus capacitor bank, which is often referred to as capacitor passive decoupling. In one cycle, the energy storage requirement for the capacitor bank can be expressed as

$$\begin{aligned} E_{\text{buffer}} &= \frac{P_{\text{ave}}}{2\pi f_{\text{line}}} \\ &= \frac{1}{2}CV_{\max}^2 - \frac{1}{2}CV_{\min}^2 \\ &= \underbrace{\frac{1}{2}(V_{\max}+V_{\min})}_{\text{average}}\ \underbrace{(V_{\max}-V_{\min})C}_{\text{ripple}}, \end{aligned} \tag{1}$$

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where P_{ave} is the average power of the dc–ac converter, f_{line} is the line frequency, and $V_{\max}$ and $V_{\min}$ are the two extremes of the voltage across the capacitor bank. The energy storage requirement in one cycle is determined by the average load power (i.e., $\frac{P_{\text{ave}}}{2\pi f_{\text{line}}}$), and is fulfilled by charging and discharging the capacitors. According to (1), the capacitor bank needs to have enough capacitance C and voltage ripple (i.e., $V_{\max} - V_{\min}$) to provide the required buffering capability. Most applications impose strict constraints on the magnitude of the allowed voltage ripple on the dc bus. Therefore, to meet certain energy storage requirement, the capacitance C typically has to be very large. Note that although from (1), it may seem that increasing the average voltage, $\frac{1}{2}(V_{\max} + V_{\min})$, can also help reduce capacitor volume, this is generally not the case in practice. High average voltage does reduce the *capacitance* needed, but the capacitor would require higher voltage rating given certain volume. A capacitor rated at higher voltage typically has lower capacitance. In other words, the energy density of the ceramic capacitors considered here vary relatively little with rated voltage (with deviations caused by practical issues such as packaging), so the total capacitor volume changes relatively little with average voltage. The experimental evaluation of a large number of commercial capacitors in [2] demonstrated this trend.

The aforementioned large capacitance is usually provided by electrolytic capacitors, which offer large capacitance at low cost. However, electrolytic capacitors are known for their high power loss, low reliability, and limited current ripple capability [1]. In fact, in practice, the volume of the electrolytic dc bus capacitor bank is often limited by the ripple current capability [3], rather than the capacitance requirement of (1). Therefore, due to efficiency and reliability considerations, ceramic or metal film capacitors are often preferred despite their lower capacitance and higher cost, but the large volume required becomes a major limitation. Various solutions have been proposed in the literature that significantly increase the energy density of the power decoupling buffer and allow for the use of film or ceramic capacitors [4]–[20]. However, most of these solutions suffer from high circuit complexity, high component voltage stress, or a large efficiency or volume penalty, as will be discussed in Section II.

In this study, we propose a low complexity buffer architecture that overcomes the drawbacks of previous solutions, and simultaneously achieves both high efficiency and high power density. This paper presents the analysis and design of the circuit architecture as well as the control techniques for voltage balancing and loss compensation that enables the practical implementation of this architecture. The remainder of this paper is organized as follows: Section II reviews related previous work and explains the rationale that leads to the proposed idea; Section III illustrates the operation of the proposed buffer and derives the design constraints; Section IV discusses the control challenge imposed by this architecture and presents the feedback control scheme to achieve power loss compensation and voltage balancing; Section V presents the hardware prototype. Section VI presents the experimental results under various static and dynamic operating conditions; Section VII compares the series-stacked buffer architectures with state-of-the-art solutions in the literature. Section VIII concludes this paper.

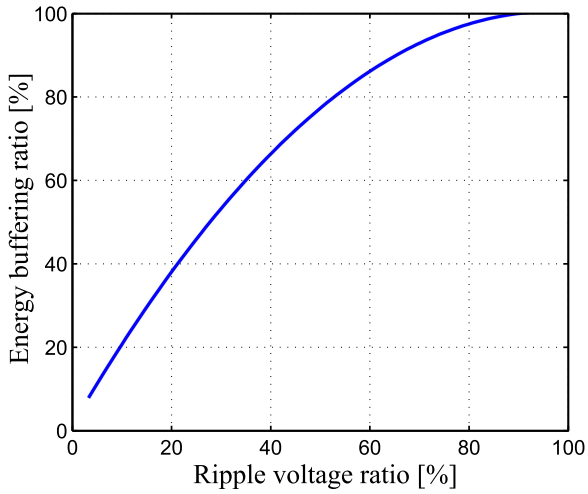


Fig. 2. Energy buffering ratio[1] as a function of the ripple voltage ratio (i.e., the magnitude of voltage decrease during discharge over the maximum voltage).

II. Energy Buffering Background

Fundamentally, the problem of the passive dc bus capacitor power pulsation decoupling is that the two requirements of energy storage and dc voltage regulation are tightly coupled but contradicting to each other. Fig. 2 plots the energy buffering ratio[1] of the capacitor bank as a function of how much the capacitors discharge from the maximum voltage. In practical applications, only a small portion of the capacitors' energy potential is utilized due to the limited ripple allowed. As shown in Fig. 2, for an application that allows only 3% ripple on the dc bus, the energy buffering ratio is only approximately 6%. The key to overcoming this limitation is to separate the energy storage and voltage regulation functionalities from the capacitors. Various embodiments of such schemes have been presented in the literature that are often referred to as active decoupling. A few comprehensive reviews can be found in [21]–[23], while only the works that are directly related to our proposed architecture are reviewed here.

For dc side decoupling, a magnetic-based bidirectional power converter can be inserted between the dc bus and the buffer capacitor such that one can control the conversion ratio to discharge the buffer capacitor more deeply, while still maintaining a close to ripple-free bus voltage. One example of such a structure is shown in Fig. 3(a). Although stand-alone switched-inductor converter implementations have been proposed [5], [6], [9], [11], many of the buffer converters proposed to date are merged into the operation of the main inverter/rectifier to eliminate a separate bulky inductor [4], [7], [8] or extra switches [12]. One of the major limitations of these solutions is the fact that the buffer converter is directly connected to the dc bus, yielding high component voltage stress. Consequently, for the added buffer converter, high-voltage, slow-switching transistors have to be used, which limits the achievable switching frequency, leading to large magnetic elements. Thus, the volume reduction

[1]Energy buffering ratio: The actual energy exchanged in one cycle over the full energy storage at the maximum voltage, i.e., $\Gamma_b = \frac{E_{\max} - E_{\min}}{E_{\max}}$ [15].

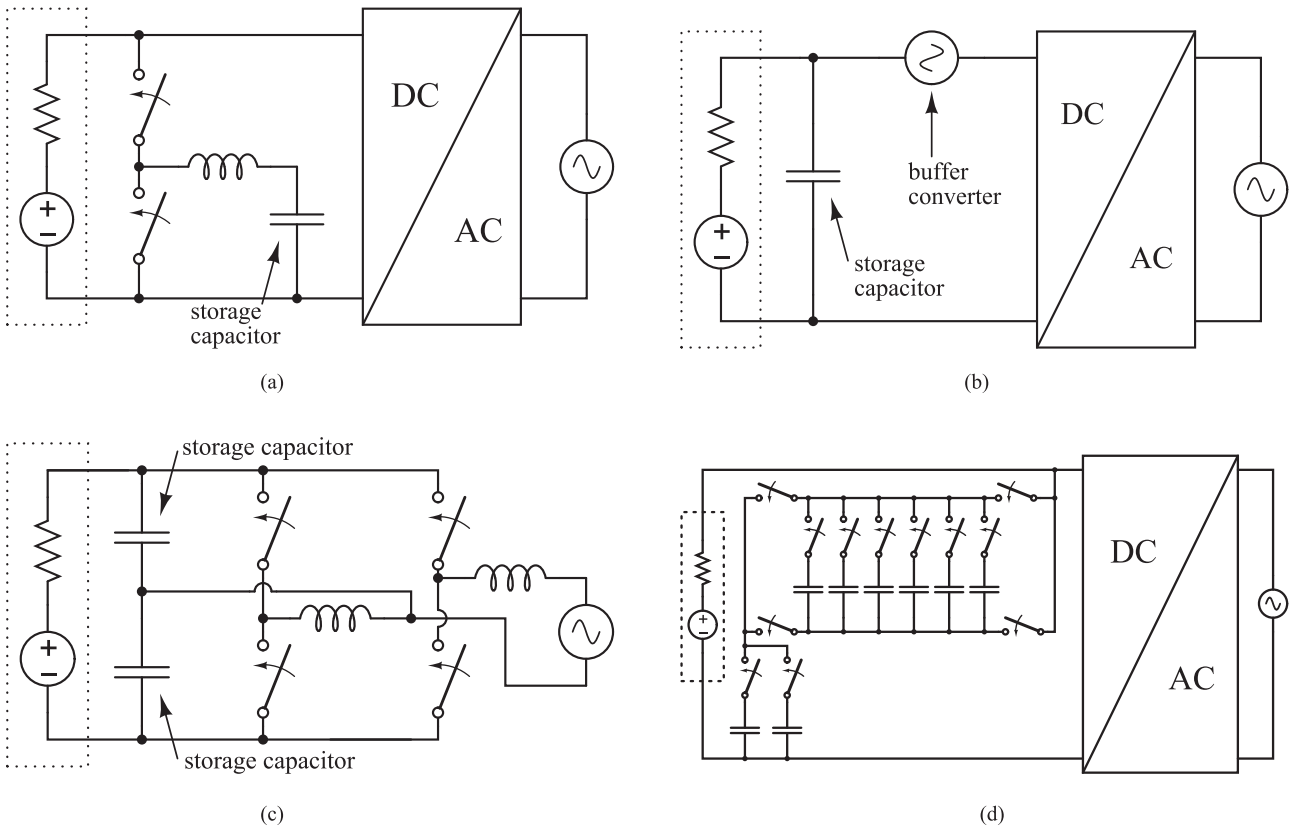


Fig. 3. Active decoupling solution examples in previous literature. (a) Full ripple port buffer. (b) Series voltage compensator. (c) Active-filter-integrated converter. (d) Stacked switched capacitor buffer.

from smaller energy storage capacitor is often offset by the volume overhead introduced by the buffer converter itself. Another major limitation is the efficiency penalty incurred by the buffer converter. As illustrated in Fig. 1, an average power of $\frac{2}{\pi}P_{\text{ave}}$ is flowing into, and then out of the capacitor in each cycle. Therefore, to the first order, the overall efficiency is approximately

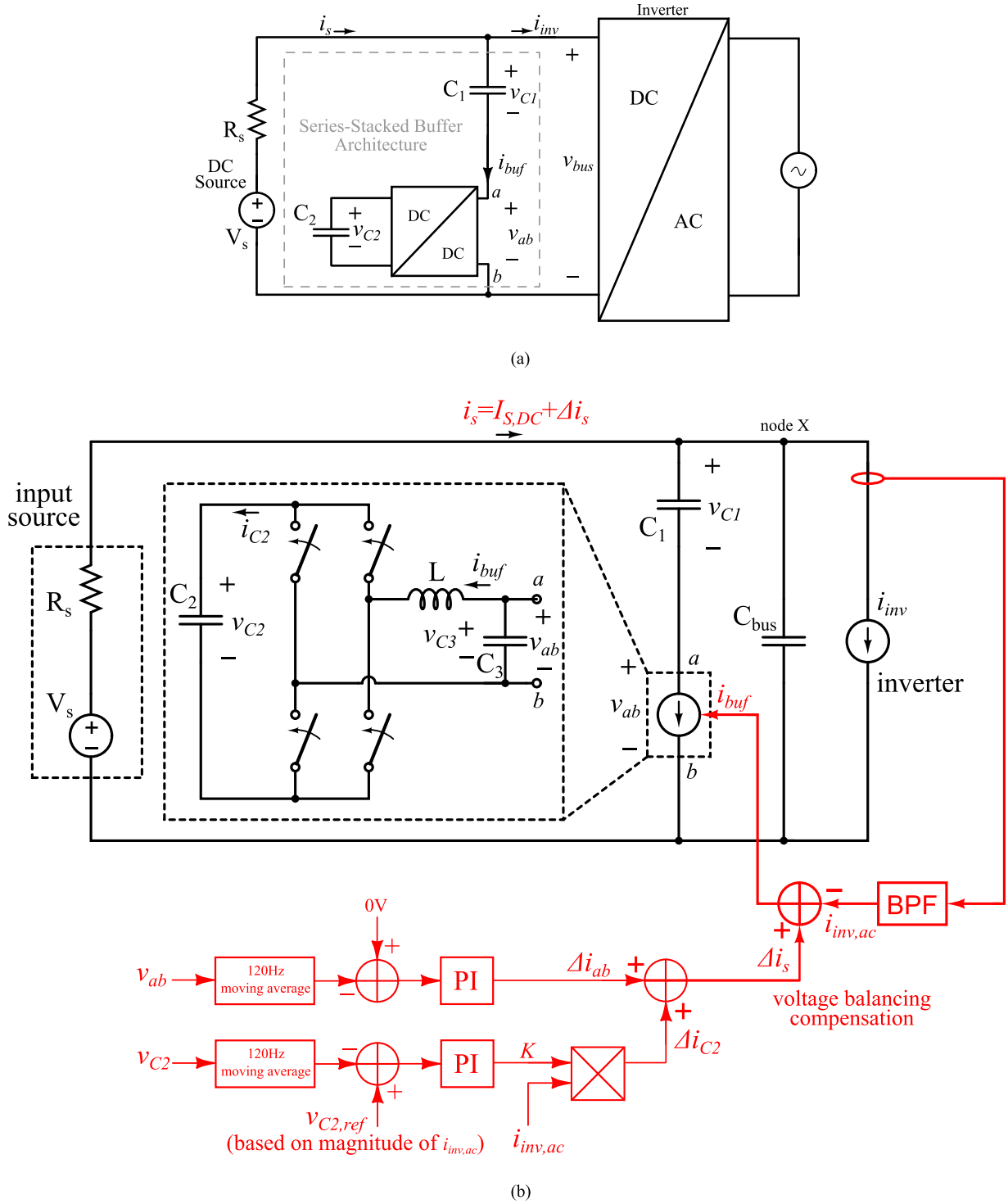
$$\eta \approx \eta_{\text{main}} - \underbrace{\frac{2}{\pi}(1-\eta_{\text{buffer}})}_{\text{efficiency penalty}}, \tag{2}$$

where η_{main} is the efficiency of the main inverter/rectifier and η_{buffer} is the efficiency of the buffer converter. Even if the buffer converter can be made efficient, since it is processing a large portion of the total power, it can still incur significant power loss.

To overcome the problem of low efficiency and high voltage stress, a series voltage compensator has been proposed in [10]. As shown in Fig. 3(b), this structure allows a very large voltage ripple on the capacitor. A buffer converter is connected in series with the dc–ac converter (or in series with the dc bus) to cancel this ripple, such that the dc–ac converter (or the dc bus) sees only a small ripple. The series connection of the buffer converter allows the buffer converter to see only the voltage ripple magnitude and to process only part of the total power. The main drawback is that the ripple is only reduced on one side (dc bus or dc–ac converter), while the other side that is directly connected to the capacitor lacks voltage regulation. Moreoever, the voltage swing on the capacitor is limited by the operating voltage of the converter connected to this capacitor.

Recently, an active-filter-integrated converter solution, as shown in Fig. 3(c), has been proposed [13], [14]. This solution is derived as a natural extension from the aforementioned works [4]–[9], [11], [12], but it is different in the sense that active decoupling is integrated into the operation of an H-bridge dc–ac converter through advanced control and no extra power components are added (except for splitting and rearranging some existing passive components). Since it does not require a distinct add-on decoupling stage, the system efficiency is not impaired. While this solution is effective in H-bridge converters, a key limitation is that it does not apply to all dc–ac converter topologies (e.g., unfolding inverters), as opposed to other active decoupling solutions that generally operates independent of the dc–ac converter topology. Moreover, the H-bridge transistors in this solution experience high voltage stress especially during light-load conditions (or equivalently, the output voltage range is limited).

An alternative approach to magnetic-based buffer converters is the stacked switched capacitor (SSC) buffer [15], [16]. One embodiment of the SSC buffer is shown in Fig. 3(d). The SSC buffer consists of an array of capacitors and switches. As the capacitors charge and discharge, the SSC buffer reconfigures the array in different series and parallel combinations to regulate the dc bus voltage. Compared to a magnetic-based converter that continuously processes the buffer power, the SSC buffer



(a)

(b)

Fig. 4. Diagrams of the proposed buffer architecture. (a) High-level schematic of the proposed buffer architecture. (b) Medium-level schematic of the proposed buffer architecture with a simplified circuit schematic of the full bridge converter implementations. The DC/AC converter is abstracted as a current sink. The buffer control scheme is highlighted in red color.

takes advantage of the natural stacking of capacitor voltages to maintain the dc bus voltage and only exercises the switches a few times in each line cycle to adjust the stacking. Hence, the power loss associated with the SSC architecture is greatly reduced. However, the configurations of the SSC are discrete in nature, so the bus voltage experiences a discontinuous jump whenever the SSC reconfigures. To meet a strict ripple requirement (e.g., a few percent), a complicated circuit with a large number of switches and capacitors has to be built. These components and their auxiliary circuits (i.e., the signal level shifting and gate

driving circuit) occupy a large PCB area, undermining the goal of high energy density.

The features and limitations of these previous solutions suggest the following desired characteristics: on one hand, we want the capacitor voltage stacking as in the SSC to reduce the buffer converter voltage stress and the amount of power that needs to be processed; on the other hand, we want the capability to regulate the bus voltage continuously as in magnetic-based converters such that strict ripple requirements can be met with a relatively simple circuit. Our proposed buffer architecture represents a hybrid solution that combines the best features of these two approaches. As shown in the following sections, the proposed architecture achieves very high efficiency and power density while tightly regulating the dc voltage; it achieves excellent buffering independent of the dc–ac converter topology and features a low-complexity circuit.

III. Operation Principle and Design Constraints

A. Analysis of Operation

The schematic of the proposed buffer architecture is shown in Fig. 4. Here, C_1 is the main energy storage capacitor and is allowed a relatively large ripple (e.g., 20% or more of the nominal voltage) to improve its energy utilization ratio. Unlike conventional active decoupling solutions that interface the dc bus through a parallel-connected buffer converter, C_1 is stacked in *series* with the buffer converter across the dc bus. With proper control (the control implementation is presented in Section IV), the buffer converter can behave as a controlled bidirectional current source to source/sink any instantaneous current difference between the dc side current i_s and the ac side current $i_{\rm inv}$. Capacitor C_1 is then charged and discharged in series with the converter to buffer the energy. Capacitors C_3 and $C_{\rm bus}$ are both small filter capacitors to absorb the switching transients, whose effect can be ignored at line frequency. With the aforementioned current control, the voltage across node a and b (i.e., v_{ab}) naturally varies contrary to the voltage change of C_1 (i.e., $v_{C1}+v_{ab}=$ constant). Moreover, since the instantaneous current difference (i.e., $i_{\rm buf}$) sums up to zero within a twice-line-frequency cycle, the energy is balanced each cycle and the buffer converter does not need an active energy source to fulfill its current source function. A support capacitor C_2 is used to maintain the necessary voltage for the correct operation of the buffer converter. Waveforms illustrating the aforementioned operation is shown in Fig. 5.

There are several possible topological implementations of the buffer converter, among which the full-bridge topology and the noninverting buck–boost topology show the most promise. A full-bridge implementation is shown in Fig. 4(b) and is used in the following analysis to illustrate the operation of the proposed buffer architecture. The analysis presented here is general. It applies to noninverting buck–boost and other topologies as well.

Consider a single-phase inverter with unity power factor, as shown in Fig. 4(a). The inverter input power is given as

$$P_{\rm inv,in}=v_{\rm bus}i_{\rm inv}, \tag{3}$$

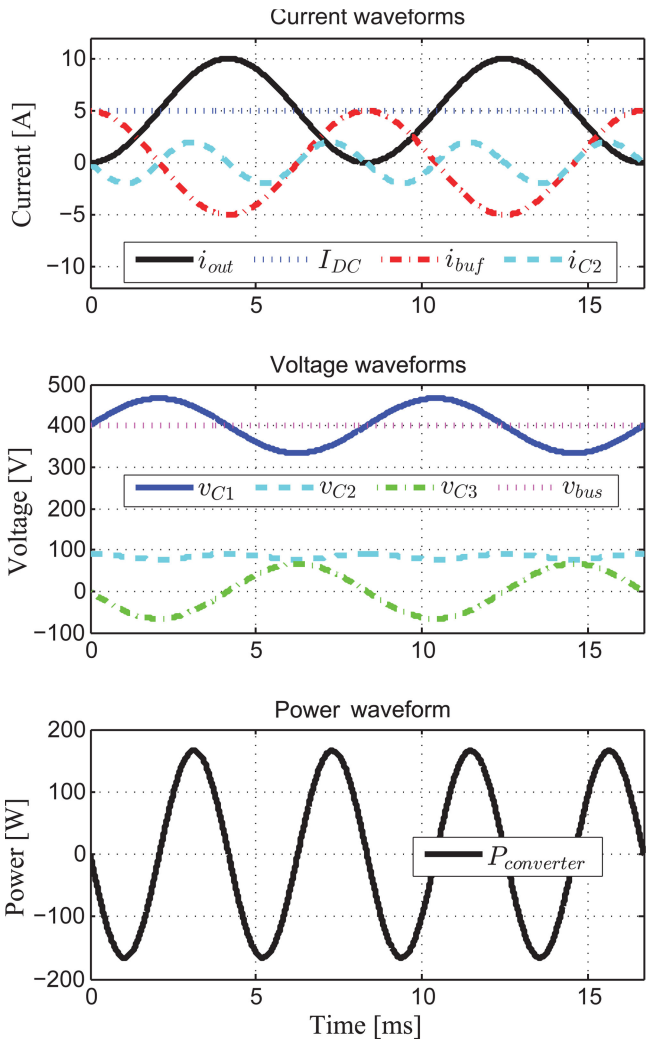


Fig. 5. Key waveforms illustrating the operation of the proposed buffer. The waveforms are calculated for the numerical example outlined in Section III-B (2-kW load power, 400-V bus voltage).

where $v_{\rm bus}$ is the dc bus voltage and $i_{\rm inv}$ is the current flowing into the inverter. Its output power is given as

$$\begin{aligned} P_{\rm inv,out}&=v_{\rm AC}i_{\rm AC}=V_{\rm AC}\sin(\omega t)\times I_{\rm AC}\sin(\omega t)\\ &=V_{\rm AC}I_{\rm AC}\frac{1-\cos(2\omega t)}{2}, \end{aligned} \tag{4}$$

where ω is the line angular frequency, and $V_{\rm AC}$ and $I_{\rm AC}$ are the ac output voltage and current amplitude, respectively. Assuming a certain inverter efficiency η, it is easy to show that

$$\begin{aligned} &P_{\rm inv,out}=\eta P_{\rm inv,in}\\ &\Rightarrow i_{\rm inv}=\frac{\eta V_{\rm AC}I_{\rm AC}}{v_{\rm bus}}\frac{1-\cos(2\omega t)}{2}. \end{aligned} \tag{5}$$

Given a constant $v_{\rm bus}$, the inverter input current $i_{\rm inv}$ resembles the shape of a shifted sine wave, whose average equals the average input current from the dc source, $I_{S,\rm DC}$ (i.e., $<i_{\rm inv}>=I_{S,\rm DC}$), as shown by the current waveforms in Fig. 5. To maintain a constant dc bus voltage, the current through the buffer branch, $i_{\rm buf}$, should take up the instantaneous difference

between $i_{\rm inv}$ and $I_{S,\rm DC}$. In our proposed architecture, this can be achieved with appropriate control of the full-bridge converter, as presented in Section IV. Then, by the KCL at node X in Fig. 4(b), the small filter capacitor $C_{\rm bus}$ should have no current (except for the switching frequency filtering), and therefore, maintain a constant bus voltage. The instantaneous *change* of charge and voltage on C_1 is given by

$$\Delta q_1 = \int i_{\rm buf} dt = \int (i_{\rm inv} - i_{S,\rm DC}) dt, \tag{6}$$

$$\Delta v_{C1} = \frac{\Delta q_1}{C_1}. \tag{7}$$

Since the aforementioned current control ensures a constant bus voltage

$$\Delta v_{ab} = -\Delta v_{C1}. \tag{8}$$

As will be shown in Section V, the buffer converter uses a small inductor and is designed to switch at a high frequency (several hundred kilohertz). Its switching ripple and other dynamics can thus be ignored in the line frequency analysis. Assuming bipolar pulsewidth modulation (PWM) control of the buffer converter, the voltages of its two ports [i.e., v_{ab} and v_{c2} in Fig. 4(b)] can be related by the converter duty ratio d as

$$\frac{v_{ab}}{v_{C2}} = 2d - 1. \tag{9}$$

Similarly, the currents of the two ports of the full-bridge converter in Fig. 4(b) can be related by the converter duty ratio d as

$$\frac{i_{ab}}{i_{C2}} = \frac{i_{\rm buf}}{i_{C2}} = \frac{1}{2d-1}, \tag{10}$$

since the buffer current $i_{\rm buf}$ flows through port ab. From (10) and (7), the change of charge on C_2 can be obtained as

$$\begin{aligned}\Delta q_2 = \int i_{C2} dt &= \int (2d-1) i_{\rm buf} dt \\ &= (2d-1)\Delta q1. \end{aligned} \tag{11}$$

Thus, the instantaneous charge on C_2 is given as

$$q_2 = Q_{2,\rm init} + \Delta q_2 = Q_{2,\rm init} + (2d-1)\Delta q_1, \tag{12}$$

where $Q_{2,\rm init}$ is the initial charge on C_2 at the beginning of every twice-line-frequency cycle. Moreover, from (9), it can be derived that

$$v_{C2} = \frac{1}{2d-1} v_{ab} = \frac{1}{2d-1}(\Delta v_{ab} + V_{ab,\rm init}), \tag{13}$$

where $V_{ab,\rm init}$ is the initial voltage across terminal a and b at the beginning of every twice-line-frequency cycle. As discussed in Section IV, $V_{ab,\rm init}$ can be set by appropriate control in a practical implementation. Choosing $V_{ab,\rm init} = 0$ by design and substituting (7) and (8) into (13) gives

$$v_{C2} = -\frac{1}{2d-1}\frac{\Delta q_1}{C_1}. \tag{14}$$

Combining (14) and (12) through $q_2 = C_2 v_{C2}$ renders

$$\Delta q_1 m^2 + Q_{2,\rm init} m + C_2 \frac{\Delta q_1}{C_1} = 0, \tag{15}$$

where $m = 2d - 1$ is the conversion ratio of the full-bridge converter. The aforementioned analysis applies to noninverting buck–boost converter and other converter topologies as well, except that the conversion ratio m needs to be changed accordingly.

In (15), the only operation-dependent variable is Δq_1, which is fully determined by the inverter current $i_{\rm inv}$ according to (7). $Q_{2,\rm init}$, C_2, and C_1 are all selected by the component and control design choices. Solving (15) for m will give the instantaneous conversion ratio and duty ratio of the buffer converter, from which all the voltages and current waveforms can be calculated according to (8) through (14). The waveforms in Fig. 5 are obtained in MATLAB by first solving (15), and then, inserting the solution into (8) through (14), given the $i_{\rm inv}$ of the 2-kW inverter.

B. Numerical Example

In order to illustrate the operation of the proposed buffer architecture and to establish a common baseline for comparison, consider a numerical example according to the specifications outlined in the Google/IEEE Little Box Challenge: a 2-kW, 60-Hz inverter/rectifier with 400-V dc bus voltage and up to 3% ripple ($\pm$6 V around 400 V) [24]. Note that this example is chosen only for illustrative purposes; the proposed architecture is applicable to a much larger voltage and power range. If one can design an ideal magnetic-based buffer converter to charge and discharge the buffer capacitor(s) between 406 and 0 V, it can be calculated from (1) that only 64 μF of the buffer capacitor is required (at the price of larger buffer converter volume and lower efficiency, as discussed in Section II). This capacitor volume represents the ideal case where the rated voltage is fully utilized for energy storage. On the opposite extreme, if only a conventional passive decoupling solution is used, at least 1.1 mF is required for the dc bus capacitor bank to maintain less than 3% ripple. Moreover, if practical ripple current limitations of electrolytic capacitors are taken into consideration in a passive filtering solution, even larger capacitors are typically needed. Practical active decoupling solutions will result in capacitor requirement somewhere between the two aforementioned extremes.

If in this example, we choose to allow a 130 V (32%) ripple on C_1, then its capacitance is determined through (7) to be 100 μF. Furthermore, C_2 is chosen to be 430 μF (exact design guideline for C_2 sizing is provided in Section III-C). Using the equations derived in Section III-A, all the component voltages and currents for this 2-kW example can be calculated. Fig. 5 plots some key voltage waveforms calculated in MATLAB to illustrate the operation of the buffer for one line cycle.

As shown in Fig. 5, the current stress on the buffer converter depends on the ripple current (i.e., maximum of $i_{\rm buf}$), while the voltage stress on the buffer converter (i.e., maximum of v_{C2}) is less than 25% of the bus voltage. Such low voltage stress allows for the use of low-voltage rating transistors with low device capacitance and low on-resistance. Fig. 5 also plots the instantaneous power processed by the buffer converter, which is defined as $P_{\rm conv} = v_{ab} i_{\rm buf}$. While the *peak* power of the

entire buffer architecture is 2 kW, the *peak* power processed by the converter is only 166 W, less than 8.4% of that of the entire buffer architecture. Since the converter is only processing a fraction of the full power, the converter power rating (and thus, physical size) can be made small. Furthermore, the overall efficiency is approximately

$$\eta \approx \eta_{\text{main}} - \underbrace{\frac{2}{\pi}(1-\eta_{\text{buffer}}) \times 8.4\%}_{\text{efficiency penalty}}, \tag{16}$$

which is considerably higher than a conventional active decoupling architecture, as given by (2). Note that (16) is approximate, as the buffer converter efficiency (η_{buffer}) varies somewhat across the full line cycle. This equation, while approximate, does capture the key point that less power is processed by the buffer converter, which leads to higher overall efficiency.

C. Design Constraints

Equation (15) reveals important design guidelines for the buffer converter. To achieve the aforementioned benefits, the choice of components values and operating parameters has to meet certain constraints for the design to be practical. For a practical full-bridge converter, the conversion ratio is constrained by

$$-1 < m < 1 \tag{17}$$

to avoid overmodulation. The choice of components values and operating parameters (i.e., C_1, C_2, and $Q_{2,\text{init}}$) should guarantee that for all Δq_1 values within a line cycle, (15) has a solution for m within the range of (17). Therefore, the design constraint on the values of C_1, C_2, and $Q_{2,\text{init}}$ is

$$\left| \frac{-Q_{2,\text{init}} + \sqrt{Q_{2,\text{init}}^2 - 4\Delta q_1^2 \frac{C_2}{C_1}}}{2\Delta q_1} \right| < 1 \tag{18}$$

and

$$\delta = Q_{2,\text{init}}^2 - 4\Delta q_1^2 \frac{C_2}{C_1} \geqslant 0, \tag{19}$$

where δ is the discriminant of (15). Substituting $Q_{2,\text{init}} = C_2 V_{2,\text{init}}$ and simplifying (19) results in

$$\frac{1}{2} C_2 V_{C2,\text{init}}^2 \geqslant 2\frac{\Delta q_{1,\max}^2}{C_1}. \tag{20}$$

This result indicates that for proper operation, the support capacitor C_2 needs to have a certain minimum *initial energy* stored at the beginning of each cycle. This can be ensured through appropriate sizing of C_2 and proper precharge during system startup. Furthermore, substituting $Q_{2,\text{init}} = C_2 V_{2,\text{init}}$ and simplifying (18) results in

$$\frac{C_2}{C_1 + C_2} V_{C2,\text{init}} > |\Delta v_{C1,\max}| = |\Delta v_{ab,\max}|. \tag{21}$$

This result indicates that the lowest value of v_{C2} has to be larger than the maximum ripple of v_{ab} (i.e., as shown in the voltage waveforms in Fig. 5, the dashed blue signal has to be higher than the dash-dotted red signal any time within a cycle), which can be ensured by proper sizing of C_1 and C_2 and proper precharge of C_2. To facilitate calculation, (20) and (21) can be written as

$$\sqrt{C_1 C_2} V_{C2,\text{init}} \geqslant 2|\Delta q_{1,\max}| \tag{22}$$

and

$$\frac{C_1 C_2}{C_1 + C_2} V_{C2,\text{init}} > |\Delta q_{1,\max}|, \tag{23}$$

where $\Delta q_{1,\max}$ is a known variable determined by the load. The parameters C_1, C_2, and $V_{2,\text{init}}$ need to be selected within these constraints in the design. In fact, it can be derived that (22) holds as long as (23) is satisfied, so in practice, (23) is a sufficient design constraint. Based on the aforementioned constraint, the circuit parameters of the example in Fig. 5 are chosen as $C_1 = 100$ μF, $C_2 = 430$ μF, and $V_{2,\text{init}} = 90$ V. Note that although the capacitance of C_2 is larger than C_1, C_2 is rated at a much lower voltage, so its physical volume in a practical implementation will be smaller than that of C_1, as demonstrated in Section V.

In general, given the full-load inverter current, the selection of capacitors C_1 and C_2 can be optimized for the smallest volume under the constraint defined in (23) [45]. The choice of other components such as L and C_3 is based on efficiency and ripple considerations in the same way as in typical converter designs, and is introduced in Section V. Although the aforementioned analysis is for a full-bridge converter, it applies to non/inverting buck–boost converter and other circuit topologies as well, as long as (17) is modified accordingly. The full-bridge converter was chosen here because it enables higher capacitor utilization of C_1, as it allows for bipolar voltage swing. A benefit of using a noninverting buck–boost converter is that it relaxes the energy storage requirement on C_2, since it does not require v_{C2} to be larger than v_{ab}. The optimal topology for the smallest overall size depends on the bus voltage and load current of the application, as well as practical implementation issues such as component selection. A detailed comparison will be pursued in future work. The rest of this paper will focus on the full-bridge topology for control implementation and experimental verification.

IV. Control Implementation

While (15) reveals the duty ratio of the proposed buffer architecture during its operation, it is not the most suitable form for real-time control implementation. Instead, we propose a current hysteresis control method to reduce the required real-time computation. Moreover, real-world factors such as loss and measurement error may greatly affect the performance of the buffer. In this section, we identify these control challenges and describe our solutions.

A. Control for Bulk Energy Buffering

The key to maintaining a constant bus voltage is to precisely control the buffer current i_{buf} to match the difference between the dc source current $I_{S,\text{DC}}$ and the inverter current i_{inv}, as

shown in Fig. 4(b). This difference equals to the ac component of $i_{\rm inv}$, since $I_{S,\rm DC}$ and $i_{\rm inv}$ have the same *average* value.

The inverter current $i_{\rm inv}$ is, therefore, measured and bandpass filtered to extract its double-line-frequency component (i.e., $i_{\rm inv,ac}$) and used as the reference for $i_{\rm buf}$, as illustrated pictorially in Fig. 4(b). The bandpass filter consists of a low-pass filter in the analog sensing circuit and a digital moving average filter in the microcontroller. The low-pass filter in the analog sensing circuit is intended to filter out the switching ripple of the inverter. The moving average filter at 120 Hz is implemented in the microcontroller to obtain the dc component, and the measured signal is substracted by the dc component. This effectively forms a high-pass filter to remove the dc component. Note that $i_{\rm buf}$ should take the opposite value of $i_{\rm inv,ac}$, i.e., $i_{\rm buf} = -i_{\rm inv,ac}$, as indicated in the figure.

Inductor current hysteresis control is employed in this application to ensure that $i_{\rm buf}$ closely follows the reference. The widely used constant frequency feedback control techniques such as average current-mode control [25] is not used as it is challenging to implement in this application: although current-mode control with bidirectional power transfer capabilities has been proposed [26] in other scenarios, small-signal analysis of the full-bridge buffer converter in this architecture reveals that a low-frequency right half-plane zero (RHP) exists in the system. The frequency of this RHP approaches dc when $i_{\rm buf}$ approaches zero value (which happens every cycle given its sinusoidal nature), making the system very hard to stabilize. Given these small-signal characteristics of the proposed architecture, the inductor current hysteresis control is chosen instead.

Note that the proposed current control method reacts only to the ac component but not dc component of i_s, so the buffer branch behaves like a virtually infinite capacitor to the twice-line-frequency current, while it does not affect the dc bus voltage level at all. The dc bus voltage level is set by other circuits external to the buffer (e.g., the power factor correction (PFC) front end in a ac/dc converter), so the proposed buffer circuit can be seamlessly integrated into existing ac/dc or dc/ac converter as a dc bus capacitor replacement, without changing the existing design or control method of these systems.

B. Capacitor C_1 Voltage Balancing

Since the main capacitor C_1 is connected in series with the buffer converter, ideally $i_{\rm buf}$ should be a pure 120-Hz ac waveform such that the voltage across C_1 is balanced in each cycle. In steady-state operation, the cycle average (i.e., dc component) of v_{C1} should equal the bus voltage and the average of v_{ab} should be zero. In practice, errors from multiple sources exist in the current hysteresis control, so $i_{\rm buf}$ might contain a small dc component. This dc offset error, if left unchecked, will keep charging or discharging C_1 over multiple cycles and cause the average values of v_{C1} and v_{ab} to drift. As mentioned in Section III, the amplitude of v_{ab} has to remain smaller than that of v_{C2} for the correction operation of the full-bridge buffer converter. Therefore, this drift, if left uncompensated, will accumulate and eventually disrupt the operation of the buffer converter. In our proposed control scheme, v_{ab} is measured and averaged every 120-Hz cycle. As shown in Fig. 4(b), the error between the average of v_{ab} and its reference value (i.e., 0 V) is passed through a proportional-integral (PI) controller to generate a dc correction term Δi_{ab}. This term is added to the reference of $i_{\rm buf}$ to correct this dc offset, such that the buffer current is pure ac.

C. Capacitor C_2 Voltage Balancing

In the proposed architecture, C_2 is charged through the buffer converter and since the buffer current $i_{\rm buf}$ is pure ac, ideally the voltage across C_2 should be balanced every cycle such that its average value remains constant. In practice, however, the buffer converter incurs certain power loss while charging and discharging C_2 in a cycle. If uncompensated, such loss will gradually decrease the average voltage of C_2 over multiple cycles to the point that v_{C2} is lower than v_{ab} and the normal operation of the full-bridge converter is disrupted. Care has to be taken in any effort to directly extract additional current from the dc bus to charge C_2, since it will create a dc offset in $i_{\rm inv}$ and cause C_1 imbalance. This would conflict with the control loop that balances C_1. Adding a dedicated auxiliary circuit to draw power from the dc bus to charge C_2 and compensate for this loss is also undesirable since it contradicts the goal of small converter volume and low component voltage stress. In this study, we develop a compensation scheme that makes use of the existing small bus voltage ripple to provide extra energy to C_2 without affecting C_1. The derivation of this compensation scheme is presented below.

Consider the buffer current reference $i_{\rm buf}$ in Fig. 4(b) where a compensation term $\Delta i_{C2}(t)$ is added such that

$$i_{\rm buf} = -i_{\rm inv,ac} + \Delta i_{C2}, \tag{24}$$

where $i_{\rm inv,ac}$ is the ac component of $i_{\rm inv}$ as discussed in Section IV-A. At the same time, in periodic steady state, the dc component of $i_{\rm inv}$ should equal the dc source current i_s, i.e.

$$< i_{\rm inv} > \; = I_{S,\rm DC}. \tag{25}$$

By the KCL, at the output node

$$i_s = i_{\rm buf} + i_{\rm inv}. \tag{26}$$

Substituting (24) and (25) into (26) renders

$$\begin{aligned} i_s &= (-i_{\rm inv,ac} + \Delta i_{C2}) + (< i_{\rm inv} > + i_{\rm inv,ac}) \\ &= I_{S,\rm DC} + \Delta i_{C2}. \end{aligned} \tag{27}$$

As $i_{\rm buf}$ flows through C_1, the instantaneous voltage on C_1 is

$$v_{C1}(t) = V_{C1,\rm DC} + \frac{\int_0^t i_{\rm buf} d\tau}{C_1}. \tag{28}$$

Moreover, in steady state

$$V_{C1,\rm DC} = V_s - R_s \times I_{S,\rm DC}. \tag{29}$$

Ignoring the effect of the small filter capacitor $C_{\rm bus}$, it can be shown that

$$v_{C1} + v_{ab} = v_{\rm bus} = V_s - R_s \times i_s. \tag{30}$$

Substituting (27)–(29) into (30), the voltage across terminal *a* and *b* of Fig. 4(b) is given as

$$v_{ab} = V_s - R_s \times (I_{S,\mathrm{DC}} + \Delta i_{C2}) - v_{C1} = -\Delta i_{C2} R_s - \frac{\int_0^t i_{\mathrm{buf}} d\tau}{C_1}. \quad (31)$$

Furthermore, based on (28), maintaining the average voltage on C_1 every twice line frequency cycle requires

$$v_{C1}\left(\frac{1}{120}\right) = v_{C1}(0) = V_{C1,DC} \Rightarrow \int_0^{\frac{1}{120}} i_{\mathrm{buf}} d\tau = 0. \quad (32)$$

Since $i_{\mathrm{inv,ac}}$ is pure ac at 120 Hz

$$\int_0^{\frac{1}{120}} i_{\mathrm{inv,ac}} d\tau = 0. \quad (33)$$

Combining (24), (32), and (33) yields the constraint on the compensation term Δi_{C2}, i.e.,

$$\int_0^{\frac{1}{120}} \Delta i_{C2} d\tau = 0. \quad (34)$$

This constraint suggests that a good compensation term for C_2 voltage balancing would be a pure ac signal at 120 Hz.

The net energy flowing into the buffer converter within *one cycle* is

$$E_{\mathrm{conv}} = \int_0^{\frac{1}{120}} v_{ab} i_{\mathrm{buf}} dt. \quad (35)$$

Substituting (31) and (24) into (35) results in (36), shown at the bottom of the page. Furthermore, we can make the observation that if Δi_{C2} takes the form

$$\Delta i_{C2} = -K i_{\mathrm{inv,ac}}, \quad (37)$$

where K is a multiplying factor, (37) certainly satisfies the constraint outlined in (34) since $i_{\mathrm{inv,ac}}$ is a pure ac waveform at 120 Hz. Moreover, with Δi_{C2} given by (37), the buffer converter net energy given by (36) can be simplified as shown in (38), shown at the bottom of the page. Note that since $i_{\mathrm{inv,ac}}$ is a pure sine wave, $\int_0^t i_{\mathrm{inv,ac}} d\tau$ will be exactly out of phase with $i_{\mathrm{inv,ac}}$. Thus, the integral of their product over a full cycle is zero. Therefore, the second term in (38) equals zero and

$$E_{\mathrm{conv}} = -K(1+K) R_s \int_0^{\frac{1}{120}} i_{\mathrm{inv,ac}}^2 dt. \quad (39)$$

As long as $-1 < K < 0$, the net energy will be larger than zero to provide loss compensation to the buffer converter. At the same time, this compensation will not affect the average voltage on C_1 since it satisfies (34). The average power loss compensation this scheme can provide is given by

$$P_{\mathrm{comp}} = E_{\mathrm{conv}} f, \quad (40)$$

where f is the twice line frequency. Note that in principle, this compensation scheme is effective not only with pure 120-Hz waveform but also when higher order harmonics are present, such as in certain PFC applications. Analysis and experimental verifications of such applications are in progress.

To implement this compensation, the average value of v_{C2} is measured every cycle. A PI controller is employed to adjust K between -0.5 and 0 based on the error between the measured average and desired reference value of v_{c2} to maintain the average voltage level of C_2, as shown in Fig. 4. The parameters of the PI controller are fine tuned manually to obtain a good response. Essentially, this compensation scheme intentionally adjusts i_{buf} to slightly mismatch $i_{\mathrm{inv,ac}}$ to create a small dc bus ripple represented by $\Delta i_{C2} R_s$. As will be shown in the experiment, in steady-state operation, the bus voltage ripple is typically less than 2% of the nominal bus voltage in all load range, while providing enough compensation to maintain C_2 voltage. During startup, as the dc bus voltage increases, the C_2 voltage balancing loop naturally charges C_2 to the desired voltage level.

Fig. 6 plots the power loss compensated by this scheme as a function of the input current ripple amplitude during full-load (2 kW) operation of the buffer. The maximum amount of energy compensation that this scheme is able to provide in each cycle can be calculated from (39) with $K = -0.5$. Under full-load condition, this compensation scheme can compensate for an average power loss of up to 31W. Given that the buffer converter is only processing an average power of about 100W as discussed in Section III, the proposed compensation scheme is practically feasible, even for very low efficiency converters. As the

$$E_{\mathrm{conv}} = -\int_0^{\frac{1}{120}} \Delta i_{C2} R_s i_{\mathrm{buf}} dt - \frac{1}{C_1}\int_0^{\frac{1}{120}} \left(\int_0^t i_{\mathrm{buf}} d\tau\right) i_{\mathrm{buf}} dt = -\int_0^{\frac{1}{120}} \Delta i_{C2} R_s (-i_{\mathrm{inv,ac}} + \Delta i_{C2}) dt - \frac{1}{C_1}\int_0^{\frac{1}{120}} \left(\int_0^t (-i_{\mathrm{inv,ac}} + \Delta i_{C2}) d\tau\right)(-i_{\mathrm{inv,ac}} + \Delta i_{C2}) dt \quad (36)$$

$$E_{\mathrm{conv}} = -\int_0^{\frac{1}{120}} -K i_{\mathrm{inv,ac}} R_s (-1-K) i_{\mathrm{inv,ac}} dt - \frac{1}{C_1}\int_0^{\frac{1}{120}} \left(\int_0^t (-1-K) i_{\mathrm{inv,ac}} d\tau\right)(-1-K) i_{\mathrm{inv,ac}} dt = -K(K+1) R_s \int_0^{\frac{1}{120}} i_{\mathrm{inv,ac}}^2 dt - \frac{(1+K)^2}{C_1}\int_0^{\frac{1}{120}} \left(\int_0^t i_{\mathrm{inv,ac}} d\tau\right) i_{\mathrm{inv,ac}} dt \quad (38)$$

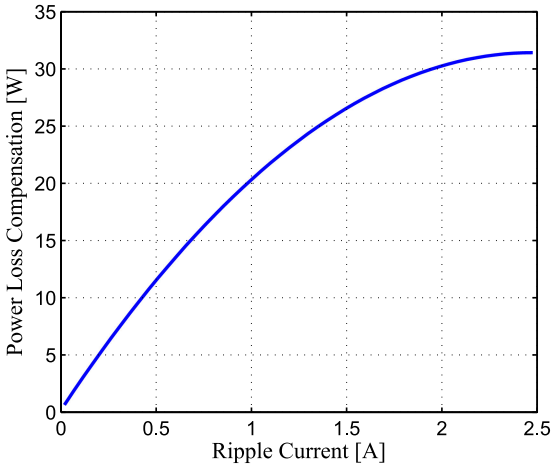


Fig. 6. Power provided by the proposed C_2 compensation scheme as a function of the input current ripple amplitude under full-load condition.

load current decreases, the compensation capability decreases as well, but the power that needs to be processed by the buffer converter also decreases, so the power loss is also reduced. A light-load control scheme will be introduced in Section IV-F to further reduce the power loss at light-load condition. The proposed compensation scheme thus scales well with different load power levels.

It is important to note that besides loss compensation, this C_2 voltage balancing feedback loop also improves current matching of $i_{\rm buf}$ to $i_{\rm inv,ac}$. While the C_1 voltage balancing feedback loop eliminates the offset error (dc component) as discussed in Section IV-B, the C_2 voltage balancing feedback loop corrects the gain error (ac component magnitude mismatch). To see this, suppose the magnitude of $i_{\rm buf}$ is considerably smaller than that of $i_{\rm inv,ac}$ because of a gain error. This mismatch will cause a undesirable ripple on the dc bus voltage. Conceptually, this mismatch has the same effect as if there is no gain error, but the multiplying factor K is too close to -0.5. As a result, according to (39), C_2 will have more energy compensated than the loss, so v_{C2} will increase. The C_2 voltage balancing feedback loop will then adjust K and thus Δi_{C2} to balance v_{C2}. This effectively corrects the mismatch between $i_{\rm buf}$ and $i_{\rm inv,ac}$ with Δi_{C2}, except for the small amount of mismatch intentionally introduced for C_2 compensation. In other words, the C_2 voltage balancing loop will minimize the gain error of current matching, and thus the dc bus voltage ripple, while maintaining sufficient compensation to C_2 to keep its average voltage at the desired level.

D. Steady-State Simulation

A simulation in PLECS is performed to verify the circuit design calculated according to Section III and the control method just presented previously. The circuit parameters used in the simulation are listed in Table I. The design requirements are specified according to [24] and the capacitor sizing are chosen following the design procedure, as discussed in Section III-C. Other circuit parameters in Table I such as filter inductor L_f are chosen according to the general design procedure of

TABLE I
BUFFER DESIGN EXAMPLE

Application requirements	Nominal power	2 kW
	Nominal input current	5 A
	DC source voltage	450 V
	DC source resistance	10 Ω
Circuit parameters	Main capacitor C_1	100 μF
	Support capacitor C_2	430 μF
	Filter inductor L_f	94 μH
	Filter capacitor C_3	1 μF
	DC bus capacitor $C_{\rm bus}$	5 μF
	Current hysteresis band	$I_{\rm ref} \pm 1$A

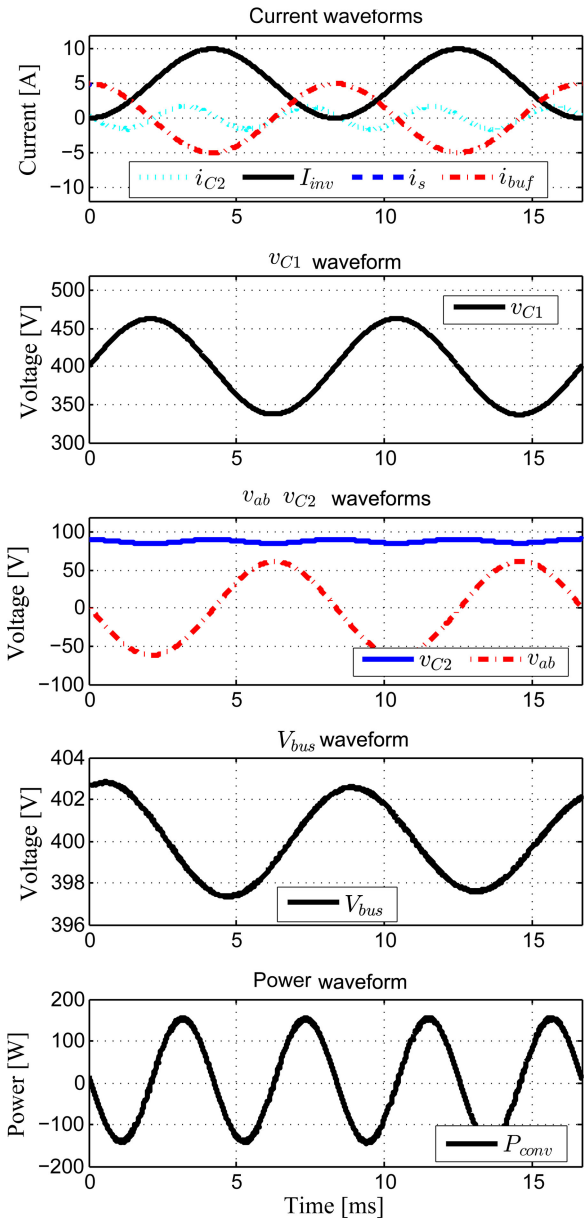


Fig. 7. Simulation waveforms in PLECS illustrating steady-state operation of the series-stacked buffer architecture. Note that i_{C2} in the simulation contains current ripple due to the converter switching, while the i_{C2} waveform shown in this figure is a low-pass-filtered version for better clarity of illustration.

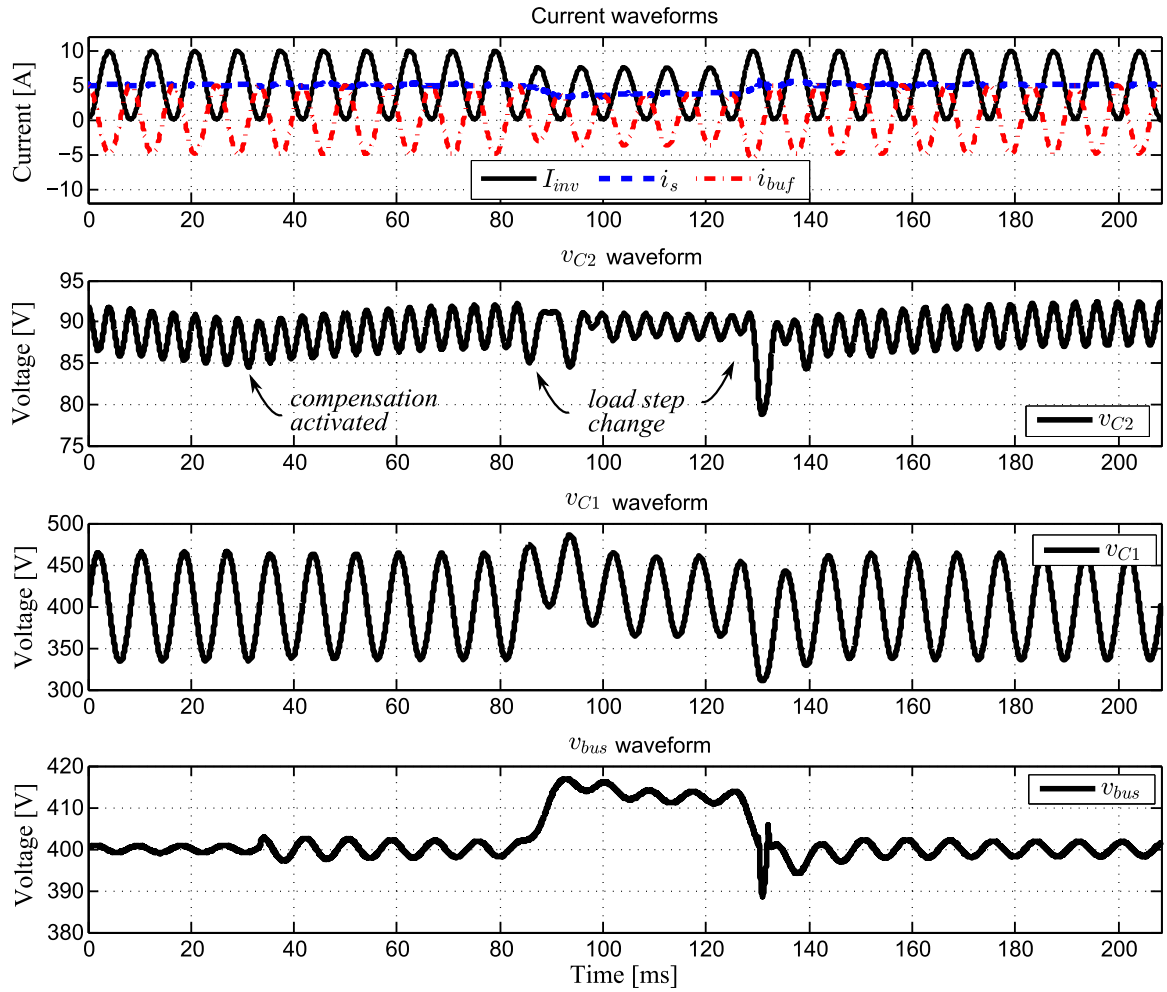


Fig. 8. Simulation waveforms in PLECS illustrating the effects of the voltage balancing compensation loops during transients. Initially, no compensation loop is activated. At $t = 30$ ms, both compensation loops are activated. At $t = 83.3$ ms, the load current takes a step change from 5 to 3.75 A. At $t = 125$ ms, the load current takes a step change from 3.75 to 5 A.

magnetic-based converters. The control method is implemented with C-script in the PLECS simulation. The simulation incorporates practical factors such as loss in the converter, analog-to-digital converter (ADC) sampling delay and quantization, etc. The simulated waveforms are shown in Fig. 7, which matched closely with the calculated waveform in Section III. Note that i_{C2} in the simulated waveform contains current ripple due to the converter switching, while i_{C2} in the calculated waveform is the low-pass-filtered version of its simulated counterpart.

E. Transient Simulation

The two voltage balancing control loops maintain the voltages on the capacitors during steady-state operation and also make them settle quickly to a new steady state in case of a load transient. To demonstrate the effect of these voltage balancing control loops, a PLECS simulation example is illustrated in Fig. 8. The simulation condition is the same as in Table I expect that the load power experiences a step change. As shown in Fig. 8, no compensation loop is activated initially, so the average voltage of C_2 keeps decreasing owing to the converter loss. Once the compensation loops are activated (at $t = 30$ ms), the average value of v_{C2} is regulated. Since this compensation scheme takes advantage of the existing ripple, it does not add much extra ripple to the dc bus in steady state, as illustrated by the bus voltage waveform of Fig. 8. In the event of a load change, the C_1 compensation loop quickly adjusts the average value of v_{C1} such that the bus voltage settles to the new steady state within just a few cycles. The average value of v_{C2} is maintained throughout this process.

F. Implementation Considerations for Light-Load and Reactive-Load Conditions

As shown by (27), the compensation term Δi_{C2} adds a ripple to the dc input current. Some applications require the ripple current to be smaller than a certain percentage of the dc value (e.g., 20% in [24]), which imposes a limit on the value of K. At the same time, the amount of buffer converter power loss that can be compensated is quadratically proportional to the ac component of the inverter current $i_{\mathrm{inv,ac}}$, as calculated in (39). Note that the buffer converter current ideally equals to $i_{\mathrm{inv,ac}}$. Therefore, to adequately compensate the buffer converter power loss while still staying within dc side

TABLE II
COMPONENT LISTING FOR THE ACTIVE ENERGY BUFFER

Component	Mfr. and Part number	Parameters	Notes
GaN FETs	EPC EPC2016C	100 V, 16 mΩ	
Capacitors ($C_{\rm bus}$)	TDK C5750X6S2W225K250KA × 10	450 V, 2.2 μF	0.431μF at 400V
Capacitors (C_1)	TDK C5750X6S2W225K250KA × 239	450 V, 2.2 μF	0.431μF at 400V
Capacitors (C_2)	TDK CGA9P3X7S2A156M250KB × 126	100 V, 15 μF	3.44μF at 80V
Capacitors (C_3)	TDK C3225X5R2A225M230AB × 2	100 V, 2.2 μF	
Inductors (L_1, L_2)	Vishay IHLP6767GZER470M11	8.6 A, 47 μH	
Power isolators	Analog Devices ADuM5210		
Logic level shifters	Texas Instruments SN74LV4T125PWR		
Microcontroller	Texas Instruments TMX320F28377D		
Current Sensing Amp	Linear Technology LT1999		
Voltage Sensing Amp	Linear Technology LT1990		

ripple specifications, the buffer converter power loss needs to scale quadratically with $i_{\rm inv,ac}$ as well. In other words, the buffer converter power loss needs to scale quadratically with the buffer converter current.

The power loss calculation of synchronous buck/full-bridge type converters has been thoroughly studied in the literature [27]–[29] and this paper will not repeat the details. At a high level, the conduction related losses (MOSFET on-resistance, capacitor equivalent series resistance, winding, and sensing resistance) scale quadratically with the converter current that aligns well with the loss compensation capability as discussed previously. The switching related losses scale quadratically with the voltage (capacitive turn-on), or linearly with the product of both (MOSFET overlap), or other factors (core loss, gate drive loss). To align scaling of these switching losses with the converter current as well, we also need to scale the converter voltage with converter current. We observe that the highest voltage applied on the buffer converter switches is v_{C2}; at the same time, as the load current decreases, the magnitude of v_{ab} decreases proportionally as well. Therefore, as long as v_{C2} stays above the peak value v_{ab}, it can be adjusted according to the magnitude of $i_{\rm inv,ac}$ to minimize loss. To this end, the reference value for v_{C2} in the aforementioned PI control loop is set to be proportional to the magnitude of $i_{\rm inv,ac}$, such that the switching losses (except for the gate drive loss and core loss) now scale quadratically with the load current. Finally, the width of the hysteresis band for the current hysteresis control is adjusted according to the load current magnitude as well. This adjustment changes both the inductor current switching ripple and the converter switching frequency to dynamically balance the conduction losses and the switching losses, such that the remaining core loss and gate drive loss is alleviated at light load and the overall power loss is at a minimum. Since it is not easy to precisely calculate all the power losses, the equations for scaling the reference of v_{C2} and the hysteresis band are determined through empirical fine tuning after first-order loss calculations.

The proposed buffer architecture and control scheme work naturally with reactive loads without any modification. It only requires some care to be taken in the hardware implementation: since $i_{\rm inv}$ will have negative instantaneous value with reactive load, the current measurement hardware needs to be capable of bidirectional current measurement.

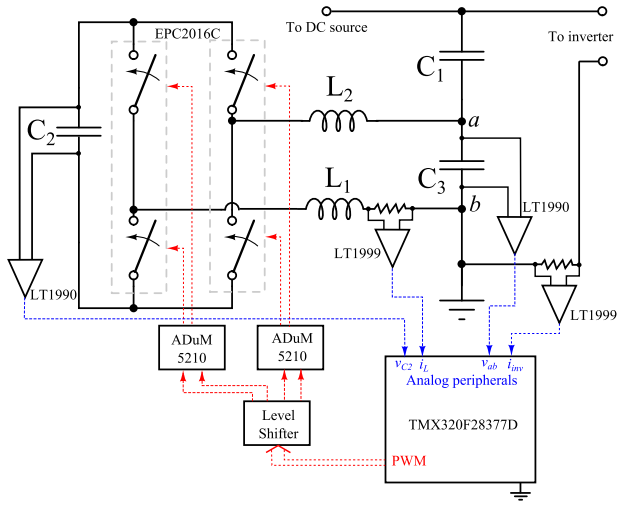


Fig. 9. Schematic of the hardware prototype. Control outputs (PWMs) are highlighted in red and control inputs (measurements) are highlighted in blue. The gate driver for GaN transistors and the resistor voltage dividers for v_{C2} and v_{ab} measurement are omitted for simplicity.

V. HARDWARE PROTOTYPE

A hardware prototype has been built to demonstrate the proposed buffer architecture. Table II lists the main components used and Fig. 9 provides a simplified schematic of the prototype.

The main capacitor C_1 is implemented with 239 2.2-μF, 450-V ceramic capacitors. This capacitance, at first glance, seems to be much larger than the 100 μF calculated for C_1 in Section III-B. This is because the voltage derating of the multilayer ceramic capacitor has to be considered. For the selected capacitor, 2.2 μF is the capacitance at zero voltage bias, while the effective capacitance at 400 V is only approximately 0.43 μF[2]. Therefore, 239 capacitors yield a total capacitance of 103 μF at 400 V. Similarly, 126 15-μF, 100-V ceramic capacitors are used for C_2, yielding a total capacitance of 433 μF at 80 V considering derating. Capacitors C_3 and $C_{\rm bus}$ are only for switching frequency filtering purposes and are implemented with only a small number of capacitors.

Each current signal used for control is measured with a current sensing resistor and an LT1999 amplifier. Each voltage signal

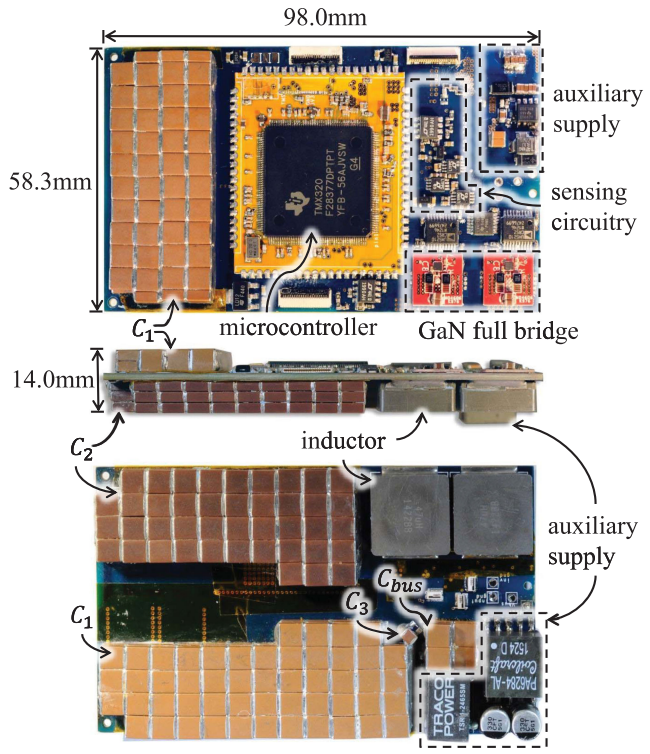


Fig. 10. Hardware prototype.

TABLE III
HARDWARE PROTOTYPE VOLUME BREAKDOWN

Total rectangular box volume	80.0 cm^3 (4.88 in^3)
Total energy storage component volume	32.9 cm^3 (2.01 in^3)
$C_{\rm bus}$ volume	0.7 cm^3 (0.043 in^3)
C_1 volume	19.1 cm^3 (1.16 in^3)
C_2 volume	9.0 cm^3 (0.55 in^3)
Inductor volume	4.1 cm^3 (0.25 in^3)
Power density by box volume	25 W/cm^3 (410 W/in^3)
Power density by component volume	60.8 W/cm^3 (995 W/in^3)

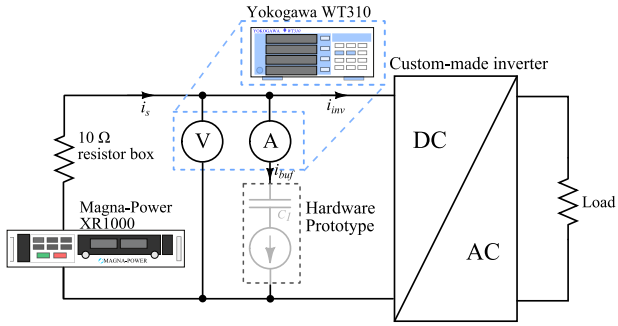


Fig. 11. Experimental setup.

is measured with a resistor voltage divider and an LT1990 difference amplifier. A TMX320F28377D microcontroller is used to process these signals, execute the proposed control scheme and generate the PWM signal for the power stage. Signals of v_{C2}, v_{ab}, and $i_{\rm inv}$ are sampled by the on-chip ADC and i_L is connected to the built-in analog comparator of the microcontroller. The PWM module of the selected microcontroller can directly achieve SR latch logic necessary for the inductor current hysteresis control while still allowing for insertion of PWM deadtime, therefore, providing an ideal one-chip solution for the proposed control scheme. A flyback dc–dc converter is also implemented as an auxiliary supply to draw control power from the dc bus.

The power stage is implemented with EPC2016C GaN switches on a custom made half-bridge module printed circuit board (PCB). The low transistor voltage stress allowed by this architecture enables the use of this 100-V GaN FET, switching at hundreds of kilohertz for small inductor size. In this implementation, the switching frequency varies between 100 and 350 kHz due to the current hysteresis control.

Annotated photographs of the hardware prototype are shown in Fig. 10. Most of the ICs including the GaN modules and the microcontroller are placed on the front side of the board, while the energy storage components (i.e., C_1, C_2, L_1 and L_2) are placed on the back side. Table III lists the volume breakdown of the prototype. It should be noted that the current hardware prototype is designed to fit with a single-phase inverter together into one enclosure for the best overall power density, as presented in [30]. As highlighted in Table III, the enclosed box volume is still considerably larger than the total component volume. Further size reduction is thus expected through layout optimization if the buffer is considered as a standalone unit.

VI. EXPERIMENTAL RESULTS

Experiments are performed on the hardware prototype to verify the performance of the proposed buffer architecture. The experiment is configured as in Fig. 11, according to the specifications in [24], where a power supply (Magna-Power XR/1000) is connect to the dc side of the buffer through a 10-Ω resistor and a custom made 2-kW inverter [30] is connected to the ac side of the buffer.

A. Steady-State Operation

Figs. 12 and 13 illustrate the operation of the buffer architecture in the experiments. The dc source voltage is set to 450 V. The inverter load is drawing a 10-A peak-to-peak *shifted* sinusoidal current $i_{\rm inv}$ and the control of the buffer converter enforces a buffer current $i_{\rm buf}$ equal to the ac component of $i_{\rm inv}$, as shown in Fig. 13. Note that Fig. 13 shows the waveform of $-i_{\rm buf}$ instead of $i_{\rm buf}$, to allow for easier illustration that $i_{\rm buf}$ resembles the shape of the ac component of $i_{\rm inv}$. Also note that the buffer capacitors also function as the input capacitor of the inverter, so the current ripple due to inverter switching (at 120 kHz for the inverter used here) is present in $i_{\rm inv}$ and $i_{\rm buf}$. A low-pass filter is applied to the measured $i_{\rm inv}$ in the control implement such that the control will only respond to the double-line-frequency ripple but not to the switching ripple. As a result of the buffer operation, the input current i_s is an almost constant 5 A with a small ripple.

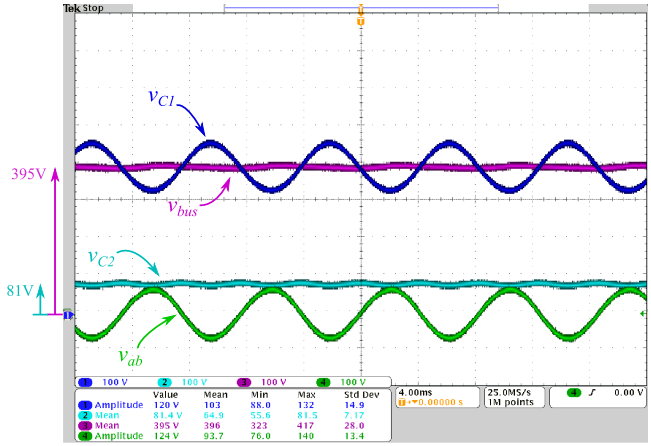


Fig. 12. Experimental waveforms of the C_1 voltage v_{C1} (channel 1), C_2 voltage v_{C2} (channel 2), bus voltage $v_{\rm bus}$ (channel 3), and terminal ab voltage v_{ab} (channel 4) during the full-load operation of the buffer.

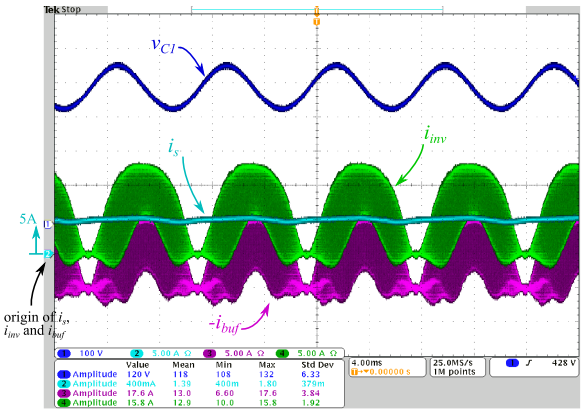


Fig. 13. Experimental waveforms of the C_1 voltage v_{C1} (channel 1), input current i_s (channel 2), inverter current $i_{\rm inv}$ (channel 3), and buffer current in its reverse direction $-i_{\rm buf}$ (channel 4) during the full-load operation of the buffer.

As observed from the experimental measurement in Fig. 12, the main buffer capacitor C_1 has a large voltage swing of 120 V, indicating high energy utilization of this capacitor. Due to the buffer control, the voltage across terminals a and b varies complimentary to this voltage swing such the sum of these two, i.e., the bus voltage, remain nearly a constant with only very small ripple below 5 V as shown in Fig. 12. The v_{ab} waveform is symmetric with respect to zero, indicating that the v_{C1} PI compensation loop is functioning properly to remove the dc offset in the buffer current. Moreover, the voltage of C_2 is held at 80 V with small ripple, indicating that the v_{C2} PI compensation loop is indeed extracting extra power from the bus voltage ripple to compensate for the buffer converter power loss and maintain the power balance of C_2.

As a benchmark reference, in order to achieve the same 5 V bus voltage ripple with the conventional passive decoupling, C_1 would have to be as large as 2654 μF, which can be calculated according to (1). Note that in the experiment, the dc source is 450 V with a 10-Ω resistor. During full-load operation, the bus voltage is 400 V, but during very light load, the bus voltage rises to close to 450 V. If dc-link capacitors are used, the capacitors have to be

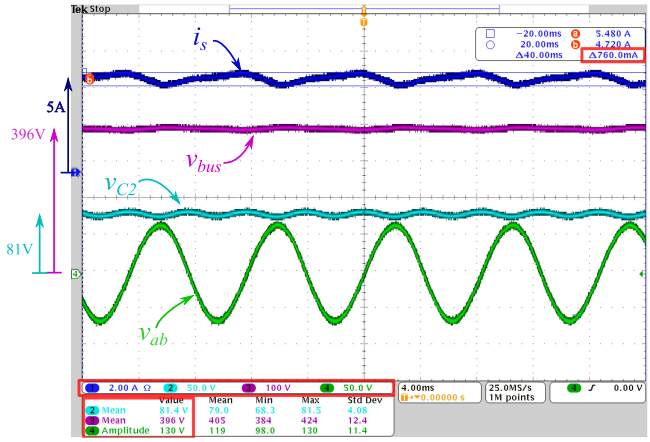


Fig. 14. Experimental waveforms of the input current i_s (channel 1), C_2 voltage v_{C2} (channel 2), bus voltage $v_{\rm bus}$ (channel 3), and C_3 voltage v_{C3} (channel 4) in the full-load (2 kW) condition. The input current ripple is 760 mA as highlighted on the top right corner.

rated at 450 V, which is approximately the same voltage rating for C_1 in the series-stacked buffer prototype. If electrolytic capacitors were used (we consider Nichicon UCP2W121MHD6 as an example) for this 2654-μF capacitance, at least 95 cm^3 is required for the capacitance. In practice, designers should consider the RMS current rating, the temperature rise limit and component lifetime, which typically results in even larger volume when electrolytic capacitors are used. If the same type of long-lifetime, low-loss ceramic capacitors were used, this capacitance would result in a volume of 506 cm^3, much larger than the volume listed in Table III.

B. Light-Load Operation and Input Current Ripple

As discussed in Section IV-F, the ripple in the input current needs to meet strict requirements, so special light-load considerations are taken in the control to ensure that input current ripple scales with power level. This part of the experimental is to verify this light-load functionality in the control.

The operation of the buffer under full-load (2 kW) conditions is illustrated in Fig. 14 with the input current ripple measurement highlighted. The input current is approximately constant at 5 A with a ripple as small as 760 mA (15%). The operation of the buffer in the half-load (1 kW) condition is illustrated in Fig. 15 and in the quarter-load (0.5 kW) condition is illustrated in Fig. 16 (note the y-axis scales are different in Figs. 14–16). As marked in Figs. 14–16, while the load power level decreases, the average input current decreases. The reference of v_{C2} is also reduced accordingly to reduce the buffer converter power loss such that smaller ripple is needed for loss compensation, as discussed in Section IV-F. As shown in Figs. 15 and 16, the input current ripple indeed scales down with the average input current value. Fig. 17 plots the input current ripple as a function of the average input current. Because of the light-load control scheme, the ripple stays well below 20% except for very light-load conditions. In very light-load conditions, as the input ripple current becomes very small, the effect of the dc bus filter

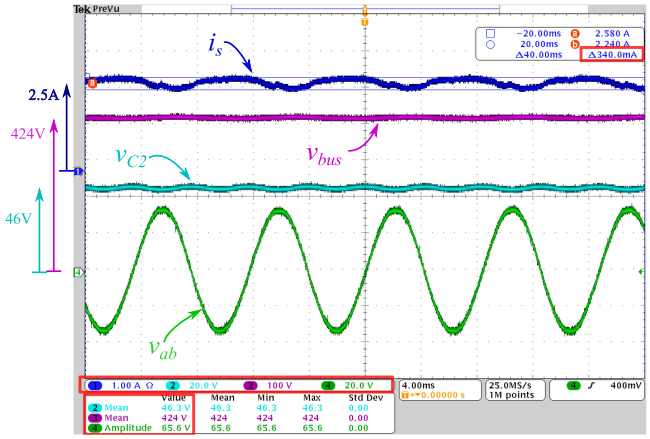


Fig. 15. Experimental waveforms of the input current i_s (channel 1), C_2 voltage v_{C2} (channel 2), bus voltage $v_{\rm bus}$ (channel 3), and C_3 voltage v_{C3} (channel 4) in the 50% load (1 kW) condition. The input current ripple is 340 mA as highlighted on the top right corner.

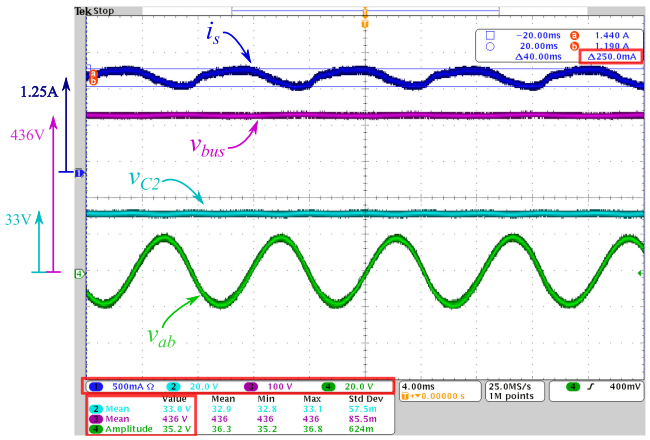


Fig. 16. Experimental waveforms of the input current i_s (channel 1), C_2 voltage v_{C2} (channel 2), bus voltage $v_{\rm bus}$ (channel 3), and C_3 voltage v_{C3} (channel 4) in the 25% load (0.5 kW) condition. The input current ripple is 250 mA as highlighted on the top right corner.

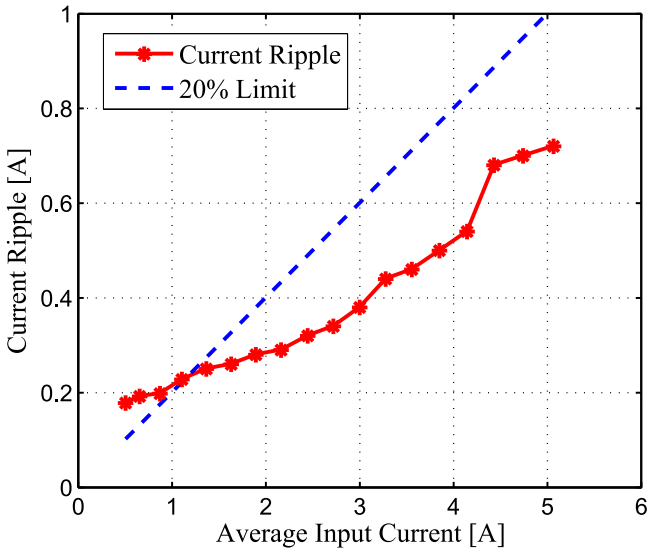


Fig. 17. Current ripple in dc source current i_s under different power levels. Each power level is indicated by its average dc source current.

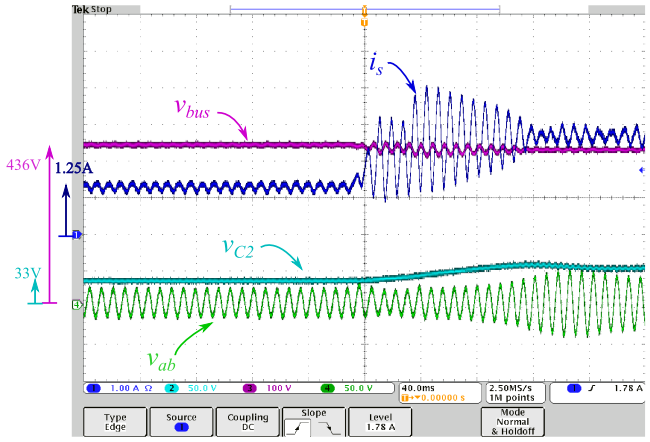


Fig. 18. Experimental waveforms of the input current i_s (channel 1), C_2 voltage v_{C2} (channel 2), bus voltage $v_{\rm bus}$ (channel 3), and C_3 voltage v_{C3} (channel 4) during a 25–50% load step transient.

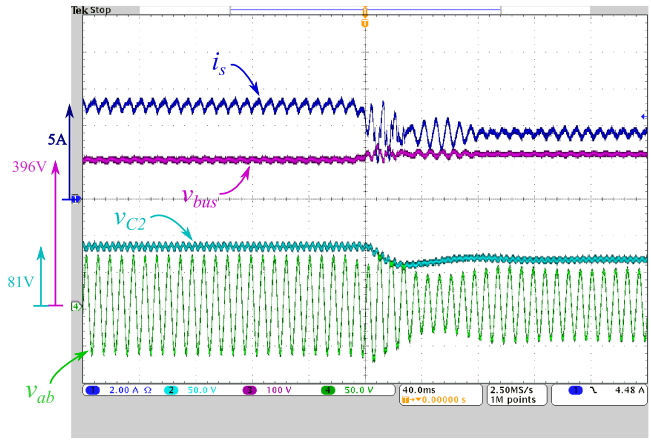


Fig. 19. Experimental waveforms of the input current i_s (channel 1), C_2 voltage v_{C2} (channel 2), bus voltage $v_{\rm bus}$ (channel 3), and C_3 voltage v_{C3} (channel 4) during a 100–75% load step transient.

capacitor $C_{\rm bus}$ absorbing part of the ripple current can no longer be neglected, which impairs the loss compensation capability specified in (39). Therefore, the current ripple saturates at about 200 mA in very light-load conditions.

C. Transient Operation

Fig. 18 demonstrates the buffer architecture responding to a load step change from 25% to 50%. The bus voltage settles to the new steady state within a few cycles and the voltages of C_2 and C_3 return to the reference value after a short transient, suggesting the effectiveness of the proposed control scheme. The input current ripple increases during this transient to provide extra energy to charge up C_2. Similarly, the transient of a load step change from 100% to 75% is shown in Fig. 19.

D. Reactive-Load Operation

Fig. 20 demonstrates the buffer architecture operating with a reactive load. The output of the inverter is connected to a 2-kVA load with 0.72 leading power factor. Compared to the

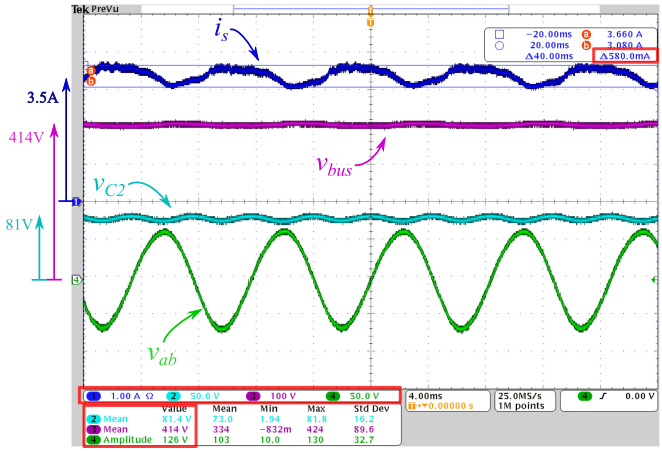


Fig. 20. Experimental waveforms of the input current i_s (channel 1), C_2 voltage v_{C2} (channel 2), bus voltage $v_{\rm bus}$ (channel 3), and C_3 voltage v_{C3} (channel 4) in a reactive-load (2 kVA, PF=0.72) condition.

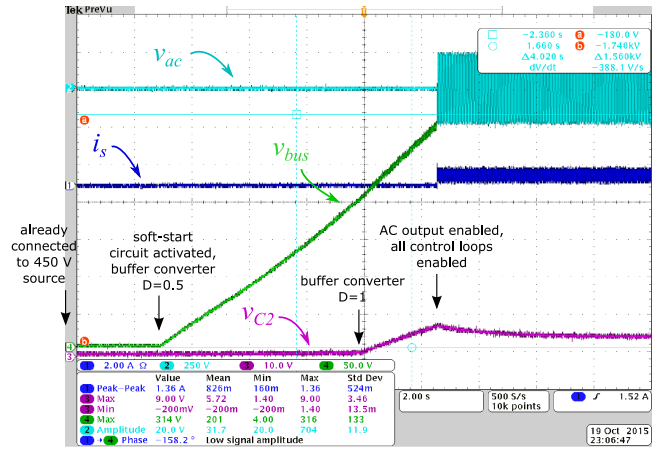


Fig. 21. Experimental waveforms of the input current i_s (channel 1), inverter ac output voltage $v_{\rm AC}$ (channel 2), C_2 voltage v_{C2} (channel 3), and bus voltage $v_{\rm bus}$ (channel 4) during the startup.

2-kW pure resistive load operation in Fig. 14, the average input current is lower and the bus voltage is higher in this reactive load condition due to smaller real power, but the magnitude of v_{C3} and the average of v_{C2} is almost the same given that the load current $i_{\rm out}$ is of the same magnitude. The buffer architecture operates the same with a lagging reactive load, since leading and lagging load with the same power factor will give identical load current $i_{\rm out}$.

E. Startup

The startup sequence of the entire system including the inverter and the series-stacked buffer is shown in Fig. 21. Upon startup, the system is connected to the 450-V dc source and 10-Ω resistor through a soft-start circuit. This soft-start circuit is essentially a MOSFET in linear region to limit the inrush current into the capacitors. More details about this soft-start circuit is introduced in [30]. Such inrush current limiting mechanism is often found in systems with dc-link capacitors as well. As the soft-start circuit is enabled, the buffer converter is switching

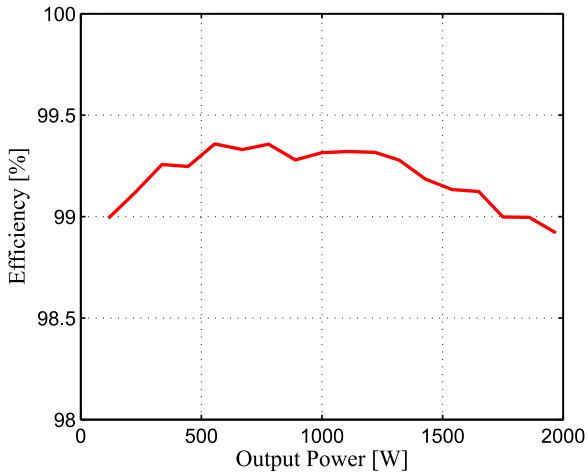


Fig. 22. Efficiency of the buffer architecture as a function of the output power level with 450-V dc source voltage (dc bus voltage varies due to the 10-Ω source resistor).

at a constant duty ratio of 0.5, such that $v_{ab} = 0$. Therefore, C_1 is connected across the dc bus and is gradually charged up. Once the bus voltage reaches a certain level (200 V in this case), the buffer converter changes the duty ratio to 1, which effectively connect C_2 and C_1 in series, so both of them are being charged and the bus voltage continues to rise. When the bus voltage reaches 300 V, the inverter is enabled and starts the ac output. This is in accordance with the requirement in [24]. Once there is ac output, current and voltage ripple are present on the dc side, then the loss compensation loop presented in Section IV can effectively balance all the voltages. Therefore, all the control loops during normal operation are enabled at this point. The voltage on C_2 is automatically adjusted to the right value according to the load power, as discussed in Section IV-F. Note that in Fig. 21, the voltage on C_2 is regulated to a relatively low value as it is a light-load condition. The bus voltage continues to rise to above 400 V, and then, the soft-start circuit is bypassed by a fully-on switch, which completes the startup sequence. Note that it is preferable to start with a light load on the ac side, as it is the case for Fig. 21. This is because once the ac output is enabled, the input current i_s increases depending on the load power level, which puts additional thermal burden on the soft-start circuit. Light-load condition reduces the time needed for the bus voltage to rise from 300 to 400 V and the power loss on the soft-start circuit.

F. Efficiency Measurement

The efficiency of the hardware prototype is evaluated. Since the power loss is very small compared to the total processed power, care must be taken to perform accurate power measurement free from the interference of ripples, etc. To this end, we adapt the efficiency measurement setup intended for evaluating film and ceramic capacitors (both of which have very small loss factor) from [2]. A Yokogawa WT310 digital power meter is connected as shown in Fig. 11. The integration function of a Yokogawa WT310 power meter is used to measure the energy flowing into and out of the buffer branch for many line cycles.

TABLE IV
COMPARISON OF THE PROPOSED SERIES-STACKED BUFFER AND PREVIOUS WORK IN THE LITERATURE

Reference	Decoupling Method	Power Level (W)	Efficiency	Volume (in^3)	Energy Density ($W/inch^3$)	Bus Voltage Ripple
This paper	Series-stacked buffer (active)	2000	Above 98.9%, peak 99.4%	By component: 2.01, by rectangular box: 4.88	by component: 995, by rectangular box: 410	2.5%
Chen et al. TPELS 2013 [15]	SSC (active)	135	Above 95.2%, peak 97%	By component: 1.7	by component: 79.4	20% (estimated)
Tang et al. TPELS 2015 [12]	Symmetrical half-bridge buffer (active)	1000	98% (estimated)	By component: >35 (estimated)	by component: <57 (estimated)	3% (estimated)
Wang et al. TPELS 2011 [6]	Full ripple port buffer (active)	15000	98% (estimated)	By rectangular box: 347.8 (estimated)	by rectangular box: 43 (estimated)	5% (estimated)
Lyu et al. JESTPE 2016 [31]	Series voltage compensator (active)	2000	Above 92.7%, peak 96.3%	By rectangular box: 36.54 (including inverter)	by rectangular box: 55 (including inverter)	3%
Neumayr et al. ECCE Asia 2016 [32]	Full ripple port buffer (active)	2000	Peak 98.7%	By component: 2.9 (no cooling), by rectangular box: 4.7 (with cooling)	by component: 689 (no cooling), by rectangular box: 425 (with cooling)	$<3\%$
Zhao et al. JESTPE 2016 [33]	*LC* filter (passive)	2000	Peak 99.8% (estimated)	By component: 4.3 (estimated)	by component: 465 (estimated)	$<3\%$
Zhao et al. APEC 2016 [34]	Front-end buck converter (active)	2000	Peak 99.6%	By rectangular box: 6.6	by rectangular box: 303	0.8%

The ratio of the integrated outflow and inflow of the energy gives the buffer efficiency. The power measurements are conducted and integrated for 30 s. The efficiency measurement result is plotted in Fig. 22.

Note that the measured efficiency *excludes* the controller and gate driver loss. This is because the auxiliary power (including microcontroller, gate driver, sensing circuit, and cooling fans) is shared between the buffer circuit and the custom-made inverter. The auxiliary power for both of them is generated by the same auxiliary supply circuit when the full system is running. It is difficult to include the auxiliary power of the buffer part in the digital meter measurement as shown in Fig. 11. Instead, we estimate the auxiliary power for the buffer circuit alone is about 2.5 W. A detailed efficiency and loss breakdown of the overall inverter system is presented in [30].

As analyzed in Section III, since the buffer converter is processing only a fraction of the total power, the overall efficiency of the buffer architecture is decoupled from the buffer converter efficiency. The partial power processing architecture and control scheme together result in a buffer efficiency higher than 99% across a wide load range, which is even comparable to the efficiency of passive decoupling with film or ceramic capacitors.

VII. COMPARISON

In this section, the proposed series-stacked buffer is compared with the state-of-art solutions in the literature. The difficulty for this comparison is that although there are a large number of papers on active decoupling, very few publish the result of hardware volume or power density. Some of the papers do not report efficiency as well. In fact, to the best of our knowledge, among publications before the year of 2016, only [15] directly gives power density of the decoupling circuit. The power density in [31] is given together with an inverter and the power density of the decoupling stage alone cannot be inferred from the available information. A few other papers on active decoupling such as [6], [12], and [31], provide certain information (component selection, photograph of the hardware prototype, etc.) from which we make our best effort estimation. Many other solutions in the literature either do not provide enough hardware information for an estimate or have power density similar to or lower than those compared here. The comparison result is listed in Table IV, where the nominal power, measured efficiency, hardware volume (by component volume and/or by the volume of the rectangular enclosure), power density (by component volume and/or by the volume of the rectangular enclosure), and ripple on the dc bus are compared. In general, the power density of comparable solutions in the literature is at least an order of magnitude lower compared to the series-stacked buffer architecture proposed in this study.

It should be noted that the recent Google/IEEE little box challenge unveils a few high power density single-phase inverter designs. Many of these designs incorporate high-power-density decoupling circuits. Although details of most of the designs are not available in the literature, upon the completion of this paper, three such designs were published. The performance metrics of these designs as presented in this papers are listed in the last three rows in Table IV. We note that our solution achieves the highest power density among these designs, and an efficiency that is close to the best passive solution.

Compared to other solutions in Table IV, the fundamental reason for the superior power density and efficiency achieved by the series-stacked buffer architecture is that the series-stacked topology allows for flexible tradeoff between the volume of the energy storage capacitors and the filter inductor and enables greatly increased efficiency owing to its partial power processing characteristics. In previous magnetic-based topologies, such as [6], [7], [11], and [12], the filter inductor is under the full

voltage stress of the bus voltage, so the filter inductor is typically much larger than the energy storage capacitor. The SSC topology [15] is on the opposite extreme where no inductor is used but the capacitor volume is relatively large. There is a middle ground where the inductor volume is balanced with capacitor volume for the minimum overall volume, but these aforementioned solutions do not allow tradeoff between inductors and capacitors. Alternative topologies that allow such tradeoffs are first proposed conceptually in [19]. The work in [10] and [35] represents an earlier attempt on developing a topology that allows such tradeoff, where the buffer converter only process the capacitor ripple voltage and the relative volume of the inductor and capacitors can be adjusted by choosing the magnitude of the capacitor ripple voltage allowed. However, the range of tradeoff is limited by the operating voltage of the ac/dc converter in the system, as analyzed in Section II.

The proposed series-stacked topology is the first one to allow free tradeoff across the full voltage range. The magnitude of v_{ab} in Fig. 4(b) basically determines the volume of inductors and capacitors in the series-stacked buffer architecture and its value can be chosen anywhere between 0 and $V_{\rm bus}$ to minimize the overall volume. Moreover, as the technology of inductors and capacitors develop, the optimal point of their tradeoff might change. New designs of series-stacked buffers can readily adopt these changes, while the previous solutions do not allow such tradeoff. A key issue that previously made practical realizations of the application of the series-stacked buffer difficult is the average current mismatch problem due to the series connection of two components with different losses. In this study, we have presented a control scheme that solves this problem with no additional power stage hardware requirement.

VIII. Conclusion

In this paper, the advantages and drawbacks of previous power pulsation decoupling techniques have been analyzed and a buffer architecture combining their advantages has been proposed to achieve high power density, high efficiency, and small dc bus ripple. The operating principles and design constraints were derived for the full-bridge topology and illustrated by simulation, while the same analysis can be easily applied to other possible topologies such as buck–boost. We identify the capacitor voltage imbalance problem imposed by the series-stacked structure and propose a compensation scheme that uses the ripples in the bus voltage and the dc input current to our advantage. The principle of the power loss compensation has been derived. Light-load and reactive-load considerations are also discussed. A hardware prototype was developed to demonstrate the proposed idea. The experimental results verified a power density as high as 410 W/in^3 by box volume and 995 W/in^3 by power component volume. A high efficiency above 98.9% were measured across a wide load range.

To summarize the reason why the proposed buffer architecture achieves these superior features compared to the conventional active decoupling techniques, two fundamental ideas stand out as the key enablers. First, instead of blocking the high dc bus voltage with switches directly, the bulk voltage is blocked by capacitors. Such arrangement mitigates the voltage stress on the active circuit, so fast-switching transistors can be employed, which enables the use of switching frequency to tradeoff for energy density. This concept is similar to the idea behind many multilevel converter designs [36]–[39]. Second, instead of directly processing the full power, the proposed buffer architecture controls the full power by processing only a fraction of it. By avoiding processing the full power in the first place, the overall system efficiency is no longer limited by the power converter efficiency and a highly efficient system can be built with less efficient converters, similar to ideas explored in [40]–[44].

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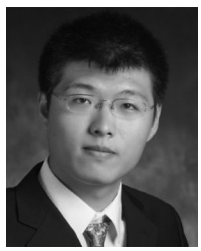

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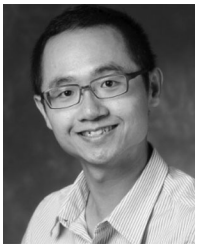

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