# A Family of Neutral-Point-Clamped Circuits of Single-Phase PV Inverters: Generalized Principle and Implementation

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***Abstract*—The common-mode leakage current should be carefully considered when designing a transformer-less photovoltaic (PV) inverter since the leakage current can cause the output current distortion and increase the operational risk. The unipolar sinusoidal pulse width modulation of the traditional H-bridge inverter can produce the superior output performance but will cause a high-frequency fluctuated common-mode voltage and consequently the nonnegligible leakage current. To attenuate the fluctuation phenomena of common-mode voltage, few neutral-point-clamped (NPC) circuits have been designed to clamp the neutral-point voltage and maintain the common-mode voltage constant. This paper analyzes the equivalent common-mode circuit of single-phase inverters and proposes a generalized design principle of multiterminal NPC circuits, whose unidirectional and bidirectional variations are fully analyzed. Subsequently, two types of single-phase PV inverters with the NPC circuits are proposed. Also, the operational losses and component counts are compared between the proposed topologies and the traditional NPC inverters. The experimental results verified the theoretical findings.**

***Index Terms*—Common-mode voltage, neutral-point-clamped (NPC) circuit, photovoltaic (PV) inverter, single-phase inverter.**

## I. Introduction

In the grid-connected photovoltaic (PV) inversion system, high efficiency, high performance, and low cost are the three main targets pursuing. Traditionally, a line-frequency or high-frequency transformer is employed in the PV inverter to isolate the grid from the PV source to attenuate the common-mode leakage current and step up the output voltage. However, the transformer will unavoidably reduce the operational efficiency and increase the system cost and size [1], [32]. Therefore, the transformerless PV inverters are now attracting much more attention. The main problem of transformerless PV inverter is that it has no galvanic isolation and then the common-mode leakage current can flow through the parasitic capacitor between ground and PV array, which will threaten people safety and cause other severe problems [2]. To attenuate the common-mode leakage current in transformerless inverter, the most effective solution is to keep the common-mode voltage constant [3]. So far, several single-phase topologies have been proposed to maintain the common-mode voltage constant as half of dc-bus voltage, for example, H5, HERIC, and H6 topologies [4]–[7]. However, the common-mode voltage is indeed variable during the freewheeling stage because of the potential variation induced by charging and discharging the switch junction capacitance. Thus, the leakage current still exists in the common-mode circuit. Besides, few neutral-point-clamped (NPC) circuits have been proposed to effectively clamp the common-mode voltage to be half of dc-bus voltage during the whole fundamental period [8]–[14]. These NPC topologies are mainly applicable in the transformerless PV generation systems with the required low-level leakage current. But the general design principles and the implementation procedures of the NPC circuits were not included in the already published literatures.

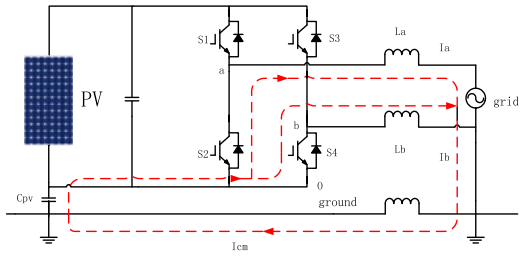


Fig. 1. Equivalent common-mode circuit of a single-phase PV inverter.

Therefore, this paper presents the general design method of clamping circuits and proposes the corresponding unidirectional and bidirectional NPC circuits and analyzes their operational theory. And then, two types of NPC single-phase PV inverters are proposed by using the unidirectional and bidirectional clamping circuits. The full comparison between the generalized NPC PV inverters and the traditional NPC PV topologies in terms of their operational efficiency and component counts is also presented. The experimental results verified the performance of the proposed circuits.

## II. Modeling of Common-Mode Circuit in a Single-Phase PV Inverter

Fig. 1 shows the topology of a traditional single-phase H-bridge inverter, where four switches operate at high frequency

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and the corresponding common-mode voltage can be expressed as follows [15]–[17]:

$$u_{\rm cm} = \frac{u_{\rm ao} + u_{\rm bo}}{2} \tag{1}$$

where $u_{\rm ao}$ and $u_{\rm bo}$ are the pulsating voltages between the midpoints of two legs and the negative dc rail, respectively. The common-mode current $i_{\rm cm}$ is mainly induced by the fluctuation of $u_{\rm cm}$ as follows [18], [19]:

$$i_{\rm cm} = C_{\rm pv}\frac{du_{\rm cm}}{dt}. \tag{2}$$

Without the isolation transformer, the common-mode leakage current can flow through the parasitic capacitor between ground and PV array, the equivalent grid impedance, and the output filter. As a consequence, the leakage current may exceed the permissible levels defined by standards, e.g., DIN VDE 0126-1-1, and will cause the safety problems and distort the output current [20]–[22].

Several single-phase inverters have the capability of attenuating the common-mode current, such as H5, Heric, HB-ZVR, and H6 topologies. These inverters can use the auxiliary switches and diodes to provide the additional freewheeling path to make the common-mode voltage constant during the whole fundamental period in theory. However, because of the charging and discharging of switch junction capacitances between the freewheeling modes and the energy transferring modes, the common-mode voltage is indeed not constant. Specifically taking the topology of Fig. 2(a) as an example, during the energy transferring modes in the positive fundamental period, the equivalent junction capacitances $C_2$, $C_3$, and $C_6$ are charged as shown in Fig. 2(b), but $U_{\rm an}$ and $U_{\rm bn}$ are held at $V_{\rm dc}$ and 0, respectively. On the other hand, the junction capacitances $C_1 - C_4$, $C_6$ are charged in the freewheeling mode as shown in Fig. 2(c) and $U_{\rm pa}$, $U_{\rm bn}$ are increased; thus, the potentials of *a* and *b* vary. Then, the common-mode voltage is not strictly half of the dc-bus voltage, especially during the freewheeling modes. Fig. 3(a) and (b) shows the equivalent resonant common-mode circuits in energy transferring mode and freewheeling mode during the positive fundamental period. Specifically, in the energy transferring mode of Fig. 3(a), $u_{\rm an}$ equals to $u_{\rm dc}$ and $u_{\rm bn}$ is 0. However, in the freewheeling mode of Fig. 3(b), the potential of $u_{\rm an}$ and $u_{\rm bn}$ can be expressed as follows:

$$\begin{aligned} u_{\rm an} = \ u_{\rm bn} &= \frac{C_1 + C_3}{C_1 + C_3 + \frac{C_2 \times C_6}{C_2 + C_6} + C_4} \times u_{\rm dc} \\ &= \frac{1}{1 + \frac{C_2C_6 + C_2C_4 + C_4C_6}{C_1C_2 + C_2C_3 + C_1C_6 + C_3C_6} + C_4} \times u_{\rm dc}. \end{aligned} \tag{3}$$

It is obvious that $u_{\rm an}$ and $u_{\rm bn}$ are not half of dc-link voltage during the freewheeling mode. Therefore, according to (1) and (3), the common-mode voltage will not be constant in the H6 inverter. Especially, in the transition between two modes in Fig. 3, the average value of the bridge voltages $u_{\rm an}$ and $u_{\rm bn}$ vary from $u_{\rm dc}/2$ to the calculated result in (3). Thus, during the freewheeling modes, an oscillation of common-mode voltage will be induced by the resonant circuit, which consists of the junction capacitors $C_1 - C_4$, $C_6$, the parasitic capacitors $C_{\rm PV}$ between ground and PV panels, and the filter inductors $L_a$ and $L_b$ [21]. When assuming all switch junction capacitances are equal, the variation of common-mode voltage can be estimated as $u_{\rm dc}/14$. For cases, where the high switching frequency and the relatively large PV capacity are employed, the leakage current could exceed the permissible level. For example, under the operation conditions of $u_{\rm dc} = 360$ V, 20 kHz of switching frequency and $C_{\rm pv} \geq 590$ nF without considering the resonant phenomenon induced by the filter inductors in Fig. 3, the leakage current could exceed 300 mA. Besides, the practical operation conditions, e.g., the unbalanced filter inductors, will further worsen the common-mode voltage performance. The high-level leakage current should be attenuated in PV applications. Hence, it is necessary to add a NPC circuit to make the common-mode voltage constant more effectively [23]–[26].

## III. General Design Principle of NPC Circuits

The function of NPC circuits is to clamp the output voltage of two phase-legs during the freewheeling modes [27], [28]. Thus, the design of clamping circuits should follow the principles as follows:

1) the NPC circuit should be bidirectional to effectively balance the common-mode voltage during the freewheeling modes;
2) the NPC circuit should not shoot-through dc rails under any working conditions;
3) the NPC circuit should connect to the midpoint of dc link and form a complete freewheeling path.

Following the aforementioned principles, the NPC circuit should have at least three effective connection terminals, one of which will connect to the midpoint of dc link and others will connect to the output terminal per leg to form a freewheeling path. Fig. 4 shows the general configuration of NPC circuit in the single-phase inverter, where the NPC circuit can be inserted at three different locations. Specifically, the NPC circuit can be inserted between two output terminals of phase legs as shown in Fig. 4(a), while the NPC circuits can also be inserted into the phase leg as shown in Fig. 4(b) and (c), respectively.

Furthermore, to fully satisfy the operational principle of NPC circuits, two types of NPC circuits can be designed with the unidirectional and bidirectional current flow capability. In particular, Fig. 5 shows the specific configurations of the unidirectional clamping circuit, which consists of two diodes and one switch. It is noted that only diode $D_{\rm c}$ connects to the midpoint of dc link allowing current flow in one direction. Therefore, a complete NPC circuit for a single-phase PV inverter should combine both unidirectional NPC circuits in Fig. 5. Alternatively, Fig. 6 shows the bidirectional clamping circuits, which consists of three switches, where the switch connected to the midpoint of dc link could use its body diode to conduct the leakage current in one direction. Since $S_c$ in Fig. 6 has the bidirectional current flowing capability, only assuming one of configurations in Fig. 6 could build the complete NPC inverter.

## IV. Implementation of NPC Circuits

This section presents the detailed implementations of unidirectional and bidirectional NPC circuits.

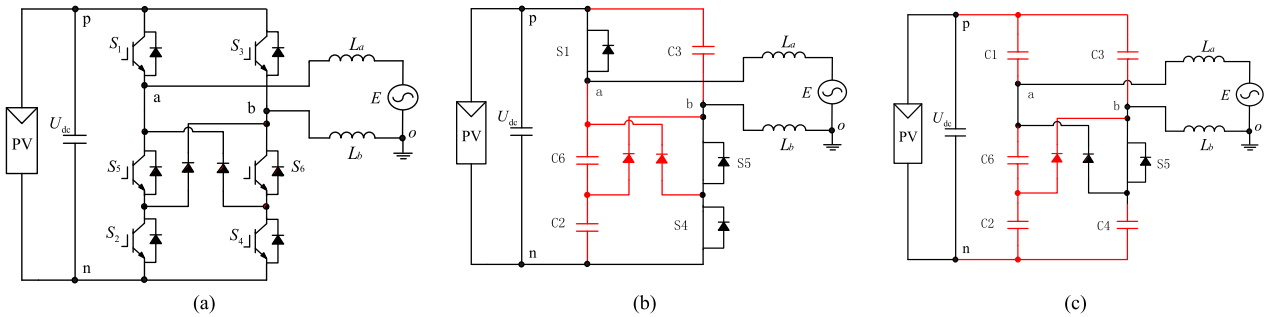


Fig. 2. (a) Topology of the H6 inverter and the equivalent circuits during (b) power transferring mode and (c) freewheeling mode during the positive fundamental period.

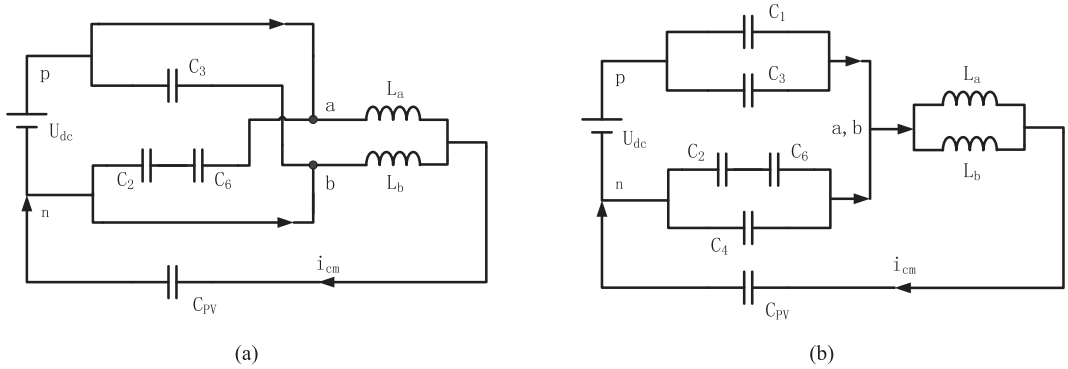


Fig. 3. Equivalent resonant common-mode circuits in (a) energy transferring mode and (b) freewheeling mode during the positive fundamental period.

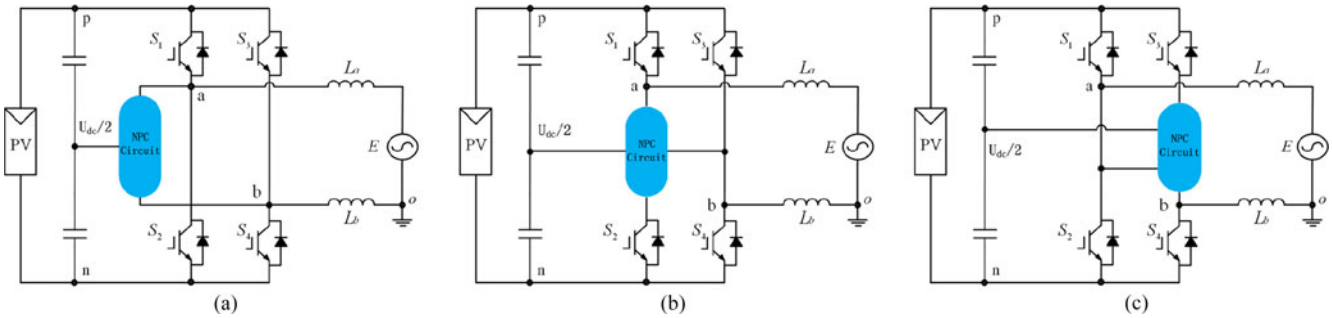


Fig. 4. General configuration of NPC circuits inserted at three different locations.

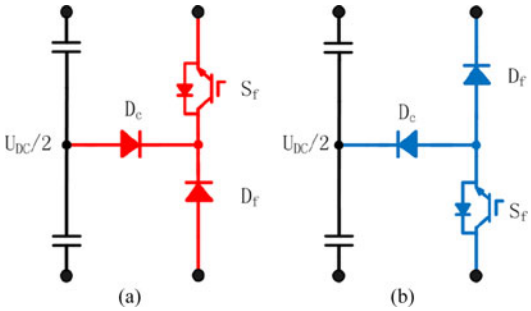


Fig. 5. Unidirectional NPC circuits.

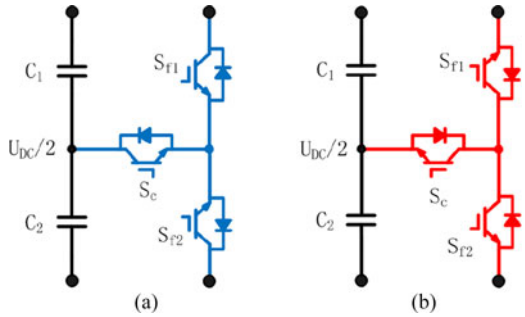


Fig. 6. Bidirectional NPC circuits.

### *A. Implementation of Unidirectional Clamping Circuits*

As indicated by Figs. 4 and 5, two unidirectional clamping circuits should be combined together to form a bidirectional freewheeling path. Also, the variations of circuit combination can be inserted in the traditional H-bridge inverter as generalized in Fig. 4. Fig. 7(a)–(g) shows the produced topologies

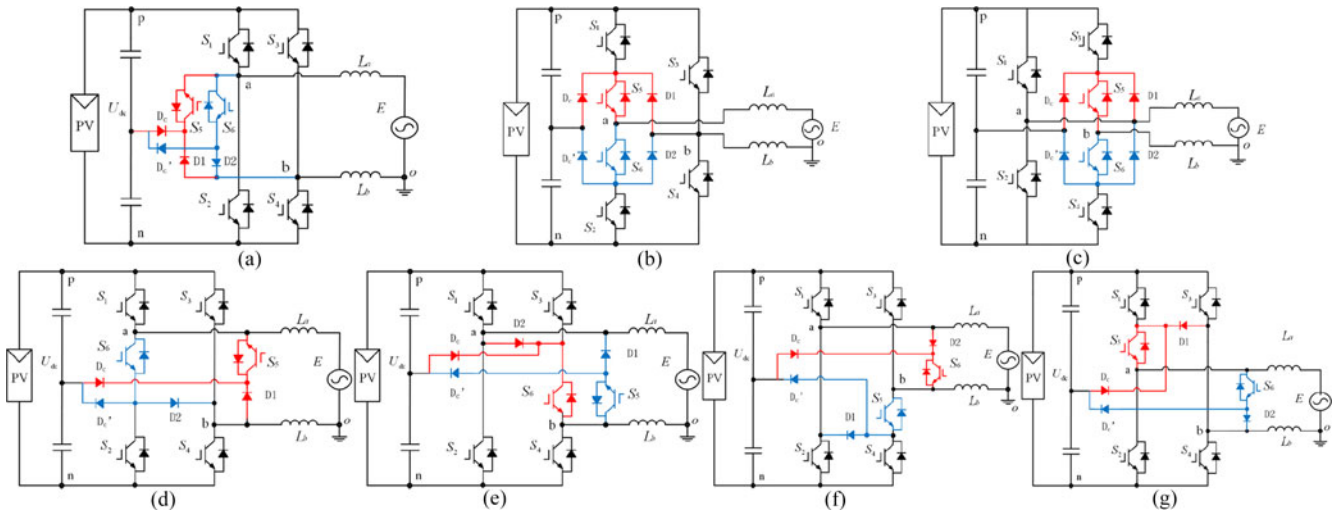


Fig. 7. Type of single-phase inverters with unidirectional clamping circuits.

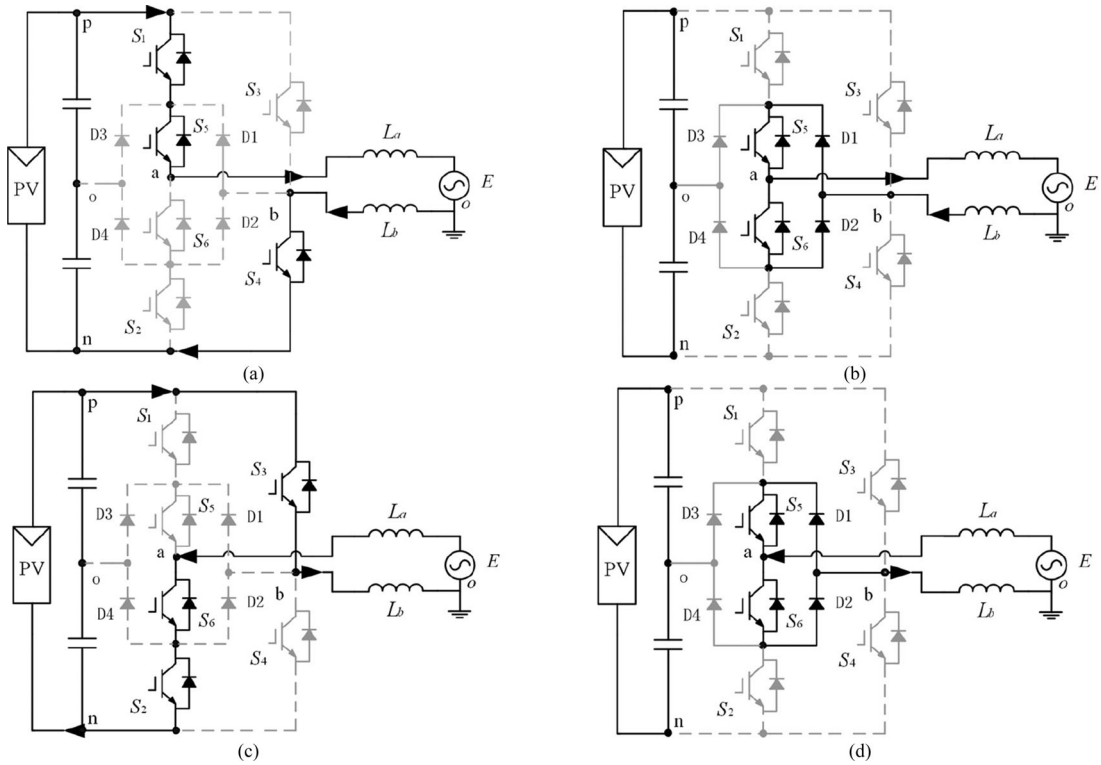


Fig. 8. (a) Energy transferring mode and (b) freewheeling mode during the positive half period. (c) Energy transferring mode and (d) freewheeling mode during the negative half period of the NPC inverter in Fig. 7(b).

using the unidirectional clamping circuits, which make up a type of NPC single-phase inverters, where two kinds of unidirectional clamping circuits in Fig. 5(a) and (b) are labeled in blue and red, respectively, to highlight their inserting positions in the H-bridge inverter. In particular, Fig. 7(a) shows the topologies with clamping circuits inserted between dc link and H-bridge as indicated by Fig. 4(a) [9], [10]. And Fig. 7(b) and (c) shows that the clamping circuits can be inserted in any phase-leg to form a freewheeling path, which corresponds to the general illustration of Fig. 4(b) and (c). Besides, two unidirectional clamping circuits can be inserted flexibly as shown in Fig. 7(d), (e), (f), and (g), where one unidirectional clamping circuit is inserted in one phase-leg and another connects the midpoint of dc link and output terminals of H-bridge directly.

To briefly illustrate the operational principle of the proposed single-phase inverters with the unidirectional clamping circuits, only the topology of Fig. 7(b) is assumed as an example for analysis, since the topologies in Fig. 7 have the same operational principles, which all have four operation modes in general. In specific, Fig. 8 shows the output current flow paths and the semiconductor devices conduction behaviors during two energy transferring modes and two freewheeling modes of Fig. 7(b),

where the ON switches and diode are black and the OFF switches and diodes are gray under each operation mode.

*Mode 1:* During the positive half period of the modulation reference, $S_1$ and $S_4$ are modulated at high frequency, while $S_5$ is always ON, $S_2$ and $S_3$ are OFF and $S_6$ works complementarily to $S_1$ and $S_4$. When the inverter works under the energy transferring mode, $S_1$ and $S_4$ are ON and $S_6$ is OFF, the current flows through $S_1$, $S_5$, grid, and $S_4$ successively as shown in Fig. 8(a). The common-mode voltage is

$$u_{\rm cm} = \frac{u_{\rm an} + u_{\rm bn}}{2} = \frac{u_{\rm dc} + 0}{2} = \frac{u_{\rm dc}}{2}. \tag{4}$$

*Mode 2:* During the positive half period of the modulation reference, when the inverter works under the freewheeling mode, $S_1$ and $S_4$ are OFF, $S_5$ and $S_6$ are ON, the current flows through $S_5$, $D_1$, and grid successively as shown in Fig. 8(b), or $S_6$, $D_2$, and grid while the grid current and the modulation reference are not in phase. The common-mode voltage is

$$u_{\rm cm} = \frac{u_{\rm an} + u_{\rm bn}}{2} = \frac{u_{\rm dc}/2 + u_{\rm dc}/2}{2} = \frac{u_{\rm dc}}{2}. \tag{5}$$

*Mode 3:* During the negative half period of the modulation reference, $S_2$ and $S_3$ are modulated at high frequency, while $S_6$ is always ON, $S_1$ and $S_4$ are OFF and $S_5$ works complementarily to $S_2$ and $S_3$. When the inverter works under the energy transferring mode, $S_2$ and $S_3$ are ON and $S_5$ is OFF, the current flows through $S_3$, grid, $S_6$, and $S_2$ successively as shown in Fig. 8(c). The common-mode voltage is

$$u_{\rm cm} = \frac{u_{\rm an} + u_{\rm bn}}{2} = \frac{0 + u_{\rm dc}}{2} = \frac{u_{\rm dc}}{2}. \tag{6}$$

*Mode 4:* During the negative half period of the modulation reference, when the inverter works under the freewheeling mode, $S_2$ and $S_3$ are OFF, $S_5$ and $S_6$ are ON, the current flows through $S_6$, $D_2$, and grid successively as shown in Fig. 8(d), or $S_5$, $D_1$, and grid while the grid current and the modulation reference are not in phase. The common-mode voltage is

$$u_{\rm cm} = \frac{u_{\rm an} + u_{\rm bn}}{2} = \frac{u_{\rm dc}/2 + u_{\rm dc}/2}{2} = \frac{u_{\rm dc}}{2}. \tag{7}$$

When the potential of points a and b falls to be lower than that of the midpoint of dc link during the freewheeling modes in Fig. 8(b) and (d), the common-mode leakage current flows through $D_3$; thus, it will balance the potential of freewheeling path as shown in Fig. 9(a), where the leakage current flowing path is highlighted by yellow. On the other hand, when the potential of points a and b rises to be higher than that of the midpoint of dc link during the freewheeling modes, the common-mode current will flow through $D_4$ and balance the potential of two legs as shown in Fig. 9(b). Therefore, the common-mode voltage can keep constant during the whole fundamental period.

The corresponding modulation strategy is shown in Fig. 10, where $S_1 - S_6$ are the gating signals of the proposed inverters in Fig. 7(b). In specific, in the positive modulation period, the diagonal switches of $S_1$ and $S_4$ work at high frequency and the freewheeling switch $S_6$ works complementarily to $S_1$ and $S_4$ while another freewheeling switch $S_5$ remains ON. Similarly, in the negative modulation period, another diagonal switches of

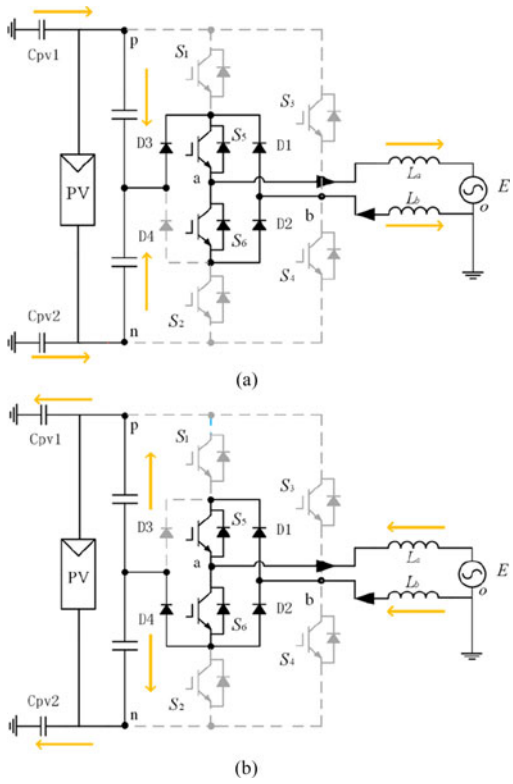


Fig. 9. Common-mode leakage current paths of the NPC inverter in Fig. 7(b) when the potential of freewheeling path is (a) lower than the midpoint of dc link and (b) higher than the midpoint of dc link.

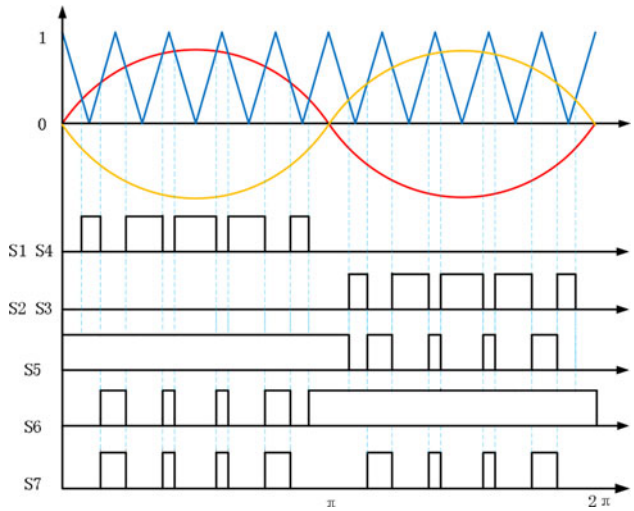


Fig. 10. Illustration of a modulation strategy.

$S_2$ and $S_3$ work at high frequency, which are complementarily to the freewheeling switch $S_5$. Another freewheeling switch $S_6$ remains ON. The aforementioned modulation principle is universal for all NPC inverters in Fig. 7.

### B. Implementation of Bidirectional Clamping Circuits

As indicated by Figs. 4 and 6, three switches combined together with the common emitters or common collectors can form a bidirectional freewheeling path. Also, the NPC circuit

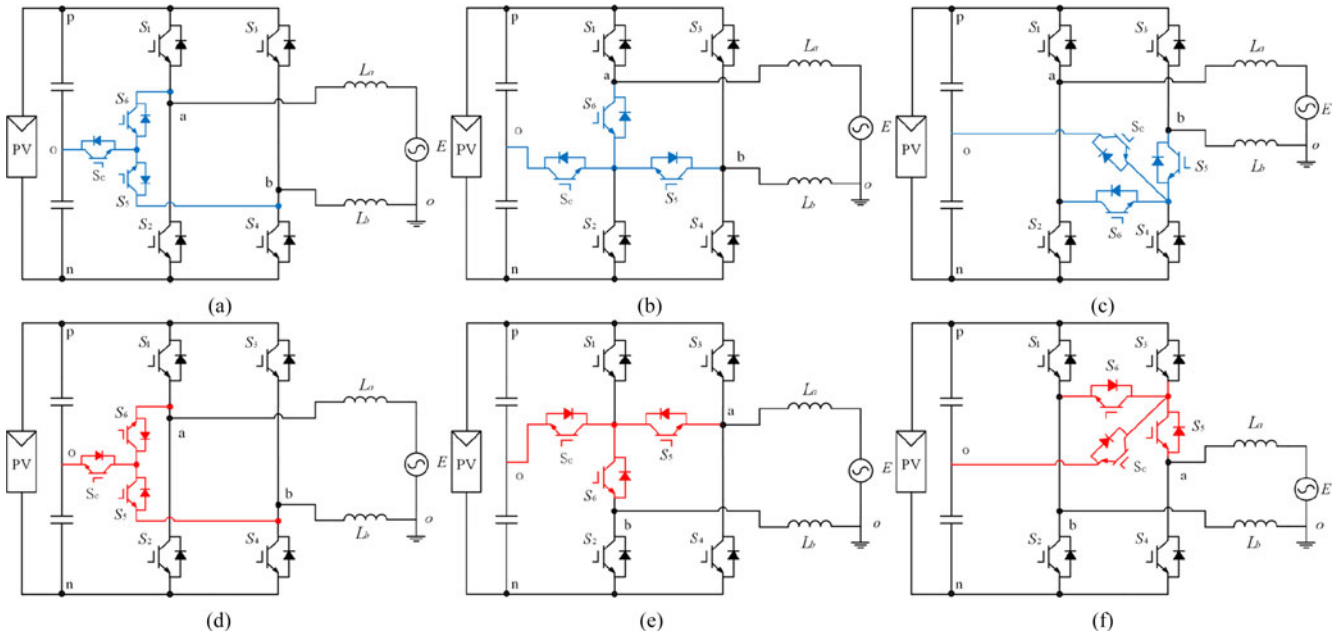


Fig. 11. Type of single-phase inverters with bidirectional clamping circuits.

can be inserted in the traditional H-bridge inverter as generalized in Fig. 4. Fig. 11 shows the produced topologies using the bidirectional clamping circuits, which make up a type of NPC single-phase inverters. In particular, Fig. 11(a) and (d) shows the topologies with clamping circuits inserted between dc link and H-bridge as indicated by Fig. 4(a) [8]. And Fig. 11(b), (c), (e), and (f) shows that the clamping circuits can be inserted in any phase-leg to form a freewheeling path, which corresponds to the general illustration of Fig. 4(b) and (c). Also, it can be observed that Fig. 11(a)–(c) shows the applications of the NPC circuit in Fig. 6(a), while Fig. 11(d)–(f) shows the applications of the NPC circuit in Fig. 6(b), respectively.

In order to briefly illustrate the operational principles of the proposed single-phase inverters with bidirectional clamping circuits, the topology of Fig. 11(b) is assumed as an example, which also has four general operation modes. Fig. 12 shows the specific current flow paths and the switches conduction behaviors during two energy transferring modes and two freewheeling modes. When the potential of points a and b falls to be lower than that of the midpoint of dc link in the freewheeling modes, the common-mode leakage current flows through $S_7$; thus, it will balance the potential of freewheeling path. On the other hand, when the potential of points a and b rises to be higher than that of the midpoint of dc link, the common-mode current will flow through $S_7$ and its body diode so as to balance the potential of two legs either. Thus, the common-mode voltage can keep constant during the whole fundamental period.

The corresponding modulation strategy can also be illustrated by Fig. 10, where $S_1 - S_7$ are the gating signals of the proposed inverters in Fig. 11(b). Similarly, the rest of the NPC inverters in Fig. 11 could also follow the modulation strategy shown in Fig. 10. Specifically, the clamping switch of $S_7$ works complementarily to $S_1$ and $S_4$ in the positive modulation period or $S_2$ and $S_3$ in the negative modulation period.

### C. Analysis of the NPC Inverters With Practical Operation Considerations

During operation, the PV inverters could suffer some nonstandard operation conditions, e.g., the nonunity power factor operation, the distorted grid voltage, and the unbalanced filter inductors.

In detail, when the output power factor is not unity, the presented NPC inverters can still work properly with the constant common-mode voltage obtained, which can be concluded by specifically analyzing the freewheeling modes in Fig. 8, where, e.g., when the output current in Fig. 8(b) has the opposite direction, $S_6$ and $D_2$ are the conducting devices instead of $S_5$ and $D_1$. Such the freewheeling behavior can still effectively maintain the common-mode voltage constant.

For cases, where the grid voltage is distorted, the common-mode behaviors of the presented NPC inverters will not be influenced, because the fundamental frequency and the low-order harmonics' frequencies of grid voltage are far smaller than the switching frequency. In detail, according to (2) and the equivalent common-mode circuits in Fig. 3, the low-order harmonics of grid voltage will almost not increase the leakage current [3].

When two output filters of the NPC inverter are not symmetrical, the potentials of output points a and b will not be equal. Specifically taking the working modes of Fig. 9(a) and (b) as the examples during the positive modulation period, the parasitic capacitor voltage in Fig. 9(a) can be expressed as follows:

$$u_{C\mathrm{pv}} = \frac{E - u_{\mathrm{dc}}}{L_a + L_b} L_b = \frac{E}{\frac{L_a}{L_b} + 1} - \frac{u_{\mathrm{dc}}}{\frac{L_a}{L_b} + 1}. \tag{8}$$

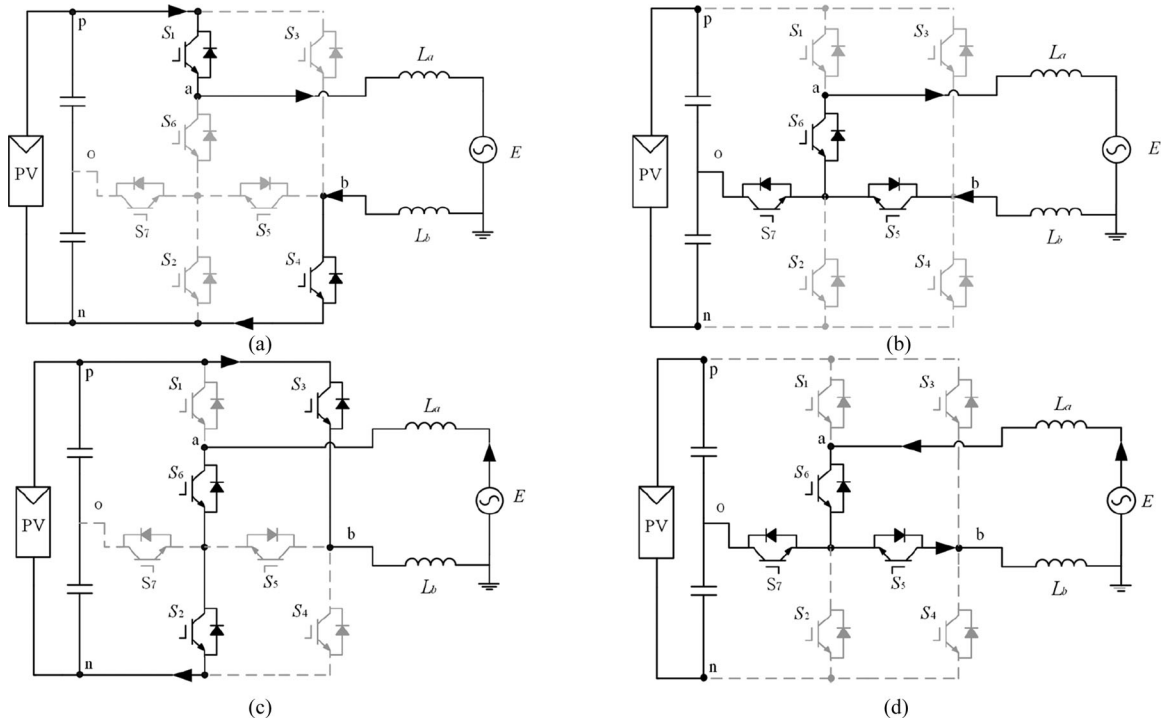


Fig. 12. (a) Energy transferring mode and (b) freewheeling mode during the positive half period. (c) Energy transferring mode and (d) freewheeling mode during the negative half modulation reference period of the NPC inverter in Fig. 11(b).

While the parasitic capacitor voltage in Fig. 9(b) can be derived as follows:

$$u_{C\mathrm{pv}} = \frac{E}{L_a + L_b} L_b - \frac{u_{\mathrm{dc}}}{2} = \frac{E}{\frac{L_a}{L_b} + 1} - \frac{u_{\mathrm{dc}}}{2}. \tag{9}$$

Equations (8) and (9) reveal that the unbalanced filters $L_a$ and $L_b$ could cause the parasitic capacitor voltage of $u_{C\mathrm{pv}}$ fluctuating during the transition of energy transferring modes and the freewheeling modes. Furthermore, when the filter inductors are saturated, the equivalent inductance of $L_a$ and $L_b$ may be unbalanced. Thus, the high frequency fluctuation of $u_{C\mathrm{pv}}$ will also occur according to (8) and (9).

## V. Comparison With Other NPC Topologies

To make a specific analysis of the presented two types of NPC inverters with the unidirectional and bidirectional clamping circuits, respectively, a comparison between the generalized NPC topologies in this paper and the traditional NPC inverters is presented in this Section.

Fig. 13 shows the traditional NPC single-phase inverters, which have been previously reported in [11]–[14]. They also have the same function of clamping the common-mode voltage to be half of the dc-link voltage during the freewheeling modes. From the point of switch counts and device losses, the comparative analysis between the generalized NPC inverters in Figs. 7 and 11 and the traditional NPC inverters in Fig. 13 is given in Tables I and II. In specific, Table I lists the total device counts and the conduction device numbers under different operation modes and Table II lists the numbers of high frequency switching devices with the analysis of the corresponding voltage stresses during the transitions of switching modes. Because the topologies in Figs. 7, 11, and 13 are all modulated by the unipolar sinusoidal pulse width modulation (SPWM), according to Table II, when the circuit parameters and the device types are the same, the switching losses among the aforementioned topologies will be similar except for the topology of Fig. 13(b). However, the conduction device counts of the presented inverters are quite different. So, based on the circuit parameters listed in Table III, a quantitative calculation to compare the losses can be derived from the following losses calculation procedures. The switch conduction losses, $P_{\mathrm{CON-S}}$, can be calculated as follows [18], [29], [30]:

$$\begin{aligned} P_{\mathrm{CON-S}} &= U_{\mathrm{CE-S}} \times I_{\mathrm{C}} \\ &= \frac{1}{2\pi} \int_0^{\pi} i_{\mathrm{C}}(t) \times u_{\mathrm{CE-S}}(t) \times d(t) d(\omega t). \end{aligned} \tag{10}$$

The diodeconduction losses, $P_{\mathrm{CON-D}}$, can be calculated as

$$\begin{aligned} P_{\mathrm{CON-D}} &= U_{\mathrm{ak-D}} \times I_C \\ &= \frac{1}{2\pi} \int_0^{\pi} i_C(t) \times u_{\mathrm{ak-D}}(t) \times d(t) d(\omega t) \end{aligned} \tag{11}$$

where $U_{\mathrm{CE-S}}$ is the collector–emitter voltage drop of insulated-gate bipolar transistors (IGBTs), $U_{\mathrm{ak-D}}$ is the anode–cathode voltage drop of diodes, $I_C$ represents the conducting current through the devices, and $d(t)$ is the duty ratio of SPWM.

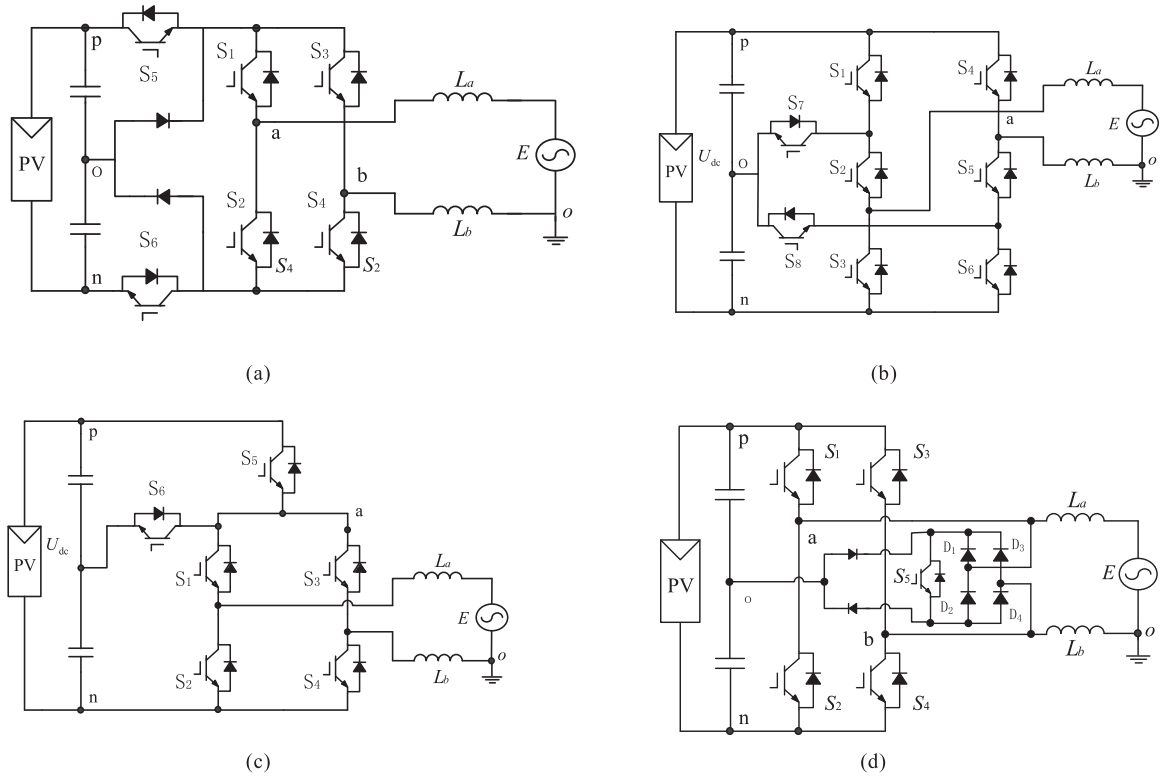


Fig. 13. Traditional NPC topologies in (a) [12], (b) [13], (c) [11], and (d) [14].

TABLE I
COMPARISON OF THE DEVICE COUNTS AND CONDUCTION LOSSES

| Topologies | Switches count | Diodes count | Conduction switches in positive energy transferring modes | Conduction switches in negative energy transferring modes | Conduction devices in freewheeling modes |
|---|---|---|---|---|---|
| Fig. 7(a) | 6 | 4 | 2 | 2 | 1 switch and 1 diode |
| Fig. 7(b), (c) | 6 | 4 | 3 | 3 | 1 switch and 1 diode |
| Fig. 7(d), (e) | 6 | 4 | 2 | 3 | 1 switch and 1 diode |
| Fig. 7(f), (g) | 6 | 4 | 3 | 2 | 1 switch and 1 diode |
| Fig. 11(a), (d) | 7 | 0 | 2 | 2 | 2 switches |
| Fig. 11(b), (e) | 7 | 0 | 2 | 3 | 2 switches |
| Fig. 11(c), (f) | 7 | 0 | 3 | 2 | 2 switches |
| Fig. 13(a) | 6 | 2 | 4 | 4 | 2 switches |
| Fig. 13(b) | 8 | 0 | 4 | 2 | 4 switches |
| Fig. 13(c) | 6 | 0 | 3 | 3 | 2 switches |
| Fig. 13(d) | 5 | 6 | 2 | 2 | 1 switch and 2 diodes |

TABLE II
COMPARISON OF THE HIGH SWITCHING FREQUENCY DEVICE COUNTS AND THE CORRESPONDING VOLTAGE STRESS

| Topologies | Number of high frequency switching switching switches per switching transient | Voltage stress of switches | Number of high frequency switching switching diodes per switching transient | Voltage stress of diodes |
|---|---|---|---|---|
| Fig. 7, Fig. 13(d) | 2 | $U_{\mathrm{dc}}/2$ | 1 diode | $U_{\mathrm{dc}}$ |
| Fig. 11, Fig. 13(c) | 2 | $U_{\mathrm{dc}}/2$ | 1 body diode | $U_{\mathrm{dc}}$ |
| Fig. 13(a) | 2 | $U_{\mathrm{dc}}/2$ | 2 body diodes | $U_{\mathrm{dc}}$ |
| Fig. 13(b) | 2 (positive period)<br>4 (negative period) | $U_{\mathrm{dc}}/2$<br>$U_{\mathrm{dc}}/2, U_{\mathrm{dc}}/4$ | 2 body diodes | $U_{\mathrm{dc}}/2$ (positive period)<br>$U_{\mathrm{dc}}/4$ (negative period) |

TABLE III
PARAMETERS USED IN EXPERIMENTAL VERIFICATIONS

| Parameters | Value |
|---|---|
| Rate power | 1 kW |
| Input voltage | 200 V |
| Switching frequency | 10 kHz |
| Filters inductors $L_a$ , $L_b$ | 2 mH |
| Grid voltage | 110 V/50 Hz |
| IGBT | FF100R12RT4 |
| Diode | MUR8100T |
| PV parasitic capacitor, $C_{\mathrm{PV}}$ | 470 nF |

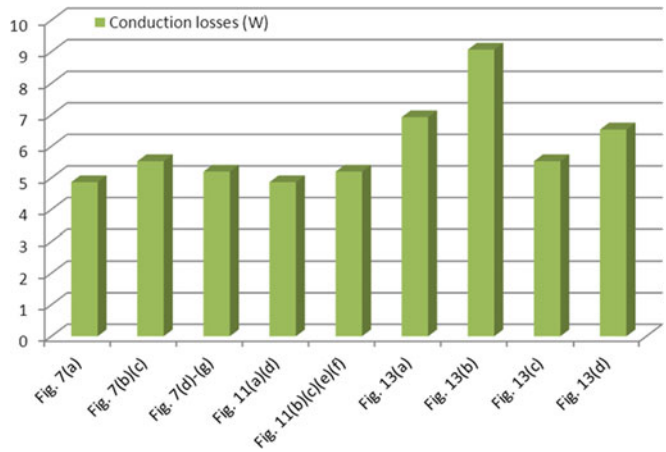


Fig. 14. Calculated conduction losses per NPC topology.

In addition, the switching losses during turning on and off transients can be calculated as follows:

$$P_{\mathrm{SW-ON}} = \frac{U_{\mathrm{CE}} \times I_C}{2} \times t_{\mathrm{tr-on}} \times f_{\mathrm{sw}} \tag{12}$$

$$P_{\mathrm{SW-OFF}} = \frac{U_{\mathrm{CE}} \times I_C}{2} \times t_{\mathrm{tr-off}} \times f_{\mathrm{sw}} \tag{13}$$

where $P_{\mathrm{SW-ON}}$ and $P_{\mathrm{SW-OFF}}$ are the switching losses during turn-on and turn-off transients, respectively, $U_{\mathrm{CE}}$ is the blocking voltage, $t_{\mathrm{tr-on}}$ and $t_{\mathrm{tr-off}}$ represent the switching time of ON and OFF transitions, and $f_{\mathrm{sw}}$ is the switching frequency. All calculated losses of the presented NPC inverters are derived with the same circuit parameters and operation conditions as listed in Table III. Fig. 14 shows the calculated conduction losses of all NPC topologies presented in this paper, which well match with the analysis of conducting devices of NPC inverters in Table I. Fig. 15 illustrates the calculated switching losses of all NPC topologies presented in this paper. It is noted that the NPC topologies will have the very similar switching losses in theory except of the topology in Fig. 13(b). Then, the total losses per topology are drawn in Fig. 16 to clearly demonstrate the efficiency performance of all NPC topologies. It can be observed that the NPC topologies in Figs. 7 and 11 show the similar efficiency performance, which can be further verified in Section VI.

Besides, the current flowing through the neutral-point-clamping switch or diodes is the leakage current, which is normally less than 0.01 A. Therefore, the losses induced by the neutral-point-clamping switch or neutral-point-clamping diodes can be neglected [31].

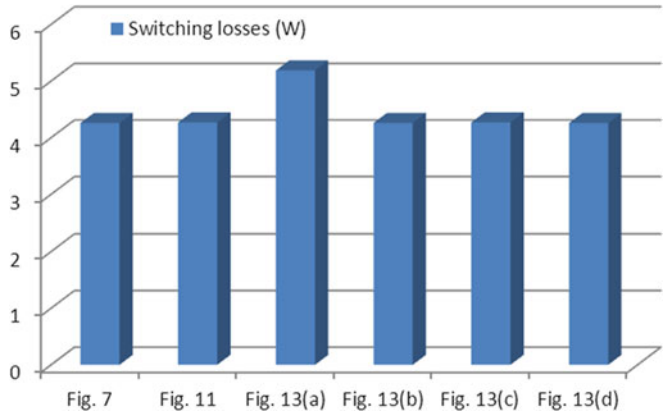


Fig. 15. Calculated switching losses per NPC topology.

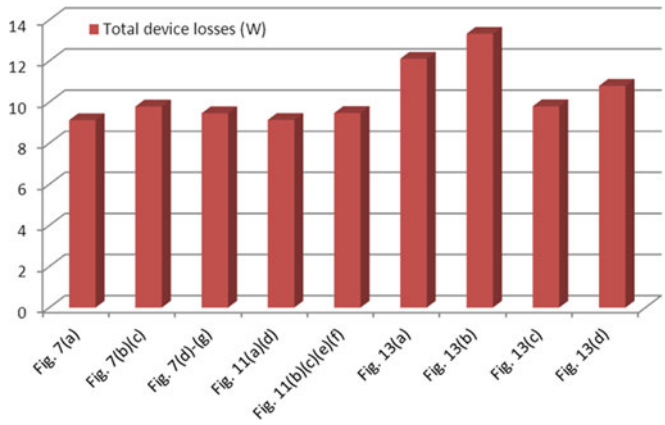


Fig. 16. Calculated total device losses per NPC topology.

## VI. EXPERIMENTAL RESULTS

Since the proposed inverters have the similar output performance, the topologies in Figs. 7(b) and 11(b) were assumed as examples in experimental verifications, whose circuit parameters and operation conditions are listed in Table III. Fig. 17 shows the picture of experimental prototype, where a conventional PR controller was programmed into a dSPACE1103 platform to generate the corresponding gating signals of all switches.

Figs. 18 and 19 show the switching sequences of two inverters proposed in Figs. 7(b) and 11(b). It is observed that the produced gating signals are completely in accordance with the illustrated pulse width modulation strategy in Fig. 10.

Fig. 20 shows the grid voltage and grid current of the inverter in Fig. 2. Also, the leakage current $i_{\mathrm{cm}}$, the bridge voltages $u_{\mathrm{an}}$ and $u_{\mathrm{bn}}$, and the common-mode voltage $u_{\mathrm{cm}}$ of the inverter in Fig. 2 are shown in Fig. 21. It is noted that the common-mode voltage of the traditional H6 inverter is not strictly constant as half of the dc-bus voltage. To make a specific observation of the common-mode behavior, the zoomed in waveforms are given in Fig. 22, which clearly show the fluctuation of bridge voltages. It can be noted that the bridge voltage oscillation is up

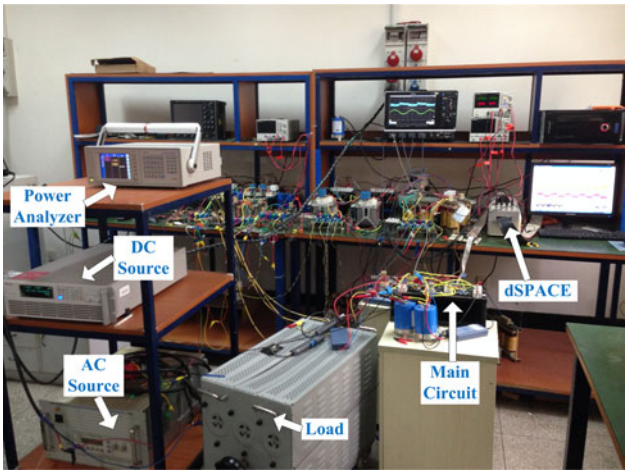


Fig. 17. Experimental platform of NPC inverters.

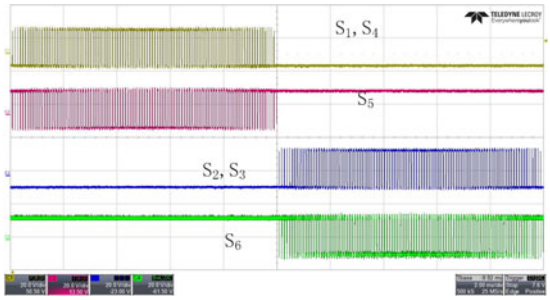


Fig. 18. Gating signals of the NPC inverter in Fig. 7(b).

to 100 V, which is induced by the charging and discharging of switch junction capacitances in freewheeling mode as analyzed in Section II.

Fig. 23 shows the grid voltage and the injected grid current of the NPC inverter in Fig. 7(b), which has the similar output performance as those in Fig. 20. Fig. 24 shows the leakage current $i_{\rm cm}$, the bridge voltages $u_{\rm an}$, $u_{\rm bn}$, and the common-mode voltage $u_{\rm cm}$ of the NPC inverter in Fig. 7(b). Obviously, the generalized NPC inverter has the better performance than the traditional H6 inverter. The zoomed in waveforms of the NPC inverter is shown in Fig. 25, which specifically illustrated the superior common-mode behavior. Similarly, the experimental waveforms of the NPC inverter in Fig. 11(b) were captured in Figs. 26, 27, and 28, which show the similar output performance but a better common-mode behavior than the traditional H6 inverter in Fig. 2. Finally, the neutral-point voltages of the NPC inverters in Figs. 7(b) and 11(b) are captured in Figs. 29 and 30, respectively, where they are both constant as half of the dc-link voltages, respectively.

To further verify the efficiency performance, the operational efficiencies of all NPC topologies presented in this paper were measured by the power analyzer VOLTECH PM6000. Fig. 31 shows the efficiency curves of the topologies in Figs. 7, 11, and 13. Since the experimental prototypes were not optimized, the measured efficiency values are not as high as those of commercial products. But Fig. 31 can effectively demonstrate the comparative efficiency performance of all NPC topologies, which well match with the theoretical calculation in Section V. It is noted that the NPC topologies in Figs. 7 and 11 have the very similar efficiency performance.

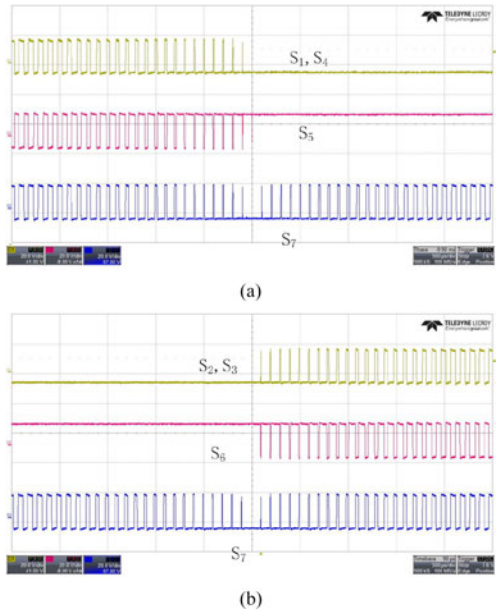


Fig. 19. Gating signals of (a) $S_1 - S4$ and $S_7$, (b) $S_5 - S6$ and $S_7$ of the NPC inverter in Fig. 11(b).

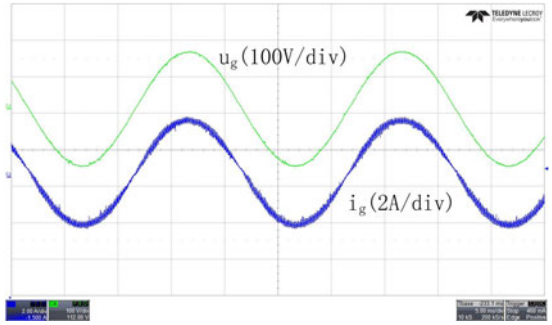


Fig. 20. Experimental grid voltage and grid current of the traditional H6 inverter in Fig. 2.

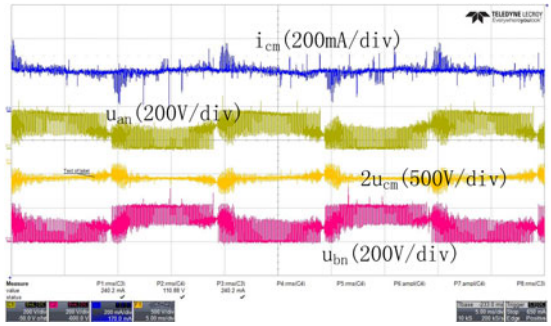


Fig. 21. Experimental waveforms of the traditional H6 inverter in Fig. 2: (from top to bottom) leakage current, switching voltage of bridge a, common-mode voltage, and switching voltage of bridge b.

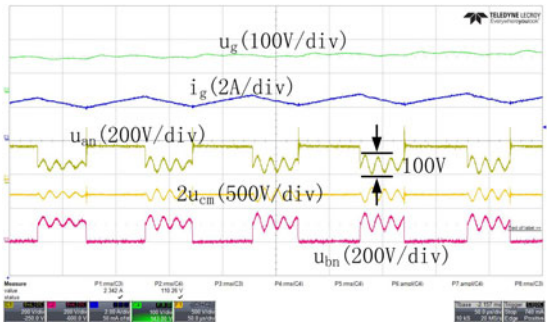


Fig. 22. Zoomed view waveforms of the traditional H6 inverter in Fig. 2: (from top to bottom) grid voltage, grid current, switching voltage of bridge a, common-mode voltage, and switching voltage of bridge b.

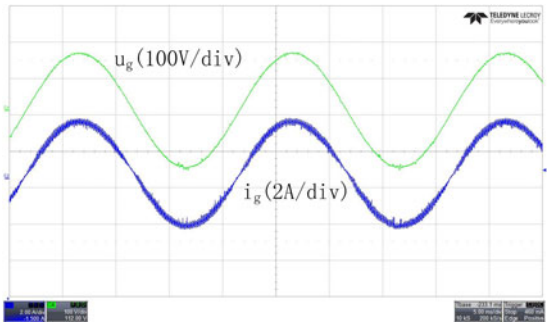


Fig. 23. Experimental grid voltage and grid current of the NPC inverter in Fig. 7(b).

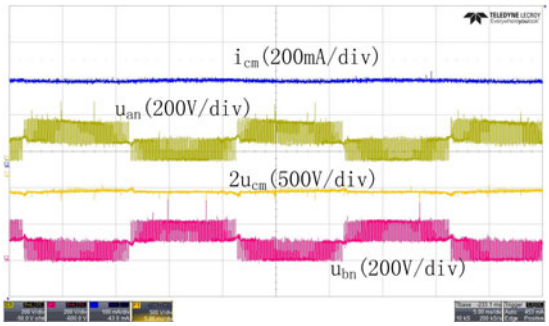


Fig. 24. Experimental waveforms of the NPC inverter in Fig. 7(b): (from top to bottom) leakage current, switching voltage of bridge a, common-mode voltage, and switching voltage of bridge b.

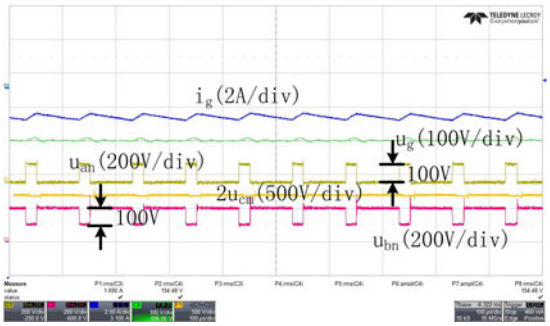


Fig. 25. Zoomed view waveforms of the NPC inverter in Fig. 7(b): (from top to bottom) grid current, grid voltage, switching voltage of bridge a, common-mode voltage, and switching voltage of bridge b.

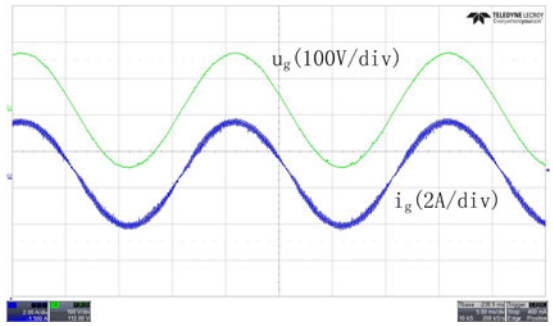


Fig. 26. Experimental grid voltage and grid current of the NPC inverter in Fig. 11(b).

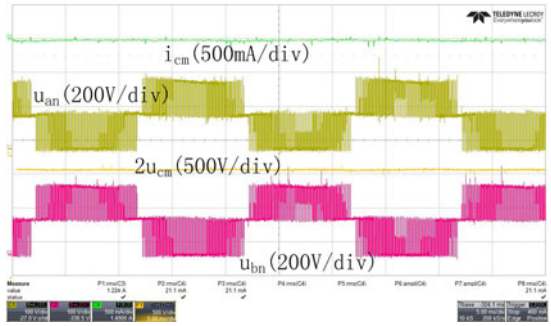


Fig. 27. Experimental waveforms of the NPC inverter in Fig. 11(b): (from top to bottom) leakage current, leg A voltage, common-mode voltage, and leg B voltage.

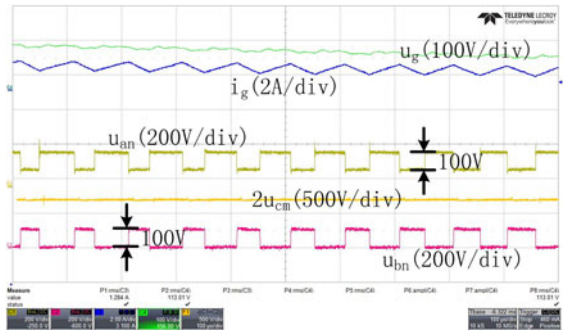


Fig. 28. Zoomed view waveforms of the NPC inverter in Fig. 11(b): (from top to bottom) grid voltage, grid current, leg A voltage, common-mode voltage, and leg B voltage.

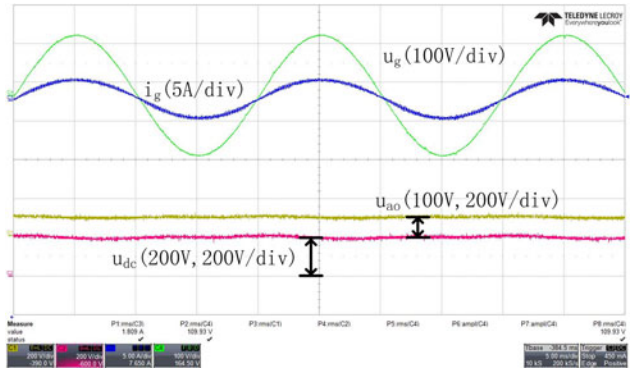


Fig. 29. Experimental waveforms of the NPC inverter in Fig. 7(b).

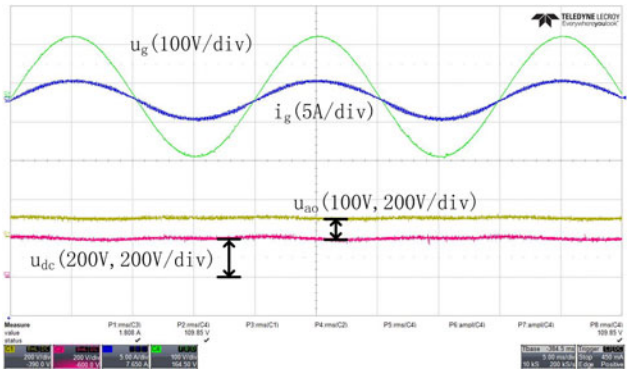


Fig. 30. Experimental waveforms of the NPC inverter in Fig. 11(b).

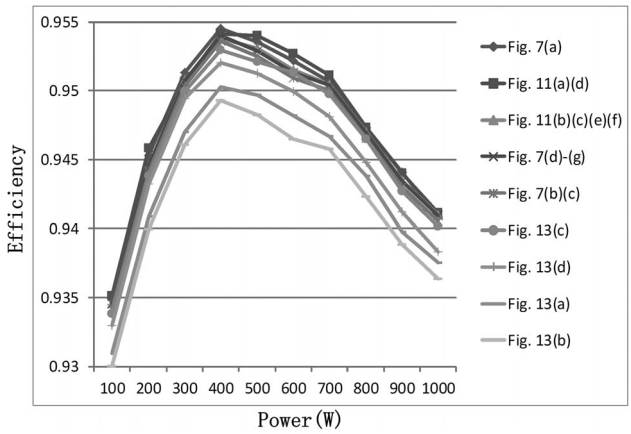


Fig. 31. Measured efficiency curves of all NPC inverters presented in this paper.

## VII. Conclusion

This paper generalizes two kinds of NPC circuits with the unidirectional or bidirectional current flow capability. Then, this paper implements the specific NPC circuits in single-phase PV inverters, where two types of single-phase NPC inverters are fully analyzed. Doing so, the common-mode voltage of single-phase inverter can be effectively maintained constant as half of dc-link voltage. This paper also presents the comparison between the generalized inverters and the traditional NPC topologies. The experimental results verified the performance of the NPC inverters.

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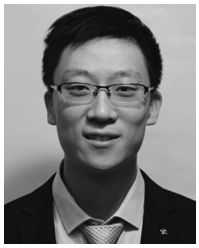

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