Single-Switch High-Frequency DC–DC Converter Using Parasitic Components

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***Abstract*—This paper presents a single-switch isolated dc–dc converter suited for a very high-frequency switching operation, especially above 10 MHz. The converter features a small number of passive components, low-switching loss, and low-voltage stress on the switch. In order to achieve low-voltage stress while maintaining zero voltage switching, the voltage waveform across the switch is shaped by designing the resonant network of the converter. The resonant network includes main parasitic components, such as leakage inductances of the transformer and the junction capacitance of the switch. Furthermore, some resonant elements are entirely replaced by these parasitic components under the specific condition. This paper derives the conditions and then minimizes the number of passive components. To validate the design procedure and the performance of the proposed converter, a GaN-based prototype was implemented. It operates at 10 MHz and provides the output power of 10 W from the dc input voltage of 50 V. The output voltage is regulated to 20 V by the ON–OFF control. Experimental results show that the peak voltage on the switch is reduced to 2.2–2.3 times the dc-input voltage and the efficiency of 69% is achieved under the full load.**

***Index Terms*—High-frequency switching converter, isolated converter, parasitic, resonant converter, single switch, zero voltage switching.**

I. Introduction

INCREASING the power density is one of the most important objectives in power electronics. Since passive components, such as inductors, capacitors, and transformers take significant volume of the converter, it is required to reduce the size and weight of them as much as possible for improving the power density. One of the most effective ways to lessen the size of passive components is increasing the switching frequency [1]–[3]. Recently, advanced switching devices which are suitable for high switching frequency become available, and it gives further chances to enhance the power density.

However, numerous problems are encountered as the switching frequency increases above 10 MHz. The most critical issue is switching losses which are proportional to the switching frequency. Hence, resonant converters using soft-switching techniques, such as zero voltage switching (ZVS) have been highly recommended in high-frequency converter in order to relieve switching losses [4], [5]. Another issue in high-frequency converters is the implementation of gate drive circuit. No matter which gate drive circuits are used, there exists some timing error in gate drive signal. This timing error cannot be neglected when the switching frequency increases to several megahertz. Hence, the switch ON–OFF signal should be controlled more precisely in order to safely operate multiple switches [6]. In addition, even small parasitic capacitances results in high dv/dt noises under high-frequency switching operation. In severe cases, the noises can falsely turn on the high-side switch. In order to immune the dv/dt noises, several candidates such as optocoupler and digital isolator-based drivers have been researched [7]. However, the implementation of these gate drive circuits still increases cost and complexity of the converter.

A single switch resonant converter is an attractive way to address these problems. Switching losses are highly relieved by soft-switching techniques. In addition, the implementation of the gate drive circuit is quite simple since there is no high-side switch. In contrast to these advantages, however, a single-switch resonant converter often has relatively high-voltage stress on the switching device. For instance, in class E topology, which has been widely used for a high-frequency switching, the voltage stress is up to 4.4 times the input voltage [8], [9]. In order to overcome the problem, there have been several approaches to reduce the voltage stress. In [10], the voltage stress on the switch of class E power amplifier is relieved by the additional circuit so called the double resonance circuit. Alternatively, Lee *et al.* [11] present a new design scheme for a class E converter for shaping the voltage waveform and reducing the peak voltage on the switch without additional passive components. Also, several modified topologies with harmonic tuned branches (class F, class Φ, and class Φ_2) have been widely researched [12]–[20]. These topologies utilize harmonic tuned branches to achieve a quasi-square voltage waveform by generating several voltage harmonics at the drain to source node of the switch.

These concepts are also adopted for several isolated type converters in [21]–[25]. Galvanic isolation of a converter operating at several megahertz switching frequency can be achieved by two ways: capacitive isolation and magnetic isolation. In [21] and [22], the capacitive isolation is applied to the class Φ_2 converters, which means they achieve galvanic isolation by capacitors without using transformer. On the other hand, the structure of the magnetically isolated class Φ_2 converter with a transformer is presented in [23], and its design strategy based on an iterative method is proposed in [24].

Manuscript received February 15, 2016; revised May 3, 2016; accepted June 13, 2016. Date of publication June 21, 2016; date of current version February 2, 2017. This work was supported by the Brain Korea 21 Plus Project in 2016. Recommended for publication by Associate Editor J. M. Rivas Davila.

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Digital Object Identifier 10.1109/TPEL.2016.2582831

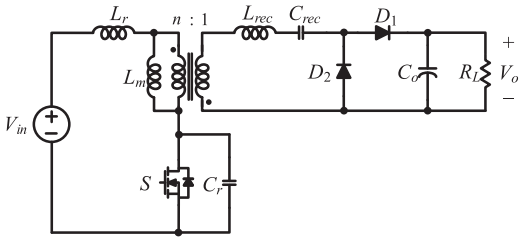

Fig. 1. Schematic of the proposed isolated dc–dc converter.

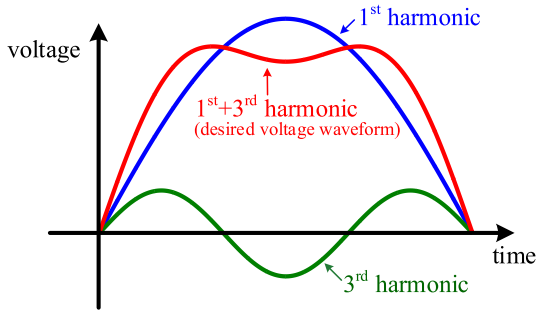

Fig. 2. Half-wave symmetric quasi-trapezoidal waveform.

A previous research of [25] introduces a novel magnetic-isolated type high-frequency converter with reduced number of passive components. This paper presents the details of the previous research [25], and extends it with the analysis about the operation principle of the converter. The converter features low-voltage stress and low switching losses of the switch. Another major benefit of this converter is that the resonant network absorbs the parasitic components, such as leakage inductances of the transformer and the junction capacitance of the switch. Parasitic absorption has actually been widely used in many topologies [17], [26]. Especially in [26], not only leakage inductances are absorbed to the resonant network but also they entirely replace some inductive components, which simplifies the circuit and lowers the cost. The proposed design scheme also includes the condition to replace several resonant elements by the parasitic components. Then, the number of passive components is minimized while still maintaining the merits of the converter such as the low-voltage stress and ZVS operation.

The design scheme is applied to implement a 10-MHz 10-W laboratory prototype providing 20-V dc output from 50-V dc input. Since the operating frequency of the prototype converter is fixed at 10 MHz, an ON–OFF control scheme is employed to achieve ZVS operation over a wide load range [27], [28]. Simulation and experimental results of the prototype are shown to validate the proposed concept.

II. Design Scheme for Proposed Isolated DC–DC Converter

Fig. 1 shows the schematic of the proposed isolated single-switch dc–dc converter. The converter is divided by two stages: inverter stage and rectifier stage. For the rectifier stage, a half-wave rectifier which consists of diodes D_1 and D_2 is utilized. The inverter stage of the converter consists of a switch S, a high-frequency transformer which has turns ratio of n, and several resonant components such as $L_r, L_{\rm rec}, C_{\rm rec}$, and C_r. In Fig. 1, the transformer is described as an equivalent model. Here, the magnetizing inductance of the transformer is denoted as $L_{\rm m}$, and leakage inductances are absorbed into L_r and $L_{\rm rec}$. In this paper, the design scheme focuses on selecting all the resonant elements (L_m, L_r, $L_{\rm rec}$, $C_{\rm rec}$, and C_r) to satisfy 1) the low-voltage stress with the ZVS operation and 2) the required output power.

A. Design of the Resonant Elements for Shaping the Switch Voltage Waveform

For achieving the low-voltage stress and ZVS of the switch at the same time, the voltage waveform across the switch is required to be shaped to a half-wave symmetric quasi-square waveform shown in Fig. 2 [19]. This waveform is dominated by the fundamental component and includes the third-order harmonic component which has negative peak around the maximum point of the fundamental component. Also, it should be noted that the second-order harmonic component is highly attenuated in the waveform. That is because the second-order harmonic component makes the waveform be asymmetric, consequently results in high peak voltage on the switch. By realizing the desired waveform, the voltage stress is reduced to about two times the dc-input voltage [20].

Rivas [19] shows that a voltage waveform is closely related to pole and zero locations of the impedance seen at the drain to source node of the switch Z_{ds}. A pole makes Z_{ds} have a high impedance at the pole frequency, and allows the frequency content to predominate in the voltage across the switch. On the other hand, a zero impose a low impedance at the frequency, which means that the frequency content is highly suppressed in the switch voltage. Therefore, as elaborated in [19], the desired voltage waveform in Fig. 2 is realized by locating the zero at $2\omega_{\rm sw}$ and two poles near $\omega_{\rm sw}$ and $3\omega_{\rm sw}$ where $\omega_{\rm sw}$ is the switching frequency.

In the case of the proposed structure, the five resonant elements (L_m, L_r, $L_{\rm rec}$, $C_{\rm rec}$, and $C_{\rm r}$) compose Z_{ds}, and the equivalent circuit of Z_{ds} is depicted as Fig. 3. Here, the half-wave rectifier stage is considered as a resistor model, and represented as $R_{\rm rec}$. Then, Z_{ds} is given by

$$Z_{ds}(s) = \frac{N_1 s^3 + N_2 s}{K_1 s^4 + K_2 s^2 + K_3}$$
$$\begin{cases} N_1 = \left(L_r L_{\rm rec} + L_m L_r/n^2 + L_m L_{\rm rec}\right) C_{\rm rec} \\ N_2 = (L_m + L_r) \\ K_1 = \left(L_r L_{\rm rec} + L_m L_r/n^2 + L_m L_{\rm rec}\right) C_r C_{\rm rec} \\ K_2 = \left(L_r C_r + L_m C_r + L_{\rm rec} C_{\rm rec} + L_m C_{\rm rec}/n^2\right) \\ K_3 = 1 \end{cases} \tag{1}$$

As explained above, the zero of Z_{ds} needs to be placed exactly at $2\omega_{\rm sw}$ in order to suppress the second-order harmonic component of the switch voltage as much as possible. From the numerator of (1), the condition that Z_{ds} has zero at $2\omega_{\rm sw}$ is

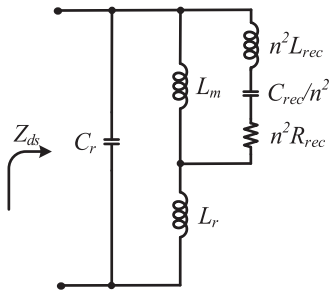

Fig. 3. Equivalent circuit of drain-to-source impedance of the switch $Z_{\rm ds}$.

given by

$$\omega_{\rm sw} = \frac{1}{2}\sqrt{\frac{L_m + L_r}{(L_r L_{\rm rec} + L_m L_r/n^2 + L_m L_{\rm rec})C_{\rm rec}}}. \quad (2)$$

The next step is to locate two poles near $\omega_{\rm sw}$ and $3\omega_{\rm sw}$, respectively, since high impedances at these frequencies ensure the switch voltage V_{ds} is dominated by the fundamental and third-order harmonic components. Here, the first pole should be located slightly higher than $\omega_{\rm sw}$, because this pole location makes Z_{ds} become inductive at $\omega_{\rm sw}$. Then, the voltage touches zero point before the switch turns on, i.e., ZVS of the switch. The other pole should be located lower than $3\omega_{\rm sw}$ in order to make Z_{ds} become capacitive at $3\omega_{\rm sw}$. This condition allows the fundamental and third-order harmonic components of V_{ds} to be in phase, and ensure that the switch has a flat peak voltage while maintaining ZVS of the switch [18]. In this paper, the location of the first pole is defined as $m_1\omega_{\rm sw}$ and the other pole is defined as $m_2\omega_{\rm sw}$. From the above requirements, it is clear that the value of m_1 is in the range of 1 to 2 and that of m_2 is in the range of 2 to 3. Pole locations are closely related to the characteristic equation which is the denominator of (1). From (1), the conditions for the desired pole locations are derived as

$$\frac{K_2}{K_1} = \left(m_1^2 + m_2^2\right)\omega_{\rm sw}^2$$
$$\frac{K_3}{K_1} = m_1^2 m_2^2 \omega_{\rm sw}^4. \quad (3)$$

From (2) and (3), following equations are derived:

$$L_m = \frac{n}{m_1^2 m_2^2 \omega_{\rm sw}^2}\sqrt{\frac{4\left(m_1^2 + m_2^2 - 4\right) - m_1^2 m_2^2}{C_r C_{\rm rec}}},$$
$$L_{\rm rec} = \frac{\left(m_1^2 + m_2^2 - 4\right)}{m_1^2 m_2^2 C_{\rm rec}\omega_{\rm sw}^2} - \frac{1}{n^2}L_m,$$
$$L_r = \frac{4}{m_1^2 m_2^2 C_r \omega_{\rm sw}^2} - L_m. \quad (4)$$

As a result, resonant elements satisfying (4) assure that poles are located at $m_1\omega_{\rm sw}$ and $m_2\omega_{\rm sw}$, respectively, and zero is located at $2\omega_{\rm sw}$. From these pole and zero locations, the switch obtains the desired quasi-trapezoidal voltage waveform if m_1 and m_2 are properly selected. Reasonable values of m_1 and m_2 will be discussed in the Section II-D.

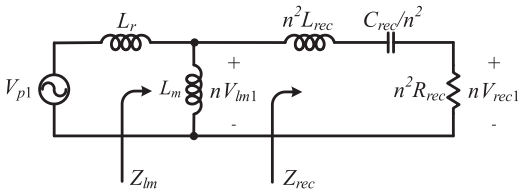

Fig. 4. Simplified circuit of the proposed converter with the fundamental-harmonic approximation.

B. Design of the Resonant Elements for Achieving the Desired Output Power

While the voltage waveform is designed to be the desired waveform, the power transferred to the load is not considered in (4). Therefore, additional analysis is needed to achieve the desired output power. In order to simplify the analysis, it is assumed that the switch has a square waveform which has an average value of V_{in} and swings between 0 and $2{\rm V}_{\rm in}$ [18]. Thus, the primary-side voltage $V_p = (V_{\rm in} - V_{\rm ds})$ has a square waveform which has an average value of zero and swings between $-V_{\rm in}$ and $V_{\rm in}$. Since the output power is mainly delivered by the fundamental component, V_p is considered as its fundamental component V_{p1}.

In this paper, the rectifier stage is simply modeled as the resistance $R_{\rm rec}$. Here, the effect of the diode junction capacitance is neglected since it does not severely affect the operation of the converter. The value of $R_{\rm rec}$ is determined as $2R_{\rm L}/\pi^2$ and then the power consumption of the rectifier stage is equal to that of $R_{\rm rec}$. This simplification reduces the design complexity under the assumption that the main power is transferred by the fundamental component and there is no loss in the rectifier circuit. The details of the rectifier modeling are explained in [29]. Here, the fundamental voltage component across $R_{\rm rec}$ is defined as $V_{\rm rec1}$.

By the above assumptions, the structure of the proposed converter is simplified as shown in Fig. 4. Here, the reflected impedance of the secondary network which consists of $L_{\rm rec}$, $C_{\rm rec}$, and $R_{\rm rec}$ is represented as $Z_{\rm rec}$, and it is given by

$$Z_{\rm rec} = n^2\left(j\omega_{\rm sw}L_{\rm rec} + \frac{1}{j\omega_{sw}C_{\rm rec}} + R_{\rm rec}\right). \quad (5)$$

The impedance of the parallel circuit of L_m and $Z_{\rm rec}$ is represented as Z_{lm}, and it is given by

$$Z_{lm} = j\omega_{\rm sw}L_m || Z_{\rm rec} = \frac{j\omega_{\rm sw}L_m Z_{\rm rec}}{j\omega_{\rm sw}L_m + Z_{\rm rec}}. \quad (6)$$

From the simplified circuit, $V_{\rm rec1}$ is calculated as follows:

$$V_{\rm rec1} = \left|\frac{nZ_{lm}R_{\rm rec}}{(j\omega_{\rm sw}L_r + Z_{lm})\,Z_{\rm rec}}\right| V_{p1}. \quad (7)$$

Consequently, the output power delivered to load is calculated as

$$P_{o,\rm calc} = \frac{V_{\rm rec1}^2}{R_{\rm rec}} = \frac{8r^2 R_{\rm rec}}{\pi^2 n^2\left(\left(\omega_{\rm sw}L_{\rm rec} - \frac{1}{\omega_{\rm sw}C_{\rm rec}}\right)^2 + R_{\rm rec}^2\right)}V_{\rm in}^2 \quad (8)$$

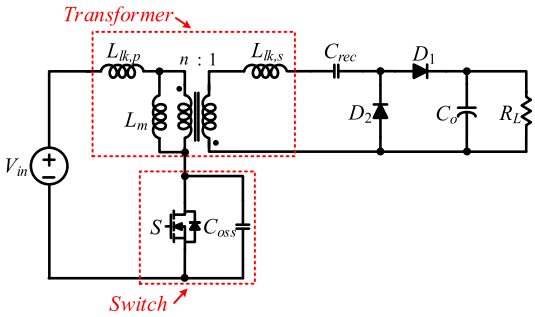

Fig. 5. Schematic of the proposed structure with the minimal number of passive components.

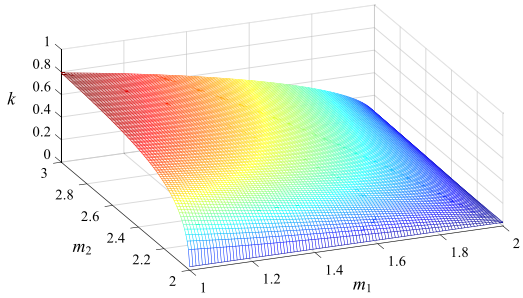

Fig. 6. Coupling coefficient determined by m_1 and m_2.

where $r = |Z_{lm}/(j\omega_{\rm sw}L_r + Z_{lm})|$.

From (8), where P_o is given as the desired output power, the value of $C_{\rm rec}$ is be derived as

$$C_{\rm rec} = \frac{1}{\omega_{\rm sw}^2 L_{\rm rec} + \omega_{\rm sw}\sqrt{\frac{R_{\rm rec}\left(8r^2V_{\rm in}^2 - \pi^2 P_o R_{\rm rec}\right)}{n^2\pi^2 P_o}}}. \quad (9)$$

Once the resonant elements satisfy (4) and (9) simultaneously, the desired output power is approximately achieved while maintaining the voltage waveform on the switch. The real output power, however, is always higher than the calculated output power $P_{o,\rm calc}$ because the output power calculation is based on the fundamental-harmonic approximation. In fact, the output power is delivered, unlike the previous assumption, not only by the fundamental component but also by other harmonic components. Nevertheless, it is a good starting point of designing the secondary-side capacitance $C_{\rm rec}$. If the more accurate power design is required, the value of $C_{\rm rec}$ needs to be tuned. By adopting a tuning factor β which has a value less than 1, the value of $C_{\rm rec}$ can be adjusted as

$$C_{\rm rec}^* = \frac{1}{\omega_{\rm sw}^2 L_{\rm rec} + \omega_{\rm sw}\sqrt{\frac{R_{\rm rec}\left(8r^2V_{\rm in}^2 - \pi^2\beta P_o R_{\rm rec}\right)}{n^2\pi^2\beta P_o}}}. \quad (10)$$

The effects of high-order harmonic components to the output power will be explained in Section IV.

C. Minimization of Passive Components

As shown in the above sections, there are four equations from (4) and (9) to be satisfied. However, it is noted that there are more resonant elements than given equations. Thus, there are infinite solutions to satisfy all the requirements. It means that the converter has more design freedom. In this paper, the number of passive components is minimized by the degree of freedom.

In the proposed converter, the leakage inductances of the transformer ($L_{lk,p}$ and $L_{lk,s}$) and the junction capacitance of the switch (C_{oss}) are absorbed into Z_{ds}. The goal of this section is to replace L_r, $L_{\rm rec}$, and C_r with $L_{lk,p}$, $L_{lk,s}$, and $C_{\rm oss}$, respectively, in order to minimize the number of passive components and improve the power density of the converter. The schematic of the converter with the minimal number of passive components is described in Fig. 5. The transformer is represented by a typical equivalent model which has the magnetizing inductance, leakage inductances, and the ideal transformer. The switch device is depicted as a parallel connection of the ideal switch S and the junction capacitor C_{oss}. In this case, the inverter stage of the converter consists of the transformer, the switch, and $C_{\rm rec}$. The other resonant elements are provided by parasitic components of the transformer and the switch device.

The conditions which L_r and $L_{\rm rec}$ are replaced by $L_{lk,p}$ and $L_{lk,s}$ are derived by a relationship between the magnetizing inductance and leakage inductances of the transformer. The relationship is restricted by the coupling coefficient of the transformer as follows:

$$L_r = L_{lk,p} = \frac{1-k}{k}L_m$$
$$L_{\rm rec} = L_{lk,s} = \frac{1-k}{n^2 k}L_m \quad (11)$$

where k is the coupling coefficient of the transformer. From (4) and the additional constraints of (11), the resonant elements and k are determined by

$$L_m = \frac{n^2\left(m_1^2+m_2^2-4\right)}{m_1^2 m_2^2\omega_{\rm sw}^2}\sqrt{1-\frac{m_1^2m_2^2}{4\left(m_1^2+m_2^2-4\right)}}\frac{1}{C_{\rm rec}}$$
$$L_{\rm rec} = \frac{\left(m_1^2+m_2^2-4\right)}{m_1^2m_2^2\omega_{\rm sw}^2}\left[1-\sqrt{1-\frac{m_1^2m_2^2}{4\left(m_1^2+m_2^2-4\right)}}\right]\frac{1}{C_{\rm rec}}$$
$$L_r = \frac{n^2\left(m_1^2+m_2^2-4\right)}{m_1^2m_2^2\omega_{\rm sw}^2}\left[1-\sqrt{1-\frac{m_1^2m_2^2}{4\left(m_1^2+m_2^2-4\right)}}\right]\frac{1}{C_{\rm rec}}$$
$$C_r = \frac{1}{n^2}\left(\frac{4}{m_1^2+m_2^2-4}\right)C_{\rm rec}$$
$$k = \sqrt{1-\frac{m_1^2m_2^2}{4\left(m_1^2+m_2^2-4\right)}}. \quad (12)$$

As shown in (12), the coupling coefficient k is determined by m_1 and m_2. As previously defined, m_1 is the value between 1 and 2 and m_2 is the value between 2 and 3. Then, the value of k is given in the reasonable range which is between 0 and 0.79 as shown in Fig. 6. Fortunately, k is adjustable factor which is related to the gap between the primary and secondary windings. Thus, it is possible to replace L_r and $L_{\rm rec}$ by the leakage inductances of the transformer.

The subsequent step is to find the condition that the capacitor which is externally connected to the switch device is completely

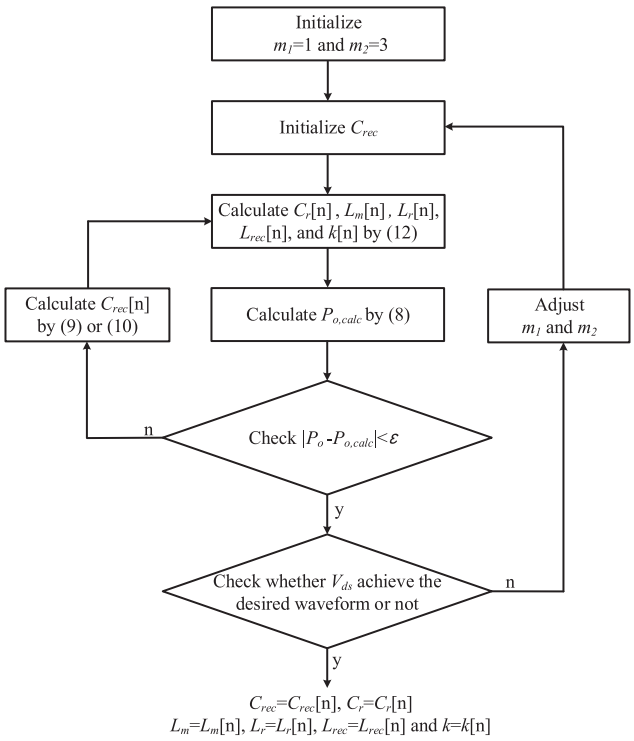

Fig. 7. Flowchart of the design procedure determining parameters.

eliminated, i.e., C_r is equal to C_{oss}. According to (12), the condition is given by

$$n = \sqrt{\left(\frac{4}{m_1^2 + m_2^2 - 4}\right)\frac{C_{\rm rec}}{C_{\rm oss}}}. \tag{13}$$

However, without the additional capacitor, the junction capacitance of the switch device is nonlinearly changed by the voltage across the switch in many practical cases. It implies that the desired characteristics of the converter cannot be achieved where the input voltage is widely varied. This nonlinearity effect is suppressed by attaching the large capacitor to the switch in parallel. Therefore, the constraint to eliminate the extra capacitor in (13) is not applied in this paper.

D. Overall Design Procedure

In (12), the resonant elements L_m, $L_{\rm rec}$, L_r, and $C_{\rm r}$ are expressed by $C_{\rm rec}$. On the other hand, the value of $C_{\rm rec}$ is determined by the other resonant elements as shown in (9). In order to solve the recursive equations, this paper applies an iterative method. The overall design procedure based on the iterative method is shown in Fig. 7.

The design procedure starts from setting $m_1 = 1$ and $m_2 = 3$. Next, an arbitrary initial value of $C_{\rm rec}$ is selected. Then, the value of L_m, L_r, $L_{\rm rec}$, C_r, and k are determined by (12). Subsequently, the output power is calculated by (8). If the difference between the required output power P_o and the calculated output power $P_{o,\rm calc}$ is larger than the acceptable margin (denoted as ε in Fig. 7), the value of $C_{\rm rec}$ is adjusted to reduce the power difference. The value of $C_{\rm rec}$ is obtained by two ways (9) and (10). In (9), $C_{\rm rec}$ is calculated from the output power (8) obtained by the simplified equivalent circuit of the converter with fundamental-harmonic approximation. However, it results in an excessive output power as mentioned in Section II-B. In (10), the output power tuning factor β is adopted to tune the value of resonant elements and achieve the desired output power accurately. Using the calculated value of $C_{\rm rec}$, the other parameters are recalculated by (12) again. After several iterations, $P_{o,\rm calc}$ gradually converges to P_o. Consequently, L_m, L_r, $L_{\rm rec}$, C_r, $C_{\rm rec}$, and k are determined by the given m_1 and m_2. Then, the designed resonant elements are verified by simulation in order to check whether the desired voltage waveform is obtained or not. If not, m_1 and m_2 need to be adjusted.

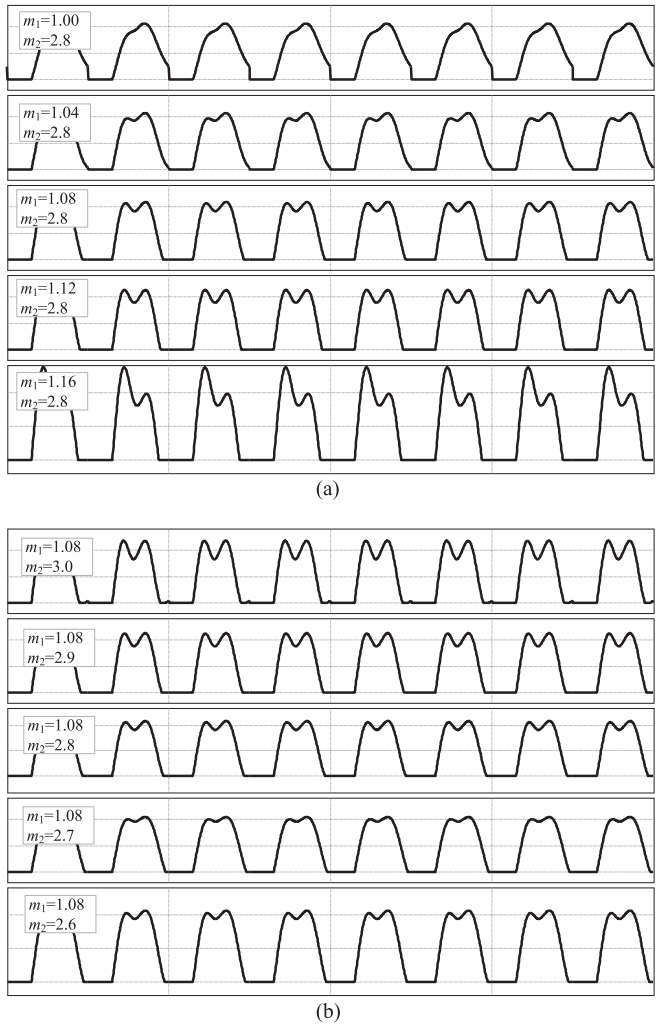

Fig. 8. Waveform of V_{ds} according to m_1 and m_2 where (a) the value of m_2 is fixed to 2.8 and (b) the value of m_1 is fixed to 1.08.

Fig. 8 shows the influence of m_1 and m_2 on the voltage waveform. Fig. 8(a) shows the voltage waveforms where m_2 is fixed and m_1 is changed. The value of m_1 is closely related to ZVS condition of the switch. As shown in Fig. 8(a), ZVS fails if the value of m_1 is exactly at 1. Increasing m_1 allows Z_{ds} to become inductive at the switching frequency and realizes the ZVS operation. However, excessive increase of m_1 lowers the

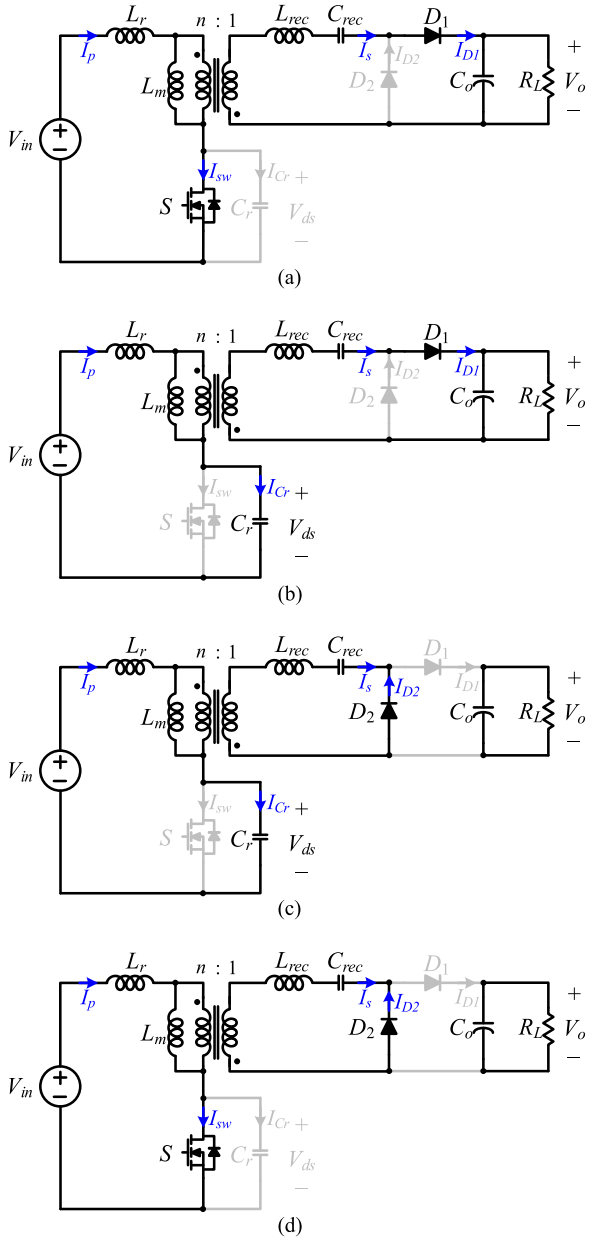

Fig. 9. Equivalent circuits of the proposed converter over Mode 1 to 4.

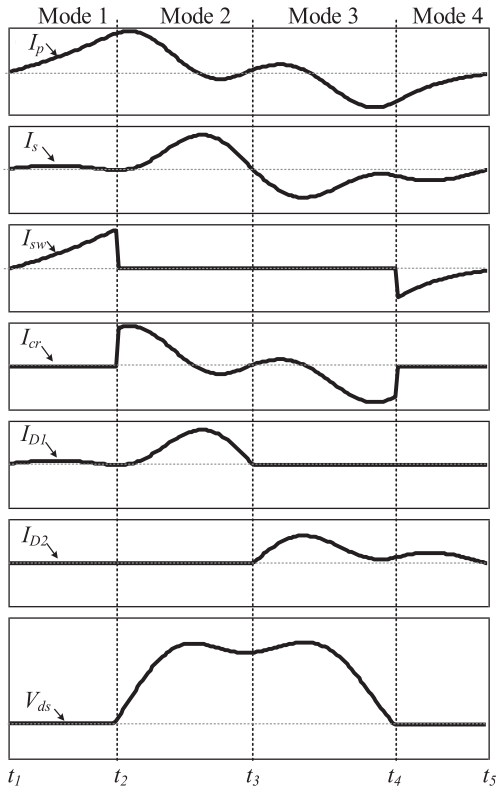

Fig. 10. Key waveforms of the proposed converter.

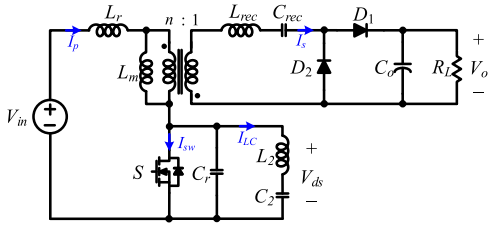

Fig. 11. Conventional isolated dc–dc converter with the second-order harmonic tuned branch (defined as "Converter A" in this paper).

impedance of Z_{ds} at the fundamental frequency, and it ruins the voltage waveform. Based on our experience, the value of m_1 is selected in the range of 1.06 to 1.1. Fig. 8(b) shows the opposite case where m_1 varies but m_2 is fixed. The value of m_2 mainly determines the magnitude of the third-order harmonic component of V_{ds}. If m_2 has a value of 3, the voltage stress is increased since excessive third-order harmonic is included in the voltage waveform. On the other hand, too low value of m_2 causes the second-order harmonic to appear, and the voltage waveform is skewed. Therefore, the acceptable range of m_2 is from 2.7 to 2.9.

III. Mode Analysis

The converter has four modes of operation. Fig. 9 describes the operating modes of the proposed converter during a single-switching period T_s. Fig. 10 shows key waveforms at each mode. In Mode 1, the primary-side current I_p is zero at the end of the previous mode. At t_1 where Mode 1 starts, the switch, S, and the load-side diode, D_1, are conducting. From t_1 to t_2, the primary-side current increases and the primary-side inductor is continuously charged. During this interval, the secondary-side current I_s flows through D_1 and supplies load power. At t_2, Mode 2 starts with S turned OFF. Then, the parallel capacitor C_r is involved in the conducting path of the circuit. Thus, I_p and I_s are determined by the resonant network which consists of the five resonant elements. Also, the voltage waveform is shaped to the desired waveform by Z_{ds} designed in the previous section. Mode 2 finishes where I_s drops to zero at t_3, and D_1 is turned OFF. Note that D_1 and D_2 are complementary pair. Therefore, I_s flows in the reverse direction through D_2 in Mode 3. Subsequently, the resonant energy of C_r is discharged, and the voltage across the switch is decreasing. Where C_r is fully

TABLE I
PARAMETERS FOR SIMULATIONS

Parameters	Conventional converter	Proposed converter	
	Converter A	Converter B	Converter C
$C_{\rm rec}$	5.11 [nF]	415 [pF]	354 [pF]
C_r	500 [pF]	332 [pF]	283 [pF]
L_m	285 [nH]	246 [nH]	289 [nH]
L_r	28.5 [nH]	87.8 [nH]	103 [nH]
$L_{\rm rec}$	550 [nH]	87.8 [nH]	103 [nH]
L_2	186 [nH]	–	–
C_2	340 [pF]	–	–
n	1	1	1

discharged at t_4, the back diode of S is turned ON. In Mode 4, $I_{\rm sw}$ flows through the back diode and it continuously discharges the energy of the primary-side inductor. Where $I_{\rm sw}$ and I_p reach to zero, Mode 4 finishes and the operation of the circuit is returned to Mode 1.

IV. CONVENTIONAL CONVERTER WITH HARMONIC TUNED BRANCH

There is an alternative and more intuitive way to achieve a reduced voltage peak and ZVS of the switch. It is to use harmonic tuned branches. This strategy has been widely used in many conventional topologies. For instance, class F amplifier uses several odd harmonic tuned branches to inject the odd-harmonic components, and successfully flattens the peak voltage of the switch [12], [13]. Also, class Φ_2 (class EF2) makes use of the *L-C* branch which is tuned two times the switching frequency in order to reject the second-order harmonic and ultimately achieve a quasi-trapezoidal voltage waveform on the switch [17], [20].

The similar concept is applied to the isolated class Φ_2 converter in [24]. The schematic of the converter presented in [24] is illustrated in Fig. 11. As shown, the isolated converter has a similar structure with the proposed converter except for the *L-C* branch. For that reason the converter in Fig. 11 is selected as the comparison target in this paper. For convenience, the converter is defined as "Converter A" in the remaining part of this section. The proposed converter is compared with the Converter A by simulation.

Simulations are conducted under the same operating condition: $V_{\rm in}=$ 50V, $V_o=$ 20V, $P_o=$ 10W, and $f_{\rm sw}=$ 10MHz. Parameters for Converter A are determined by the design procedure scheme explained in Section II. The designed parameters are shown in Table I. Here, the proposed converters are classified into "Converter B" and "Converter C" by the usage of the output power tuning factor β. Converter B is designed without output power tuning procedure (i.e., designed by (9)), and Converter C is designed with output power tuning procedure (i.e., designed by (10)).

Fig. 12 shows the drain-to-source voltage V_{ds}, the primary-side current I_p, the rectifier-side current I_s, the current through the *L-C* branch I_{LC}, and the switch current $I_{\rm sw}$. Waveforms of Converter A are represented by red lines, those of Converter B are represented by blue lines, and those of Converter C are represented by green lines. Note that the desired voltage waveform on the switch is maintained in all cases. Instead, the noticeable differences are shown in current waveforms. In Converter A, the second-order harmonic current passes through the *L-C* branch, so the fundamental component is dominant in I_p and I_s. On the other hand, in Converter B and Converter C, the second- and third-order harmonic components take up a large portion of the current waveforms. Since the switch voltage waveform contains not only the fundamental component but also the third-order component, the third-order harmonic in current waveforms has the possibility to provide the additional output power to the load. Table II shows the simulation results of the real output power ($P_{o,\rm real}$), the output power transferred by the fundamental term ($P_{o1,\rm real}$), and the output power transferred by the third-order term ($P_{o3,\rm real}$). As shown in the result in Table II, most of the output power is obtained by the

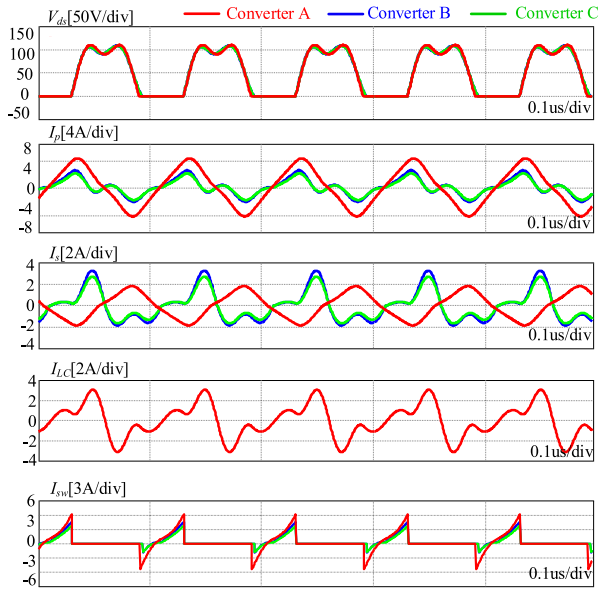

Fig. 12. Simulation results of the drain-to-source voltage, primary-side current, rectifier-side current, *L-C* branch current, and switch current.

TABLE II
SIMULATION RESULTS OF OUTPUT POWER

Parameters	Converter A	Converter B	Converter C
$P_{o,\rm real}$ [W]	10.7	14.1	10.4
$P_{o1,\rm real}$ [W]	10.5	12.0	8.83
$P_{o3,\rm real}$ [W]	0.16	2.06	1.53

TABLE III
SIMULATION RESULTS OF RMS VALUE OF CURRENTS

Parameters	Converter A	Converter B	Converter C
RMS value of I_p [A]	3.34	1.53	1.31
RMS value of I_s [A]	1.17	1.46	1.22
RMS value of I_{LC} [A]	1.63	–	–
RMS value of $I_{\rm sw}$ [A]	1.24	0.82	0.67

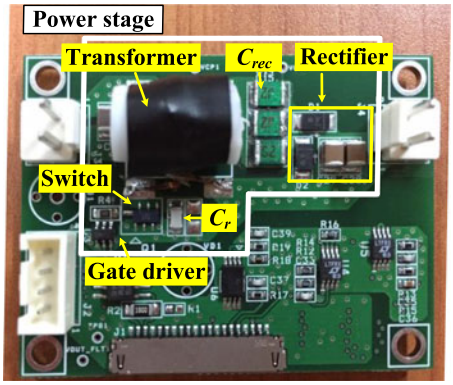

Fig. 13. Photography of prototype (55 mm × 45 mm).

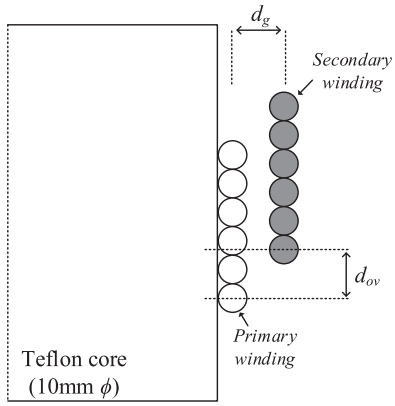

Fig. 14. Structure of the transformer (cross-sectional view).

TABLE IV
POWER STAGE COMPONENTS

Components (Parameters)	Value
$C_{\rm rec}$	433 [pF]
$C_{\rm ext}$	100 [pF]
Switch	EPC2010
D_1, D_2	DB2441700L
Transformer	Teflon rod air core (10 mm diameter) and Litz-wires (0.08 mm/20 strands) $L_m = 231[\rm nH], L_r = L_{\rm rec} = 88[\rm nH], k = 0.724$

fundamental component in Converter A. On the other hand, $P_{o3,\rm real}$ is not negligible in Converter B and Converter C due to the third-order harmonic component as expected. When Converter B is designed, it is assumed that the output power is solely obtained by the fundamental component without consideration of the third-order harmonic component in the design procedure; therefore, it results in an excess power supply to the load. In Converter C, however, the designed parameters are tuned by (10) in anticipation of the effect of the third-order harmonic component. Then, the total power delivered to the load is accurately obtained. Table III shows RMS values of I_p, I_s, I_{LC}, and $I_{\rm sw}$. As shown in the results, the RMS value of I_p and $I_{\rm sw}$ of Converter C is much less than those of Converter A. Also, the RMS value of I_s of Converter C is comparable to Converter A though the output power is same.

V. EXPERIMENTAL RESULTS

A. Experimental Setup

The 10-MHz/10-W GaN-based prototype providing 20-V dc output from 50-V dc input is implemented as a design example in order to verify the proposed concept. All resonant elements are determined by the proposed design procedure where $m_1 = 1.08$ and $m_2 = 2.8$. Here, the output power tuning factor β is not used. Then, the designed parameters are same as "Converter B" in Table I. Fig. 13 shows the photography of the prototype. Components used in the power stage of the prototype are shown in Table IV.

As a switch device, a 200-V GaN device (EPC2010) is used for the prototype since the switch device is suitable for a high-frequency converter due to high dv/dt characteristics. Due to the output junction capacitance of the switch device (C_{oss}), the value of external capacitance ($C_{\rm ext}$) which is connected to the switch in parallel is determined by ($C_r - C_{oss}$). C_{oss} is varied by the drain–to-source voltage, so $C_{\rm ext}$ is not clearly defined. In the prototype, C_{oss} is assumed as its value at the normal operating condition, and $C_{\rm ext}$ is determined by 100 pF.

In this prototype converter, a high-frequency transformer which has unity turns ratio is constructed. In order to eliminate core losses, a cylindrical Teflon rod (10 mm diameter) is utilized instead of magnetic cores. The primary and secondary windings each of which have 6 turns of Litz wire (0.08 mm/20strands) is wound around the core in order to reduce ac winding losses caused by the skin and proximity effects. The measured magnetizing and leakage inductances of the transformer are 231 and 88 nH, respectively. Also, the value of coupling coefficient is measured as 0.724 which is sufficiently close to the desired value of 0.737. With the coupling coefficient, the designed value of L_r and $L_{\rm rec}$ can be provided by the leakage inductances of the transformer as explained in Section II. It is noted that there are no additional inductors which are connected to the windings of the transformer in Fig. 13.

The structure of the transformer is illustrated in Fig. 14. In this structure, the primary and secondary self-inductances are determined by the number of turns of windings and the diameter of the core, and the coupling coefficient is determined by the air-gap distance (d_g) and the overlap distance ($d_{\rm ov}$) between windings. In the prototype, d_g is fixed so as that the coupling coefficient is solely designed by d_{ov}. Here, d_g is much smaller than the diameter of the core, so difference between the primary and secondary inductances which results from the air gap (d_g) is negligible. The design error in the transformer parameters results in the undesirable characteristics. In particular, the error in the coupling coefficient is highly related to the pole and zero locations, which subsequently affects the switch voltage waveform. A transformer which has a higher value of coupling coefficient than expected leads to failure in ZVS condition. On the other hand, a transformer with a lower coupling coefficient

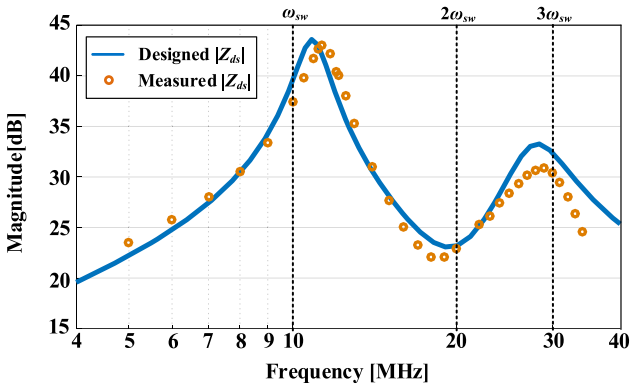

Fig. 15. Designed and measured data of drain-to-source impedance where $m_1 = 1.08$ and $m_2 = 2.8$.

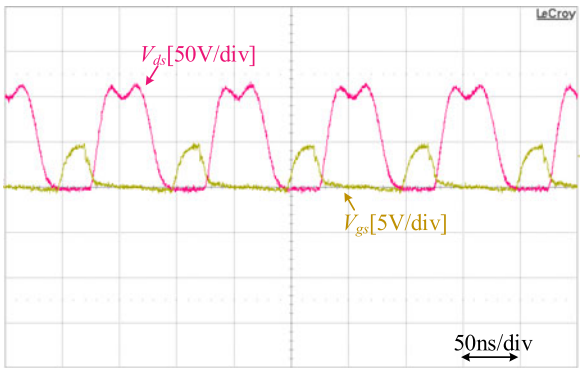

Fig. 16. Gate–to-source and drain-to-source voltage under the input voltage of 50 V.

results in a skewed voltage waveform and an unexpected high-voltage stress. Therefore, the allowable range of the coupling coefficient is typically determined from 0.71 to 0.76.

B. Experimental Verification

The drain–to-source impedance of the switch (Z_{ds}) is mainly designed in the proposed design scheme. The simulation result of Z_{ds} obtained by the designed parameters is described as a solid line in Fig. 15. As expected, the magnitude of Z_{ds} has maxima at $1.08\omega_{\rm sw}$ and $2.8\omega_{\rm sw}$, and has minimum at $2\omega_{\rm sw}$. In the same figure, the experimental data of Z_{ds} which is measured by an impedance analyzer is shown as circular markers. When the experimental data are measured, the switch device is replaced by the capacitor of which the value is equal to that of the device output capacitance (C_{oss}) at the operating drain-source voltage to emulate $Z_{\rm ds}$ under normal operating condition. From the measured data, it is observed that Z_{ds} has maxima at $1.1\omega_{\rm sw}$ and $2.9\omega_{\rm sw}$, and has minimum at $1.9\omega_{\rm sw}$. Although the pole and zero are slightly deviated due to the difference between the designed parameters and the experimental parameters, the voltage waveform on the switch device is close to the original intent. The experimental result of the switch voltage waveform is shown in Fig. 16. The switch device successfully achieves ZVS and also the peak voltage is reduced to 113 V which is 2.26 times the input voltage.

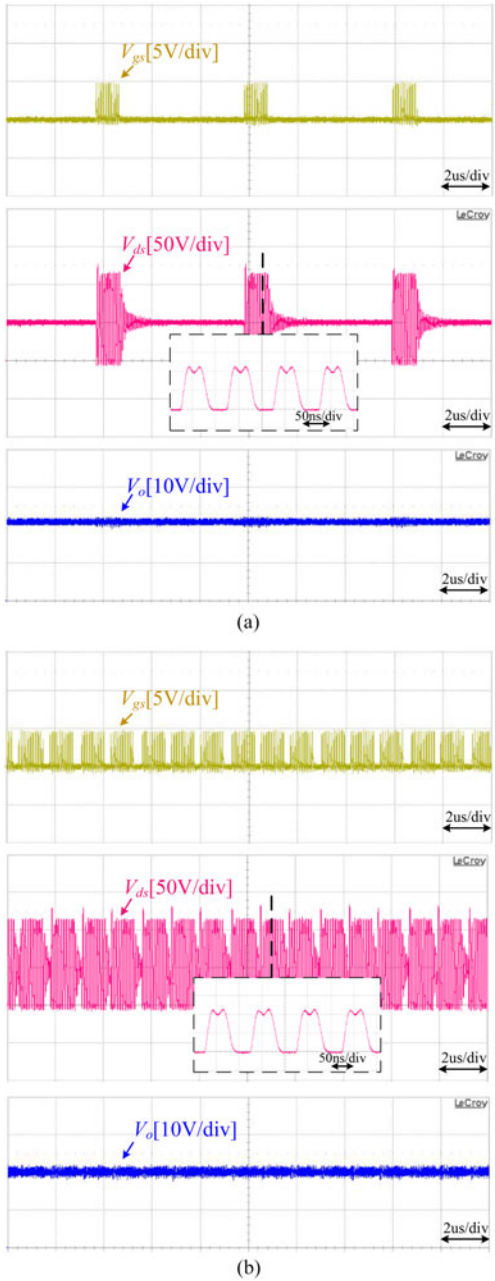

Fig. 17. Gate–to-source voltage, drain–to-source voltage, and output voltage (a) at 20% load and (b) at 100% load condition.

The output voltage of the prototype converter is regulated by an ON–OFF control scheme. Where all parameters of the converter are tuned at the specific frequency, an ON–OFF control is useful because it allows the converter to maintain the operating frequency and obtain the consistent performance regardless of the load [27], [28]. In this paper, among various ON–OFF control methods, the constant on-time ON–OFF control which is presented in [11] is used. In this ON–OFF control, ON duration of the converter is fixed and OFF duration is modulated in order to regulate the output power. Fig. 17 shows the waveforms of the switch voltage V_{ds}, gate voltage V_{gs}, and the output voltage V_o, under the different load condition (100% load and 20% load). As shown in Fig. 17, the output voltage is regulated to

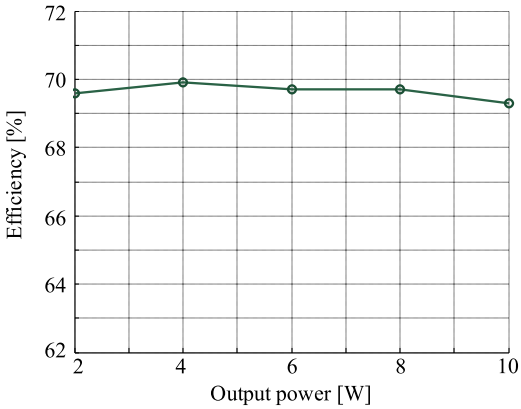

Fig. 18. Measured efficiency versus output power of the prototype.

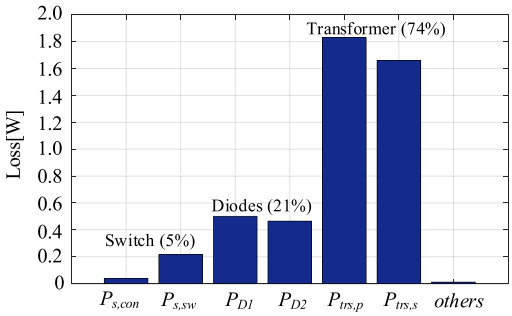

Fig. 19. Estimated loss distribution at the rated condition.

20 V by manipulating the OFF duration of the converter. Also, as expected, the voltage waveform is always maintained irrespective of the load variation since the converter operates under the same frequency and same duty cycle during ON duration of the converter.

The measured efficiency of the converter is shown in Fig. 18. At the rated condition, the efficiency is 69% and the converter maintains the efficiency under wide load range. Theoretically, an ON–OFF control scheme allows a converter to have consistent efficiency regardless of the load since there is no power consumption while the converter is OFF [28]. The estimated loss distribution of the prototype converter at the rated condition is shown in the Fig. 19. The loss breakdown shows that the switch device, rectifier diodes, and coreless transformer are the major sources of power dissipation in the converter. The losses of the switch and diode are calculated as in [30]. The switch losses are calculated as the sum of conduction loss ($P_{s,\mathrm{con}}$) and switching loss ($P_{s,\mathrm{sw}}$). Here, the switch turn-on loss is neglected since the switch achieves ZVS condition under the operating condition. The losses of the rectifier stage are the sum of conduction losses of two diodes (P_{D1} and P_{D2}). The transformer winding losses account for the largest portion of the loss in the prototype converter. Although the dc resistance of the windings is designed to be low, the winding losses are increased with the switching frequency because the effective ac resistance is much higher than the dc resistance at several megahertz owing to skin effect and proximity effect. The ac resistance of the Litz wire winding

Fig. 20. Thermal image of the prototype converter.

is calculated by using the analytic model in [31] to determine the losses in the primary and secondary windings denoted as $P_{\mathrm{trs,p}}$ and $P_{\mathrm{trs,s}}$, respectively. The estimated loss breakdown is supported by the thermal image of the prototype converter illustrated in Fig. 20. As shown, the transformer shows the highest temperature on the board, which implies that the most of the power loss is due to the transformer winding losses. Therefore, the efficiency of the converter can be improved by relieving the ac losses of transformer windings through design optimization of transformer structure [23], [32]–[34].

VI. Conclusion

A single-switch isolated dc–dc converter and the design procedure is proposed in this paper. The converter is suitable for a high-frequency switching operation especially above 10 MHz. The impedance of the drain-to-source node of the switch is designed in order to make the desired voltage waveform on the switch. By locating the pole and zero of the impedance appropriately, the switch has the reduced voltage stress and achieves ZVS condition at the same time. In order to minimize the number of passive components of the converter, the parasitic components are used as resonant elements by themselves. It leads to a compact design of the converter. This paper also shows the operation principles and the comparison to the conventional high-frequency single-switch converters.

As a design example, 10-MHz 10-W GaN-based laboratory prototype is implemented. Experimental results of the prototype are presented to validate the proposed design scheme and the performance of the converter. The prototype achieves ZVS of the switch, and it has the reduced peak voltage of 2.26 times the input voltage at the full load. In addition, the converter maintains the performance over a wide load range by exploiting the constant-on-time ON–OFF control scheme. The converter achieves the consistent efficiency of 69%.

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