Letter

Passive Balancing of Peak Currents Between Paralleled MOSFETs With Unequal Threshold Voltages

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***Abstract*—The peak switching currents of two paralleled MOSFETs turned ON/OFF by one gate driver could differ significantly owing to the mismatch in threshold voltages ($V_{\rm th}$). The passive balancing method described herein employs one inductor and one resistor per MOSFET to force the currents to track with negligible penalty in loss. Sensors, feedbacks, and knowledge of gate-related parameters (such as gate charge, polarity of $V_{\rm th}$ difference, gate impedances, etc.) are not required. The passive components are designed using an inequality involving $V_{\rm th}$, rise time, and unbalance percentage. The mismatch in peak currents is reduced from 15% to 1% between SiC MOSFETs tested at 20 A and 300 V with 19% $V_{\rm th}$ variation.**

***Index Terms*—Current balancing, paralleled MOSFETs, passive compensation, threshold voltage mismatch.**

I. Introduction

THE parallel connection of MOSFETs increases the current capability considering cost effectiveness and manufacturability [1], [2]. Paralleled MOSFETs cannot resemble a single device due to the unavoidable variation in device parameters during production. The variations in on-state resistance ($R_{\rm ds(on)}$) and threshold voltage ($V_{\rm th}$) cause imbalance during steady state and switching transients, respectively. The positive temperature coefficient of $R_{\rm ds(on)}$ can help balance the currents. Its influence is not investigated here. The negative temperature coefficient of $V_{\rm th}$ tends to worsen the mismatch of currents. Dynamic current imbalance can cause localized overcurrent and overtemperature. The reliability and lifetime of MOSFETs are adversely affected [3], [4]. Current derating is required even with screened devices [5].

Previous publications balance the transient currents by two categories of "active" compensation. One is with feedback loop and current/voltage sensors. The currents in [5] are measured by Rogowski coils fabricated on a printed circuit board. The sensed rising/falling edges and peak values of the currents are fed to a field-programmable gate array (FPGA) and a digital signal processor (DSP) to adjust the gate driving signals. A few cycles are required to balance the currents. The imbalance information in [6] is extracted from the measured voltages across the stray inductances. The feedback compensation varies the delay time of gate signals. Balanced currents are achieved after several cycles. The difference of currents is measured by a differential current transformer in [3]. The feedback scheme is able to continuously adjust the delay time based on the sensed current difference. The peak currents are balanced after more than ten cycles. The other category of active compensation is without the feedback loop. The two-level dynamic gate resistances indirectly control the delay time between gate drivers [7]. The peak currents can be balanced in one switching cycle. The asymmetry of threshold voltages needs to be known due to the loss of automatic compensation.

The objective of the letter is to automatically limit the mismatch of peak currents in one switching cycle and by one gate driver without using current/voltage sensors and feedback loop. Section II introduces the topology and principle of the passive balancing solution. One inductor and one resistor are employed per MOSFET to force the currents to track with negligible penalty in loss. The design guideline involving $\rm V_{th}$, rise time, and unbalance percentage are provided for the selection of passive components. Section III demonstrates the effectiveness of the passive balancing technique by an experiment.

II. Passive Compensation Topology and Operating Principle

The influence of power-source inductance (L_s) and drive-loop resistance connected to the source (R_k) on dynamic sharing with mismatched threshold voltage and balanced layout is shown in Fig. 1. The parasitics of package are not included in the analysis for simplicity. The theory upholds well when parasitics are considered as shown in the experimental verification (see Fig. 6), which has parasitics from device package and copper traces. The double-pulse tester (DPT) is used for the testing of switching transients. The lower side is composed of two SiC MOSFETs with mismatched $V_{\rm th}$, where $V_{\rm th1}$ and $V_{\rm th2}$ are threshold voltages of M1 and M2, respectively. The upper side is a SiC Schottky barrier diode (SBD). The inductive

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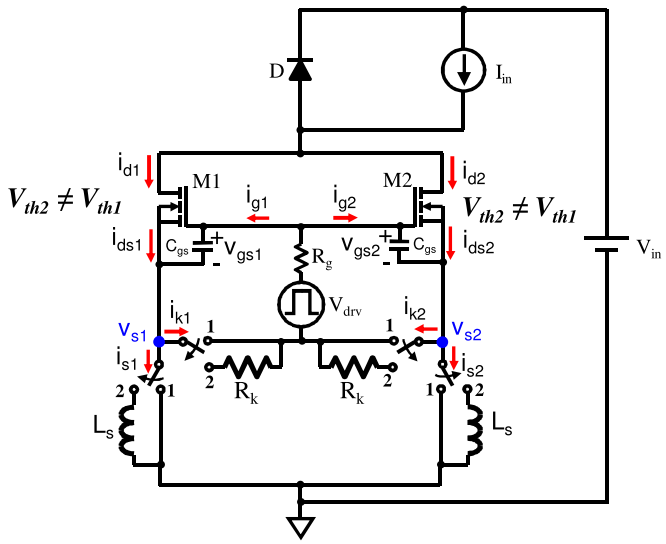

Fig. 1. Influence of power-source inductance (L_s) and drive-loop resistance connected to the source (R_k) on dynamic sharing, where lower side is paralleled SiC MOSFETs with mismatched $V_{\rm th}$ and upper side is SiC SBD.

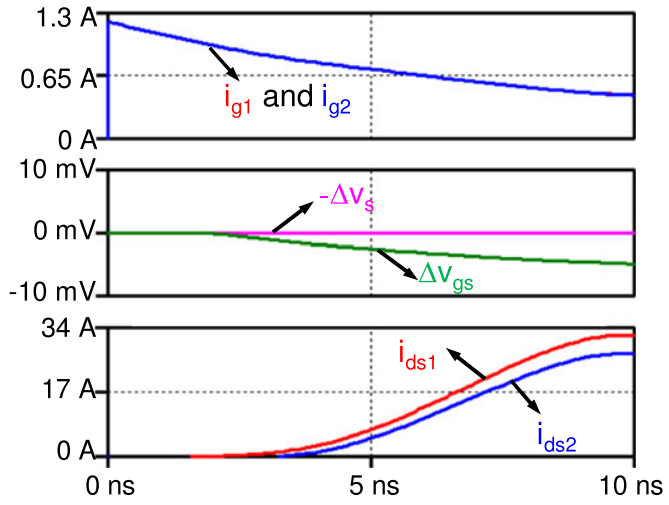

Fig. 2. Simulation results of Fig. 1 without R_k and $L_s = 15$ nH. MOSFETs (C2M0160120D) and SBD (CPW51200Z050B) were simulated with SPICE model from Cree. Threshold voltages were $V_{\rm th1} = 2.48$ V and $V_{\rm th2} = 3.08$ V. The gate–source voltage was measured across $C_{\rm gs}$, excluding the voltage across the 6.5 Ω internal gate resistance.

load is modeled by a constant current source for simplicity. The scheme with two switches for every branch represents different structures (with symmetry maintained); the influences of L_s and R_k on dynamic sharing can be tested.

The variation in threshold voltage leads to the imbalance in channel current during switching transients. The channel current $i_{\rm ds}$ during saturation region is modeled by

$$i_{{\rm ds}_j} = g_{\rm fs}\left(v_{{\rm gs}_j} - V_{{\rm th}_j}\right)^2,\ v_{{\rm gs}_j} < V_{{\rm th}_j}\ ,j = 1,2 \qquad (1)$$

where $V_{\rm th1}$ and $V_{\rm th2}$ are the threshold voltages of M1 and M2, respectively. The large-signal transconductance $g_{\rm fs}$ is assumed to match for both devices [8].

The difference of drain-source currents can be obtained by taking the differentiation of (1)

$$\Delta i_{\rm ds} = 2g_{\rm fs}\left(v_{\rm gs} - V_{\rm th}\right)\left(\Delta v_{\rm gs} - \Delta V_{\rm th}\right),\ \ v_{\rm gs} < V_{\rm th} \qquad (2)$$

where

$$\Delta x = x_1 - x_2,\quad x = 0.5\left(x_1 + x_2\right). \qquad (3)$$

If there is no R_k and/or L_s, i.e., one of the two switches is connected to position 1, $\Delta v_{\rm gs}$ approximately equals zero; the MOSFET with smaller $V_{\rm th}$ carries larger current according to (2), as illustrated in Fig. 2.

Equation (2) shows that the difference of drain-source currents is zero when

$$\Delta v_{\rm gs} = \Delta V_{\rm th}. \qquad (4)$$

Voltage $\Delta v_{\rm gs}$ can be produced by the difference between gate voltages (v_{g1} and v_{g2}) or between source voltages (v_{s1} and v_{s2}). Currents i_{g1} and i_{g2} are normally matched with unequal drain-source currents. The passive components on gate traces are not effective in current balancing. Voltage $\Delta v_{\rm gs}$ approximately equals $-\Delta v_s$ as shown in Fig. 2 (where MOSFETs have 6.5 Ω internal gate resistances). This can also be demonstrated by simulation with gate inductance. The following analysis neglects the gate inductance and internal gate resistance to simplify the analysis. Voltage potentials $v_{\rm s1}$ and $v_{\rm s2}$ are different with inserted L_s and R_k when $i_{\rm ds1}$ and $i_{\rm ds2}$ do not match. The difference of gate–source voltages can be obtained by the loop containing $C_{\rm gs}$s, L_ss and the loop containing $C_{\rm gs}$s, R_ks

$$\Delta v_{\rm gs} = -L_s\frac{d\Delta i_s}{dt} \qquad (5)$$

$$\Delta v_{\rm gs} = -R_{\rm ks}\Delta i_k \qquad (6)$$

where Δi_s is the current difference of power-source inductances; Δi_k is the current difference of drive-loop resistances connected to the source. Similar results can be obtained if resistance R_k is replaced by inductance L_k. The analysis is not elaborated here for conciseness.

The currents through $C_{\rm gs}$ and $C_{\rm ds}$ are approximated to be zero during $i_{\rm ds}$ rising interval to simplify the analysis [9]. Taking the difference of KCLs at node v_{s1} and v_{s2} in Fig. 1

$$\Delta i_s + \Delta i_k \approx \Delta i_{\rm ds} = 2g_{\rm fs}\left(v_{\rm gs} - V_{\rm th}\right)\left(\Delta v_{\rm gs} - \Delta V_{\rm th}\right). \qquad (7)$$

Substitution of $d\Delta i_s/dt$ from (5) and $d\Delta i_k/dt$ from (6) into the derivative of (7) yields

$$\frac{d\Delta v_{\rm gs}(t)}{dt} = \frac{2g_{\rm fs}\frac{dv_{\rm gs}(t)}{dt}L_s\Delta V_{\rm th} - \left(2g_{\rm fs}\frac{dv_{\rm gs}(t)}{dt}L_s + 1\right)\Delta v_{\rm gs}(t)}{2g_{\rm fs}\left(v_{\rm gs}(t) - V_{\rm th}\right)L_s + \frac{L_s}{R_k}}. \qquad (8)$$

The initial value of $\Delta v_{\rm gs}$ in (8) is zero as the gate driver charges the gate–source capacitances of M1 and M2 equally before the channels of MOSFETs are turned ON. The slew rate of $\Delta v_{\rm gs}$ is larger than zero when $\Delta V_{\rm th} > 0$ and smaller than zero when $\Delta V_{\rm th} < 0$ (as shown in Fig. 3). The MOSFET with larger $V_{\rm th}$ has higher gate current. The steady state of $\Delta v_{\rm gs}(t)$ is achieved

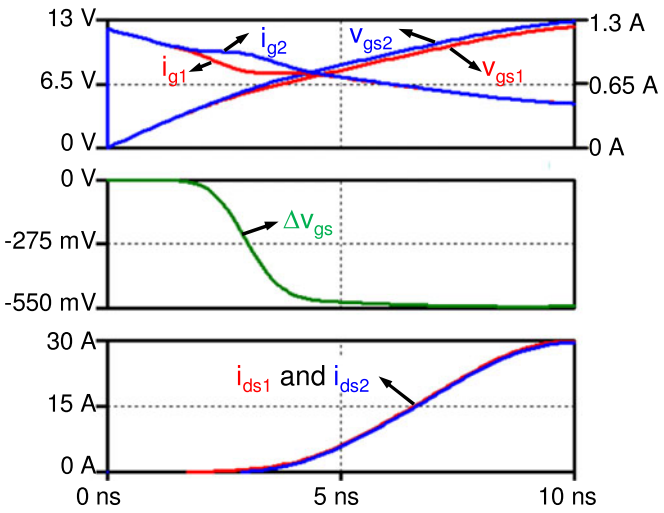

Fig. 3. Simulation results of Fig. 1 with $L_s = 15$ nH, $R_k = 6\,\Omega$, $V_{\rm th1} = 2.48$ V, and $V_{\rm th2} = 3.08$ V.

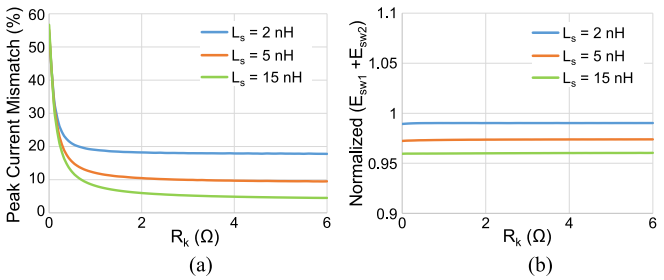

Fig. 4. Influence of R_k and L_s on (a) peak current mismatch and (b) normalized total switching loss, based on simulation of Fig. 1 with $R_g + 0.5\,R_k = 5\,\Omega, V_{\rm in} = 600$ V, $I_{\rm in} = 20$ A, $V_{\rm th1} = 2.48$ V, and $V_{\rm th2} = 3.08$ V.

when the numerator of (8) reaches zero and is expressed as

$$\Delta v_{\rm gs\_ss} = \frac{1}{1 + \frac{1}{2g_{\rm fs}L_s\, dv_{\rm gs}/dt}} \Delta V_{\rm th} \tag{9}$$

where subscript "ss" denotes steady state. The voltage $\Delta v_{\rm gs\_ss}$ can be approximated by $\Delta V_{\rm th}$ when $2g_{\rm fs}L_s dv_{\rm gs}/dt \gg 1$. Dynamic balancing with unknown asymmetric $V_{\rm th}$ is obtained by utilizing a single gate driver. One example is shown in Fig. 3, where parameter $g_{\rm fs} = 0.44$ A/V^2, $dv_{\rm gs}/dt \approx 1$ V/ns, $L_s = 15$ nH, $\Delta V_{\rm th} = -0.6$ V, and $2g_{\rm fs}L_s dv_{\rm gs}/dt = 13.2$. The steady state of $\Delta v_{\rm gs}$ calculated by (9) is –558 mV.

The inductance $L_{\rm s}$ influences the steady state of $\Delta v_{\rm gs}(t)$ according to (9), whereas the resistance R_k affects the slew rate of $\Delta v_{\rm gs}$ according to (8). This resistance needs to be sufficiently large to allow $\Delta v_{\rm gs}(t)$ to reach a steady state before $i_{\rm ds}$ peaks. The simulation results with varying R_k and L_s are shown in Fig. 4, where $E_{\rm sw1}$ and $E_{\rm sw2}$ are the switching losses (including turn-on loss and turn-off loss) of M1 and M2, respectively. Losses of bare dice are set as the normalizing factor. The mismatch of peak currents is defined as

$$\text{current mismatch} = \frac{i_{\rm pk1} - i_{\rm pk2}}{I_{\rm ss}} \times 100\% \tag{10}$$

where $i_{\rm pk1}$ and $i_{\rm pk2}$ are the peak currents of M1 and M2, respectively, and $I_{\rm ss}$ is the steady-state current of every MOSFET, namely half of $I_{\rm in}$.

The current mismatch decreases with increasing L_s and R_k, whereas the simulated total switching loss does not change significantly as long as $(R_g + 0.5R_k)$ is kept constant according to Fig. 4.

The effectiveness of R_k and L_s on current balancing has been analyzed. The design guideline for the selection of inductance and resistance is derived as follows. According to (9), $|\Delta v_{\rm gs}| \le |\Delta V_{\rm th}|$. The maximum $|i_{\rm ds1(pk)} - i_{\rm ds2(pk)}|$ is obtained from (5)–(7)

$$\max\left|i_{\rm ds1(pk)} - i_{\rm ds2(pk)}\right| = \frac{|\Delta V_{\rm th}|}{R_k} + \frac{|\Delta V_{\rm th}|}{L_s} t_r \tag{11}$$

where t_r is the time for current rising from 0 to the peak.

The above equation consists of two terms. The first term shows the effect of R_k and the second term indicates the influence of L_s. To bound $|i_{\rm ds1(pk)} - i_{\rm ds2(pk)}|$ to $\varepsilon I_{\rm in}/2$,

$$\frac{|\Delta V_{\rm th}|}{R_k} + \frac{|\Delta V_{\rm th}|}{L_s} t_r < \varepsilon \frac{I_{\rm in}}{2} \tag{12}$$

where ϵ is preferably a small number (e.g., 5%) specified by the designer.

Equation (12) provides one design relationship between R_k and L_s. Voltage stress [9], [10] or some other switching characteristics could be another one.

III. Experimental Verification

The measurement method of drain-source current needs to be determined before testing. The channel current of MOSFET cannot be measured directly. It can be approximated by source current i_s or drain current i_d, as shown in Fig. 1. The source current is usually measured because it is ground-referenced. Simple current sensor without isolation capability can be used. The sensing resistor [11], [12] and co-axial shunt [13], [14] are popular choices for accuracy. However, the current imbalance may not appear in the measured i_{s1} and i_{s2} waveforms. The difference of the drain-source currents is the sum of Δi_s and Δi_k. Most of the differential current flows though drive loop with minor R_k. Matched source currents occur when R_k equals 0 Ω and two L_ss are directly paralleled. Instead of source currents, drain currents were measured. The difference of channel currents can be accurately detected considering negligible displacement currents of $C_{\rm ds}$ and $C_{\rm gd}$. The split core current probe (TCP0030A) with enough dynamic range and bandwidth was used in the experiment.

The hardware of DPT for experimental verification of the balancing effect of L_s and R_k is shown in Fig. 5. Two discrete SiC MOSFETs (C2M0160120D) with different threshold voltages ($V_{\rm th1} = 2.34$ V, $V_{\rm th2} = 2.78$ V from measurements) were paralleled in a symmetrical layout. The upper side was a SiC Schottky diode (C4D20120A) from Cree. The gate driver board (CRD-001) was connected through the connector on the power board. Small L_k (1.89 nH based on Q3D simulation) from the printed circuit board (PCB) layout ensured limited initial balancing effect.

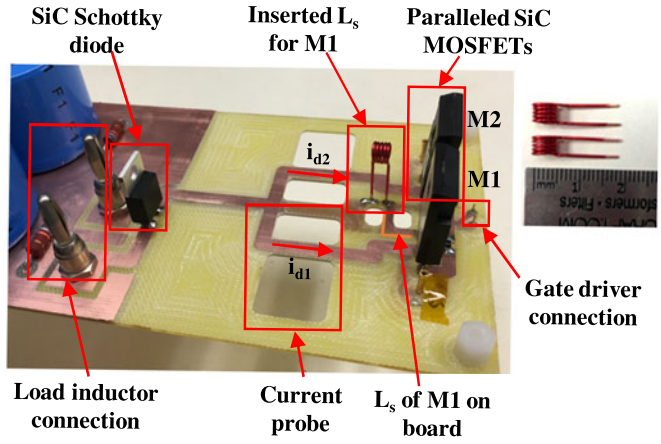

Fig. 5. Photo of hardware for demonstration of dynamic balancing solution shown in Fig. 1. The power-source inductances are tuned by the air-cored inductors.

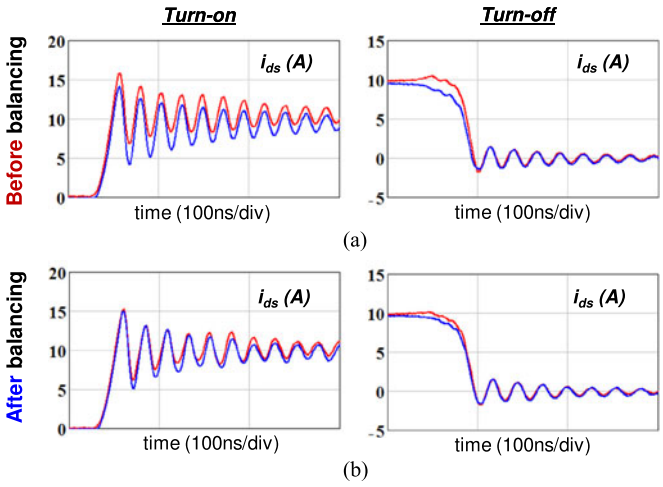

Fig. 6. Experimental results tested at $V_{\rm in} = 300$ V, $I_{\rm in} = 20$ A, $R_g + 0.5\ R_k = 20\,\Omega$, $V_{\rm th1} = 2.34$ V, $V_{\rm th2} = 2.78$ V for verification of current balancing solution in Fig. 1. Drain-source currents for turn-on and turn-off transients (a) without L_s and R_k design, and (b) with L_s and R_k design.

The impedance of drive-loop connected to the source was dominated by R_k. The PCB layout had relatively large power-loop inductance (around 120 nH from copper traces and ESLs of dc link capacitors) and drain inductance (around 26 nH) due to the accommodation of current probes. The ringing during turn-on transient was severe [9], [15]. Those parasitics were not purposely reduced in order to verify the performance of design guideline (12) under an awful layout. The same board was utilized for fair comparison of baseline and passive balancing solution. The only difference was the designed parts: L_s and R_k. Openings on the corresponding traces were prepared for insertion of extra inductors or resistors. For baseline design, $0\,\Omega$ resistors were soldered to short the openings. For verification of the passive balancing effect, small air-cored inductors and SMD resistors with designed values were inserted. Two air-cored inductors with the same inductance increased the power-source inductance, as shown in Fig. 5. One was placed on the top of the board, the other was on the bottom and blocked by the board. Drive-loop resistances connected to the source were varied by surface mount resistors, which were also on the bottom of the board.

TABLE I
COMPARISON OF L_s AND R_k FOR DIFFERENT DESIGNS

	Baseline in Fig. 6(a)	Solution in Fig. 6(b)
L_s (nH)	11.5	47.2
R_k (Ω)	0	5.6

TABLE II
COMPARISON BETWEEN BASELINE AND PASSIVE BALANCING SOLUTIONS WITH 10 A STEADY-STATE CURRENT

	Peak current diff. (A)	Total switching loss (μJ)
Baseline in Fig. 6(a)	1.5	174.22
Solution in Fig. 6(b)	0.1	174.29

The DPT tests two short pulses. The switching transients are captured at the first falling and rising edges at room temperature (with negligible change in device junction temperatures). The experimental results of the baseline design are shown in Fig. 6(a). The corresponding on-board L_s (obtained by Q3D simulation) and $R_{\rm k}$ are illustrated in Table I. The current imbalance is obvious due to the slight balancing effect. Then L_s and R_k are designed to achieve better sharing. The specific values are listed in Table I. According to Fig. 6(a), current rise time t_r is 35 ns. The difference of peak currents can be bounded within 5% of $0.5I_{\rm in}$ (namely 0.5 A) based on the design guideline (12)

$$\begin{aligned} i_{\rm ds1(pk)} - i_{\rm ds2(pk)} &\le \frac{V_{\rm th2} - V_{\rm th1}}{R_k} + \frac{V_{\rm th2} - V_{\rm th1}}{L_s} t_r \\ &= \frac{0.44\ \text{V}}{5.6\ \Omega} + \frac{0.44\ \text{V}}{47\ \text{nH}} 35\ \text{ns} \\ &= 0.406\ \text{A} < 0.5\ \text{A}. \end{aligned} \tag{13}$$

Fig. 6(b) shows the experimental results with designed L_s and R_k. The desired current sharing is obtained within one switching cycle by utilizing a single gate driver. Better sharing is also achieved for the turn-off transient compared to the baseline shown in Fig. 6(a). Other combinations of R_k and L_s that satisfy (12) are also effective in current balancing.

Table II summarizes the comparison between baseline and passive balancing solution. The measured difference of peak currents is reduced from 1.5 to 0.1 A (below 5% of steady-state current) without increasing total switching loss. The design guideline (12) is successfully verified. The ringing is not worsen by the increased L_s under the testing condition ($V_{\rm in} = 300$ V, $I_{\rm in} = 20$ A, and $R_g + 0.5R_k = 20\ \Omega$). The prototype in Fig. 5 has relatively large parasitics due to the accommodation of current probes. The current balancing solution in Fig. 1 does not require any sensor in practical applications. Parasitic inductance along the current commutation loop can be maintained small after the elimination of current probe and/or addition of decoupling capacitor. The switching speed can be increased

without introducing severe ringing, and less L_s is expected as shown in Fig. 4.

IV. Conclusion

A passive solution is investigated to balance the peak currents between paralleled MOSFETs caused by unequal threshold voltages. The current/voltage sensors, feedback loop design, and multiple gate drivers are avoided. The difference of peak currents can be limited to a predetermined percentage by one resistance and one inductance per switch without sacrificing the total switching loss. The aforementioned benefits were demonstrated by two paralleled SiC MOSFETs (C2M0160120D) tested at $V_{\rm in} = 300$ V, $I_{\rm in} = 20$ A, $R_g + 0.5R_k = 20\,\Omega$, $V_{\rm th1} = 2.34$ V, and $V_{\rm th2} = 2.78$ V. The difference of peak currents can be reduced from 1.5 to 0.1 A (15–1%) by $R_k = 5.6\,\Omega$ and $L_s = 47.2$ nH in every switching transient. The values of R_k and L_s were determined by the design guideline in (12) involving threshold voltage mismatch, current rise time, and unbalance percentage. The junction temperatures of paralleled devices will vary under continuous testing. The $\Delta V_{\rm th}$ may be different from the value under the same junction temperatures due to the negative temperature coefficient. The worst $\Delta V_{\rm th}$ can be approximated by referring to the temperature coefficient of $V_{\rm th}$ provided in the datasheet. The R_k and L_s can be calculated by (12) with the updated $\Delta V_{\rm th}$. This letter did not cover the case of different junction temperatures. Further investigation could be done in the future work. This method can be extended to the case of more than two MOSFETs because it does not need to consider the asymmetry of $V_{\rm th}$ and uses one gate driver. The current rise time in the experimental demonstration was determined by the baseline tested at one operating condition $V_{\rm in}$, $I_{\rm in}$, and R_g. The design covers wide range of $V_{\rm in}$, $I_{\rm in}$, and R_g will be analyzed in the future. Methods to reduce R_k and L_s, e.g., magnetic coupling, will also be investigated.

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