Modified Synchronous Pulsewidth Modulation of Current-Fed Five-Level Inverter for Solar Integration

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***Abstract*—Large-scale photovoltaic (LSPV) energy conversion systems have been installed at many places across the world. The essential component of the LSPV system is the dc–ac conversion stage. The usage of multilevel converters is one of the recent advances in the dc–ac conversion stage of the LSPV system to enable transformer-less inversion. Current-fed multilevel inverter has been chosen in this paper as it provides high power inversion with inherent voltage boosting, and thus, avoids the usage of transformer. High power conversion necessitates low device switching frequency operation in order to satisfy thermal constraint of semiconductor devices and also to improve efficiency. However, low device switching frequency operation leads to higher harmonic distortion of inverter output currents. Synchronous optimal pulsewidth modulation (SOP) technique is an emerging low device switching frequency modulation technique that has been successfully implemented for voltage-source multilevel inverters. However, the state-of-the-art SOP technique cannot be directly applied to modulate current-source multilevel inverter topologies due to additional constraints on the switching commutations. Therefore, the purpose of our study was to propose a modified SOP technique to achieve: low device switching frequency and minimal harmonic distortion of inverter output currents. The topology of current-fed five-level inverter was used for demonstrating the performance of proposed technique. A generalized conversion method was introduced in the modified SOP technique for including switching constraints of the current-fed inverter. In addition, a state-sequencing machine was developed by utilizing redundant inverter states to produce equal switching commutation among all semiconductor devices at minimal switching frequency of 350 Hz. The experimental results obtained from the five-level current-source inverter of 1.2 kW demonstrated the effectiveness of the proposed SOP technique.**

***Index Terms*—Current-fed multilevel inverter, low-frequency modulation, solar power integration, synchronous optimal pulsewidth modulation (SOP).**

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I. Introduction

SOLAR energy generation using large-scale photovoltaic (LSPV) power plants has seen exponential growth in the recent decades due to reduction in the cost of photovoltaic (PV) cells. The LSPV system handles power levels ranging from a few hundred kilowatts to several hundred megawatt. At present, several LSPV power plants have been installed around the world by growing group of companies [1]. Among them, Topaz solar farm is the largest LSPV system, which produces 550 MW of electric power [2]. These LSPV systems utilize millions of PV modules for the solar energy generation and use power conversion stage for grid integration. Centralized and multistring configurations are two well-established configurations for interfacing power to the grid. Among these, the multistring configuration is more efficient in extracting maximum power even under partial shading and mismatching in the PV modules [3].

The multistring configuration is shown in Fig. 1. It consists of strings with PV-modules, dc–dc converter with maximum power point tracking (MPPT) control for each string and a central dc–ac inverter for grid integration [4]. The dc–dc converter handles fraction of total power, whereas the central inverter has to handle total power, which is in the order of megawatt. For such high power, the classical two-level (2L) voltage or current-source inverter (CSI) topologies will not be able to produce better quality due to the limitation of power semiconductor devices. This can be overcome by replacing 2L topology with multilevel converter (MLC) topology. It provides better power quality, maximum allowed switching frequency, higher voltage operation, reduction in filter size, and so on [5]. Multilevel converters are of two basic types: voltage-source MLC and current-source MLC. Current-source topologies are the suitable topology for PV applications due to inherent boosting nature, direct output current control capability, longer lifetime of storage elements, overcurrent/short-circuit protection, transformer-less operation and also due to current-source nature of PV panel output [6]–[8].

The modulation and control techniques of the multilevel converter play a major role in achieving better power quality, active and reactive power control, and maximum dc bus utilization for the LSPV to grid integration. The modulation techniques utilized for large-scale PV integration can be broadly classified into two categories such as vector-based modulation techniques and carrier-based modulation techniques [6], [9]–[12]. However, these techniques need higher switching frequency for achieving better quality of output current. Higher switching frequency leads to higher switching losses, and thereby, it limits the con-

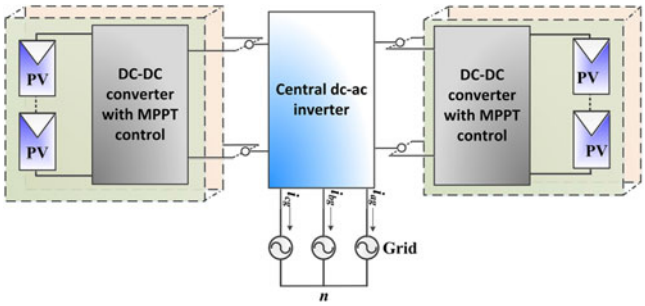

Fig. 1. Multistring configuration.

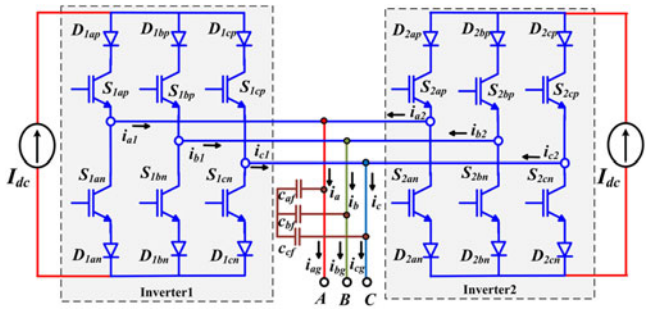

Fig. 2. 5L CSI topology.

verter power rating to few megawatt. In order to integrate large-scale solar power, the limited power rating leads to usage of several hundreds of inverters for PV integrations [3]. In other words enabling low-device switching frequency operation on multilevel inverters used in LSPV increases the inverter power handling capacity. Hence, by doing so, the total number of inverters required to handle the overall LSPV power can be reduced. In addition, energy efficiency can be significantly improved by reducing the device switching frequencies, which brings down the dominating switching losses. Then, it is possible to operate multilevel inverter at lower frequency (<1 kHz), without any violation of junction temperature limits of power semiconductor devices. However, low device switching frequency operation increases harmonic distortion of output currents. Therefore, the challenge is to minimize the harmonic distortion of output current at low device switching frequency operation. Classical modulation techniques such as sinusoidal pulsewidth modulation (SPWM) and space vector modulation (SVM) techniques require higher device switching frequency to achieve better quality of output current waveforms [13]. Some of the notable low device switching frequency modulation technique includes selective harmonic elimination (SHE) technique, staircase modulation technique, synchronous optimal pulsewidth modulation technique (SOP) and model predictive control (MPC) technique. Among them, SOP and MPC techniques have better steady state as well as dynamic performance [14].

The SOP technique conducts offline optimization to produce global optimal results for desired device switching frequency. Since SOP is an offline technique, global optimal angles can be achieved for multilevel operation that produces the least possible total harmonic distortion (THD). Since SOP is based on steady-state analysis, it requires a closed-loop controller such as stator flux trajectory tracking control or MPC technique to achieve better dynamic performance [14]. In case of MPC technique, the optimal angels are obtained through online computation. Hence, using MPC, the optimal values may not be global optimal that results in compromising distortion slightly at low device frequency and at frequencies above 200-Hz MPC produce optimal results almost similar to that of offline optimal modulation techniques [15]. The issue with MPC is that the computation burden increases for higher level inverter operation [16]. SOP is an emerging low device switching frequency modulation technique that has been successfully implemented in commercial medium-voltage (MV) drives [17]. It is based on an offline optimization technique to compute switching patterns that minimize harmonic distortion of inverter output currents. The SOP technique has only been implemented to voltage-fed (buck) MLC topologies [18]–[20], so far. The state-of-the-art SOP technique cannot be directly applied to CSI topology due to inverter operational constraints.

From the literature study, it has been found that the operational constraints of the CSI are implemented using trilogic conversion [21], [22]. However, the trilogic conversion is applicable only to the three-level (3L) CSI. In [23] and [24], five-level CSIs are modulated by space vector modulation technique, wherein the vectors are defined such that they are included with operational constraints of the CSI. However, this is a vector-based modulation technique, whereas SOP technique is a reference-based modulation. Therefore, a modified SOP technique should be proposed to handle the operational constraints of the CSI topology.

The contribution of this paper are as follows [25]: 1) analysis and implementation of modified SOP technique to handle constraints of the CSI topology by utilizing a special conversion method; and 2) low THD of the output current within grid integration standards, while limiting the device switching frequency to 350 Hz.

The contents of this paper are organized as follows: circuit topology and operation of the five-level (5L) CSI is discussed in Section II; modulation and control of the 5L CSI with modified SOP technique for current-source operation is proposed in Section III; experimental results are presented in Section IV to validate the proposed technique.

II. Paralleled 5L CSI

The topology of the paralleled 5L CSI is shown in Fig. 2. It consists of two 3L CSI supplied with independent dc current sources of magnitude $I_{\rm dc}$. Each 3L inverter has three phase legs and each leg has one top, $S_{\rm qxp}$ and one bottom $S_{\rm qxn}$ semiconductor device with series power diodes $D_{\rm qxp}$, and $D_{\rm qxn}$, respectively ($x \in a, b, c$, and q represents inverter 1 or 2). The series diode provides a reverse voltage blocking capability and unidirectional input-current flow for the inverter. The outputs of two 3L inverters are connected in parallel to produce output current i_x with five levels $2I_{\rm dc}$, $I_{\rm dc}$, 0, $-I_{\rm dc}$, and $-2I_{\rm dc}$. At the output side, the CSI requires three phase capacitors C_{af}, C_{bf}, and C_{cf}, to assist in the commutation of power semiconductor devices. In addition, capacitor also acts as a harmonic filter, improving the grid current waveforms.

TABLE I
SWITCHING STATES AND OUTPUT CURRENT OF 3L CSI

State	I_a	I_b	I_c	S_{ap}	S_{an}	S_{bp}	S_{bn}	S_{cp}	S_{cn}
1	0	I_{dc}	$-I_{dc}$	0	0	1	0	0	1
2	I_{dc}	$-I_{dc}$	0	1	0	0	1	0	0
3	I_{dc}	0	$-I_{dc}$	1	0	0	0	0	1
4	$-I_{dc}$	0	I_{dc}	0	1	0	0	1	0
5	$-I_{dc}$	I_{dc}	0	0	1	1	0	0	0
6	0	$-I_{dc}$	I_{dc}	0	0	0	1	1	0
7	0	0	0	1	1	0	0	0	0
8	0	0	0	0	0	1	1	0	0
9	0	0	0	0	0	0	0	1	1

TABLE II
SWITCHING STATES AND OUTPUT CURRENT OF 5L CSI

State	I_a	I_b	I_c	$(3L_1$ state, $3L_2$ state$)_{\text{option}}$
1	0	0	0	$(7,7)_1$ or $(8,8)_2$ or $(9,9)_3$
2	0	I_{dc}	$-I_{dc}$	$(7,1)_1$ or $(1,7)_2$
3	0	$2I_{dc}$	$-2I_{dc}$	$(1,1)_1$
4	0	$-I_{dc}$	I_{dc}	$(7,6)_1$ or $(6,7)_2$
5	0	$-2I_{dc}$	$2I_{dc}$	$(6,6)_1$
6	I_{dc}	0	$-I_{dc}$	$(8,3)_1$ or $(3,8)_2$
7	I_{dc}	I_{dc}	$-2I_{dc}$	$(3,1)_1$ or $(1,3)_2$
8	I_{dc}	$-I_{dc}$	0	$(9,2)_1$ or $(2,9)_2$
9	I_{dc}	$-2I_{dc}$	I_{dc}	$(2,6)_1$ or $(6,2)_2$
10	$2I_{dc}$	0	$-2I_{dc}$	$(3,3)_1$
11	$2I_{dc}$	$-I_{dc}$	$-I_{dc}$	$(2,3)_1$ or $(3,2)_2$
12	$2I_{dc}$	$-2I_{dc}$	0	$(2,2)_1$
13	$-I_{dc}$	0	I_{dc}	$(8,4)_1$ or $(4,8)_2$
14	$-I_{dc}$	I_{dc}	0	$(9,5)_1$ or $(5,9)_2$
15	$-I_{dc}$	$2I_{dc}$	$-I_{dc}$	$(1,5)_1$ or $(5,1)_2$
16	$-I_{dc}$	$-I_{dc}$	$2I_{dc}$	$(4,6)_1$ or $(6,4)_2$
17	$-2I_{dc}$	0	$2I_{dc}$	$(4,4)_1$
18	$-2I_{dc}$	I_{dc}	I_{dc}	$(4,5)_1$ or $(5,4)_2$
19	$-2I_{dc}$	$2I_{dc}$	0	$(5,5)_1$

$3L_1 \rightarrow$ inverter-1 $3L_2 \rightarrow$ inverter-2

A. Operational Constraint

The switching states of the CSI are limited by the following operational constraints [26]:

1) *Continuous path for input dc current* i_{dc}*:* Since the inverter is supplied with constant current source, it is required to maintain continuous path for the input current. Discontinuity in the current path causes high voltage across the devices.
2) *Inverter output current* i_x *should be defined:* In case of voltage-source inverters, the output currents are decided by the load, whereas in CSI, the magnitudes of output currents should be defined by the switching operation of the CSI. For instance, if the switches S_{1ap}, S_{1bp}, and S_{1cn} are turned ON, then the magnitude of i_{a1} and i_{b1} is dependent on the load. Hence, to avoid this dependence, at any time interval of inverter operation only two switches are turned ON, i.e., one of the top devices S_{xp} and one of the bottom devices S_{xn}.

By applying these constraints for the 5L CSI, the switching states and output currents of the 3L and 5L CSI can be obtained as shown in Tables I and II, respectively. There are 19 possible 5L output combination and each combination is achieved by one or more switching combination of two 3L CSIs. These redundancies can be utilized for achieving equal commutation of semiconductor devices. The method of utilizing redundant states is explained in detail in Section III-B5. It should also be observed from the Table II that the summation of three phase current levels is zero for each switching state.

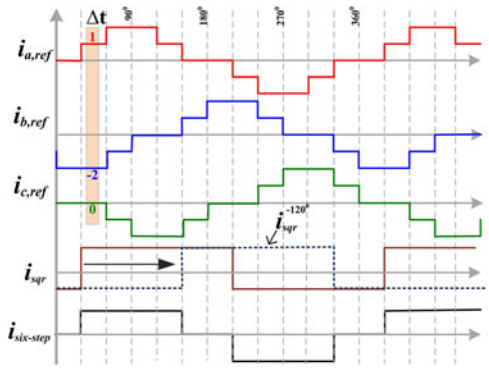

Fig. 3. Reference waveforms considered for analyzing conversion method.

III. MODULATION AND CONTROL

The modulation and control of the 5L CSI involves identifying optimal reference signal using offline computation and assigns the optimal pulses for each semiconductor device. The SOP technique is utilized to obtain optimal quasi-sine reference waveform and a conversion method is utilized to incorporate constraints on the reference waveform as mentioned in Section II-A. The conversion method and SOP optimization technique are given next.

A. Conversion Method

The objective of the conversion method is to derive realizable waveform from any quasi-sine reference wave in order to include the operational constraints mentioned in Section II-A, while maintaining the objective of the reference waveform. It should be noticed from Table II, that at any instant of time, the sum of three phase output current levels should be zero. For example, the inverter needs to be modulated to produce 5L three-phase output current waveforms, $i_{a,\text{ref}}$, $i_{b,\text{ref}}$, and $i_{c,\text{ref}}$, as shown in Fig. 3. The equation that governs the constraint is given by

$$i_{a,\text{ref}} + i_{b,\text{ref}} + i_{c,\text{ref}} = 0 \tag{1}$$

where, $i_{a,\text{ref}}$, $i_{b,\text{ref}}$, and $i_{c,\text{ref}}$ are reference currents for three phases with 120° rotation. Consider a small time interval Δt as shown in Fig. 3, the sum of these three waveforms during this interval gives a nonzero value -1. Therefore, these references cannot be utilized for operating the 5L CSI.

Fourier-series analysis demonstrates that the sum of three waveforms with 120° phase shift will have only three multiples harmonic components $(3, 6, 9, 12, ..)$. Hence, in order to satisfy (1), the current reference should not contain three multiples harmonic. Elimination of three multiples harmonic component on any quasi reference waveform can be achieved by delaying it to 120° and subtracting the delayed signal from actual wave-

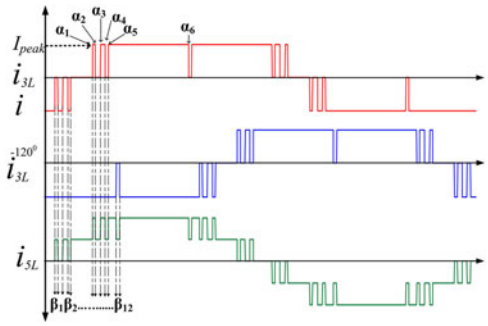

Fig. 4. 3L and 5L waveforms with optimal switching angles.

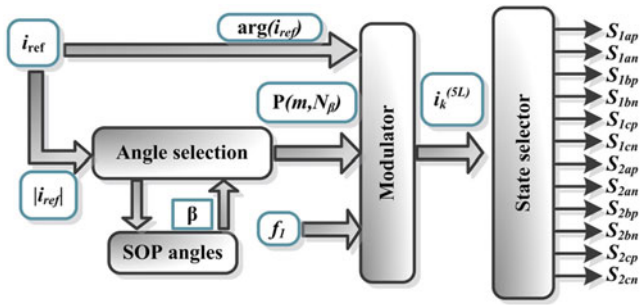

Fig. 5. Modified SOP control Flow for 5L CSI.

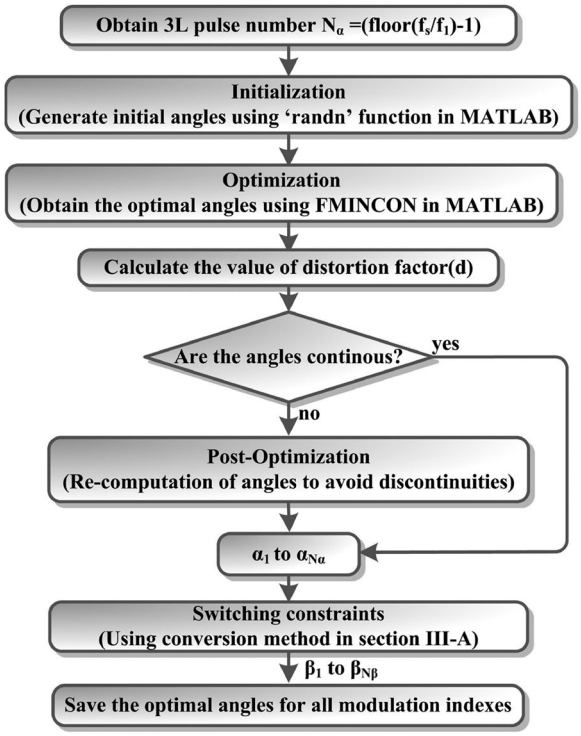

Fig. 6. Modified SOP optimization method.

form. For example, consider square wave $i_{\rm sqr}$ as reference, it is then phase shifted by 120° as shown in Fig. 3, and subtracted with actual waveform to obtain reference signal, $i_{\rm six-step}$. The resultant waveform is a 3L waveform without three multiples harmonic content and it can be directly utilized as a reference signal for the 3L CSI to produce maximum fundamental ($m = 1$). It could be observed that $i_{\rm six-step}$ is a 3L reference signal obtained from 2L square waveform. Similarly, if this conversion technique applied on 3L reference waveform the resultant waveform will be a 5L reference signal and so on. Hence, for the topology under study that is the 5L CSI, this conversion method requires a 3L optimal switching angles.

B. Modified SOP for Current-Source Operation

The SOP technique is the combination of synchronous PWM and optimization. The technique is proposed for the 3L VSI topology [27], and later a generalized methodology has been developed for voltage-fed multilevel converters with any number of voltage levels [19]. Synchronous here refers to the ratio between the device switching frequency f_s and operating frequency f_1 is an integer. This is utilized to eliminate subharmonic frequencies, which are undesirable in many applications. The first step in the SOP technique is to determine the number of switching angles for each steady-state operating point, and then, optimization is performed to obtain switching angles that minimize the harmonic distortion of inverter output currents. In the last step, optimal switching angles are assigned to each semiconductor device to realize optimal current waveforms based on a systematic procedure. The step by step procedure of the classical SOP technique can be referred in [19].

The classical SOP technique requires some modifications in order to modulate and control the 5L CSI. One possible option is to modify the optimization algorithm to directly obtain 5L optimal switching angles that satisfy operational constraints of 5L CSI topology discussed in Section II-A. Another option is to modify the last step of the SOP technique to convert 3L optimal switching angles into 5L optimal switching angles using the conversion method explained in Section III-A and assign them to each power semiconductor device. In this paper, the second approach has been implemented for SOP modulation of 5L CSI topology.

1) Mathematical Analysis: Consider 3L reference current waveform i_{3L} shown in Fig. 4 has switching angles at α_1–α_6 in a quarter period. In order to eliminate all even-order harmonics, half-wave and quarter-wave symmetries is introduced in the switching pattern. Using Fourier series analysis, harmonic components of i_{3L} can be obtained as

$$i_{k,3L} = \frac{4I_{\rm peak}}{k\pi}\left(\sum_{i=1}^{N_\alpha} s(i)\cos(k\alpha_i)\right) \tag{2}$$

where $I_{\rm peak}$ represents the peak value of reference current waveform, k is the harmonic order (k=3,5,7...), $i_{k,3L}$ is the amplitude of kth harmonic current component of i_{3L}, N_α is the number of switching angles for 3L waveform in a quarter period, $s(i)$ represents the slopes of switching transients at switching angles α_i, $s(i) = (-1)^{i+1}$ for three-level waveform. The total

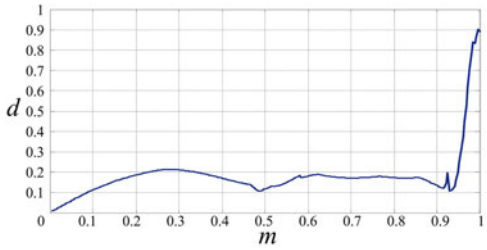

Fig. 7. Distortion factor d versus modulation index m for 5L CSI.

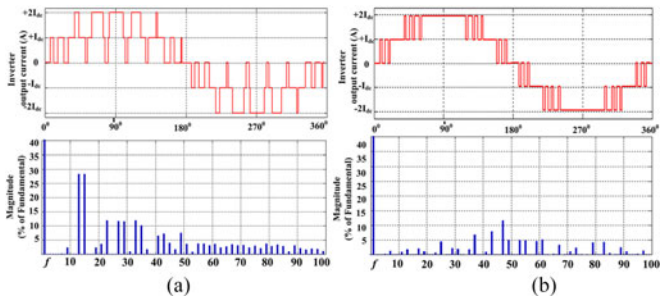

Fig. 8. Comparison of modulation technique results: (a) 5L waveform and FFT of CPS-PWM, (b) 5L waveform and FFT of SOP.

harmonic rms current of i_{3L} is given by

$$i_{h,3L} = \sum_k \sqrt{i_{k,3L}^2} \tag{3}$$

$$i_{h,3L} = \frac{4I_{\text{peak}}}{\pi}\sqrt{\sum_k \frac{1}{k^2}\left(\sum_{i=1}^{N_\alpha} s(i)\cos(k\alpha_i)\right)^2}. \tag{4}$$

The switching angles are optimized to reduce the harmonic distortion. In order to eliminate the system parameters in optimization function, distortion factor d is obtained as follows [27]:

$$d = \frac{i_{h,3L}}{i_{h,\text{sqr}}} \tag{5}$$

where $i_{h,3L}$ represents the total harmonic content of 3L reference current at a given operating point and $i_{h,\text{sqr}}$ represents the total harmonic content of square waveform I_{sqr} in Fig. 4. The total harmonic contents of I_{sqr} is given by

$$i_{h,\text{sqr}} = \frac{4I_{\text{peak}}}{\pi}\sqrt{\sum_k \frac{1}{k^2}}. \tag{6}$$

After simplifying (5) and (6), the final expression for d is obtained as

$$d = \frac{\sqrt{\sum_k \frac{1}{k^2}\left(\sum_{i=1}^{N_\alpha} s(i)\cos(k\alpha_i)\right)^2}}{\sqrt{\sum_k \frac{1}{k^2}}}. \tag{7}$$

From (7), it should be noted that, d is dependent only on k, $s(i)$, and α_i. The conventional SOP technique utilizes optimization algorithm for determining 3L switching angles α_i to minimize the value of d in (7) by including only harmonics of k = 5,7,11,.... It should be noted that in the distortion factor calculation, the three multiples components are not included in the conventional SOP technique. However, these optimal 3L switching angles cannot be utilized for operating CSI. Hence, these 3L angles need to be converted into 5L angles by utilizing the conversion method explained in Section III-A. For example, consider the 3L angles α_1, α_2, ...α_6, of waveform i_{3L} shown in Fig. 4, are the optimal switching angles obtained from the SOP technique. On applying the conversion method, these six angles are converted into 12 5L angles β_1, β_2,....β_{12}. The 5L waveform i_{5L} with the resultant twelve angles is shown in Fig. 4

In general, the conversion of N_α number of 3L angles obtains N_β number of 5L angles as $N_\beta = (2 * N_\alpha)$. The relation between device switching frequency f_s and selection of pulse number N_α is given by

$$N_\alpha = \left[\text{floor}\left(\frac{f_s}{f}\right) - 1\right]. \tag{8}$$

The harmonic component of i_{5L} is obtained as, $i_{k,5L} = \sqrt{3}i_{k,3L}$ if k=5,7,11,... and $i_{k,5L} = 0$ if k=3,6,9,.... The maximum value of fundamental component on inverter output current can be obtained if the 5L CSI is modulated with reference signal as six-step waveform $i_{\text{six-step}}$ in Fig. 3, i.e., $m = 1$. The harmonic components of $i_{\text{six-step}}$ is given by $i_{k,\text{six-step}} = \sqrt{3}i_{k,\text{sqr}}$ for k = 5,7,11,.... Therefore, the total harmonic content $i_{h,\text{six-step}}$ and $i_{h,5L}$ of $i_{\text{six-step}}$ and i_{5L} are given by

$$i_{h,5L} = \sum_k \sqrt{i_{k,5L}^2} = \sqrt{3}\sum_k \sqrt{i_{k,3L}^2} \tag{9}$$

$$i_{h,\text{six-step}} = \sum_k \sqrt{i_{k,\text{six-step}}^2} = \sqrt{3}\sum_k \sqrt{i_{k,\text{sqr}}^2}. \tag{10}$$

The distortion factor d with respect to 5L waveform is given by

$$d = \frac{i_{h,5L}}{i_{h,\text{six-step}}} \tag{11}$$

$$d = \frac{\sqrt{\sum_k \frac{1}{k^2}\left(\sum_{i=1}^{N_\alpha} s(i)\cos(k\alpha_i)\right)^2}}{\sqrt{\sum_k \frac{1}{k^2}}} \tag{12}$$

where, $k = 5, 7, 11, \ldots$. Hence, the distortion factor is unchanged with the conversion operation. The SOP technique requires optimal switching patterns to be calculated offline for all steady-state operating points. The modulation index m is ratio of fundamental amplitudes of I_{sqr} and i_{3L} which is $i_{1,3L}/i_{1,\text{sqr}}$ at the given operating point. To obtain the desired fundamental amplitude of inverter output current, the switching angles should satisfy the following equality constraint:

$$m = \frac{i_{1,3L}}{i_{1,\text{sqr}}} = \left(\sum_{i=1}^{N_\alpha} s(i)\cos(k\alpha_i)\right). \tag{13}$$

2) Inverter Control: A detailed signal flow graph that explains control algorithm is shown in Fig. 5. Angle selection in

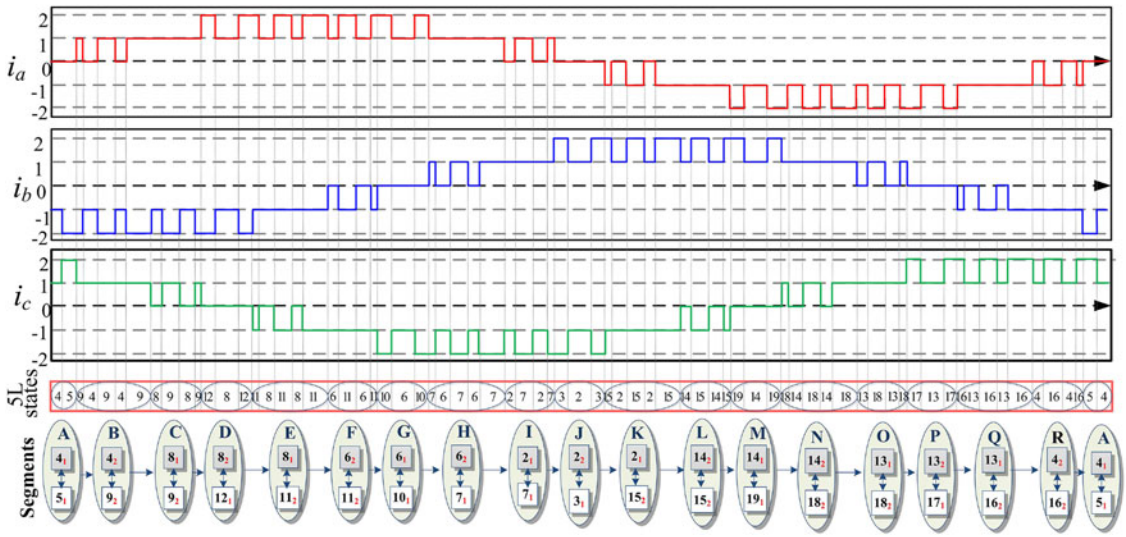

Fig. 9. 5L CSI redundant switching states sequencing.

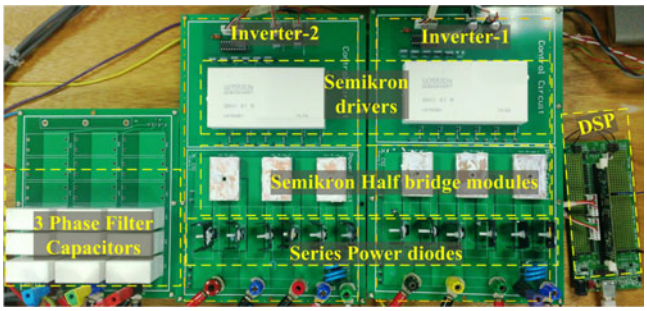

Fig. 10. Experimental setup of 5L CSI.

TABLE III
DEVICES AND PARAMETERS

Device/ Parameter	Part number/ Value
Converter power	1200 W
Input DC current	3.1 A
Switching frequency	350 Hz
AC output frequency	50 Hz
Output capacitor	30 μF
Load resistance	15.6 Ω
Load inductance	10 mH
Power diode	STTH30R04-Y
	I_f 30 A, V_{RRM} 400 V
Half-bridge module	SK 25 GB 12T4
	V_{CES} 1200 V, I_C 25 A
Six-pack driver	SKHI 61R

the control flow utilizes the magnitude of the reference current vector i_{ref} to select optimal 5L pattern $P(m, N_\alpha)$ that consists of optimized switching angles along with switching transitions $s(i)$. The optimal 5L pattern $P(m, N_\beta)$, phase angle of reference current vector and fundamental frequency f_1, are given as input to modulator which generates 5L switching state vector $i_k^{(5L)}$. The state selector utilizes the redundant states in Table II to minimize the overall switching transition and produces the gating signals for each semiconductor device of the CSI. The mechanism of redundant state selection can be referred to Section III-B5.

3) Optimization Algorithm: The aim of the optimization algorithm is to identify N_β number of 5L switching angles, which can be utilized for modulating the 5L CSI to obtain minimal THD for an operating point m (i.e.) distortion factor value given by (5) should be minimal. The optimal switching angles need to be identified for all range of modulation indexes (i.e.) $0 < m < 1$. By the property of conversion technique discussed in Section III-A, to obtain 5L switching angles with CSI operational constraint, it is sufficient to identify 3L switching angles. Hence, the algorithm focuses in obtaining optimal 3L switching angles and the conversion technique is used at the end of the algorithm for converting them into 5L switching angles as shown in Fig. 6. In addition to aiming at angles with minimal d, the switching angles are required to satisfy the following constraints [25]:

1) to allow minimum turn ON times and OFF times of power semiconductor devices, a sufficient gap (10 μs) between consecutive switching angles should be provided;
2) to maintain current modulation index value that satisfies the relation (13).

The modified SOP optimization algorithm involves four major stages such as initialization, optimization, postoptimization, and conversion as shown in Fig. 6.

1) *Initialization:* In this stage, the 3L angles $\alpha_2, \alpha_3, \ldots, \alpha_{N_\alpha}$ are randomly chosen such that all angles are within 0° to 90° and value of α_1 is calculated to satisfy desired modulation index m for the generated random angles α_2–α_{N_α}. Using (5), the distortion factor for the generated random angles is calculated but this value may not the minimal, and hence, these random angles are chosen with several iterations (25 000) to obtain 20 sets of 3L switching angles, which gives the least distortion among the iterations. These sets of angles are the output of the initialization stage, which can be utilized for further stage to obtain

TABLE IV
3L AND 5L SOP SWITCHING ANGLES

m	α_1	α_2	α_3	α_4	α_5	α_6	β_1	β_2	β_3	β_4	β_5	β_6	β_7	β_8	β_9	β_{10}	β_{11}	β_{12}
0.9294	9.04	11.48	15.71	19.57	22.29	88.63	7.72	10.44	14.31	18.54	20.98	39.05	41.49	45.72	49.59	52.31	58.65	61.38
0.749	21.35	40.80	46.00	51.96	55.73	86.16	8.67	10.81	16.01	21.98	25.74	51.36	56.17	63.86	70.81	76.01	81.98	85.74
0.6	19.77	43.58	52.16	60.69	64.76	80.38	10.25	13.6	22.17	30.71	34.78	49.78	50.4	69.63	73.6	82.17	85.25	89.32
0.5216	15.58	48.24	54.55	60.34	64.56	73.13	14.44	18.25	24.57	30.35	34.57	43.14	45.59	76.89	78.25	84.57	85.46	89.68

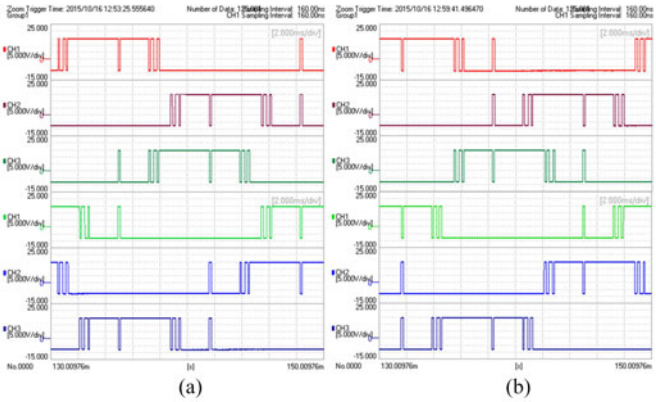

Fig. 11. Inverter gating pulses (*Y*-axis: 5 V/div; *X*-axis: 2 ms/div) for $m = 0.9294$. (a) Inverter-1 gating pulses for switches S_{1ap} to S_{1cn} (top to bottom). (b) Inverter-2 gating pulses for switches S_{2ap} to S_{2cn} (top to bottom).

global optimal. MATLAB function "randn" is used to generate random angles.

2) *Optimization:* The initial values identified in the previous stage are utilized as the starting position by optimization algorithm to find the minimal value of d with linear and nonlinear constraints. The optimization algorithms are broadly classified into active-set and interior-point algorithm. In this paper, active-set algorithm is preferred for finding optimal switching angles. With the 20 set of initial angles, the algorithm finds new 20 set of optimal values and among them the value with least distortion factor is outputted from this optimization stage. The gradient method "FMINCON" of MATLAB built-in function is used for obtaining optimized switching angles using the active-set algorithm.

3) *Postoptimization*: The initialization and optimization stages made to run for the range of modulation index m from 0 to 1 in discrete steps. In the postoptimization stage, the difference between optimal angle values of consecutive modulation indexes are checked and if the difference is higher than 5°, then optimization algorithm is executed again for the modulation index with additional limitation on optimal angles. The postoptimization enables continuity in optimal angles values for consecutive operating points, however, the new distortion factor d may be slightly higher than the previous value.

4) *Conversion:* The 3L angles α_1–α_{N_β} are then converted to 5L switching angles $(\beta_1, \beta_2, \ldots, \beta_{12})$ in order to incorporate CSI operational constraints mentioned in Section II-A. The final optimal switching angles are stored as complete patterns $P(m, N_\beta)$ in a DSP and they are retrieved during real time operation depending on the output current to be delivered to the grid.

4) *Optimization Results:* The distortion factor for the 5L CSI for $0 < m < 1$ is shown in Fig. 7. It should be observed that distortion factor approached unity at $m = 1$. This is because inverter output will be similar to six-step waveform $i_{\text{six-step}}$ shown in Fig. 3. In addition, due to reduced harmonic distortion and harmonic orders are shifted to higher frequencies, the proposed modified SOP technique reduces output filter size needed for the CSI in Fig. 2. A comparison of 5L waveform results of classical carrier-phase shifted pulsewidth modulation (CPS-SPWM) and the proposed modified SOP technique for same device switching frequency is shown in Fig. 8. It could be observed that lower order harmonics that appeared in the classical technique is reduced in the SOP technique and the overall THD of this waveform is 50% lesser than CPS-SPWM.

5) *State-Sequencing Machine:* A state-sequencing mechanism is developed in [28], the objective of this mechanism is to achieve minimal and equal number of commutation of semiconductor devices per fundamental period by utilizing redundant switching states. However, this sequencing technique is limited to the 3L CSI and it utilizes only redundant zero states. In order to achieve equal commutation for the 5L CSI, a separate state-sequencing mechanism needs to be identified, which is given next.

The redundant switching states of the 5L CSI can be referred from Table II. A state-sequencing mechanism as shown in Fig. 9 has been developed using the 5L redundant switching states. It consist of 18 sequence blocks (A, B, C, . . . R) within one complete fundamental cycle of switching pattern. A sequence block represents a pair of 5L switching states that appear repeatedly for an interval of time within a fundamental period. From the state-sequencing machine, it could be observed the redundant option for a 5L state differs from one block to another. This is explained by the following steps of procedure for choice of redundant option.

1) Identifying all the 5L state pairs for one complete fundamental period and define the number of sequence blocks.
2) Treat the states that appear in more than two blocks as master states. For example, the 5L states 4, 8, 6, 2, 14, and 13 are appearing in three sequence blocks as shown in Fig. 9. From the Table II, it could be observed in these states the inverter output current level is I_{dc} (i.e.) only one 3L inverter will be supplying load current, whereas the another 3L inverter will be in its zero 3L state (7 or 8

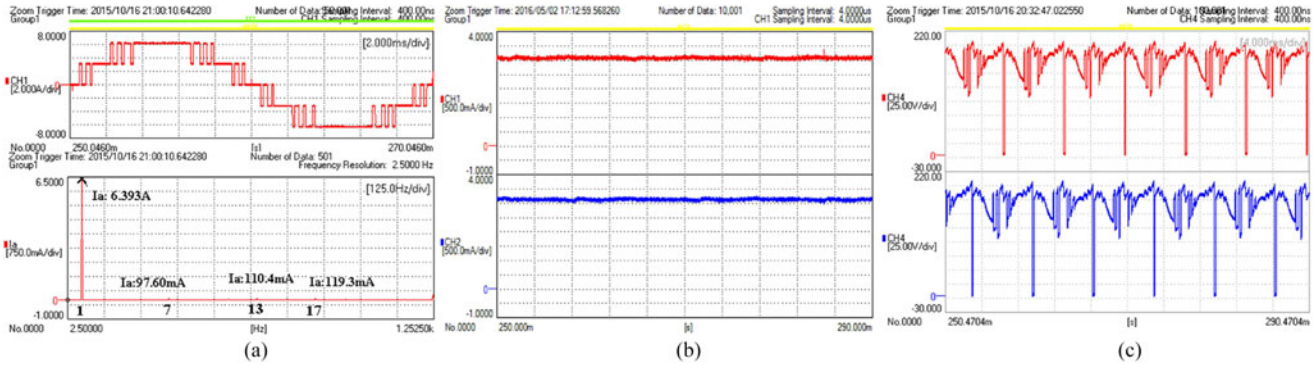

Fig. 12. Experimental results for $m = 0.9294$. (a) i_a (*Y*-axis: 2 A/div, *X*-axis: 2 ms/div) and its FFT spectrum (*Y*-axis: 0.75 A/div, *X*-axis: 125 Hz/div). (b) Inverter-1 and Inverter-2 input currents(*Y*-axis : 500 mA/div, *X*-axis: 4 ms/div). (c) Inverter-1 and Inverter-2 input voltages (*Y*-axis : 25 V/div, *X*-axis: 4 ms/div).

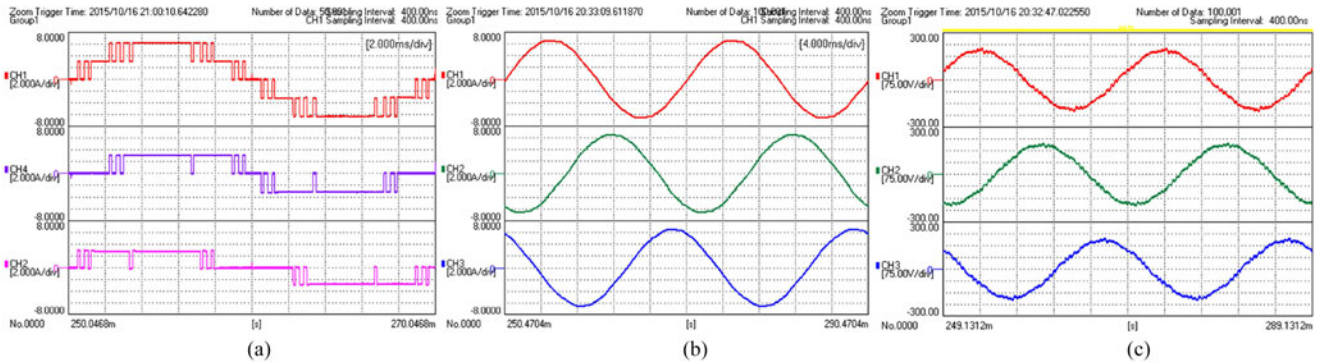

Fig. 13. Experimental results for $m = 0.9294$. (a) i_a, i_{a1}, and i_{a2} (*Y*-axis :2A/div, *X*-axis: 2 ms/div). (b) i_{ag}, i_{bg}, i_{cg} (*Y*-axis: 2 A/div, *X*-axis: 4 ms/div). (c) output voltages, v_{ab}, v_{bc}, v_{ca} (*Y*-axis: 75 V/div, *X*-axis: 4 ms/div).

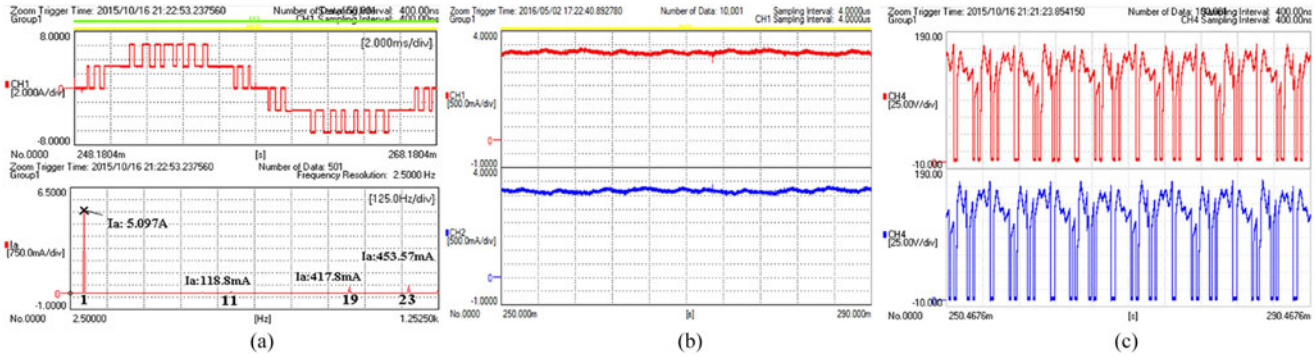

Fig. 14. Experimental results for $m = 0.749$. (a) i_a (*Y*-axis: 2 A/div, *X*-axis: 2 ms/div) and its FFT spectrum (*Y*-axis: 0.75 A/div, *X*-axis: 125 Hz/div). (b) Inverter-1 and Inverter-2 input currents (*Y*-axis: 500 mA/div, *X*-axis: 4 ms/div). (c) Inverter-1 and Inverter-2 input voltages (*Y*-axis: 25 V/div, *X*-axis: 4 ms/div).

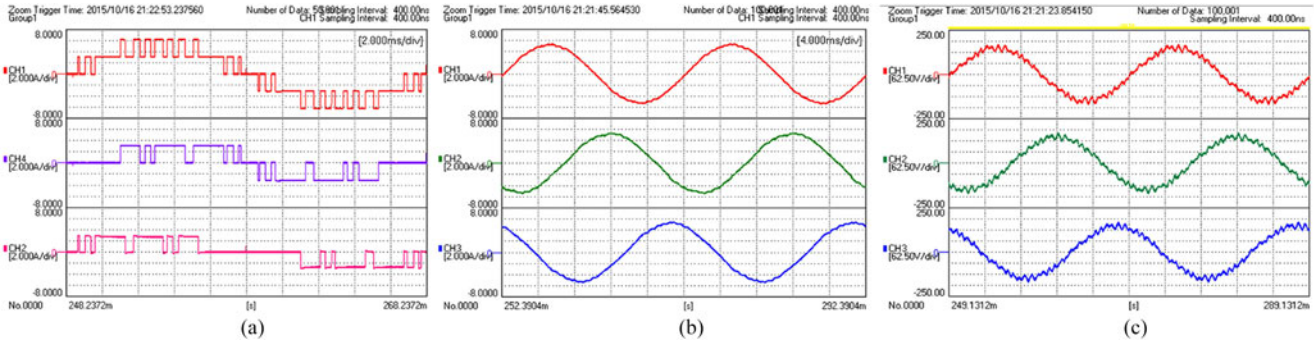

Fig. 15. Experimental results for $m = 0.749$. (a) i_a, i_{a1}, and i_{a2} (*Y*-axis: 2A/div, *X*-axis: 2 ms/div). (b) Filtered currents, i_{ag}, i_{bg}, i_{cg} (*Y*-axis: 2 A/div, *X*-axis: 4 ms/div). (c) Inverter output voltages, v_{ab}, v_{bc}, v_{ca} (*Y*-axis: 62.5 V/div, *X*-axis: 4 ms/div).

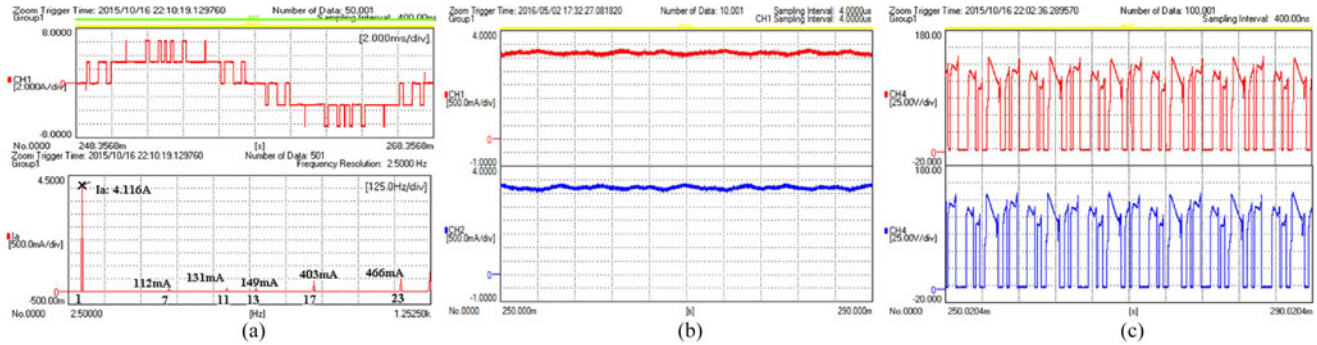

Fig. 16. Experimental results for $m = 0.6$. (a) i_a (*Y*-axis: 1.25 A/div, *X*-axis: 2 ms/div) and its FFT spectrum (*Y*-axis: 0.5 A/div, *X*-axis: 125 Hz/div). (b) Inverter-1 and Inverter-2 input currents (*Y*-axis : 500 mA/div, *X*-axis: 4 ms/div). (c) Inverter-1 and Inverter-2 input voltages (*Y*-axis : 25 V/div, *X*-axis: 4 ms/div).

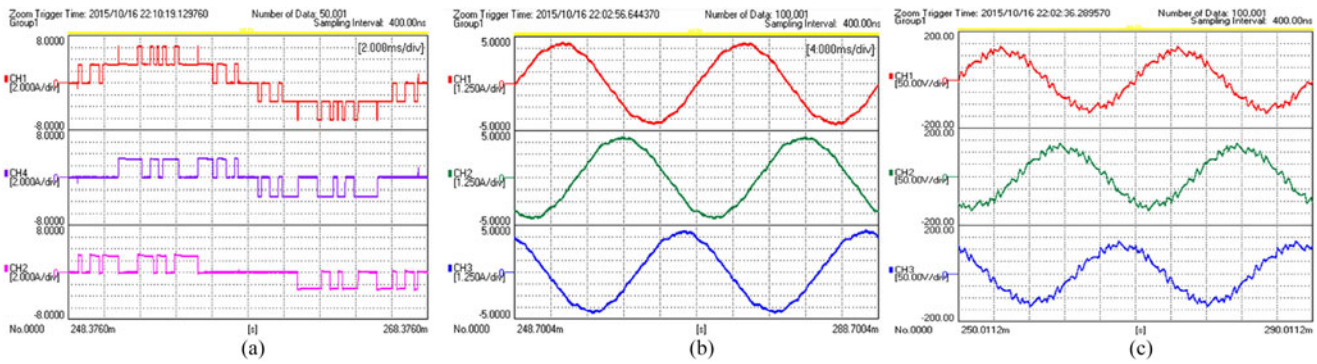

Fig. 17. Experimental results for $m = 0.6$. (a) i_a, i_{a1}, and i_{a2} (*Y*-axis: 2 A/div, *X*-axis: 2 ms/div). (b) i_{ag}, i_{bg}, and i_{cg} (*Y*-axis: 1.25 A/div, *X*-axis: 4 ms/div). (c) Inverter output voltages, v_{ab}, v_{bc}, v_{ca} (*Y*-axis: 50 V/div, *X*-axis: 4 ms/div).

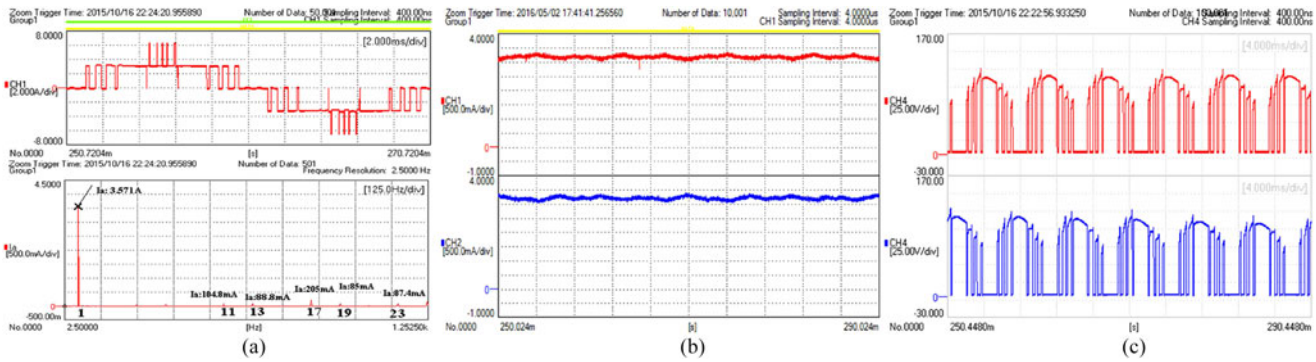

Fig. 18. Experimental results for $m = 0.5216$. (a) i_a (*Y*-axis: 2 A/div, *X*-axis: 2 ms/div) and its FFT spectrum (*Y*-axis: 0.5 A/div, *X*-axis: 125 Hz/div). (b) Inverter-1 and Inverter-2 input currents (*Y*-axis : 500 mA/div, *X*-axis: 4 ms/div). (c) Inverter-1 and Inverter-2 input voltages (*Y*-axis : 25 V/div, *X*-axis: 4 ms/div).

or 9). Hence, by changing the redundant option of these 5L master states on alternative sequence blocks, the load power will be equally shared among the 3L inverters.

3) In the previous step, the redundant option of master state in each sequence block has been fixed. The left-out state in each sequence block should be selected with a redundant option such that state transition to/from the master state brings minimal commutation. For example, in sequence block B the master state 4 is selected with redundant option 2 as per step-2. In order to achieve minimal commutation, the left-over 5L state 9 has to be selected with option 2. By this way, only two semiconductor devices (S_{2bn} and S_{2an}) turns ON/OFF during transition from 5L-state 4 to 5L-state 9, or vice versa.

IV. Experimental Results

A low-power prototype of 1.2 kW for controlling the 5L CSI using the proposed SOP technique has been setup as shown in Fig. 10. Separate PCB boards has been designed for implementing two 3L CSI. Each legs of the 3L CSI was implemented by using IGBT half-bridge power module SK25GB12T4 and a

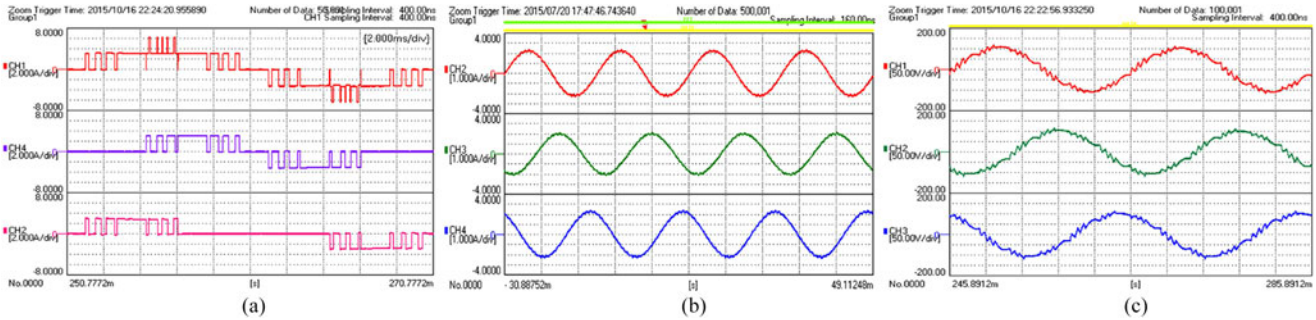

Fig. 19. Experimental results for $m = 0.5216$. (a) i_a, i_{a1}, and i_{a2} (*Y*-axis : 2 A/div, *X*-axis: 2 ms/div), (b) i_{ag}, i_{bg}, and i_{cg} (*Y*-axis: 1.25 A/div, X-axis: 4 ms/div). (c) Inverter output voltages, v_{ab}, v_{bc}, v_{ca} (*Y*-axis: 50 V/div, *X*-axis: 4 ms/div).

six-pack driver SKHI 61R from Semikron was used as a driver. The switching signals were programmed in C-language using code composer studio (CCS) and the code is flashed on a Texas Instrument TMS320F28335 DSP. It could be observed from the Table II, the number of angles per phase for quarter period is 12 in number, and hence, in total 36 angles need to be saved in DSP for three phases. However, from the conversion technique, it could be observed there are only six independent variables. Hence, in order to reduce the computation time in DSP, only these six angles are utilized with a functional routine to derive remaining angles. These stored angles are retrieved on each sampling time and by comparing the current angle with the optimal angles the states for all 12 switches of the 5L CSI are set to either 0 or 1. Table III shows the list of major components along with their parameters.The proposed modified SOP technique is utilized for generating optimal switching angles at four different operating points: ($m = 0.9294$, $N_\alpha = 6$), ($m = 0.749$, $N_\alpha = 6$), ($m = 0.6$, $N_\alpha = 6$), and ($m = 0.5216$, $N_\alpha = 6$). The 3L and 5L angles for these four operating points are shown in Table IV.

The pulse number for the operating points are maintained at N_β=12, so the device switching frequency of all semiconductor devices should be equal to 350 Hz (8). The gating signals for all the 12 semiconductor devices of the CSI for operating point $m = 0.9294$ are shown in Fig. 11(a) and (b). It is clear from the waveforms that each semiconductor devices is turned ON and OFF for seven times within one fundamental cycle, i.e., switching frequency is 350 Hz.

The waveforms of 1) inverter output current and its FFT spectrum, 2) output current for each 3L CSI, 3) filtered three phase output currents, and 4) inverter output line to line voltages pertaining to operating point ($m = 0.9294$, $N_\alpha = 6$, $f_1 = 50$ Hz) are shown in Figs. 12(a) and 13(a)–(c), respectively. It could be noticed from the FFT spectrum that the lower order harmonic components such as 7th, 13th, and 17th of the inverter output current are infinitesimal compared to the amplitude of fundamental. The magnitudes of these harmonic components are also shown in Fig. 12(a). It should also be noticed that the even-order harmonic and third-order harmonic components are eliminated. The filtered line current i_{ag} of the 5L CSI is nearly sinusoidal although the device switching frequency is reduced to 350 Hz. The THD of the filtered current is obtained as 1.36%.

Similar observations about inverter output current, FFT spectrum and filtered currents for operating points $m = 0.749$, $m = 0.6$, and $m = 0.5216$ are made from Figs. 14 to 19. It should be noticed that lower order harmonic components (<1 kHz) of inverter output current are infinitesimal for these operating points. The THD of output filtered currents for these three operating points are obtained as 1.93%, 3.14%, and 2.79%, respectively. These values are well below ($< 5\%$) the PV grid integration standard [29].

The waveforms of input voltage for each 3L CSI are shown in Figs. 12(c), 14(c), 16(c), and 18(c) for all four operating points. It should be noticed that there are no voltage spikes during switching transitions. The waveforms of inverter input currents are shown in Figs. 12(b), 14(b), 16(b), and 18(b) and it could be observed that input currents are maintained constant. This has been achieved by providing sufficient overlap (1 μs) between switching transition. It should also be noticed that, input voltage is zero for short intervals of time, which is due to turning ON both top (S_{xp}) and bottom (S_{xn}) semiconductor devices of one phase leg. Any ripple in input current will result in increase in THD. However, the input current is assumed to be constant delivered by the front-end dc/dc converter and so the current ripple has not been considered for the study. In case, the source is voltage source in nature and small inductor is used as input filter, then it will produce some ripple in the current. If the current ripple amplitude is high, then it will result in the asymmetrical ac output current, which might possess even order harmonics. In order to overcome this, redundant switching states should be utilized to keep ripple frequency as maximum possible so that ripple can be filtered out by the lower value of input inductor.

V. Conclusion

For high-power application such as large-scale solar power plants, low device switching frequency operation is required in order to satisfy the thermal constraint of semiconductor devices and efficient operation of the inverter. A modified SOP modulation technique has been proposed, analyzed, and implemented for controlling five-level voltage boost current-fed multilevel inverter topology at low device switching frequency. A simple conversion method has been introduced to include operational constraints of the CSI on the optimal switching angles. In addition, a state-sequencing machine has been developed to provide equal commutation of all semiconductor devices. A laboratory

prototype has been designed, developed, and tested at 1.2 kW to validate the proposed technique. Experimental results demonstrated the effectiveness of the proposed method and from the experimental results, it should be noticed that the inverter output current is nearly sinusoidal. The THD of line current has been maintained below 5% at all operating points of power flow without compromising on device switching frequency of 350 Hz.

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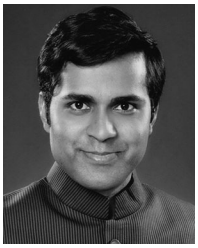

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