Harmonic Analysis and Controller Design of 15 kV SiC IGBT-Based Medium-Voltage Grid-Connected Three-Phase Three-Level NPC Converter

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***Abstract*—Cascaded converters are generally used for medium-voltage (MV) grid-connected applications due to the limitation in the voltage rating of available silicon (Si) power devices. These converters find application in active power filters, STATCOM or as the active front end converters for solid state transformers at the distribution voltage levels. The high voltage wide bandgap semiconductor devices have enabled the grid connected operation of noncascaded converters. This results in high power density, less number of switching devices, and high efficiency for three-phase MV grid interface. This also results in control simplicity without the need for complex dc bus balancing algorithms otherwise needed for cascaded converters. However, such noncascaded, grid-connected converters introduce challenges in maintaining power quality at low currents. This paper investigates the harmonic performance and current distortion of the grid-connected, three-level neutral point clamped converter using 15 kV silicon carbide Insulated Gate Bipolar Transistor (IGBTs). A suitable control scheme for stable harmonic compensation is proposed. The challenges and control performance are explained through frequency domain analysis, simulations, and experimental validation on a developed prototype of the three-phase converter up to 4.16 kV, three-phase MV grid-connected operation.**

***Index Terms*—Active front end converter, harmonic control, medium voltage (MV) grid tie, silicon carbide, 15 kV silicon carbide (SiC) IGBT.**

I. Introduction

MEDIUM voltage (MV) grid interface of power electronic converters based on silicon (Si) IGBTs is widely popular [1], [2]. Such converters find application in active power filters, STATCOM or as the active front end converters for solid state transformers (SST) and MV drives [1]–[3]. The Si IGBT available in the market currently is limited in voltage to 6.5 kV [4], [5]. As the grid voltage goes up to the distribution MV level, it is required to increase the number of cascaded converters to meet the voltage rating [1]–[3] with Si IGBTs. The large number of devices in a three-phase, cascaded structure results in poor efficiency, control complexity, and lower power density [6]. The cascaded structure is required to reduce the switching voltage since these Si devices are inefficient when switched at more than 0.5 to 1 kHz [4]–[6].

Low voltage (LV) 1.7 kV silicon carbide (SiC) MOSFET based three-phase MV grid interface is proposed in [7], switching at 50 kHz. However, this converter requires large number of devices or cascaded converter structure. Single-phase grid-connected converters are discussed in [8], [9] using 10 kV SiC MOSFETS [10]. The efficiency of MOSFETs reduces with the increase in the power due to high conduction loss and hence, IGBTs are preferred for high power applications. IGBTs have lower conduction loss due to conductivity modulation in the drift region [4]. The advent of MV SiC IGBTs has enabled the three-phase MV grid-connected operation of noncascaded three-level neutral point clamped (3L-NPC) converters [11]–[14]. The 15 kV SiC IGBT from Cree is one such device which can be used for three-phase MV grid voltage of $\geq$ 4.16 kV. It is highly efficient and can be switched at 5 kHz with only forced air cooling from 10 kV/5 A based on the characteristics given in [11], [14], [15]. This results in smaller size for the filter elements. Also, the control of 3L-NPC converter is simple in terms of dc bus voltage balancing as compared to cascaded converters [16]. The 15 kV SiC IGBT is proposed for SST application in the integration of renewable sources and distributed energy storage devices in [13].

However, 15 kV SiC IGBT when used in a noncascaded 3L-NPC grid-connected converter at MV introduces power quality challenges at lower current which is not experimentally validated in the available literature [17]. Due to the devices switching from higher blocking voltage, at 5 kHz switching frequency, with the highest ever dv/dt (25–50 kV/μs) compared to a cascaded structure, the effect of dead time harmonics is severe in such converters. Similarly, the input ac voltage across the converter terminals is higher, resulting in higher magnitude harmonics from the grid voltage seen by the converter. This causes harmonic control problems and results in poor THD at low fundamental currents [16]. This is a critical issue when operating

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TABLE I
COMPARISON OF SI AND SIC BASED MV CONVERTERS

Parameter per converter	Si-based converter	SiC-based converter
AC voltage level	$\leq$ 4.16 kV	$\geq$ 4.16 kV
DC voltage level	$\leq$ 7 kV	$\geq$ 7 kV
Switching frequency	0.5–1 kHz	3–5 kHz
Dead time	$\leq 2\ \mu$s	$\geq 3\ \mu$s
Maximum dv/dt	$\leq$ 10 kV/μs	$\geq$ 25 kV/μs
Grid current THD	$\leq 5\%$	Being analyzed in this paper

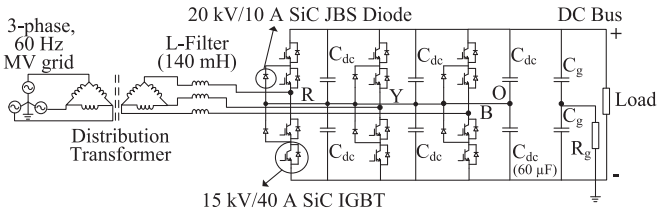


Fig. 1. Power circuit of the MV grid-connected converter.

TABLE II
SYSTEM PARAMETERS

Parameter	Value
MV grid voltage	2.64–4.16 kV
DC bus voltage	5–8 kV
Power	5.1–12.8 kW
Switching frequency	5 kHz
Dead time	3.8 μs
Filter inductance (L_f)	140 mH
Line resistance (R_f)	0.7 Ω
$C_{\rm dc}$	60 μF
Variac-transformer leakage	30 mH
C_g	80 nF
R_g	10 MΩ

under light load condition, which the converter is expected to encounter several times in the load cycle. Table I summarizes the comparison between one converter of a Si-based cascaded converter system and SiC-based noncascaded converter for MV grid tie applications.

In the literature, several methods have been proposed to eliminate lower order harmonics from grid current at lower grid voltage and higher currents [18]–[28]. These methods are complex control schemes and none of them have been validated on noncascaded MV grid-connected converters with proper stability studies. The grid voltage feed-forward is supposed to compensate the harmonic voltage present in the grid, but they are not sufficient to suppress the harmonic currents in the line due to dead time effect. Moreover, the grid voltage harmonics and dead time harmonics in the converter PWM voltage are phase shifted from each other due to active power flow. Hence, any error in their individual compensation amplifies the THD due to this phase shift. Therefore, in the closed-loop control, these harmonics propagate and pollute the total control loop [18]–[22]. Another method is to extract the current harmonics in the stationary reference frame using high pass filters, and then implement feed-forward compensation using these current harmonic components. At MV and low current levels, when the margin for error is minimal, it is not preferred to use such feed-forward compensation schemes, and rather the feedback-based approach is recommended. Also, variable switching frequency option is not considered due to thermal design challenges [23]. For the compensation of these harmonics using only the fundamental control loop, the outer dc bus voltage controller should have a bandwidth sufficiently above 360 Hz. For stable first-order transient response, the inner loop should have a bandwidth which is at least 8–10 times more than 360 Hz. With 3–5 kHz switching frequency, this is not possible and hence, increasing the bandwidth is not an option [16].

Another method is to use proportional-integral (PI) controllers with sinusoidal references in the stationary or three-phase reference frames. This method is considered unsatisfactory because it cannot completely eliminate the steady-state errors [24], [25]. This also requires very high bandwidth for the current control loops. A proportional-resonant (PR) controller or a PI-resonant controller can be used in the stationary reference frame for each lower order harmonic to be eliminated [27], [26]. But a PR controller-based grid current harmonic compensation is affected by the change in the grid voltage frequency. Also, it needs proper damping to be used for each harmonic frequency; else higher order harmonic frequencies can get injected into the current, resulting in poor THD. In addition, the digital implementation of the second-order model of the PR controller is not straightforward and is prone to higher error in fixed point implementation [25]. Digitization can also lead to deviation of frequency at which the infinite gain occurs with respect to the expected resonance frequency, thereby causing instability issues [28]. In [16], a synchronous reference frame-based control method to improve the THD under such MV, low current conditions is proposed for a 100 kVA SST application based on harmonic current extraction filter and harmonic compensation loops. However, the effect of delay introduced by the extraction filter is not considered in [16]. In this paper, the effect of extraction filter is explained in detail, and the controller design for harmonics is done for the best phase margin and bandwidth using a simple design process. Slight amount of even harmonics like 4th are also present in the grid voltage due to nonlinear loads connected to the grid, which affects the THD under light load conditions and are considered in this paper for justifying the experimental results. The converter performance also depends on the accuracy of the sensing and feedback path. The voltage sensors available for measuring MV have significant offset errors and low bandwidths. These parameters affect such control schemes implemented in the digital domain. High dv/dt switching and high peak voltage ripple at the output of the converter causes spiky current to flow through the filter inductor parasitic capacitance. This also results in current distortion in addition to the lower order harmonic current distortion.

In this paper, all these mentioned issues are quantified at MV, analytically explained in detail, supported by PLECS simulations and experimentally demonstrated on a 15 kV SiC IGBT-based 3L-NPC prototype grid connected up to 4.16 kV, three-phase MV grid. The impact of the proposed harmonic compensation is also studied. The paper organization is as follows: Section II explains the system including the power circuit and control. Section III analyzes the THD of the converter under light load conditions and studies the impact of the proposed control scheme through simulations. Section IV

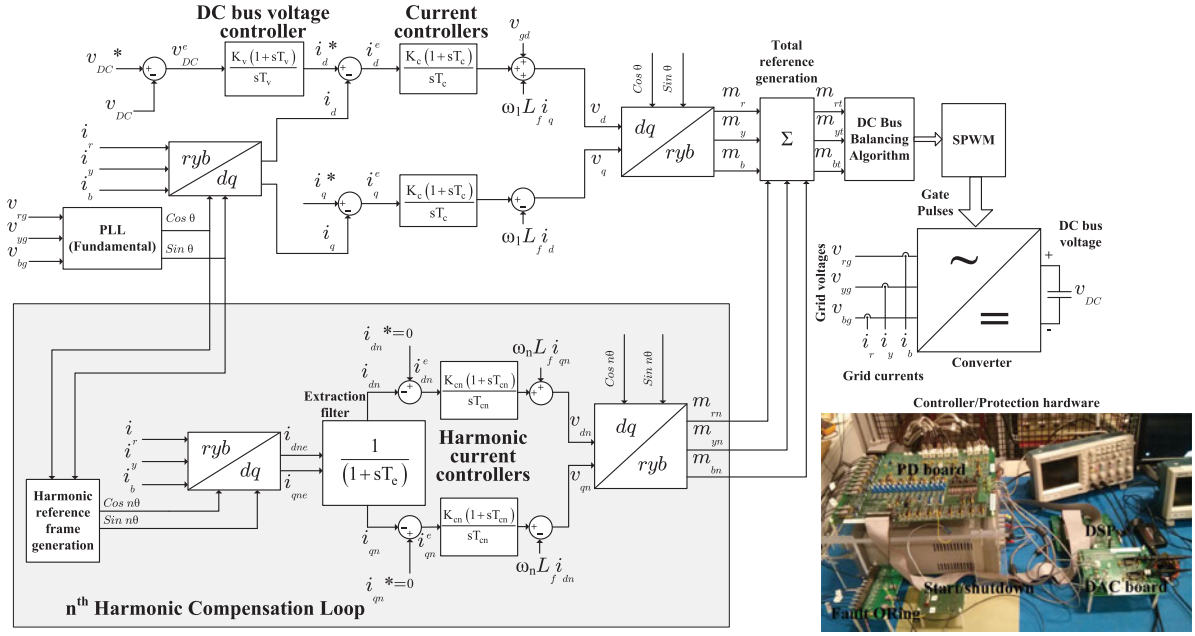


Fig. 2. Control block diagram and controller hardware of the MV grid tied converter.

gives the experimental validation of the converter harmonic performance. Section V concludes the paper.

II. Grid-Connected Converter System

A. Power Circuit Description

The power circuit of the converter system is shown in Fig. 1. A 3L-NPC converter is tied with the three-phase, MV grid through the distribution transformer and the L-filter. The distribution transformer is generally used for isolation purpose. 15 kV/40 A SiC IGBT copack module is used as the switching device while 20 kV SiC JBS diode is used as the clamping diode [29]. Table II summarizes the system parameters considered for the analysis including the voltage and power ranges. The converter is designed for 100 kVA. For the standard three-phase, 60-Hz distribution grid voltage of 4.16 kV, a load of 9.6 kW at 8 kV dc bus voltage is considered in the experiments for light load demonstrations. Below this power level, the effect of lower order harmonics becomes significant. This condition is mainly used for all analysis and simulations to compare with the experiments. Other voltage and power ranges in Table II are only demonstrated in the experiments. With 8 kV on the total dc bus, each device has to block 4 kV and switch at 5 kHz, which is way beyond the capability of any Si power device. The filter inductor used is 140 mH per phase at a switching frequency of 5 kHz. DC bus capacitance is 90 μF distributed in each phase as shown in Fig. 1. The converter grounding parameters C_g and R_g are given in Table II.

B. Control Algorithm and Design of Control Parameters

The control scheme used for grid-connected operation is shown in Fig. 2. The main advantage of using a noncascaded converter at MV is the usability of simple control algorithms for fundamental control. Synchronous reference frame-based vector control is the basic control scheme used for the 3L-NPC converter. Grid voltage is used as the reference vector as quency f_{PLL} is used for generating the reference angle (θ) by phase locking with the sensed grid voltage. All the sensed three-phase variables are converted to the equivalent synchronous dq reference frame variables using θ. In the synchronous reference frame, the fundamental component of all the variables behaves like dc parameters. For fundamental component control, there are three PI controllers used in the system—one voltage controller forming the slow acting outer control loop and two current controllers; one each in the *d*-axis and *q*-axis forming the higher bandwidth inner control loops. Feed-forward terms are used for decoupling the two current controller dynamics. The voltage controller regulates the MV dc bus voltage (v_{DC}) to the reference value ($v_{DC}*$) and generates the reference (i_d*) for the *d*-axis current controller. The *d*-axis current controller regulates the active component (i_d) of the fundamental grid current to this reference and generates the *d*-axis voltage component of the converter voltage (v_d). The objective of the *q*-axis current controller is power factor (pf) control on the grid side. The *q*-axis current controller regulates the reactive component (i_q) of the fundamental grid current to its reference (i_q*) and generates the *q*-axis voltage component of the converter voltage (v_q). Unity power factor (UPF) is achieved by keeping $i_q = 0$. Hence, the controllers ensure that the error signals v^e_{DC}, i^e_d, and i^e_q are regulated to zero. Fundamental three-phase modulating signals (m_r, m_y, m_b) are calculated from v_d, v_q.

Equation (1) gives the plant model ($G_p(s)$) of the converter. It has two time constants; the plant time constant T_f and the switching time T_{sw}. At 5 kHz switching frequency, T_{sw} = 200 μs. For the L-filter of L_f = 140 mH and considering R_f = 0.7 Ω, T_f = 200 ms. Thus, $T_f = 1000{*}T_{sw}$. This implies that for control parameter design the switching time can be neglected (verified later) and the plant model simplifies to $G'_p(s)$ in (2). The inner current control loop has to be made as fast as possible. It is possible to select 1 kHz ($\omega_i = 2 * \pi * 1000$ rad/s) bandwidth for this controller because of 5 kHz switching frequency. By canceling the dominant pole ($1/T_f$) in the system with the zero ($1/T_c$) of the current controller as shown in (3),

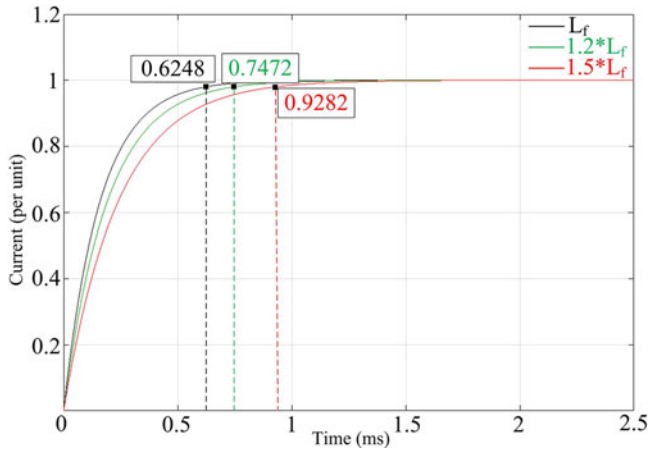


Fig. 3. Settling time variation with L_f.

very good transient response for the current control loop. The open-loop transfer function ($G_{c\_OL}(s)$) for the current control is given in (4), where K_c is the gain of the current controller and is calculated from (5) for the required bandwidth ω_i. The first-order closed-loop current control transfer function ($G_{c\_CL}(s)$) is given in (6). In all these derivations, feed-forward terms are assumed to decouple the *d*- and *q*-axes

$$G_p(s) = \frac{1}{R_f}\left(\frac{1}{1+sT_f}\right)\left(\frac{1}{1+s\frac{T_{sw}}{2}}\right) = \frac{i_d}{v_d} = \frac{i_q}{v_q} \quad (1)$$

$$G'_p(s) = \frac{1}{R_f}\left(\frac{1}{1+sT_f}\right) \quad (2)$$

$$T_c = T_f = \frac{L_f}{R_f} \quad (3)$$

$$G_{c\_OL}(s) = \frac{K_c}{sL_f} = \frac{i_d}{i_d^e} = \frac{i_q}{i_q^e} \quad (4)$$

$$K_c = \omega_i L_f \quad (5)$$

$$G_{c\_CL}(s) = \frac{1}{1+\frac{s}{\omega_i}} = \frac{i_d}{i_d*} = \frac{i_q}{i_q*}. \quad (6)$$

The pole-zero cancellation method can result in long tail in the step response, if exact cancellation does not happen in practical circuits. The effect of that can be quantified by measuring the settling time of the step response with increase in filter inductance. Fig. 3 shows the case where L_f is increased up to 1.5 times (210 mH) its designed value of 140 mH. The designed value (140 mH) of L_f is used for pole-zero cancellation, while it has increased to 210 mH in the actual system. It can be seen that the settling time increases by $\sim 300\mu$s in this case. This increase of 1.5*T_{sw} is considered as the worst-case condition. Since the outer voltage loop bandwidth is selected to be low as explained next, this is within the acceptable limit.

The open-loop transfer function ($G_{v\_OL}(s)$) for the voltage control is given by (7), where K_v and T_v are the voltage controller gain and time constant, respectively. $C'_{\rm dc}$ is the effective capacitance of the dc bus given by (8) and $R_{\rm dc}$ is the bleeder resistance. The load current is assumed to be a disturbance input in the small signal model. Here, m is the modulation index of

TABLE III
CONTROL PARAMETERS

Parameter	Value
K_c	880 Ω
T_c	0.2 s
ω_i	6283.2 rad/s
ϕ_i	90^0
K_v	0.0769 Ω^{-1}
T_v	2 s
ω_v	628.32 rad/s
ϕ_v	90.1091^0
f_{cs}	200 kHz
f_{vs}	10 kHz
f_{PLL}	60 Hz

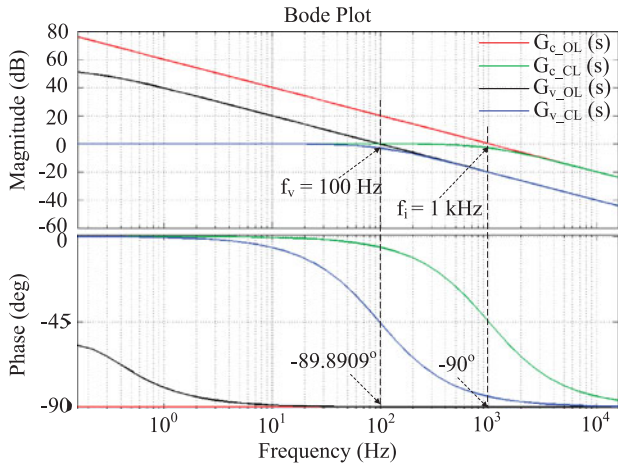


Fig. 4. Bode plots of the control transfer functions.

the converter which depends on the operating point. The closed-loop transfer function ($G_{v\_CL}(s)$) of the voltage control loop is given in (9) which can be rearranged as shown in (10). This implies that if $K_v >> \frac{1-C'_{\rm dc}R_{\rm dc}}{m\,R_{\rm dc}}$ or $K_v >> 0.0000816$ based on the system parameters, $G_{v\_CL}(s)$ can be written as in (11). This is a first-order system independent of T_v. With $m = 0.735$ for 4.16 kV grid, 8 kV dc bus and 9.6 kW operation, K_v can be selected for the required bandwidth (ω_v) of the voltage control loop as given by (12). For better dynamic response, $\omega_v = \omega_i/10$ is considered which results in a bandwidth of 100 Hz for the voltage control loop. Table III summarizes the control parameters designed for the presented converter. Fig. 4 shows the bode plot of all the transfer functions based on the designed parameters. This design ensures that both current and voltage control loops are first-order systems for stable overall performance. The phase margins ϕ_i and ϕ_v for the current and voltage loops, respectively, are found to be 90° and 90.1091°, which implies first-order transient performance for both current and voltage step changes. This is very critical at the MV level

$$G_{v\_OL}(s) = m\left(K_v\frac{(1+sT_v)}{sT_v}\right)\left(\frac{1}{1+\frac{s}{\omega_i}}\right)\left(\frac{R_{\rm dc}}{1+sC'_{\rm dc}R_{\rm dc}}\right) \quad (7)$$

$$= \frac{v_{DC}}{v_{DC}^e}$$

$$C'_{\rm dc} = \frac{3}{2}C_{\rm dc} \quad (8)$$

$$G_{v\_CL}(s) = \frac{1+sT_v}{1+s\left(\frac{1}{K_v m R_{\rm dc}}+1\right)T_v + s^2\left(\frac{C'_{dc}T_v}{mK_v}\right)} = \frac{v_{DC}}{v_{DC}*} \quad (9)$$

$$G_{v\_CL}(s) = \frac{1+sT_v}{(1+sT_v)\left(1+s\left(\frac{C'_{\rm dc}}{mK_v}\right)\right)+s\left(\frac{1-C'_{\rm dc}R{\rm dc}}{mK_vR_{\rm dc}}\right)} \quad (10)$$

$$G_{v\_CL}(s) = \frac{1}{1+s\left(\frac{C'_{\rm dc}}{mK_v}\right)} \quad (11)$$

$$K_v = \left(\frac{\omega_v C'_{\rm dc}}{m}\right). \quad (12)$$

C. Controller Hardware and Feedback Signal Processing

The controller is implemented using a 16-bit fixed-point DSP, TMS320LF2407A from Texas Instruments (TI). All the multiplications are done in 32-bit to improve accuracy. The ADC is of 10-bit and unipolar with 0–3.3 V range. The DSP communicates with a protection and delay (PD) board using FRC cables for better noise immunity. The PWM signals are the outputs from the DSP while the sensed feedback signals are the inputs to the DSP from the PD board. The PD board has three functions—scaling and processing the feedback signals for the DSP ADC, protection of the converter from grid over current and dc bus over voltage, and PWM signal processing with generation of dead time for the converter. A dead time of 3.8 μs for the converter is generated in the PD board. This controller/PD board arrangement for laboratory testing is also shown in Fig. 2.

The sensor output signals (0–$\pm$10 V) are scaled and shifted to the 0–3.3 V range for the ADC using high precision differential amplifier INA159 from TI in the PD board. It has high bandwidth of 1.5 MHz and high slew rate of 15 V/μs. The voltage sensor (bandwidth f_{vs}) used for both grid voltage and dc bus voltage sensing is rated at 4 kV nominal primary voltage (LEM LV100-4000/SP2V). This sensor is rated for 12 kV isolation voltage and hence has been selected in this application. The current signal output with 4 kV to 50 mA ratio given by this voltage sensor is converted to 0–$\pm$10 V range using 100 Ω burden resistance having 0.1% tolerance. High accuracy is very important since the MV is being scaled into 0–3.3 V scale. The current sensor used is LEM LA55P due to its high bandwidth (f_{cs}) of 200 kHz for better control dynamics and the isolation voltage of 2.5 kV. The sensors communicate with the PD board through shielded coaxial cable for eliminating high dv/dt generated noise. The shielding wire is grounded on the PD board.

III. THD Analysis of the Converter

A. Cause and Effect of Lower Order Harmonics

As the grid voltage increases, the fundamental current for same power decreases and this causes concern for the power quality as THD of the grid current increases. The main reasons for harmonic distortion of the grid currents are grid voltage harmonics and dead time generated harmonics [16]. The effect on power quality is not significant in cascaded or modular converters since the grid voltage harmonics get equally distributed across the individual converters and the dead time effect is small due to lower voltage switching with small dead time. With the noncascaded 3L-NPC converter with operating conditions listed in Table II, this effect becomes more significant. In [16], this harmonic effect is theoretically explained for 13.8 kV grid and 22 kV dc bus voltages, at 100 kW load and 5 kHz switching frequency. In this paper, an improved harmonic controller design compared to the one proposed in [16] is used, including the effect of the extraction filter time constant. The performance studied through simulation is supported by experimental results given in Section IV.

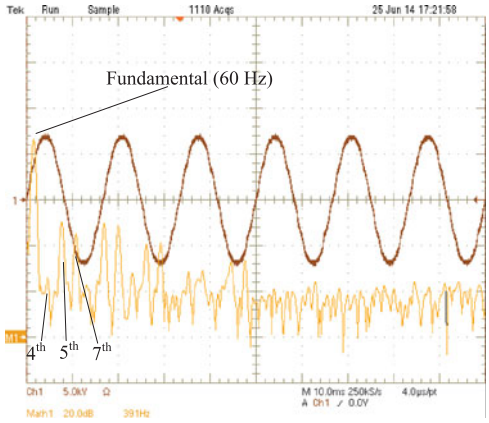


Fig. 5. Experimentally measured grid voltage harmonic spectrum (in dB).

TABLE IV
GRID VOLTAGE-GENERATED HARMONIC CURRENTS

Harmonic Component	Voltage (V)	Impedance (Ω)	Current (A)
Fundamental (60 Hz)	4160	52.78	1.33
4th (240 Hz)	29.46	211.12	0.1395
5th (300 Hz)	65.93	263.89	0.2498
7th (420 Hz)	41.59	369.45	0.1125

Since the converter is noncascaded, the entire 4.16 kV grid voltage is seen as the ac input by the converter. The THD standards like IEEE 519 allows a maximum of 3% of the dominant harmonic as well as maximum of 5% THD in the grid voltage [30]. At 4.16 kV fundamental voltage and above, this can result in high magnitude of harmonic voltage seen by the converter. In this study, for comparing with experimental results, harmonic spectrum of the grid voltage present in the laboratory is studied. The experimentally measured MV grid voltage harmonic spectrum is shown in Fig. 5 when the converter is not connected to the grid. Table IV shows the percentage distribution of the grid harmonic voltages measured. The dominant lower order harmonics till 7th harmonic are only considered for the analysis. The grid voltage THD is 2% which is very well within the 5% requirement as expected. Table IV also shows the impedance offered by the L-filter to individual harmonic frequencies. Based on these data, the individual harmonic currents are calculated. Fig. 6 (a) shows the magnitude of harmonic currents compared to the fundamental current at 4.16 kV, 9.6 kW assuming only grid voltage harmonics are present in the system and are not compensated. The grid current THD is 23.12%.

Dead time is used for protecting the devices in the 3L-NPC converter from shoot-through faults. The newly developed 15 kV/40 A SiC IGBTs have limited short circuit capability.

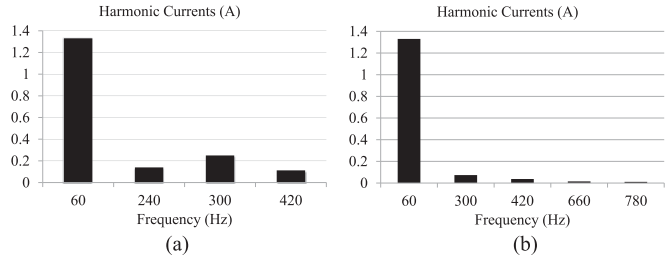


Fig. 6. Grid current harmonic spectrum without compensation. (a) Harmonics only from grid. (b) Harmonics only from dead time.

TABLE V
DEAD TIME GENERATED HARMONIC CURRENTS

Harmonic component	Voltage (V)	Impedance (Ω)	Current (A)
Fundamental (60 Hz)	4160	52.78	1.33
5th (300 Hz)	19.35	263.89	0.07334
7th (420 Hz)	13.82	369.45	0.03742
11th (660 Hz)	8.79	580.57	0.01515
13th (780 Hz)	7.44	686.12	0.01085

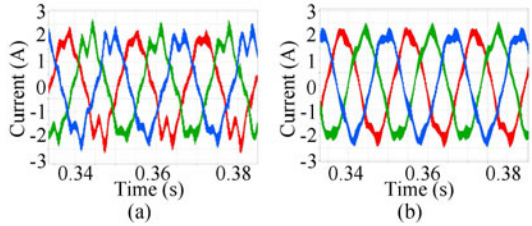


Fig. 7. Grid currents (a) without and (b) with harmonic compensation considering both grid voltage and dead time harmonics.

Hence, it is required to have large dead times when switching from higher voltages [16]. For the 8 kV dc bus considered for the converter, a dead time of 3.8 μs is chosen. This is based on the turn-on/ turn-off times, dv/dt, and the selected switching frequency of 5 kHz. This results in substantial amount of harmonics to be present in the grid current. Equation (13) gives the relation between the nth harmonic peak voltage v_n due to dead time, the dc bus voltage v_{DC}, the switching frequency f_{sw} and the dead time t_d [16]

$$v_n = \frac{4}{\pi n}\frac{v_{DC} f_{sw} t_d}{2}. \tag{13}$$

The harmonic currents contributed by a dead time of 3.8 μs at $v_{DC} = 8$ kV and $f_{sw} = 5$ kHz are calculated and given in Table V. Harmonic contents till 13th harmonic are considered. Fig. 6(b) shows the comparative plot of the harmonic contents with respect to the fundamental current at 4.16 kV, 9.6 kW assuming only dead time harmonics are present in the system and are not compensated. The grid current THD is 6.34%.

Fig. 7(a) shows the simulated waveforms when both grid voltage and dead time generated harmonics are assumed to be present in the system and are not compensated. The grid voltage harmonics and dead time harmonics in the converter PWM voltage are phase shifted from each other due to active power flow of 9.6 kW and hence does not cancel each other as discussed. Thus, the simulation shows that the cumulative effect is a THD of 18% if the harmonics are not compensated. Hence, in noncascaded converters at MV, the problem of lower order harmonics is severe at lower fundamental currents. The filter inductance is not sufficient to suppress them. Harmonic voltage magnitude even in the order of 50 to 100 V can cause very high THD. Fig. 7(b) shows the waveforms with compensation explained next.

B. Grid Current Lower Order Harmonics Compensation

The harmonic compensation loop used for the presented converter is highlighted in the shaded Section of Fig. 2. In the figure, the parallel harmonic block for general nth harmonic is shown. This is followed for all the dominant harmonics to be eliminated. The nth harmonic unit vectors (cos $n\theta$, sin $n\theta$) are generated from the outputs (cos θ, sin θ) of the fundamental PLL block using a harmonic oscillator. These harmonic unit vectors are used for converting the sensed three-phase grid currents (i_r, i_y, i_b) into the harmonic dq reference frame (i_{dne}, i_{qne}) in which the nth harmonic component behaves like dc. The fundamental current and other harmonics appear as higher frequency ripples. Since, the fundamental current amplitude is low for the presented converter, these harmonic dc components need to be extracted using low pass filters with very low bandwidth $1/(2\pi T_e)$. These extracted components (i_{dn}, i_{qn}) are used as the feedback signals for nth harmonic d, q PI controllers whose references $(i_{dn}*, i_{qn}*)$ are kept at zero. These controllers act to ensure that the nth harmonic current is regulated to zero in the system. One parallel control loop is used for each dominant harmonic to be eliminated. The outputs (v_{dn}, v_{qn}) of all the harmonic loops are converted into the three-phase harmonic modulating signals (m_{rn}, m_{yn}, m_{bn}). These are added with the fundamental modulating signals (m_r, m_y, m_b) to get the total modulating signals (m_{rt}, m_{yt}, m_{bt}) which are used in the PWM block to generate the gate pulses for the converter.

The design of harmonic controller is different from the fundamental current controller design due to the presence of another dominant pole $(1/T_e)$ contributed by the extraction filter. The delay caused by the extraction filter is neglected in the algorithm presented in [16]. The extraction process is very critical and therefore, the extraction filter bandwidth is kept at around 30 Hz in this study for the dominant 5th and 7th harmonics. The plant model seen by the harmonic controller is the same as in (2). Hence, the controller zero is used to cancel the most dominant pole in the system $1/T_f$ as in (14). Due to the transfer function $G_e(s)$ represented by (15) in the feedback path, the open-loop transfer function gets replaced by the loop gain in this case and is given in (16). This results in the harmonic closed-loop transfer function given by (17). This is a second-order system with damping coefficient (ζ) and natural frequency (ω_n) given by (18), and (19), respectively

$$T_{cn} = T_f = \frac{L_f}{R_f} \tag{14}$$

$$G_e(s) = \frac{1}{1+sT_e} = \frac{i_{dn}}{i_{dne}} = \frac{i_{qn}}{i_{qne}} \tag{15}$$

$$G_{n\_OL}(s) = \frac{K_{cn}}{sL_f(1+sT_e)} = \frac{i_{dn}}{i_{dn}^e} = \frac{i_{qn}}{i_{qn}^e} \tag{16}$$

TABLE VI
HARMONIC CONTROL PARAMETERS

Parameter	Value
K_{cn}	13.195
T_{cn}	0.2 s
T_e	5.31 ms
ζ	0.707
ω_n	0.0075 rad/s
ϕ_n	65.53^0
ω_{cn}	$2*\pi*30$ rad/s

TABLE VII
ϕ_n AND f_{cn} VARIATIONS WITH ζ

ζ	ϕ_n	f_{cn} (Hz)
0.1	11.42°	1000
0.2	22.6°	290
0.3	33.28°	110
0.5	51.83°	50
0.6	59.19°	35
0.707	65.53°	30
0.8	69.86°	25

$$G_{n\_CL}(s) = \frac{1+sT_e}{1+s\frac{L_f}{K_{cn}}+s^2\frac{L_fT_e}{K_{cn}}} = \frac{i_{dn}}{i_{dn}*} = \frac{i_{qn}}{i_{qn}*} \tag{17}$$

$$\zeta = 0.5\sqrt{\frac{L_f}{K_{cn}T_e}} \tag{18}$$

$$w_n = \sqrt{\frac{L_fT_e}{K_{cn}}}. \tag{19}$$

The value of harmonic controller gain K_{cn} needs to be decided based on the transient and stability requirements. K_{cn} is inversely related to ζ. High value of ζ is recommended for good phase margin (ϕ_n) to ensure stability but that results in low control bandwidth. To increase bandwidth, ζ needs to be low but that results in poor phase margin which affects stability. Since for the presented converter stability is very important at MV, and THD requirement needs to be met mainly during steady-state continuous operation, $\zeta = 0.707$ is selected which results in a very good phase margin of 65.53°. The bandwidth for the control (f_{cn}) consequently becomes 30 Hz. Table VI summarizes the control parameters for the 5th, 7th harmonic loops, and Table VII shows the variation of phase margin and bandwidth with ζ. Fig. 8 shows the bode plots of the harmonic loop transfer functions for two different values of ζ. It has to be noted that the phase of $G_{n\_OL}(s)$ does not change with change in K_{cn}.

Fig. 7(b) shows the grid current waveforms after implementing the 5th and 7th harmonic compensation loops [16]. It is seen that the THD has improved to 9.6% compared to the uncompensated waveform in Fig. 7(a). The half wave asymmetry is due to the 4th harmonic current present in the system. Even harmonics appear from the grid and it depends on the kind of load connected to the grid in the immediate vicinity. From Table IV, a small value (29.46 V) of 4th harmonic voltage can cause 139.5 mA of 4th harmonic current to flow in the converter if uncompensated. At low fundamental current of 1.33 A, this affects the overall THD severely. Grid voltage feed-forward in the fundamental dq loop is prone to error due to the high noise content in the sensed grid voltage owing to high dv/dt environment as well as inaccuracy of the voltage sensor. Thus, exact elimination of even harmonics in this way is not feasible. The harmonic compensation loop similar to the one proposed for odd harmonics is not effective for even harmonics. For example, in the 4th harmonic dq reference frame, 5th harmonic is present as 60 Hz ripple with sufficient magnitude and hence, 4th harmonic extraction for control is not feasible due to heavy filter requirement. Therefore, asymmetry is observed in the currents. Since this depends on the grid condition, it is not compensated in this paper and is only considered here to justify the asymmetry observed in the experimental results.

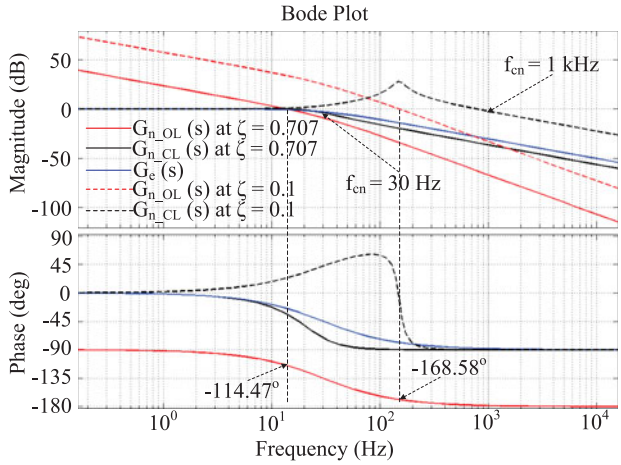


Fig. 8. Bode plots of the harmonic control transfer functions (solid line shows the plots for the selected control parameters).

C. Evaluation of Interaction of Parallel Control Loops and Effects of Digitization

The harmonic loop controller design is presented independent of the fundamental loop controller design. This is because the parallel loops do not interact with each other in the frequency range under consideration. An attempt is made to understand the performance of the fundamental loop with the harmonic loops operating in parallel and the controller implementation in digital domain. The digitization effect due to sampling is represented as a zero order hold (ZOH) transfer function ($G_{ZOH}(s)$), where the sampling frequency ($1/T_s$) is the same as the switching frequency (5 kHz) in the experimental demonstrations ($T_s = T_{sw}$). The current sensor is also represented as a low pass filter ($G_{cs}(s)$) with time constant $T_{cs} = 1/(2*\pi*f_{cs})$, where $f_{cs} = 200$ kHz. The cumulative effect is represented as the transfer function $G_{fb}(s)$ in the feedback path which is given in (20). The PWM switching effect is represented as a delay function ($G_{sw}(s)$ in Fig. 9). The computational delay time is far smaller than the switching time of 200 μs. Hence, it is already considered within the PWM switching transfer function $G_{sw}(s)$

$$G_{fb}(s) = G_{ZOH}(s)G_{cs}(s) = \underbrace{\left(\frac{1-e^{-sT_s}}{sT_s}\right)}_{ZOH}\underbrace{\left(\frac{1}{1+sT_{cs}}\right)}_{\text{CurrentSensor}} = \frac{i_{df}}{i_d}. \tag{20}$$

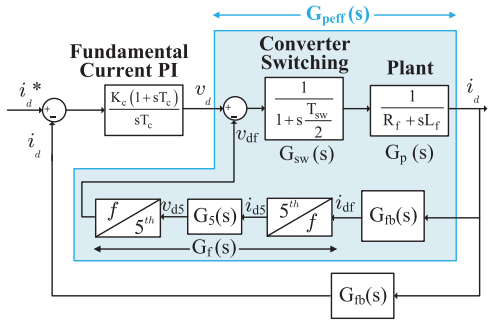


Fig. 9. Reduced form of fundamental d-axis control loop after reference frame conversion.

For the simplicity of analysis, only the 5th harmonic parallel compensation loop is considered. The same analysis can be carried out with the 7th harmonic loop also in parallel which gives similar results. For understanding the control interactions, the 5th harmonic loop is converted into the fundamental reference frame. Fig. 9 shows the rearranged and simplified d-axis control block diagram after conversion of 5th harmonic reference frame d-axis transfer function into fundamental reference frame. This is possible, since the harmonic references ($i_{dn}*, i_{qn}*$) are always zero. Similar block diagram is also used for q-axis current control. The objective is to calculate the transfer function $G_f(s)$ relating v_{df} to i_{df}, where v_{df} and i_{df} are the converter d-axis 5th harmonic voltage reference, and converter d-axis current after feedback and sampling, respectively, in the fundamental reference frame (notation "f"). These variables can be related to their 5th harmonic reference frame equivalents, v_{d5} and i_{d5}, through the reference frame conversion process as shown. The impact of the 5th harmonic control loop is basically a modification of the plant transfer function as given by (21). It is required to compute $G_f(s)$ to calculate the effective plant transfer function $G_{peff}(s)$. The 2×2 matrix expression for $[G_f(s)]$ is derived using (22) to (24) [31]. Here, $\omega_6 = 2 * \pi * 360$ rad/s is the ripple frequency of 5th harmonic components in the fundamental reference frame [31]

$$G_{peff}(s) = \frac{G_{sw}(s).G_p(s)}{1 + G_{sw}(s).G_p(s).G_f(s).G_{fb}(s)} = \frac{i_d}{v_d} \tag{21}$$

$$\begin{bmatrix} v_{df} \\ v_{qf} \end{bmatrix} = [G_f(s)] \times \begin{bmatrix} i_{df} \\ i_{qf} \end{bmatrix}$$

$$= \left([T(s)]^{-1} \begin{bmatrix} G_5(s) & 0 \\ 0 & G_5(s) \end{bmatrix} [T(s)] \right) \begin{bmatrix} i_{df} \\ i_{qf} \end{bmatrix} \tag{22}$$

$$G_5(s) = \left(\frac{K_{cn}\,(1 + sT_{cn})}{sT_{cn}} \right) \left(\frac{1}{1 + sT_e} \right) = \frac{v_{d5}}{i_{d5}} \tag{23}$$

$$[T(s)] = \begin{bmatrix} \frac{s}{s^2+\omega_6^2} & \frac{-\omega_6}{s^2+\omega_6^2} \\ \frac{\omega_6}{s^2+\omega_6^2} & \frac{s}{s^2+\omega_6^2} \end{bmatrix}. \tag{24}$$

The reference frame conversion process results in the matrix $[G_f(s)]$ having coupling terms between the d-axis and q-axis as expected in any reference frame conversion. For the sake of understanding, the grid-connected converter is assumed to operate in the UPF mode with $i_q = i_{q5} = 0$. Therefore, the transfer function $G_f(s)$ relating v_{df} to i_{df} in the d-axis can be derived by only considering the first row, first column element

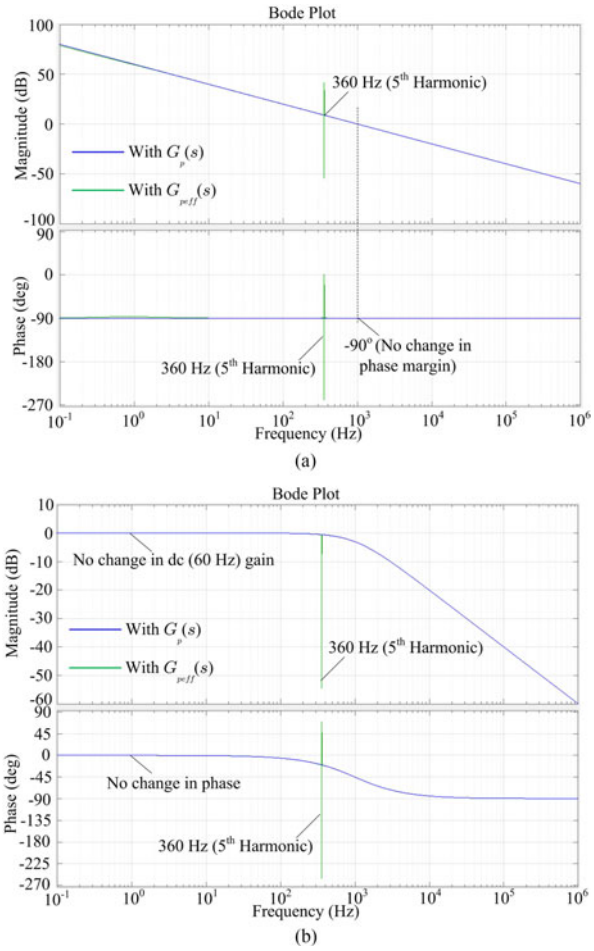


Fig. 10. (a) Loop gain and (b) closed-loop gain Bode plots of fundamental current control loop without digitization effects.

of $[G_f(s)]$ as represented by (25) which is used to calculate $G_{peff}(s)$. The performance of the fundamental current control loop with this effective plant transfer function ($G_{peff}(s)$) is compared with that using the simple filter plant model ($G_p(s)$) used in the design of the fundamental current controller

$$G_f(s) = [G_f(s)](1,1) = \frac{v_{df}}{i_{df}}. \tag{25}$$

Figs. 10 (a) and (b) show the loop gain and closed-loop gain Bode plots of the fundamental current control loop, respectively, using both $G_p(s)$ and $G_{peff}(s)$, without considering the effect of digitization ($G_{fb}(s) = G_{sw}(s) = 1$). It is seen that the 5th harmonic control loop does not modify the fundamental control loop Bode plots except at 360 Hz, which corresponds to the 5th harmonic ripple frequency in the fundamental dq reference frame. Also, the closed-loop magnitude offered to the 5th ripple frequency is very low, implying that any 360 Hz ripple in the d-axis current reference coming from the outer dc bus voltage loop is suppressed due to the effect of the 5th harmonic reference frame, which is the main requirement. The phase margin of the system is also not changed from 90°, ensuring stable operation and smooth performance under transients. Therefore, the independent design of parallel control loops is justified with accurate harmonic extraction process.

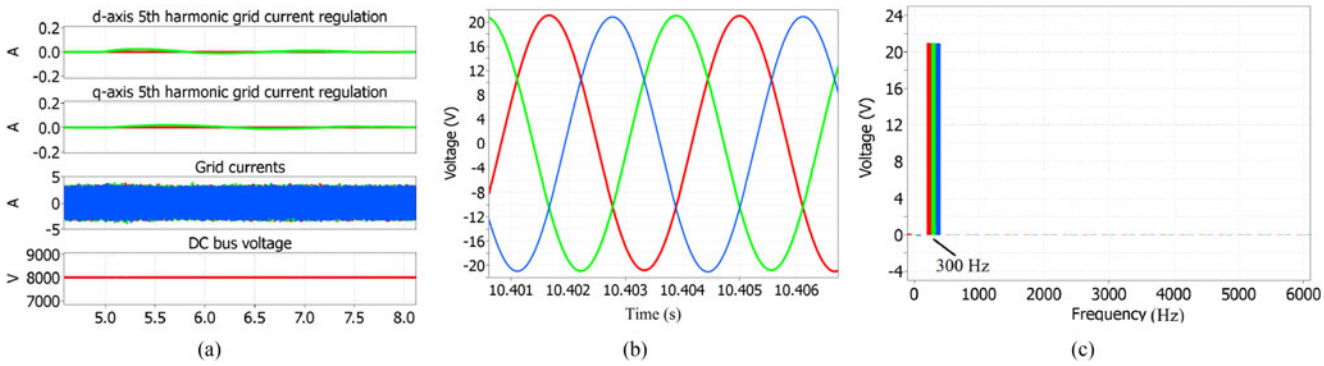


Fig. 11. (a) Controller response on 5th harmonic injection, (b) 5th harmonic three-phase modulating signals, and (c) their frequency spectrum during grid harmonic injection showing only 300 Hz.

Fig. 11(a) shows the simulation result when 3% of 5th harmonic is suddenly injected into the grid voltage at $t = 5$ s. It is seen that the 5th current controllers regulate the harmonic currents (green) to zero reference (red) without causing any transients on the fundamental grid current and dc bus voltage magnitudes. Therefore, as long as the harmonic extraction process is accurate, the interaction does not happen. This can also be seen from the 5th harmonic three-phase modulating signals and their frequency spectrum given in Figs. 11(b) and (c), respectively. The frequency spectrum of the 5th harmonic modulating signal shows only 300 Hz (in three-phase domain), when the 5th harmonic is injected into the grid voltage. Hence, the fundamental frequency currents at 60 Hz does not get affected during this control action.

The Bode plots are now studied considering the effects of digitization and sampling. Using the expression of $G_{fb}(s)$ given in (20), Figs. 12 (a) and (b) show the loop gain and closed-loop gain Bode plots of the fundamental current control loop, respectively, using both $G_p(s)$ and $G_{peff}(s)$. It is seen that the digitization effects do not modify the fundamental control closed-loop Bode plot below the 360-Hz ripple frequency significantly. Hence, the fundamental control during steady-state operation is not affected. But the transient performance can get affected due to a second-order behavior of the current control loop at high frequencies. Also from Fig. 12(a), the phase margin reduces to 40°. Therefore, the transient response can become oscillatory, but still the stability is ensured due to positive phase and gain margins. The current control loop bandwidth is not shifted from 1 kHz which is one of the main requirements.

This analysis shows that the digitization effects can cause the designed 5th harmonic control loop to influence the fundamental control loop transient performance at higher frequencies, but the stability is ensured. The impact can be reduced by increasing the sampling frequency. For example, it is observed that, twice sampling per switching period improves the phase margin to 50°. This issue of digital control is known and can be solved based on techniques available in [32]–[36]. However, this section quantifies the extent of the impact of digitization on the proposed control.

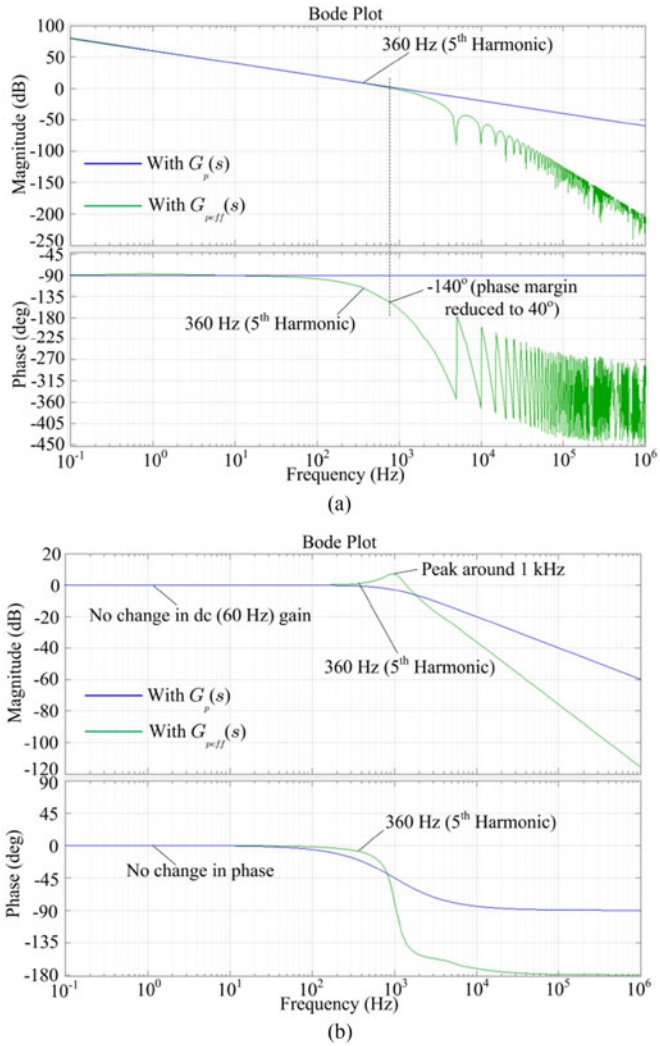


Fig. 12. (a) Loop gain and (b) closed-loop gain Bode plots of fundamental current control loop with digitization effects.

D. Sensor Offset and Error in Feedback Path

Fig. 7(b) is simulated for the case when all the sensors have 100% accuracy in the feedback path which is practically not the case. The voltage sensor (LEM LV100-4000/SP2) used for grid voltage feedback has an accuracy of $\pm 0.9\%$, burden resistance tolerance is 0.1%, and the gain error in INA159 is $\pm 0.024\%$ based on the datasheets. This gives an overall accuracy of 98.97% for the voltage feedback system under normal

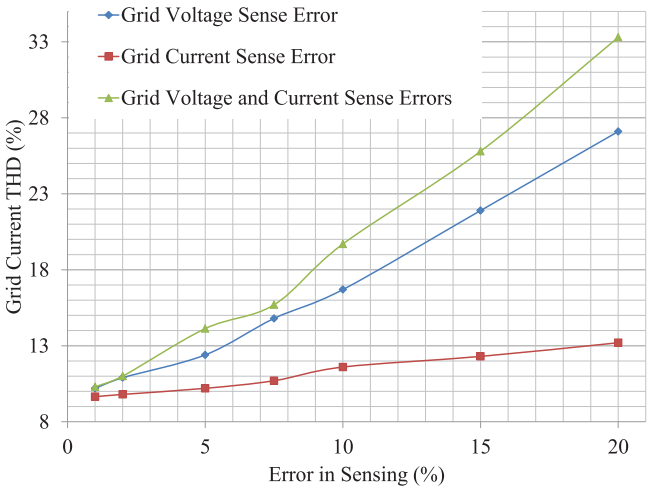


Fig. 13. THD variation in grid currents with magnitude error in sensors.

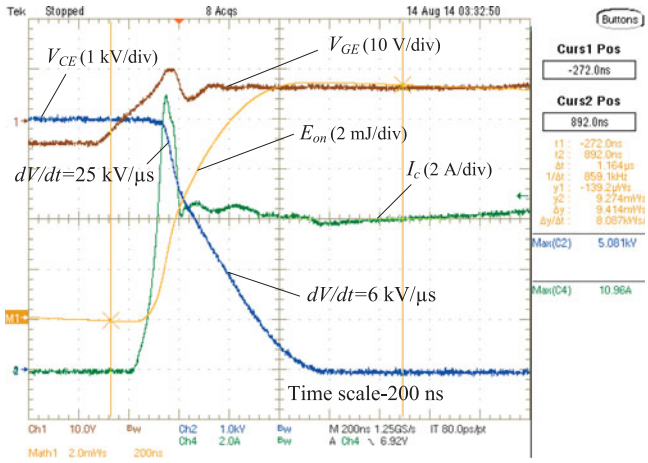


Fig. 14. 15 kV/40 A SiC IGBT turn-on characteristics at 5 kV, 5 A, 175 °C.

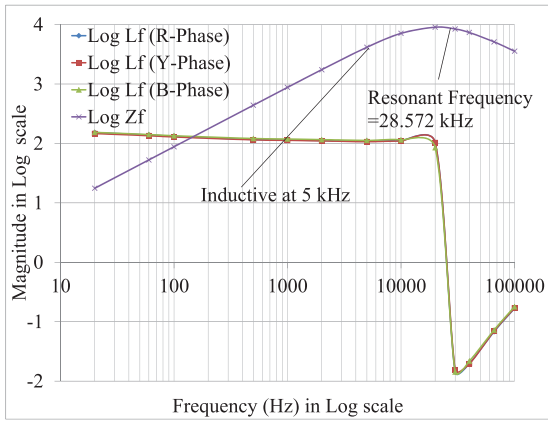


Fig. 15. Inductance and impedance versus frequency for the L-filter (in log scale).

conditions. Similarly, the grid current feedback system can be considered to have similar error. In addition, there are offsets at each stage in the feedback path including the ADC which vary with temperature. The offsets are canceled using moving average filter implemented inside the DSP controller after ADC conversion. However, the accuracy of offset cancellation is also less than 100%. These Hall effect high voltage sensors also come with low bandwidth which results in error when measuring harmonic content in the grid voltage. Fixed point implementation of feedback sensing and scaling can affect accuracy. Hence, it can be arguably assumed that the overall error can increase unpredictably during converter continuous operation and vary with temperature. As explained earlier, this can affect the grid current THD. Fig. 13 shows the grid current THD variation with sensing errors. It can be seen that THD is more sensitive to the grid voltage sensing error due to its effect on grid voltage feed-forward compensation. This implies that under light load conditions, grid voltage feed-forward can be removed to improve THD. However, this affects speed of current control and hence, a tradeoff has to be made.

E. Filter Inductance Parasitic Capacitance

An L-filter of 140 mH (0.18 p.u) is used for the 5 kHz switching ripple. Parasitic capacitance across the inductor is an important factor to consider while choosing the inductors. If this capacitance is high, the overall impedance offered at 5 kHz reduces and hence, proper filtering is not possible. Also, due to the high dv/dt seen by the inductor, this capacitance causes current spikes, polluting the grid currents. Fig. 14 shows the turn-on characteristics of the 15 kV/40 A SiC IGBT using a gate resistance of 33 Ω. The maximum dv/dt occurs during turn-on and can be seen to be 25 kV/μs at the turn-on instant. In this paper, iron core inductors are used to reduce the cost of the filter which generally have high parasitic capacitance. Thus, instead of using a single 140 mH inductor per phase, series connection of small inductors is recommended for the design [14]. Seven 20 mH inductors from Hammond (part no.195M30) are used in this converter per phase. Each inductor has a voltage rating of 750 V rms taking the total voltage rating to 5.25 kV rms which is suitable for this application.

Fig. 15 shows the plot of inductance versus frequency for the inductors used in the three phases. The three set of inductors have matching behavior. The impedance versus frequency plot of R-phase inductors is also plotted. The resonant frequency is 28.572 kHz, implying a total parasitic capacitance of 222 pF per phase. With 25 kV/μs dv/dt, the parasitic current comes out to be 5.55 A. With the parasitic capacitance of 60 Hz distribution transformer (∼1nF) also coming in series, this further reduces to around 4 A as shown in Fig. 16. The filter is inductive at the 5 kHz switching frequency which is the main requirement. However, this affects the grid current quality as seen from Fig. 16. These current spikes can be seen in the experimental waveforms with increased resolution in the oscilloscope.

F. High Power Performance Estimation

Figs. 17 (a) and (b) show the grid currents and the harmonic spectrum, respectively, at 4.16 kV grid, 8 kV dc bus voltage and 50 kW load. It can be seen that the currents are almost sinusoidal with an acceptable THD of 2.7% when the harmonic compensation is enabled. The peak current is within the acceptable current

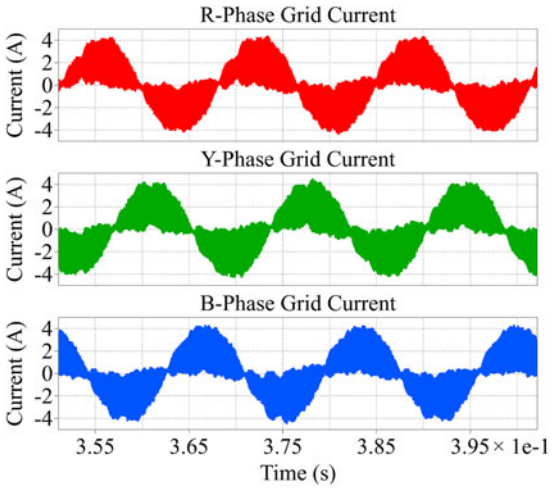


Fig. 16. Grid currents with 222 pF parasitic capacitance across the L-filter.

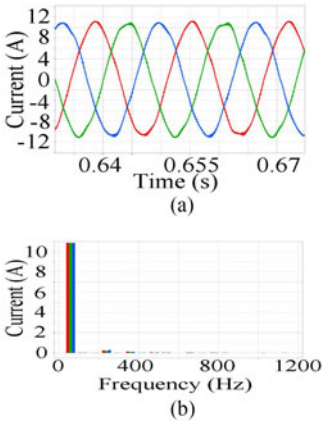


Fig. 17. (a) Grid currents and (b) harmonic spectrum at 50 kW.

rating of the SiC IGBT. Hence, the performance of the presented converter is expected to improve with power. Fig. 18 shows the variation of the THD with power and dc bus voltage. The THD is monotonically decreasing with the increase in power for all the dc bus voltage levels. Also, the THD is higher for higher dc bus voltage at the same power level. Experiments are limited to lower power in this paper due to the 10 A current rating of the available SiC JBS diodes, and considering some margin for transients. Nonetheless, the experimental results presented in the next section justify the estimated lower power harmonic performance, which is the focus of this paper.

G. Validation at Higher Grid Voltage and Dead Time

The control scheme is validated at higher grid voltage and dead time to see the performance under severe operating conditions. Simulation is carried out when the 3L-NPC converter is tied with 13.8 kV grid at 22 kV dc bus voltage, switching at 3 kHz and supplying 100 kW load. Figs. 19 (a) and (b) show the lower order harmonics in the grid current and their frequency spectrum, respectively, due to dead time and grid voltage harmonics without any compensation. The dead time used is 9 μs

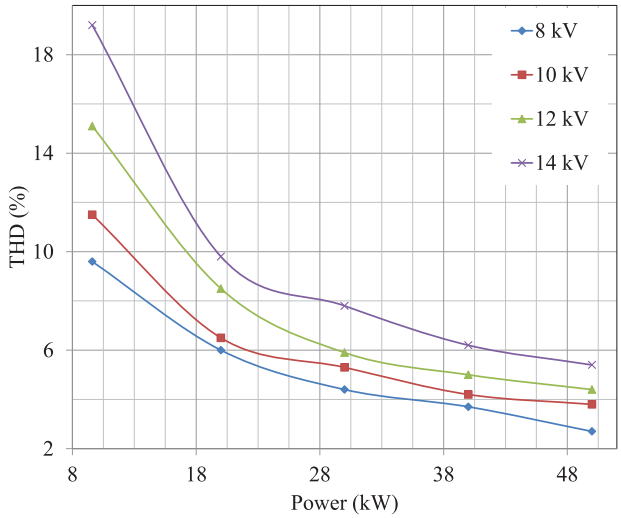


Fig. 18. THD variation in grid currents with power and dc bus voltage.

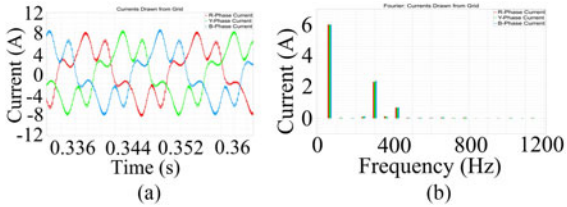


Fig. 19. (a) Grid currents and (b) harmonic spectrum at 13.8 kV grid, 22 kV dc bus, f_{sw} = 3 kHz, 100 kW without compensation.

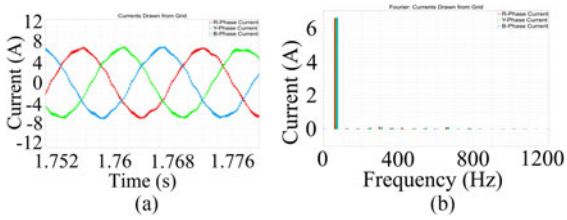


Fig. 20. (a) Grid currents and (b) harmonic spectrum at 13.8 kV grid, 22 kV dc bus, f_{sw} = 3 kHz, 100 kW with proposed control.

due to 15 kV SiC IGBT switching from 11 kV blocking voltage in this case. Also, 3% of 5th harmonic and 1% of 7th harmonic are considered to be present in the grid voltage. Filter inductance is 270 mH. It can be seen that the peak 5th and 7th harmonic currents are 2.4 and 0.7 A, respectively. These harmonic components along with little amount of 11th, 13th harmonic currents, etc. (due to dead time effect) results in a grid current THD of about 45% due to further distortion by the 360 Hz ripple in the fundamental control loop.

Fig. 20(a) shows the grid currents with the harmonic compensation loops implemented for 5th and 7th harmonics. Fig. 20(b) shows the grid current frequency spectrum for this case. It can be seen that the compensation scheme has successfully reduced the 5th and 7th harmonics from the grid currents. The overall THD is 2.8% which is a very good improvement. It is to be noted that the 4th harmonic considered in Fig. 7(b) is not considered here

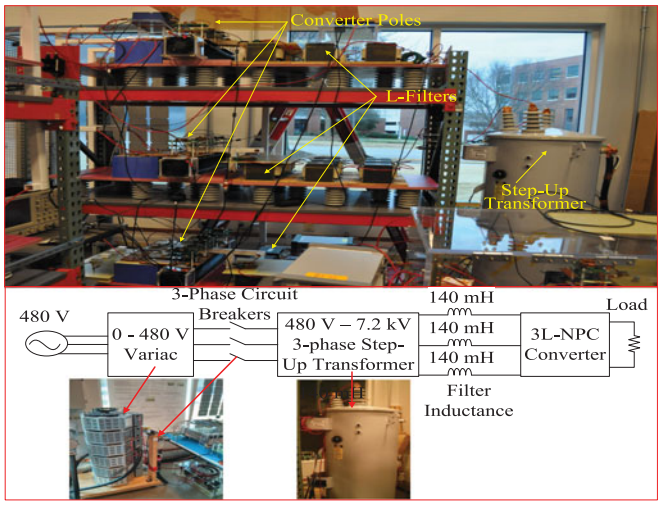


Fig. 21. Experimental prototype and test set-up schematic of 15 kV/40 A SiC IGBT based grid connected converter.

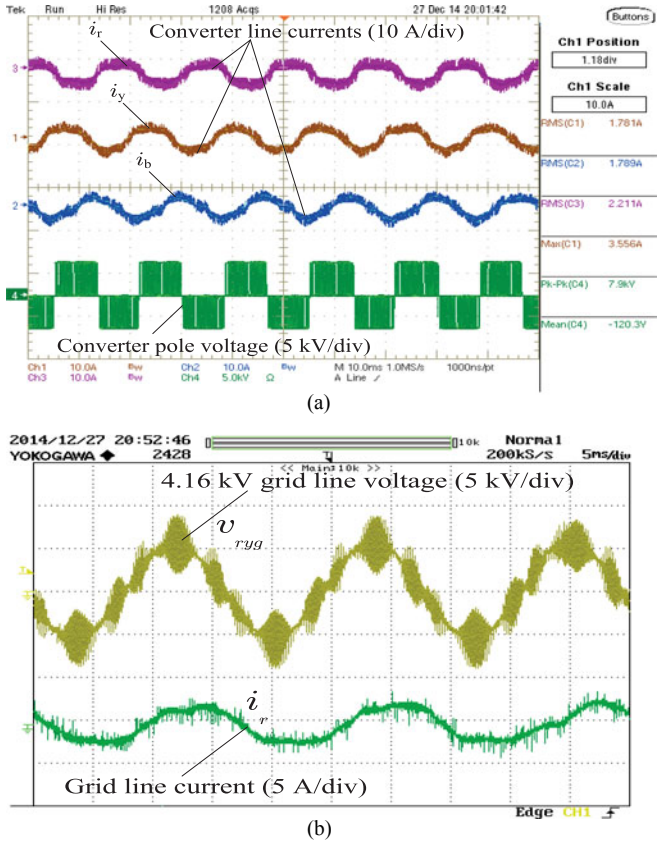


Fig. 22. (a) Converter currents (Ch1, Ch2, Ch3–10 A/div), pole voltage (Ch4–5 kV/div) and (b) grid line voltage (transformer output—5 kV/div), line current (5 A/div) at 4.16 kV ac grid, 8 kV dc bus voltage, 9.6 kW.

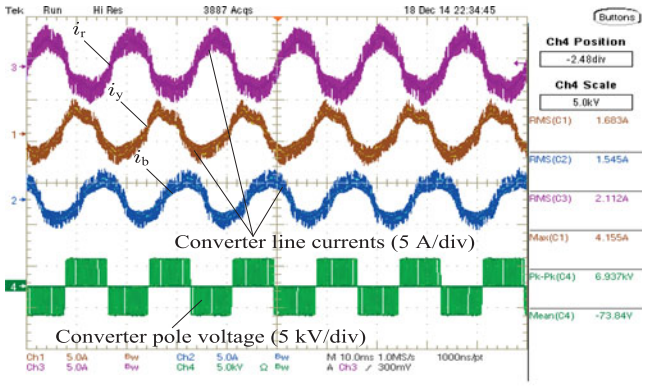
and hence, the improved THD. Nonetheless, the objective is to show that the proposed control works for different operating conditions other than the PCC condition used for experimental demonstrations. The control parameters for this case are tuned based on the discussed method.

IV. Experimental Validation

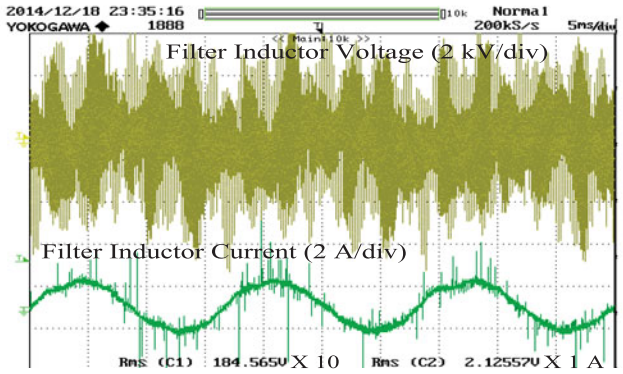
Experimental results are captured on a developed prototype of the converter using the laboratory arrangement shown in Fig. 21. The variac-60 Hz step up transformer combination is used to adjust the MV grid and represent the distribution transformer. Each pole of the converter is placed on a different shelf for MV isolation. Parameters are the same as listed in Table II. Figs. 22 (a) and (b) show the results captured at 4.16 kV ac grid, 8 kV dc bus voltage, and 9.6 kW. The currents are almost sinusoidal with THD closely matching Fig. 7(b) (9.68%). Current spike generated because of high dv/dt is not visible due to the low resolution of the oscilloscope. The grid (60 Hz transformer output) line voltage is seen to have high peak–peak ripple due to the high leakage inductance (30 mH). The variac and the transformer used for experiments in this paper has 30 mH total leakage inductance. This is mainly offered by the variac due to setting below the full rating and large inductance seen by the converter looking into grid.

Figs. 23 (a) and (b) show the results captured at 3.6 kV ac grid, 7 kV dc bus voltage, and 8 kW. The L-filter drops around 0.82% of the peak ripple voltage due to the variac-60 Hz transformer leakage inductance. Fig. 24 (a) shows the currents and pole voltage waveforms at 3.42 kV ac grid, 6.2 kV dc bus voltage and 12.8 kW. Fig. 24 (b) shows the frequency spectrum of the R-phase current plotted from experimental data [see Fig. 24 (a)]. The THD is calculated to be 5.8%. It is seen that the THD improves with power and reaches near to 5% limit. The asymmetry seen in the grid currents is due to the even harmonics as explained before. Fig. 25 shows the results at 2.64 kV ac grid, 5 kV dc bus voltage and 5.1 kW. The current quality is seen to be better at lower dc bus and grid voltages, and the switching ripple in grid current is negligible. Thus, the power quality is mainly a concern at higher voltage and lower current levels in noncascaded structure. The results with increased resolution of the oscilloscope is shown in Fig. 26 at 3 kV dc bus voltage and 2 kW in the standalone inverter mode of operation. The presence of 2 A current spikes is due to the 9 kV/μs dv/dt (at 1.5 kV blocking voltage) and significant parasitic capacitance. This effect becomes severe with higher voltages at high dv/dt which leads to EMI issues. The dv/dt after the punch-through voltage of the IGBT (around 5.5 kV) is very high and hence, the distortion can become severe. Therefore, series connection of filter inductor is recommended to reduce parasitic capacitance in such cases.

Fig. 27 shows i_d* and i_d while the dc bus is charging to 4 kV using ramp reference. To maintain the modulation index m at 0.75, the grid voltage is suddenly increased using variac at fixed time intervals which is a transient disturbance. The fundamental current loop is seen to be stable with the harmonic loops in parallel as discussed before. This experimental result shows that even with the digitization effects, the system stability is ensured as estimated analytically. The digitization effects such as sampling time and others can be compensated using the models discussed in [32]–[36] for better performance. This is beyond the scope of this paper.

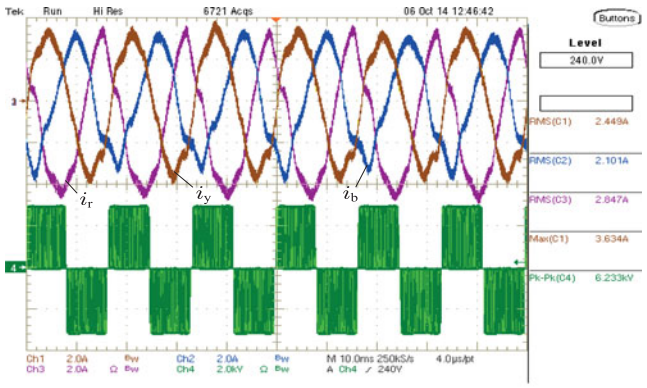


(a)

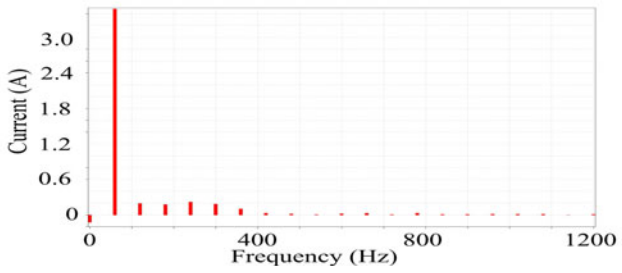


(b)

Fig. 23. (a) Converter currents (Ch1, Ch2, Ch3—5 A/div), pole voltage (Ch4—5 kV/div) and (b) L-filter voltage, current at 3.6 kV grid, 7 kV dc bus voltage, 8 kW.



(a)



(b)

Fig. 24. (a) Converter currents (Ch1, Ch2, Ch3—2 A/div), pole voltage (Ch4—2 kV/div) and (b) FFT of converter R-phase current (y-axis—0.2 A/div, x-axis—100 Hz/div) at 3.42 kV ac grid, 6.2 kV dc bus voltage, 12.8 kW.

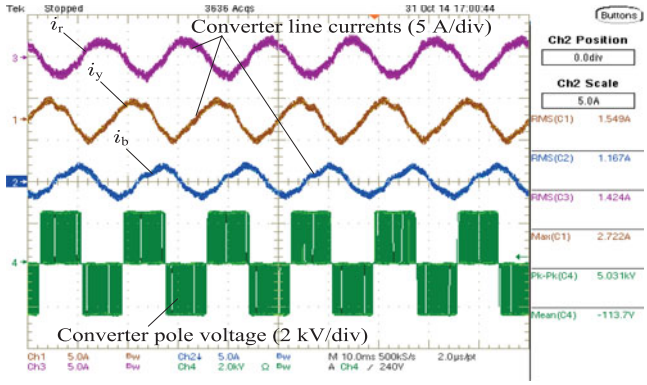


Fig. 25. Converter currents (Ch1, Ch2, Ch3—5 A/div) and pole voltage (Ch4—2 kV/div) at 2.64 kV ac grid, 5 kV dc bus voltage, 5.1 kW.

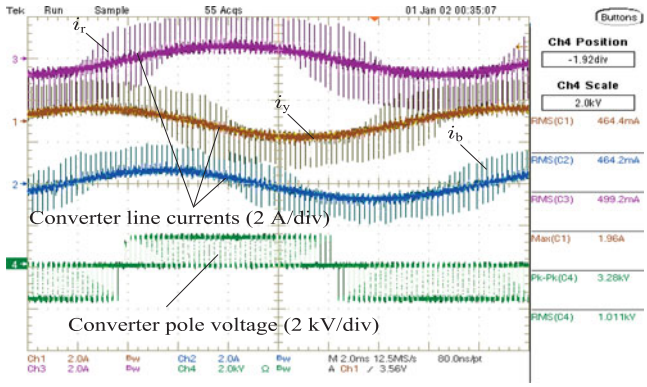


Fig. 26. Converter currents (Ch1, Ch2, Ch3—2 A/div) and pole voltage (Ch4—2 kV/div) at 3 kV dc bus voltage and 2 kW in the inverter mode.

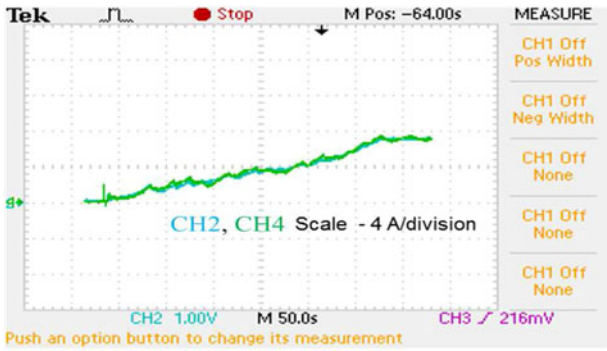


Fig. 27. Synchronous reference frame active current component (CH4—i_d) and its reference (CH2—i_d*) while the dc bus is charging to 4 kV with final steady-state power of 2.3 kW.

V. Conclusion

In this paper, the harmonic performance of a noncascaded, three-phase, MV grid-connected 3L-NPC converter based on the newly developed 15 kV SiC IGBT is analyzed. The MV converter based on 15 kV SiC IGBT has high power density, high efficiency, less number of devices and simple fundamental loop control. The challenges due to higher voltage switching and the inherent feature of being noncascaded are understood through simulations and experiments for low fundamental currents under light load conditions. An improved and robust controller design for better performance as well as stable harmonic compensation

is discussed. The converter performance is seen to be stable under light load conditions and estimated to be satisfactory at higher load. The robustness of the proposed control is validated on an experimental prototype of the grid connected converter up to 4.16 kV grid voltage. The impact of the proposed harmonic compensation loops on the fundamental control loop is analyzed. The parallel control loops are found to be independent of each other in the frequency range of interest, if the digitization effects such as sampling and converter switching are compensated. The steady-state performance of the system is not affected by the digitization effects. The transient performance is affected at higher frequencies but the system is found to be stable due to positive phase and gain margins. With further improvements in sensor accuracy and filter parasitics, this converter can be a viable candidate for MV grid-connected applications due to its many advantages.

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