Fully Integrated Buck Converter With Fourth-Order Low-Pass Filter

Nghia Tang, *Student Member, IEEE*, Bai Nguyen, *Student Member, IEEE*, Reza Molavi, *Member, IEEE*, Shahriar Mirabbasi, *Member, IEEE*, Yangyang Tang, *Member, IEEE*, Philipp Zhang, *Member, IEEE*, Jonghoon Kim, Partha Pratim Pande, *Senior Member, IEEE*, and Deukhyoun Heo, *Senior Member, IEEE*

***Abstract*—Fully integrated buck converters are typically operated with a second-order *LC* low-pass filter and a switching frequency beyond 100 MHz. The motivation for such design choices is to reduce the size of passive components in the *LC* low-pass filter required for small output voltage ripple. However, in a buck converter with on-chip planar spiral inductors, a fourth-order filter can deliver better performance characteristics without area penalty. This paper presents a comparative study of a fourth-order *LC* low-pass filter versus a second-order *LC* low-pass filter with on-chip planar spiral inductors and on-chip capacitors. A fully integrated buck converter is then designed with a quasi-V^2 controller to demonstrate the benefits of a fourth-order *LC* low-pass filter. The prototype chip, which is implemented in a 65-nm CMOS process, produces a nominal voltage of 0.7 V from a 1-V supply. The fourth-order *LC* low-pass filter uses a total inductance of 1.8 nH and a total capacitance of 4 nF. Measurement results demonstrate fast transient response on the order of nanoseconds. A peak efficiency of 76.1% is achieved, and the output voltage ripple is kept below 15 mV over the entire range of load current from 40 to 180 mA.**

***Index Terms*—Fourth-order *LC* low-pass filter, fully integrated buck converter, output ripple reduction, quasi-V^2 control.**

I. Introduction

FULLY integrated voltage regulators (FIVRs) have gained significant research attention in recent years. Such high interest in FIVRs has been driven by the need to implement point-of-load voltage regulation in multicore systems and system-on-chip. As highlighted in [1], on-chip FIVRs are essential to the effectiveness of fine-grained per-core dynamic voltage frequency scaling (DVFS) technique that is developed to reduce the power consumption of multicore systems. Fine-grained per-core DVFS demands FIVRs with high power efficiency, high current density, high power density, low output voltage ripple, and nanosecond response to load and reference changes. These stringent requirements are difficult to achieve for FIVRs due to on-chip area constraints and parasitic effects that degrade the performance.

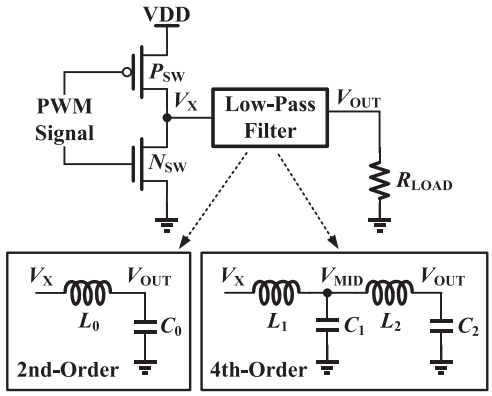


Fig. 1. Basic structure of a buck converter.

There are three main topologies of voltage regulators, i.e., linear regulators, switched-capacitor regulators, and switched-inductor regulators. Among these topologies, switched-inductor regulators can theoretically deliver higher power efficiency over a wide range of output voltage [2]. However, when being fully integrated on chip, a switched-inductor regulator faces several constraints limiting its performance. Fig. 1 illustrates a basic step-down switched-inductor regulator, i.e., a buck converter. A pulse width modulated (PWM) signal is produced to control power switches $P_{\rm SW}$ and $N_{\rm SW}$. The on/off actions of the power switches result in a square voltage waveform at node $V_{\rm X}$, which swings from VDD to ground at a switching frequency of $f_{\rm S}$. The square voltage waveform is then filtered by an *LC* low-pass filter to produce a low-ripple dc output voltage, $V_{\rm OUT}$. The characteristics of the *LC* filter are critical to all performance aspects of the buck converter including power efficiency, output voltage ripple, and transient response [3]. Given the area constraint imposed on FIVRs, the implementation of on-chip *LC* low-pass filters must be compact. Previous designs of fully integrated buck converters use high switching frequencies in the

Manuscript received January 20, 2016; revised May 11, 2016; accepted July 4, 2016. Date of publication July 27, 2016; date of current version February 2, 2017. This work was supported in part by the Center for Design of Analog-Digital Integrated Circuits (CDADIC), in part by the National Science Foundation (NSF), in part by the Natural Sciences and Engineering Research Council of Canada (NSERC), in part by the Technology Development Program of Korea Food Research Institute, and in part by the Research Department of HiSilicon at Huawei. Chip fabrication is facilitated by CMC Microsystems. Recommended for publication by Associate Editor J. A. Oliver.

N. Tang, B. Nguyen, P. P. Pande, and D. Heo are with the Electrical Engineering and Computer Science Department, Washington State University, Pullman, WA 99164 USA (e-mail: ntang@eecs.wsu.edu; bnguyen@eecs.wsu.edu; pande@eecs.wsu.edu; dheo@eecs.wsu.edu).

R. Molavi and S. Mirabbasi are with the Department of Electrical and Computer Engineering, University of British Columbia, Vancouver, BC, Canada (e-mail: reza@ece.ubc.ca; hahriar@ece.ubc.ca).

Y. Tang is with the Research Department of HiSilicon, Huawei, Shenzhen 518129, China (e-mail: tangyangyang@hisilicon.com).

P. Zhang is with the Research Department of HiSilicon, Huawei, Plano, TX 75024 USA (e-mail: philipp.zhang@huawei.com).

J. Kim is with the Korea Food Research Institute, Sungnam 463-764, Korea (e-mail: jhkim@kfri.re.kr).

Digital Object Identifier 10.1109/TPEL.2016.2593049

range of hundreds of megahertz to decrease the size of inductors and capacitors required for small output voltage ripple [4]–[11]. However, the low quality factor of on-chip inductors together with increased switching loss at higher switching frequencies degrades the power efficiency.

Several techniques have been presented to further reduce the size of the *LC* low-pass filter, such as multiphase operation [4], stacked interleave topology [7], and three-level topology [2]. Nevertheless, the available literature on the integrated *LC* low-pass filter itself is rather scarce. Most existing fully integrated buck converters use second-order *LC* low-pass filters. Intuitively, a second-order *LC* filter requires a small chip area because it uses only one inductor and one capacitor. However, we advocate that for a buck converter with on-chip planar spiral inductors, a fourth-order *LC* low-pass filter can potentially deliver better performance characteristics without area penalty. In such context, this paper presents a comparative study of second-order and fourth-order *LC* low-pass filters with on-chip planar spiral inductors in a monolithic buck converter. It is worth noting that several postprocessing techniques, such as bondwire inductors [12], magnetic-core inductors on interposer [13], silicon embedded inductors [14], and glass-substrate-integrated passive devices [15], can boost the performance of the *LC* filter. The inductors produced by these techniques tend to have better quality factors in comparison with on-die planar spiral inductors, and thus voltage regulators can be designed with higher power efficiency and higher power density. However, for fine-grained per-core DVFS in multicore systems, there is still a high interest in FIVRs with all on-chip passive components [1]. The study in this paper addresses on-chip planar spiral inductors in fully integrated buck converters and may not be applicable to other inductor technologies.

The next section of the paper analyzes the characteristics of a fourth-order *LC* low-pass filter in comparison with a second-order *LC* low-pass filter when on-chip planar spiral inductors and on-chip capacitors are used. A fully integrated buck converter using a fourth-order *LC* low-pass filter is then described in Section III. The concept of V^2 control is employed to design a stable control loop with fast load response [16]. Validation of the design is presented in Section IV, and Section V provides concluding remarks.

II. Fourth-Order Versus Second-Order *LC* Filters

A. Effect on Output Voltage Ripple

A second-order *LC* low-pass filter, as shown in Fig. 1, produces a pair of double poles at

$$f_0 = 1/\left(2\pi\sqrt{L_0 C_0}\right). \tag{1}$$

If the amplitude of V_X is 1 V, producing 10-mV output ripple requires an attenuation of –40 dB, which means that f_0 should be ten times lower than the switching frequency f_S.

A fourth-order *LC* low-pass filter, as shown in Fig. 1, produces two pairs of double poles at f_L and f_H. To simplify the analysis, L_1 and C_1 are assumed to be equal to L_2 and C_2, respectively. It can be shown that the frequencies of the two pairs of double poles can be estimated by

$$f_L = \sqrt{\frac{3-\sqrt{5}}{2}} \cdot \frac{1}{2\pi\sqrt{L_1 C_1}} \approx \frac{0.62}{2\pi\sqrt{L_1 C_1}} \tag{2}$$

$$f_H = \sqrt{\frac{3+\sqrt{5}}{2}} \cdot \frac{1}{2\pi\sqrt{L_1 C_1}} \approx \frac{1.62}{2\pi\sqrt{L_1 C_1}} \tag{3}$$

$$\sqrt{f_L \cdot f_H} = f_1 = \frac{1}{2\pi\sqrt{L_1 C_1}}. \tag{4}$$

For an attenuation of –40 dB, f_1 should be about 3.3 times lower than f_S and about three times higher than f_0 in (1). To compare the values of inductance and capacitance of the two filters, an *LC*-reduction factor *k* is defined as

$$k = \frac{L_0 C_0}{4 L_1 C_1} = \frac{f_1^2}{4 f_0^2} \tag{5}$$

where a factor of 4 appears because the fourth-order filter uses $2L_1$ and $2C_1$. Table I shows the relative pole locations of the two filters and the *LC*-reduction factor at various attenuation levels.

TABLE I
Characteristics of Fourth-Order *LC* Filter Versus Second-Order *LC* Filter

Attenuation	f_0/f_S	f_1/f_S	*K*
5.0% (–26 dB)	0.23	0.42	0.85
4.0% (–28 dB)	0.20	0.40	0.98
3.0% (–30 dB)	0.18	0.38	1.17
2.0% (–34 dB)	0.14	0.35	1.49
1.0% (–40 dB)	0.10	0.30	2.22
0.5% (–46 dB)	0.07	0.26	3.26

At –40-dB attenuation, given the same total capacitance, i.e., $C_0 = (C_1 + C_2)$, the total inductance $(L_1 + L_2)$ in the fourth-order filter can be 2.2 times smaller than the value of L_0 in the second-order filter. It should be noted that the total dimension of the inductors is not necessarily reduced by 2.2 times. The relationship between the inductance and the dimension of an on-chip planar spiral inductor can be expressed as

$$L = K_1 \mu_0 \cdot \frac{n^2 (d_o + d_i)^2}{2\left(d_o + d_i + K_2 d_o - K_2 d_i\right)} \tag{6}$$

$$d_i = d_o - 2n\,(w + s) \tag{7}$$

where K_1 and K_2 are layout-dependent coefficients, μ_0 is the free-space permeability, *n* is the number of turns, d_o is the outer diameter, d_i is the inner diameter, *w* is the trace width, and *s* is the spacing between adjacent turns [17]. These parameters are illustrated in Fig. 2 for square and octagonal inductors. Given constant width, spacing, and number of turns, the inductance is approximately linearly proportional to the outer diameter. When the chip area is a constraint, the inductance can be increased by increasing the number of turns and decreasing the width and the spacing while the outer diameter is kept constant at its maximum allowable value.

As an example, consider a second-order *LC* low-pass filter and a fourth-order *LC* low-pass filter in a 65-nm CMOS process. The second-order filter uses a 4-nF output capacitor while the fourth-order filter uses two 2-nF capacitors. By assuming

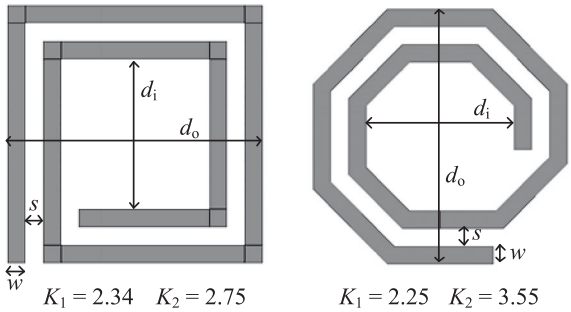


Fig. 2. On-chip planar spiral inductors: (a) square and (b) octagonal.

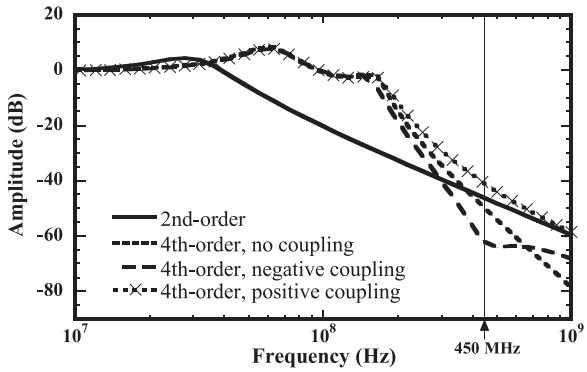


Fig. 3. Frequency response of second-order filter versus fourth-order filter.

the on-chip capacitance density to be 10 nF/mm^2, the area occupied by the capacitors is 0.4 mm^2. This area is used as a constraint for the inductors that we assume are being placed on top of the capacitors. Inductor L_0 of the second-order filter occupies the entire area of 0.4 mm^2 while inductors L_1 and L_2 of the fourth-order filter are 0.2 mm^2 each. The design target is to achieve better than –40-dB attenuation at 450 MHz. The inductors are implemented by a thick top metal layer (copper) in a 65-nm CMOS process used in this paper and are simulated by an electromagnetic (EM) field solver, i.e., Momentum. Fig. 3 shows the frequency response of the two filters. Three different configurations of the fourth-order filter are presented. In the first configuration, inductors L_1 and L_2 have no coupling between them. In the second and third configurations, they are placed at the minimum distance allowable by the process and are connected to produce negative and positive coupling, respectively. The second-order filter achieves –46 dB at 450 MHz with L_0 equal to 6.8 nH. The fourth-order filter with no coupling achieves –50 dB with L_1 and L_2 being 1.2 nH each. According to Table I, an *LC*-reduction of 3.26 is achieved at –46-dB attenuation, which requires only 1.04 nH for each of the two inductors. Fig. 3 also shows that the positive coupling between inductors L_1 and L_2 of the fourth-order filter lessens the attenuation while the negative coupling adds extra –12 dB. The coupling coefficients are found to be approximately 0.08 and –0.05 for the positive coupling and the negative coupling, respectively.

B. Effect on Power Efficiency

The current through the low-pass filter in a buck converter includes a dc load current and an ac ripple current whose fundamental frequency of variation is the switching frequency, $f_{\rm S}$. The effective resistance due to parasitic effects of the inductor(s) causes power loss. This loss can be estimated by

$$P_{L,\,\mathrm{LOSS}} \approx I_{\mathrm{DC}}^2 R_{L,\,\mathrm{DC}} + I_{\mathrm{AC}}^2 R_{L,\,\mathrm{AC}} \tag{8}$$

where $I_{\rm DC}$ is the dc load current, $I_{\rm AC}$ is the root-mean-square value of the ripple current, $R_{L,\rm DC}$ is the dc resistance, and $R_{L,\rm AC}$ is the effective ac resistance at $f_{\rm S}$. The dc resistance $R_{L,\rm DC}$ can be estimated from the geometry of the inductor by

$$R_{L,\mathrm{DC}} = K_3 R_{\mathrm{SH}} \cdot \frac{n\,(d_o + d_i)}{w} \tag{9}$$

where $R_{\rm SH}$ is the sheet resistance of the metal trace, and K_3 is equal to 2 for square inductors or 1.66 for octagonal inductors.

Equations (6) and (9) confirm that increasing inductance also increases dc resistance, and the relationship between the two quantities is approximately linear, assuming that $(d_{\rm o}-{\rm d_i})$ is small. Thus, if the *LC*-reduction factor is greater than 1, the fourth-order filter dissipates less dc power than the second-order filter does at the same load current.

Analyzing the ac power dissipation is more involved. For a specific *LC*-reduction factor *k*, inductor L_1 of the fourth-order filter is 2*k* times smaller than inductor L_0 of the second-order filter. Thus, the ripple current of L_1 is about 2*k* times larger than that of L_0. The ripple current of L_2 is often negligible since the voltage ripple at $V_{\rm MID}$ (see Fig. 1) is attenuated significantly by the L_1C_1 stage. Taking these observations into account, the power loss of the second-order filter and the fourth-order filter can be expressed as follows:

$$P_{\mathrm{second-order}} = I_{\mathrm{DC0}}^2 R_{L0,\mathrm{DC}} + I_{\mathrm{AC0}}^2 R_{L0,\mathrm{AC}} \tag{10}$$

$$P_{\mathrm{fourth-order}} = I_{\mathrm{DC1}}^2 \left(R_{L1,\mathrm{DC}} + R_{L2,\mathrm{DC}}\right) + I_{\mathrm{AC1}}^2 R_{L1,\mathrm{AC}} \tag{11}$$

where $I_{\rm DCi}$, $I_{\rm ACi}$, $R_{Li,\rm DC}$, and $R_{Li,\rm AC}$ are $I_{\rm DC}$, $I_{\rm AC}$, $R_{L,\rm DC}$, and $R_{L,\rm AC}$ of inductor $L_{\rm i}$ ($i = 0$, 1, and 2), respectively. The effective ac resistance $R_{L,\rm AC}$ is usually higher than the dc resistance $R_{L,DC}$ due to the high-frequency phenomena such as skin effect, proximity effect, and substrate coupling. At frequencies below 1 GHz, which is typically the case for fully integrated buck converters, the skin effect is not an issue due to the relatively small thickness of the conductor layer [18]. However, the proximity effect and substrate coupling should be taken into account even at frequencies below 1 GHz. Furthermore, their adverse effects are more pronounced for large inductors that have large dimension and large number of turns. They cause the effective ac resistance to increase more than linearly with the inductance, i.e., 2 × increase of inductance results in >2 × increase of ac resistance.

Two sets of inductors with different values are simulated in Momentum to evaluate their effective resistance. In the first set, the inductance is changed by adjusting *n*, *w*, and *s* while keeping $d_{\rm o}$ and $d_{\rm i}$ constant. In the second set, $d_{\rm o}$ and $d_{\rm i}$ are adjusted while *n*, *w*, and *s* are constant. All inductors are subject to the area constraint of 0.4 mm^2. Fig. 4 shows the simulated effective resistance versus the inductance at dc, 450, and 900 MHz. The plot confirms that $R_{L,\rm DC}$ increases almost linearly with the inductance while $R_{L,\rm AC}$ increases at a faster rate.

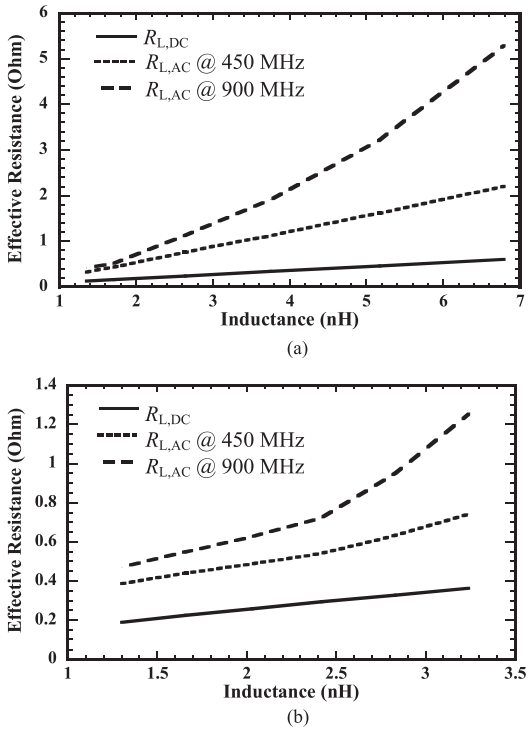


Fig. 4. Characteristics of on-chip planar spiral inductors simulated in momentum: (a) varying *n*, *w*, and *s* while keeping d_o and d_i intact; (b) varying d_o; and d_i while keeping *n*, *w*, and *s* intact.

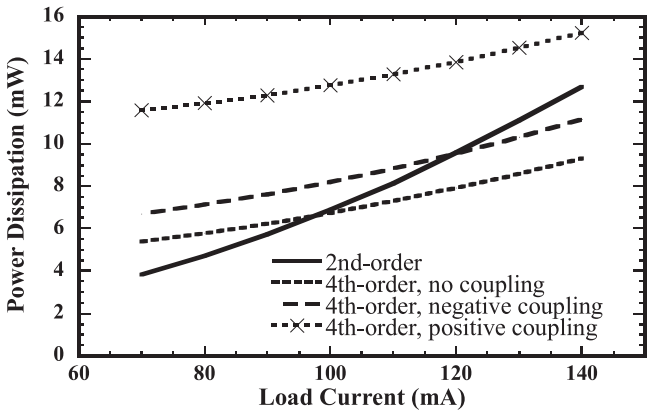


Fig. 5. Power dissipation of second-order filter versus fourth-order filter.

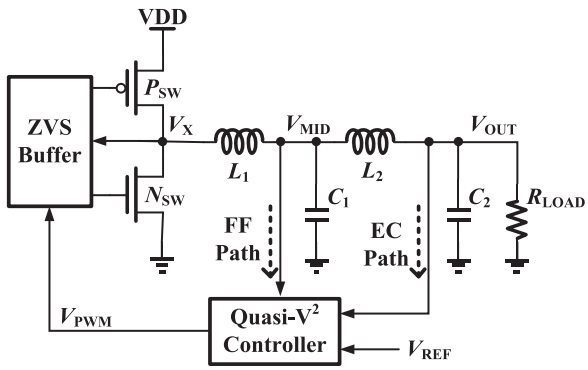


Fig. 6. System structure of the proposed buck converter with a fourth-order *LC* low-pass filter.

From the aforesaid observations, the following relations can be assumed for the second-order filter and the fourth-order filter with the same load current and the same ripple attenuation at f_S: $I_{DC1} = I_{DC0}$, $I_{AC1} = 2kI_{AC0}$, $R_{L1,DC} = R_{L2,DC} = R_{L0,DC}/(2k)$, and $R_{L1,AC}\<R_{L0,AC}/(2k)$. Then, from (10) and (11), it can be shown that the fourth-order filter is more power efficient than the second-order filter when

$$\frac{I_{DC1}^2 R_{L1,DC}}{I_{AC1}^2 R_{L1,AC}} > \frac{2k-1}{4k\,(k-1)}. \tag{12}$$

Therefore, if the load current is sufficiently high, it is more efficient to use the fourth-order filter. As an example, the second-order filter and the fourth-order filter discussed in Section II-A are simulated in a buck converter that operates at 450 MHz and produces an output voltage of 0.7 V from a 1-V supply. The power dissipation of each filter is evaluated at various load currents, and the results are displayed in Fig. 5. Compared with the second-order filter, the fourth-order filter becomes more efficient when the load current is greater than a threshold. In this example, when there is no coupling between L_1 and L_2, the threshold is 100 mA. The negative coupling between the inductors increases the ac power loss of L_1 and moves the threshold to 120 mA. In contrast, the positive coupling increases the ac power loss of both L_1 and L_2, and thus, it is undesirable.

The negative coupling between L_1 and L_2 demonstrates better attenuation and lower power loss than those with the positive coupling. Because the inductors are placed in a compact chip area, coupling between them is inevitable. Therefore, the inductors should be laid out to produce negative coupling for better efficiency and lower output voltage ripple. It is observed that in the negative coupling case, inductor L_2 contributes half of the dc power loss and less than 1% of the ac power loss. Thus, the size of L_2 can be lowered to reduce the total power loss and save silicon area while the achievable attenuation is still better than that of the second-order filter.

III. Fully Integrated Buck Converter

A fully integrated buck converter with a fourth-order *LC* low-pass filter is designed in a 65-nm CMOS process. The buck converter produces a nominal output voltage of 0.7 V from a 1-V supply. As shown in Fig. 6, the main components of the buck converter include power switches P_{SW} and N_{SW}, a zero-voltage-switching buffer, a fourth-order *LC* low-pass filter, and a quasi-V^2 controller.

A. On-Chip Fourth-Order LC Low-Pass Filter

Based on the analysis presented in Section II, a negative-coupling fourth-order *LC* filter is implemented to provide at least –40-dB attenuation at 450 MHz. The design in Section II gives –60 dB attenuation, as shown in Fig. 3, which is much more than needed; thus, instead of using 1.2 nH for both inductors, L_2 is decreased to 0.6 nH to lower its dc resistance. The total capacitance is maintained at 4 nF, with C_1 being 2.5 nF and C_2 being 1.5 nF. The capacitors are sized unevenly to assist the layout, and the ripple attenuation is slightly better than it is when

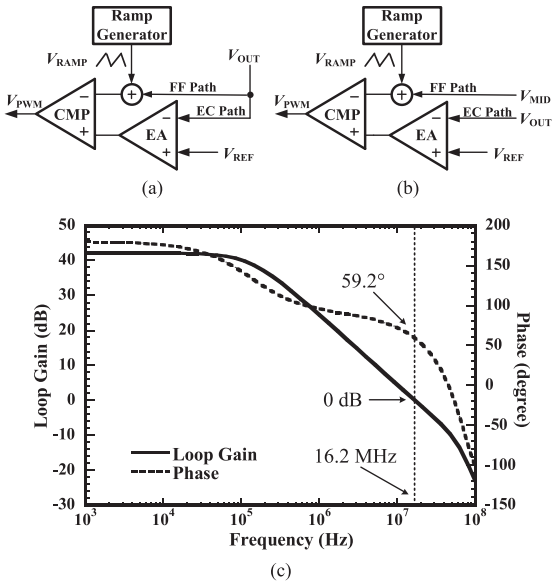


Fig. 7. (a) Basic structure of the conventional V^2 controller; (b) quasi-V^2 controller for use with the fourth-order *LC* filter; and (c) bode plot of the control loop of the proposed buck converter.

the capacitors are equal. Given these changes, an attenuation of –49 dB is obtained at 450 MHz. Capacitors C_1 and C_2 are implemented by a combination of metal-oxide-semiconductor capacitors and metal-oxide-metal capacitors, which together give a capacitance density of about 10 nF/mm^2.

B. Quasi-V^2 Controller

V^2 control has become very popular for point-of-load voltage regulators due to its simple implementation and fast load response [19]–[24]. In a conventional V^2 controller, the output voltage is fed back through a slow error-correction (EC) path and a fast feed-forward (FF) path [19], as shown in Fig. 7(a). In the slow EC path, a high-gain low-bandwidth error amplifier (EA) is used to regulate the dc output voltage to a reference voltage, which is similar to the operation of a voltage-mode controller. In the fast FF path, the output voltage ripple is used as a control signal of the PWM comparator (CMP), which is similar to the operation of other ripple-based control methods. Through the FF path, any load disturbance at the output voltage is reflected right at the input of the comparator CMP, bypassing the slow error-amplifier EA. As a result, the duty cycle is adjusted immediately, and the regulator can achieve fast load response.

For stability consideration, the EC path can be stabilized by using a sufficiently low-bandwidth EA, but the FF path may cause subharmonic oscillation similar to current-mode control approaches [21]—[26]. Thus, ramp compensation is needed in the FF path to achieve stable operation at duty cycle above 0.5 [27]. It is shown in [23] that ramp compensation may not be sufficient to ensure stability if the output capacitor has a low equivalent series resistance (ESR). Yet, the use of a high-ESR output capacitor is not attractive due to the corresponding large output voltage ripple [28]. Some solutions have been presented to enable low-ESR output capacitors in V^2 controllers, such as sensing the output capacitor current [24], differentiating the output voltage [29], and sensing the inductor current [30]; however, these require additional precision analog circuits.

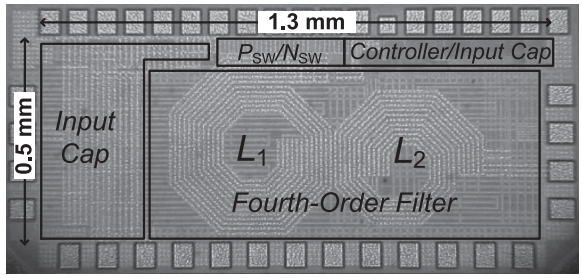


Fig. 8. Micrograph of the prototype of the proposed buck converter.

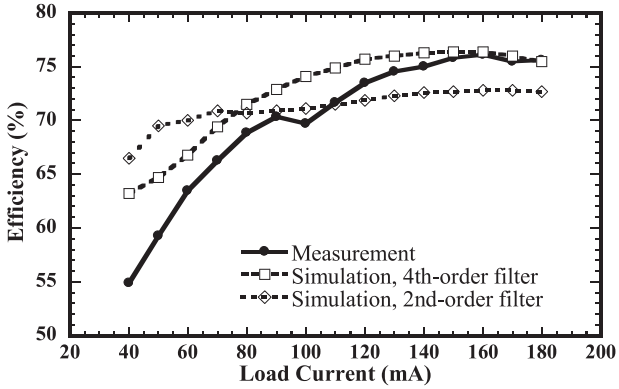


Fig. 9. Power efficiency of the proposed buck converter with the fourth-order *LC* low-pass filter.

In the proposed buck converter with the fourth-order *LC* low-pass filter, a quasi-V^2 controller is implemented, as shown in Fig. 7(b). Instead of $V_{\rm OUT}$, V_{MID} is fed back through the FF path. Since $V_{\rm MID}$ is further filtered by the L_2C_2 stage, it can tolerate large voltage ripple resulted from C_1 with a large series resistance. Therefore, ramp compensation is sufficient to ensure stability. Due to the small inductors and capacitors, the low-pass transfer function from $V_{\rm OUT}$ to $V_{\rm MID}$ has a high cutoff frequency, and a load disturbance can still be detected quickly at $V_{\rm MID}$. Thus, the quasi-V^2 controller can maintain a fast load response similar to that of the conventional V^2 controller while avoiding large output voltage ripple. The output voltage $V_{\rm OUT}$ is still fed back through the EC path. The error-amplifier EA in the EC path should be designed with high dc gain, to achieve accurate voltage regulation, and with low bandwidth, to ensure stability given the two double-pole pairs of the fourth-order filter. A Bode plot of the control loop is displayed in Fig. 7(c), demonstrating the system stability with 59.2° phase margin and 16.2-MHz bandwidth.

IV. Experiment Results

A proof-of-concept prototype of the proposed buck converter is fabricated in a 65-nm CMOS process with a thick top metal layer. Fig. 8 shows a micrograph of the chip with an area of 1.3 mm × 0.5 mm excluding pads. Fig. 9 shows the measured

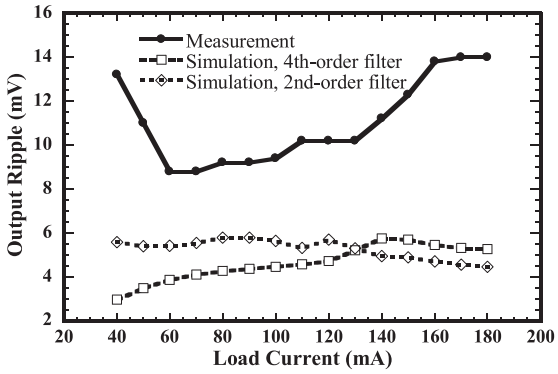


Fig. 10. Measured output voltage ripple of the proposed buck converter with the fourth-order *LC* low-pass filter.

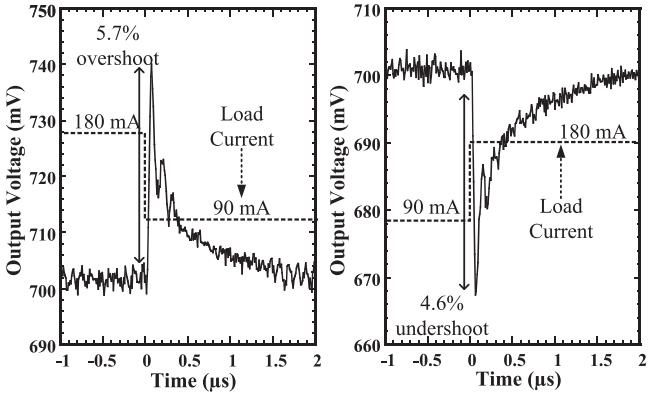


Fig. 11. Load response of the buck converter.

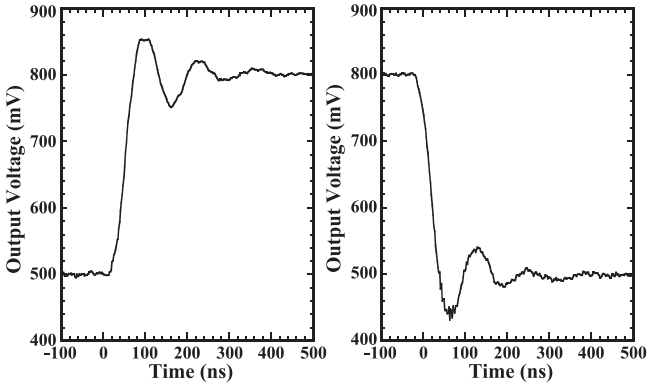


Fig. 12. Reference tracking performance of the buck converter.

and simulated efficiency of the proposed buck converter in comparison with the simulated efficiency of another buck converter that uses the second-order filter discussed in Section II (the latter will be referred to as "the second converter" for brevity). From simulation results, the proposed buck converter achieves better efficiency than that of the second converter when the load current is beyond 80 mA. This value corresponds to the load current threshold at which the fourth-order filter starts to dissipate less power than the second-order filter does. The measured efficiency of the proposed buck converter is observed to drop faster than the simulated efficiency at light load. However, it is still higher than that of the second converter when the load current is beyond 110 mA. Because the inductors are placed on top of the capacitors, it is challenging to accurately model the performance of the fourth-order *LC* filter by EM simulation. Smaller inductance and larger ac resistance should be expected from the real inductors, which cause larger voltage ripple, larger current ripple, and larger ac power dissipation than expected from simulation. As shown in Fig. 10, the measured peak-to-peak amplitude of the output voltage ripple is between 8 and 15 mV across the entire load range, whereas the simulated ripple is below 6 mV. Efficiency improvement at light load will be explored in future works. One potential solution is to add a light-load operating mode in which the fourth-order filter is reconfigured to a second-order filter operating at a lower switching frequency.

Fig. 11 shows the converter's transient response to load disturbance in both directions. The voltage drop under a load step from 90 to 180 mA is 4.6%, which is among the lowest values in comparison with prior-art fully integrated buck converters. Such a fast load response is delivered by the quasi-V^2 controller as well as the small inductors and capacitors of the fourth-order filter. Fig. 12 shows the reference tracking performance of the buck converter. The output voltage changes from 0.5 to 0.8 V within 60 ns, which is equivalent to an output voltage slew rate of 5 V/µs. Table II summarizes the performance of the proposed buck converter and compares it with previous designs. It is difficult to make a fair comparison of these works because of different process technologies and design specifications. However, it can be seen that the use of a fourth-order filter significantly reduces the output voltage ripple while requiring smaller passive components. Only the design in [9] has small output voltage ripple comparable to that of the proposed buck converter, but it uses 2.5× larger output capacitance and has a much smaller current density. Although the design in [2] features a higher output voltage slew rate, it requires an additional shunt regulator to quickly charge and discharge the output. In contrast, the

TABLE II
COMPARISON WITH PREVIOUS FULLY INTEGRATED BUCK CONVERTERS

	[2]	[7]	[8]	[9]	This Work
Process (nm)	130	130	130	22	65
Supply Voltage (V)	2.4	1.2	2–2.6	1.5	1
Output Voltage (V)	0.4–1.4	0.3–0.9	1.1–1.5	0.7–1.2	0.5–0.8
Frequency (MHz)	50–240	170	0.075–225	500	450
Filter Order	2	2	2	2	4
Total Ind. (nH)	4	4	15.6	1.5	1.8
Total Cap. (nF) [a]	28	5.2	12.2	10	4
Max Load (mA)	800	350	667	250	180
Max Power (mW)	1000	315	800	250	126
Output Ripple (mV)	<100	<40	<120	~10	8.5–14.5
Output Slew Rate (V/µs)	50 [b]	N/A	N/A	1.5 [c]	5
Output Voltage Droop (%)	7.5 [b]	15	N/A	N/A	4.6
Area (mm^2)	5	1.5	3.76	1.5	0.65
Current Density (mA/mm^2)	160	233	177	167	276
Power Density (mW/mm^2)	200	210	213	167	194
Eff. @ Max Power (%)	63	76	48	N/A	74.5
Peak Eff. (%)	77	77.9	58	68	76.1

[a] Excluding input decoupling capacitor.
[b] With shunt regulator [2].
[c] 150-mV voltage step with 100-ns rise time [9].

proposed buck converter can achieve fast reference tracking mainly due to the high slew rates associated with the small inductors and capacitors in the fourth-order filter. The load response of the proposed buck converter is the fastest for a 2× load step. The peak power efficiency is slightly lower than those reported in [2] and [7]; however, the current density is about 72% and 18% higher than the values reported in [2] and [7], respectively.

V. Conclusion

In the context of buck converter design, using a fourth-order *LC* low-pass filter instead of a second-order *LC* low-pass filter can provide better ripple attenuation while requiring smaller inductors and capacitors. This characteristic is of high interest to the design of fully integrated buck converters with on-chip planar spiral inductors. Smaller inductors can be designed with smaller series resistance, which leads to better power efficiency at high load current. At the same time, smaller passive components feature larger current and voltage slew rates, thus delivering faster transient response to load disturbance and reference transition. A fully integrated buck converter with a quasi-V^2 controller has been designed to take advantage of the characteristics of the fourth-order *LC* low-pass filter. From measurement results, as expected, the proposed buck converter demonstrates low output voltage ripple, fast transient response, high current density, high power density, and high power efficiency.

References

[1] W. Kim, M. S. Gupta, G.-Y. Wei, and D. Brooks, "System level analysis of fast, per-core DVFS using on-chip switching regulators," in *Proc. IEEE 14th Int. Symp. High Perform. Comput. Archit.*, 2008, pp. 123–134.

[2] W. Kim, D. Brooks, and G. Y. Wei, "A fully-integrated 3-level DC–DC converter for nanosecond-scale DVFS," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 206–219, Jan. 2012.

[3] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA, USA: Kluwer, 2001.

[4] P. Hazucha *et al.*, "A 233-MHz 80%-87% elfficient four-phase DC–DC converter utilizing air-core inductors on package," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 838–845, Apr. 2005.

[5] M. Alimadadi *et al.*, "A fully integrated 660 MHz low-swing energy-recycling DC–DC converter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1475–1485, Jun. 2009.

[6] C. Huang and P. K. T. Mok, "A 100 MHz 82.4% efficiency package-bondwire based four-phase fully-integrated buck converter with flying capacitor for area reduction," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 2977–2988, Dec. 2013.

[7] J. Wibben and R. Harjani, "A high-efficiency DC–DC converter using 2 nH integrated inductors," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 844–854, Apr. 2008.

[8] M. Wens and M. S. J. Steyaert, "A fully integrated CMOS 800-mW four-phase semiconstant ON/OFF-time step-down converter," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 326–333, Feb. 2011.

[9] H. K. Krishnamurthy *et al.*, "A 500 MHz, 68% efficient, fully on-die digitally controlled buck voltage regulator on 22 nm tri-gate CMOS," in *Proc. IEEE VLSI Circuits Symp. Dig. Tech. Papers*, 2014, pp. 210–211.

[10] F. Neveu, B. Allard, C. Martin, P. Bevilacqua, and F. Voiron, "A 100 MHz 91.5% peak efficiency integrated buck converter with a three-MOSFET cascode bridge," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 3985–3988, Jun. 2016.

[11] J. Murray, N. Tang, P. P. Pande, D. Heo, and B. A. Shirazi, "DVFS pruning for wireless NoC architectures," *IEEE Des. Test*, vol. 32, no. 2, pp. 29–38, Mar./Apr. 2015.

[12] M. Wens and M. Steyaert, "A fully-integrated 0.18um CMOS DC–DC step-down converter, using a bondwire spiral inductor," in *Proc. 30th IEEE Custom Integr. Circuits Conf.*, 2008, pp. 17–20.

[13] N. Sturcken *et al.*, "A 2.5D integrated voltage regulator using coupled-magnetic-core inductors on silicon interposer," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 244–254, Jan. 2013.

[14] R. X. Wu and J. K. O. Sin, "High-efficiency silicon-embedded coreless coupled inductors for power supply on chip applications," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4781–4787, Nov. 2012.

[15] C. H. Chia, R. C. H. Chang, P. S. Lei, and H. M. Chen, "A two-phase fully-integrated DC–DC converter with self-adaptive DCM control and GIPD passive components," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3252–3261, Jun. 2015.

[16] D. Goder and W. R. Pelletier, "V^2 architecture provides ultra-fast transient response in switch mode power supplies," in *Proc. High Frequency Power Convers. Conf.*, 1996, pp. 19–23.

[17] S. S. Mohan, M. D. Hershenson, S. P. Boyd, and T. H. Lee, "Simple accurate expressions for planar spiral inductances," *IEEE J. Solid-State Circuits*, vol. 34, no. 10, pp. 1419–1424, Oct. 1999.

[18] W. B. Kuhn and N. M. Ibrahim, "Analysis of current crowding effects in multiturn spiral inductors," *IEEE Trans. Microwave Theory Techn.*, vol. 49, no. 1, pp. 31–38, Jan. 2001.

[19] S. Qu, "Modeling and design considerations of V^2 controlled buck regulator," in *Proc. IEEE 16th Annu. Appl. Power Electron. Conf. Expo.*, 2001, pp. 507–513.

[20] J. Cortes, V. Svikovic, P. Alou, J. A. Oliver, and J. A. Cobos, "V^1 Concept: Designing a voltage-mode control as current mode with near time-optimal response for buck-type converters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5829–5841, Oct. 2015.

[21] S. L. Tian, F. C. Lee, Q. Li, and Y. Y. Yan, "Unified Equivalent circuit model and optimal design of V^2 controlled buck converters," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1734–1744, Feb. 2016.

[22] S. L. Tian, F. C. Lee, P. Mattavelli, K. Y. Cheng, and Y. Y. Yan, "Small-signal analysis and optimal design of external ramp for constant on-time V^2 control with multilayer ceramic caps," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4450–4460, Aug. 2014.

[23] S. L. Tian, F. C. Lee, P. Mattavelli, and Y. Y. Yan, "Small-signal analysis and optimal design of constant frequency V^2 control," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1724–1733, Mar. 2015.

[24] Y. Yan, P. Liu, F. C. Lee, Q. Li, and S. Tian, "V^2 control with capacitor current ramp compensation using lossless capacitor current sensing," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 117–124.

[25] T. Qian and W. Wu, "Analysis of the ramp compensation approaches to improve stability for buck converters with constant on-time control," *IET Power Electron.*, vol. 5, pp. 196–204, 2012.

[26] J. Cortes *et al.*, "Design-oriented stability criteria of a V^2 control compensated with inductor current of a boost converter for shipboard power systems," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 2892–2897.

[27] J. Sun, "Characterization and performance comparison of ripple-based control for voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 346–353, Mar. 2006.

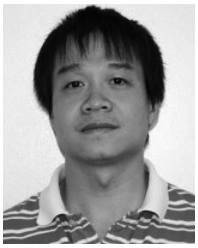
[28] C. H. Tsai, S. M. Lin, and C. S. Huang, "A fast-transient quasi-V^2 switching buck regulator using AOT control with a load current correction (LCC) technique," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3949–3957, Aug. 2013.

[29] Y. Y. Mai and P. K. T. Mok, "A constant frequency output-ripple-voltage-based buck converter without using large ESR capacitor," *IEEE Trans. Circuits Syst. II,Express Briefs*, vol. 55, no. 8, pp. 748–752, Aug. 2008.

[30] F. Su and W.-H. Ki, "Digitally assisted quasi-V^2 hysteretic buck converter with fixed frequency and without using large-ESR capacitor," in *Proc. IEEE Int. Solid-State Circuits Conf.—Dig. Tech. Papers*, 2009, pp. 445–447.

Nghia Tang (M'10) received the B.S. degree in electrical engineering, in 2009, from Washington State University, Pullman, WA, USA, where he is currently working toward the Ph.D. degree in electrical engineering.

His doctoral research primarily focuses on power management integrated circuits. He has been involved in the design of envelope tracking supply modulators for power amplifiers, fully integrated voltage regulators, and energy harvesting systems. He has served as an IC design intern at several companies, including Tagore Technology, Silicon Labs, and Texas Instruments.

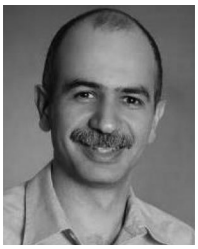


Bai Nguyen (S'13) received the B.S. degree in electronics and telecommunication from Vietnam National University, Hanoi, Vietnam, in 2005, and the M.S. degree in electrical and computer engineering from Chungbuk National University, Cheongju, Korea, in 2008. Since 2013, he has been working toward the Ph.D. degree in electrical engineering at Washington State University, Pullman, WA, USA.

He was a Research Assistant at the Institute of Material Science, Vietnam Academy of Science and Technology, a Design Engineer at Emerson Network Power, a Hardware Manager at Innova Electronics, and a Senior Researcher at Viettel R&D Institute, Viettel Group. His research interests include analog integrated circuit design for power conversion and management, emphasizing on high-efficiency switching regulator, fully integrated dc–dc converter, wireless power transfer, and energy harvesting.

Reza Molavi (S'03–M'14) received the B.Sc. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 2003 and the M.Sc. and Ph.D. degrees from the University of British Columbia (UBC), Vancouver, BC, Canada, in 2005 and 2013, respectively.

From 2007 to 2013, he was a Mixed-Signal Design Engineer with PMC-Sierra, Burnaby, BC, where he was involved in the design of several high-performance clocking and transciever buiding blocks for multigigabit serial data links and wireless chip products. He is currently a Postdoctoral Fellow and Lecturer in the Electrical and Computer Engineering Department, UBC. He received the Best Paper Finalist award in the IEEE Canadian Conference on Electrical and Computer Engineering, Montreal, QC, Canada, 2012 and the co-received the Best Student Paper Award of the 2015 Radio-Frequency Integrated Circuit Symposium. His research interests include the modeling and design of high-frequency analog and mixed-signal circuits in CMOS technology.



Shahriar Mirabbasi (M'02) received the B.Sc. degree in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 1990, and the M.A.Sc. and Ph.D. degrees in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 1997 and 2002, respectively.

Since 2002, he has been in the Department of Electrical and Computer Engineering, University of British Columbia, Vancouver, BC, Canada, where he is currently a Professor. His current research interests include analog, mixed-signal, RF, and mm-wave integrated circuit and system design with a particular emphasis on communication, sensor interface, power management, and biomedical applications.

Yangyang Tang (S'12-M'15) received the M.S. degree in research of I-MARS, and the Ph.D. degree in electronics and information engineering from the Université de Bretagne Sud, Lorient, France, in October 2009 and January 2013, respectively.

He was a Visiting Scholar from June 2011 to June 2012 in the Low-Energy/Fault-Tolerant Systems Laboratory, Utah State University. His previous research interests included EC circuit design and fault-tolerant featured hardware architecture for contemporary digital logic or nanoelectronics. After finishing the Ph.D. degree, he joined the Research Department of HiSilicon, Huawei, Shenzen, as a Senior Research Engineer, in July 2013. Since then, his research interests are in the area of low-power circuit design, dc–dc converter, low-dropout regulator (LDO), and ultra-low power circuit design. He has published over ten technical papers and has more than ten issued and nine pending patents.

Dr. Tang received the Hisilicon President's Award in 2015.

Philipp Zhang (Chen-Xiong Zhang) (M'86) received the B.S. degree in electrical engineering from Shanghai Jiao-Tong University, Shanghai, China, and the M.S. and Ph.D. degrees in electrical engineering from the University of Karlsruhe (now Karlsruhe Institute of Technology, KIT), Karlsruhe, Germany.

In 1983, he joined the Institute for Theoretical Electrical Engineering at the University of Karlsruhe, where he was involved in teaching and research activities in very large scale integration layout and circuit design. From 1991 to 1995, he was with SIEMENS Microelectronic Center, Hamburg, Germany, where he was involved in research and development of ATM broadband networks and ASIC design for telecom application. He was involved in the R&D of Advanced Communication technologies in Europe project. In 1995, he transferred to Interphase Corp., Dallas, TX, USA, and was in charge of development of communication chipsets and systems. After then, he has worked in a couple of start-up companies as CEO/CTO in the USA and in China in the area of wireless and broadband communications. He joined Huawei Technologies, Plano, TX, USA, as a Chief Scientist in 2005 and is currently in charge of corporate research programs and projects.

Jonghoon Kim received the Ph.D. degree in biomechatronics engineering from Sungkyunkwan University, Seoul, Korea, in 1997.

He is currently a Principle Researcher of smart distribution system at the Korea Food Research Institute, Sungnam, Korea.

Partha Pratim Pande (S'05–M'05–SM'11) is currently a Professor and the Boeing Centennial Chair in computer engineering in the School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA, USA. His current research interests include novel interconnect architectures for manycore chips, on-chip wireless communication networks, and hardware accelerators for biocomputing.

Dr. Pande currently serves as the Editor-in-Chief of the IEEE TRANSACTIONS ON MULTI-SCALE COMPUTING SYSTEMS (TMSCS) and an Associate Editor-in-Chief of the IEEE DESIGN AND TEST (D&T). He is on the editorial boards of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGERS (TVLSI), the *ACM Journal of Emerging Technologies in Computing Systems (JETC)*, and *Sustainable Computing: Informatics and Systems (SUSCOM)*.

Deukhyoun Heo (S'97–M'00–SM'13) received the B.S.E.E. degree in electrical engineering from Kyoungpuk National University, Daegu, Korea, in 1989, the M.S.E.E degree in electrical engineering from Pohang University of Science and Technology, Pohang, Korea, in 1997, and the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2000.

In 2000, he joined the National Semiconductor Corporation, where he was a Senior Design Engineer involved in the development of silicon RFICs for cellular applications. Since 2015, he has been a Professor in the Electrical Engineering and Computer Science Department, Washington State University, Pullman, WA, USA. He has primary been interested in RF/microwave/opto transceiver design based on CMOS, SiGe BiCMOS, and GaAs technologies for wireless and wireline data communications, batteryless wireless sensors, and intelligent power management systems for sustainable energy sources, adaptive beam former for phased-array communications, low-power high date-rate wireless links for biomedical applications, and multilayer module development for system-in-package solutions.

Dr. Heo has been a Member of the Technical Program Committee of IEEE Microwave Theory and Techniques Society International Microwave Symposium and the International Symposium of Circuit and Systems. He has served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS (2007-2009) and has served as an Associate Editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. He received the 2009 National Science Foundation CAREER Award.