# Flexible Mode Bridgeless Boost PFC Rectifier With High Efficiency Over a Wide Range of Input Voltage

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***Abstract*—For the conventional PFC rectifiers, the high efficiency cannot be achieved over a wide input range, and the efficiency will be greatly decreased at low-input voltages. In order to overcome the efficiency bottleneck under low-line input, a flexible mode bridgeless boost power factor correction (PFC) rectifier is proposed in this paper. According to the input voltage, the proposed rectifier can be flexibly adapted to the suitable operating mode to obtain the maximum efficiency. Meanwhile, the circuit components can be reused by different operating modes, so the extra cost is low. In the proposed rectifier, a back-to-back bridgeless boost PFC topology is adopted at high-line conditions and a three-level bridgeless boost PFC topology is rebuilt to reduce the switching losses at low-line conditions. Compared with the traditional bridgeless boost PFC rectifier, an extra low-voltage bidirectional switch (usually composed of two switches) is added, so the increased cost is low. In addition, the low common-mode noise can be achieved at both high- and low-line conditions due to the direct connection between the input mains and the output electrolytic capacitor. The detailed principle analysis about the proposed rectifier is presented in this paper. Finally, an experimental prototype is built to verify the feasibility and the effectiveness of the proposed topology.**

***Index Terms*—Bridgeless power factor correction (PFC), flexible mode, high efficiency, low common-mode noise.**

## I. Introduction

In order to meet the harmonic regulations and standards, such as the IEC 610000-3-2 [1], the power supplies with active power factor correction (PFC) feature are required for various types of electronic equipment. Meanwhile, the increasing requirements of high efficiency have been forcing the designers to look for any potential opportunities to reduce the converter losses. The most common solution is the conventional PFC rectifier shown in Fig. 1 which is widely used for various kinds of computers, workstations, servers, etc [2], [3]. However, it suffers from high conduction losses since the input current always flows through two bridge diodes and a power switching device. Besides, the efficiency decrease caused by conduction losses is more obvious when the input line voltage is low, which usually leads to low power density since a large heat sink is needed.

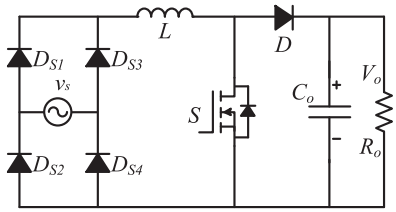


Fig. 1. Traditional full-bridge PFC converter.

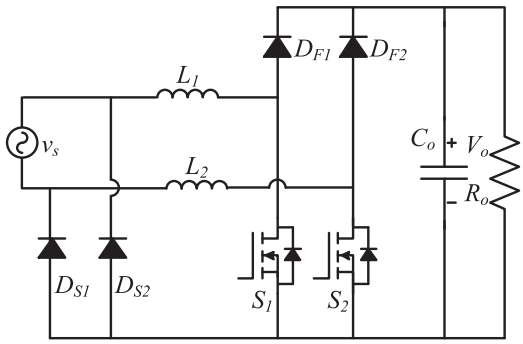


Fig. 2. DDBL PFC rectifier.

In order to overcome the shortcomings of the conventional PFC converter, many researchers have made great efforts to develop the bridgeless boost PFC rectifiers which can achieve higher efficiency by reducing the number of power components in the line current path [4]–[9], [11]–[13]. In these boost bridgeless PFC rectifiers, the most practical and potential topologies are the dual-boost bridgeless PFC rectifier (DBBL PFC) shown in Fig. 2 and the back-to-back bridgeless PFC rectifier (BTBBL PFC) shown in Fig. 3 since both of them have lower common-mode (CM) noise interference and better reliability compared with the others. Nevertheless, it can be noted that the magnetic core utilization is low for the DBBL PFC rectifier. Although a multiple winding, multicore inductor can be used to improve the utilization of the magnetic material [9], the efficiency of the rectifier is also reduced, which is not expected. For the above two rectifiers, the high efficiency can be achieved when the input voltage is high (rating value

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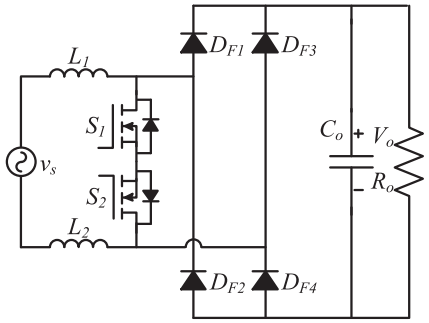


Fig. 3. Symmetrical BTBBL PFC.

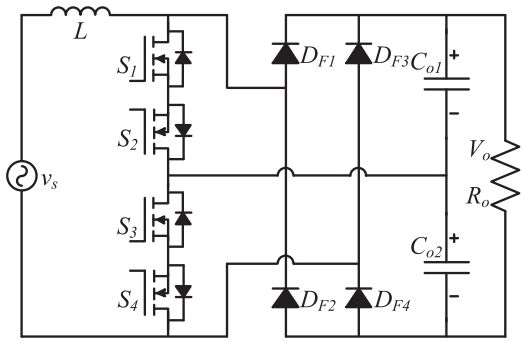


Fig. 4. Improved three-level boost PFC rectifier.

is 220–240 Vrms). If the input voltage decreases, the total conduction and switching losses although are reduced than the topology shown in Fig. 1, however are still high with the increase of input current, the efficiency under low-input voltages is still much lower than that under high-input voltages.

It seems to be much difficult to further reduce the conduction losses for the bridgeless PFC rectifiers, so many bridgeless PFC rectifiers have been modified to improve the efficiency via soft switching techniques. According to the ways of realizing soft switching, these modified PFC rectifiers can be divided into several groups. The first group adopts the discontinuous-current mode (DCM) or critical-current mode (CRM) instead of continuous-current mode [9], [14]–[17]. The rectifiers working in DCM or CRM mode are only suitable for low-power applications ($<$300 W) due to the restriction of switch current stress. Additionally, a large input filter must be employed to suppress the high-frequency components of the pulsating input current, which increases the overall volume and cost of the rectifier. The second group involves adding some auxiliary components (including the capacitors, inductors, and active switches) to the traditional bridgeless PFC rectifiers [18]–[21], which usually makes the circuit more complex and decreases the reliability of system. Besides, the voltage or current stress of the power devices is also significantly increased due to the resonance between the capacitors and inductors. That is, the higher-rated or, usually, more expensive components are needed.

Another common solution to improve the efficiency is to adopt multilevel converters which have the advantages of small inductor size, low switching losses, low device stress, etc. Based on the full-bridge PFC converter shown in Fig. 1, a traditional three-level boost converter is proposed [22], which suffers from high conduction losses due to the diode bridge. So an improved three-level PFC rectifier shown in Fig. 4 is developed to reduce the conduction losses [23]–[25] and the high efficiency can be achieved. Recently, several new three-level single-phase bridgeless PFC rectifiers are presented in [26], which have lower conduction losses than Fig. 4. However, many extra power devices and high-side drivers are needed for those complicated circuits proposed in [26]. On the other hand, the advantage of low CM noise in the previous two-level bridgeless PFC rectifiers is lost for all of the three-level rectifiers mentioned above since the voltage potential of the output bus in regard to the ground is pulsating.

A new concept of flexible converter is proposed in [27]. There are two or more topologies or operating modes involved in a flexible converter, where different topologies are formed for different applications. In order to solve the problem of low efficiency at low input for the rectifier, a flexible mode bridgeless boost PFC (FMBL PFC) converter is proposed based on the flexible converter concept. The basic design principle can be concluded as follows. According to the input voltage, the rectifier can be flexibly adapted to the suitable topology and mode for obtaining the maximum efficiency. Meanwhile, in order to reduce the extra cost, the circuit components should be reused as much as possible in different topologies and modes.

Based on this idea, a novel FMBL PFC rectifier is proposed, in which the high efficiency over a wide input range can be achieved. In the proposed rectifier, a BTBBL PFC rectifier is adopted at high-line voltages and a three-level bridgeless boost PFC rectifier (TLBL PFC) is formed to achieve high efficiency at low-line voltages. Compared with the traditional bridgeless boost PFC rectifier, an extra low-voltage bidirectional switch (usually composed of two switches) is added, therefore the increased cost is low. At both high- and low-line conditions, the low CM noise can be achieved due to the direct connection between the input power grid and the output electrolytic capacitor during half-line cycle. The detailed principle analysis about the proposed FMBL PFC rectifier is presented. Finally, an experimental prototype is built to verify the feasibility and the effectiveness of the proposed topology.

## II. Derivation of the Novel Proposed Topology and the Operating Principle

### A. Derivation of the Novel Proposed Topology

Fig. 5 shows the asymmetrical BTBBL PFC rectifier, which is a little different from the symmetrical one shown in Fig. 3. In the symmetrical BTBBL PFC rectifier, two identical inductors are adopted to make the circuit look symmetrical because the symmetrical circuit has a better capability to suppress the CM noise [11], [12]. However, four fast recovery diodes are needed in the symmetrical topology, which increases the cost. Therefore, an asymmetrical structure with single inductor $L$ shown in Fig. 5 is used here. From Fig. 5, it can be seen that the diodes in two half bridges are different: the half bridge connected to the inductor $L$ is made up of two fast recovery diodes and the other one connected to the input mains $v_s$ is made up of two slow

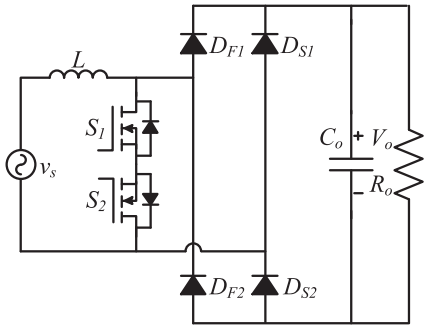


Fig. 5. Asymmetrical BTBBL PFC rectifier.

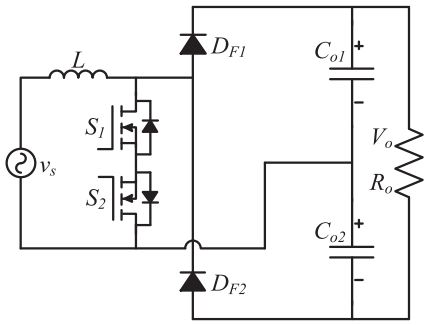


Fig. 6. TLBL PFC rectifier.

diodes. When the fast recovery diode and the slow diode are in series, the switching characteristic is determined by the fast recovery diode and the slow diode can be treated as short-circuit, which will be analyzed in the next section. Therefore, one end of the input power supply is always directly connected to the positive terminal of the output capacitor $C_o$ in the negative half-line cycle or the negative terminal of $C_o$ in the positive half-line cycle. Then, the CM noise is reduced effectively. The high efficiency under high-input voltages for the BTBBL PFC rectifier can be achieved. However, it suffers from low efficiency due to the rapid increase of switching losses and conduction losses under low-input voltages.

Fig. 6 shows the topology of a TLBL PFC rectifier whose structure is simple. The TLBL PFC rectifier has the following merits:

First, there are fewer semiconductor components in the current path. When the bidirectional switch $\mathrm{S_1S_2}$ is turned OFF, there is only one fast diode to carry the current in the TLBL PFC, while two diodes in the BTBBL PFC and DBBL PFC.

Second, low-voltage MOSFETs can be used in the TLBL PFC rectifier. For the same input current $i_L$, the switching losses in the TLBL PFC are less than that in the BTBBL PFC and DBBL PFC. In addition, if the same filter inductor is used, the operating frequency of the TLBL PFC rectifier can be reduced for the same current ripple requirement, which means the switching losses can be decreased further.

According to above analysis, the TLBL PFC should be more attractive for the industry applications. The efficiency can be increased with low-input voltage, such as 110-Vrms input and 400-Vdc output. However, when the input voltage rises, such as reaching the rating grid voltage 220 Vrms, the expected 400 Vdc cannot be achieved by using TLBL PFC. It can be seen that the input voltage limit of TLBL PFC comes from the use of half bridge, which limits its wide application.

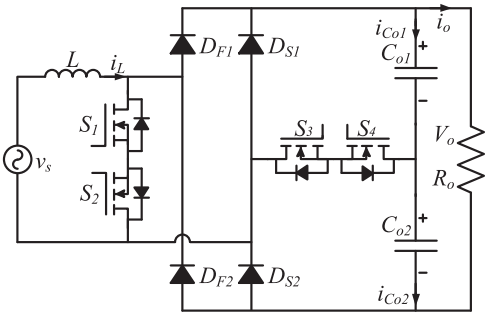


Fig. 7. Proposed FMBL PFC rectifier.

From the above analysis, the DBBL PFC and BTBBL PFC can work in a wide range of input voltage but suffer from low efficiency at low-line conditions; the TLBL PFC can achieve high efficiency, but cannot work under high-line conditions. In order to achieve high efficiency over a wide input voltage range, a potential solution is to extend the input voltage range of TLBL PFC by disconnecting the midpoint of the half bridge from the negative terminal of input supply and adding some components to convert the TLBL PFC into DBBL PFC or BTBBL PFC. That is, a flexible mode PFC rectifier is expected to be developed which can be flexibly adapted to the suitable topology and operating mode according to the input voltage.

Fortunately, the BTBBL PFC shown in Fig. 5 and the TLBL PFC shown in Fig. 6 look similar to each other, which makes it possible to combine them into a new topology. On the basis of the BTBBL PFC rectifier, an extra bidirectional switch (composed of two switches) is added to connect the drain of MOSFET $\mathrm{S_2}$ to the midpoint of the output capacitors. Therefore, a novel topology is constructed as shown in Fig. 7, which is the proposed FMBL PFC rectifier. In Fig. 7, $\mathrm{S_1S_2}$ and $\mathrm{S_3S_4}$ are two bidirectional switches; $D_{F1}$ and $D_{F2}$ are fast recovery diodes; $D_{S1}$ and $D_{S2}$ are slow diodes; $L$ is the input filter inductor; $C_{o1}$ and $C_{o2}$ are the output split capacitors ($C_{o1} = C_{o2} = C_o$); $R_o$ is the load resistance; and $v_s$ is the input line voltage and $V_o$ is the output voltage ($V_o = 2V_{C_{o1}} = 2V_{C_{o2}}$).

It is important to note that the voltage stress of MOSFETs $\mathrm{S_3}$ and $\mathrm{S_4}$ is only half of the output dc voltage. Therefore, low-voltage MOSFETs can be adopted here to reduce the extra conduction losses. For example, the MOSFET with breakdown voltage 250 V can be used for the output voltage 400 Vdc, and its conduction resistance is only 20 $m\Omega$. That is, the total conduction resistance of the bidirectional switch $\mathrm{S_3S_4}$ is only 40 $m\Omega$ and the voltage drop across $\mathrm{S_3S_4}$ is usually less than a diode forward voltage drop.

### *B. Operating Principle*

There are usually two typical line voltages (100–120 and 220–240 Vrms) around the world. The proposed FMBL PFC can be simply treated as two independent boost PFC circuits according to the line voltage. If the line voltage is within the range of 100–120 Vrms, the bidirectional switch $\mathrm{S_3S_4}$ is turned ON, the FMBL PFC is adapted to a TLBL PFC (referred as "TLBL mode") which can promote the efficiency by reducing

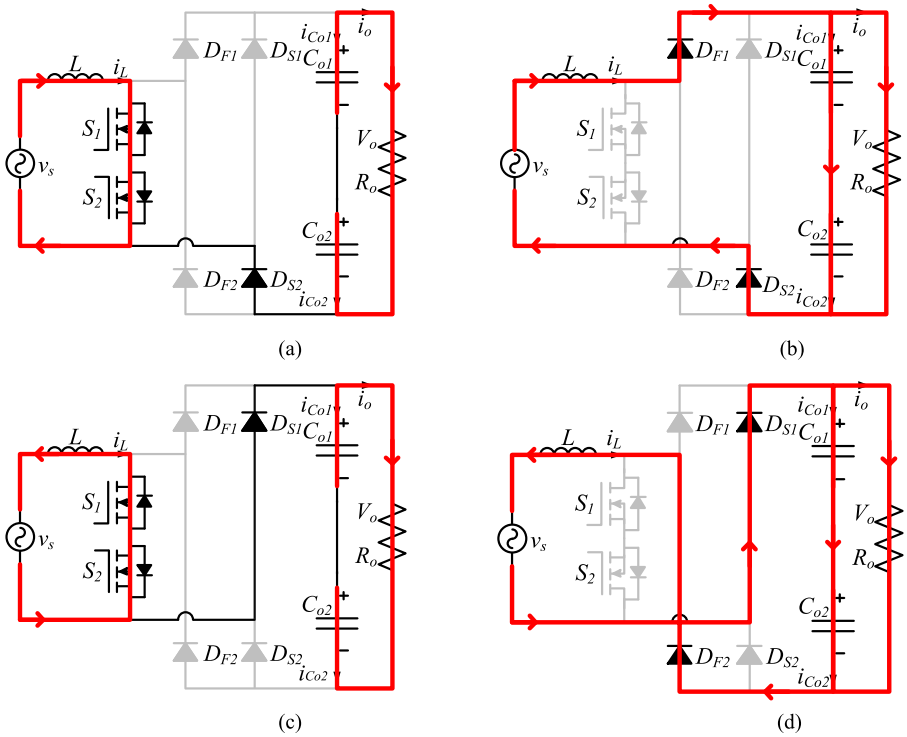


Fig. 8. Working principle of the FMBL PFC rectifier when the bidirectional switch $S_3S_4$ is in the OFF state under high-input voltage. (a) $v_s > 0$ and $S_1S_2$ is turned ON; (b) $v_s > 0$ and $S_1S_2$ is turned OFF; (c) $v_s < 0$ and $S_1S_2$ is turned ON; and (d) $v_s < 0$ and $S_1S_2$ is turned OFF.

the switching losses. If the line voltage is within the range of 220–240 Vrms, the bidirectional switch $S_3S_4$ is always turned OFF. Therefore, the proposed FMBL PFC is the same as the BTBBL PFC (referred as "BTBBL mode").

For the convenience of analysis, it is assumed that the output capacitors $C_{o1}$ and $C_{o2}$ are large enough, and all the semiconductor devices are ideal. The output voltages $V_o$, $V_{C_{o1}}$, and $V_{C_{o2}}$ can be considered as constants. If the peak input voltage of $v_s$ is larger than half of the expected output voltage $V_o$, the bidirectional switch $S_3S_4$ is always kept in the OFF state. Fig. 8 gives the detailed working processes in terms of the input state of FMBL PFC. For the positive half-line cycle, the corresponding operating modes are described by Fig. 8(a) and (b). When the bidirectional switch $S_1S_2$ is turned ON as shown in Fig. 8(a), the input inductor $L$ accumulates energy and the capacitors $C_{o1}$ and $C_{o2}$ provide power to the load $R_o$

$$v_s = L\frac{di_L}{dt}. \tag{1}$$

When the bidirectional switch $S_1S_2$ is turned OFF as shown in Fig. 8(b), the inductor releases its stored energy to the output capacitors $C_{o1}$, $C_{o2}$ and the load resistor $R_o$ through the bridge diodes $D_{F1}$ and $D_{S2}$

$$v_s = L\frac{di_L}{dt} + V_o. \tag{2}$$

Due to the fact that the reverse-recovery characteristic of the diodes in series is determined by the fast diode, the fast diode $D_{F1}$ withstands all of the reverse voltage $V_o$ when the diodes connected in series are turned OFF. The voltage across the slow diode $D_{S2}$ stays zero during the switching process so $D_{S2}$ can be treated as short circuit. The negative end of the input line is always connected to the negative terminal of the output capacitor $C_{o2}$. Therefore, the CM noise is reduced significantly. For the negative half-line cycle, the corresponding operating modes for FMBL PFC are shown in Fig. 8(c) and (d), which are similar with the positive half-line cycle.

If the peak input voltage of $v_s$ is less than half of the expected output voltage $V_o$, the bidirectional switch $S_3S_4$ is always kept in the ON state and the FMBL PFC works in TLBL mode. Fig. 9 gives the detailed working processes according to the polarity of the input line voltage $v_s$. As can be seen from Fig. 9(a) and (b), the inductor $L$ accumulates energy when the bidirectional switch $S_1S_2$ is turned ON, and releases its stored energy to the load and the capacitor $C_{o1}$ through the fast diode $D_{F1}$ when the bidirectional switch $S_1S_2$ is turned OFF

$$\begin{cases} v_s = L\frac{di_L}{dt}, & S_1S_2 \text{ is ON} \\ v_s = L\frac{di_L}{dt} + V_{C_{o1}}, & S_1S_2 \text{ is OFF.} \end{cases} \tag{3}$$

Since the bidirectional switch $S_3S_4$ is always kept in the ON state, the midpoint of output capacitors is directly connected to the negative end of the input line, which means low common noise can be realized. For the negative half-line cycle, the converter operates in a similar way with the positive half-line cycle.

### C. System Modeling and Controller Designing

According to the analysis above, the working processes of the proposed FMBL PFC rectifier are almost identical to the traditional boost PFC converter, so the open-loop transfer function

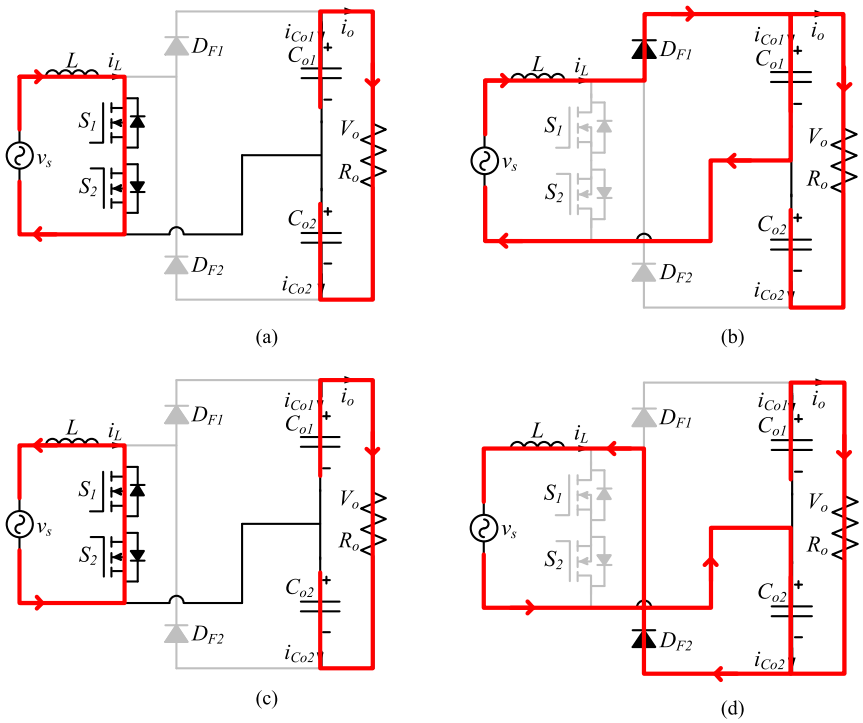


Fig. 9. Working principle of the FMBL PFC rectifier when the bidirectional switch $S_3S_4$ is in the ON state under low-input voltage. (a) $v_s > 0$ and $S_1S_2$ is turned ON; (b) $v_s > 0$ and $S_1S_2$ is turned OFF; (c) $v_s < 0$ and $S_1S_2$ is turned ON; (d) $v_s < 0$ and $S_1S_2$ is turned OFF.

of the circuit can be described as follows:

$$G_o(s) = \frac{i_L(s)}{d(s)} = \frac{V}{sL} \tag{4}$$

where $V$ equals $V_o$ when the bidirectional switch $S_3S_4$ is in the OFF state and $V_o/2$ when $S_3S_4$ is in the ON state.

If the zero-order hold (ZOH, referred as $G_{\mathrm{ZOH}}(s)$) is incorporated with (4), the discrete $z$-domain transfer function of the system is derived as

$$G_o(z) = \boldsymbol{Z}\{G_{\mathrm{ZOH}}(s)\,G_o(s)\} = \frac{V}{L}\frac{T_s}{z-1} \tag{5}$$

where $T_s$ is the calculating period and $G_{\mathrm{ZOH}}(s) = (1 - e^{-sT_s})/s$. $\boldsymbol{Z}\{G(s)\}$ is to obtain the $z$-transform of $G(s)$.

Based on (5), a controller can be designed for the system. The controllers used for the traditional PFC converters, such as the PI controller and the plug-in repetitive controller [13], can also be used.

## III. Analysis of Performance Evaluation and Design of Parameter

### A. Reverse-Recovery Characteristics of Diodes in Series

Zang *et al.* [10] give a detailed description about the MOSFET body diode's reverse recovery when the body diode is in series with a fast diode. The performance of MOSFET parasitic body diode is similar to a normal diode in a bridge rectifier, so the same analytical method can also be used here.

For the FMBL PFC rectifier working in BTBBL mode, the currents that flow through the fast diode $D_{F1}$ (referred as $i_F$) and the slow diode $D_{S2}$ (referred as $i_S$) during the discharge of the inductor are always identical and equal to the inductor current $i_L$. A simple equivalent circuit is given in Fig. 10(a). At the end of discharge, the current that flows through these two diodes is commutated to the bidirectional switch $S_1S_2$ and Fig. 10(b) gives the corresponding commutation process. A detailed description about the process can be got in [10], and a brief introduction is given as follows.

At $t_0$, the bidirectional switch $S_1S_2$ is turned ON and the current that flows through the series diodes decreases. The current falling rate is determined by the turn-on speed of the bidirectional switch and the parasitic inductance.

At $t_1$, the currents $i_F$ and $i_S$ fall to zero and increase in the opposite direction. The reverse currents will remove the same amount of reverser-recovery charges existed in these two diodes. It is known that the reverse-recovery charges in the fast diode $D_{F1}$ are far fewer than those in the slow diode $D_{S2}$.

At $t_2$, all of the reverse-recovery charges in the fast diode $D_{F1}$ are extracted out and $D_{F1}$ starts to bear the reverse voltage. After $t_3$, all of the reverse voltage is applied to the fast diode $D_{F1}$. However, there are still a lot of charges in the p-n junction of slow diode at this moment, so the voltage drop across the slow diode is always zero. The excessive charges in the slow diode can only be removed by the internal recombination process, which will take much longer time. Therefore, the slow diode can be considered as short-circuit and the fast diode dominates the performance of the diodes in series.

### B. Loss Analysis

A detailed analysis about the circuit losses is necessary for the performance evaluation of the proposed topology. The main losses of the FMBL PFC rectifier include the following aspects: inductor losses including magnetic core loss and ohmic loss;

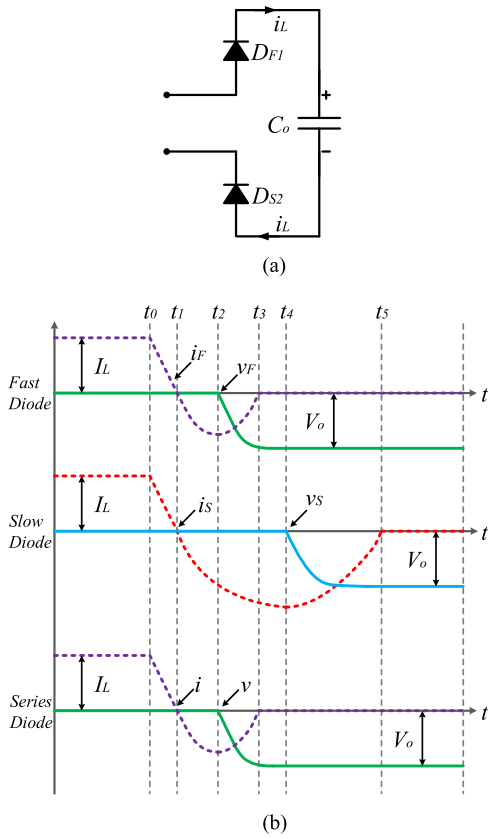


Fig. 10. Diode reverse recovery in the proposed rectifier. (a) Fast diode in series with a slow diode. (b) Diode reverse-recovery processes for single diode and the diodes in series.

TABLE I
PROTOTYPE COMPONENTS AND PARAMETERS

| Physic Meaning | Symbol | Description |
|---|---|---|
| Power MOSFET | $S_1$ $S_2$ | IPW65R080CFD |
| Auxiliary MOSFET | $S_3$ $S_4$ | IPP200N25N3 |
| Fast Diode | $D_{F1}D_{F2}$ | IDH10SG60C |
| Slow Diode | $D_{S1}D_{S2}$ | KBJ1010 |
| Input Inductor | $L$ | 502 $\mu$Hat0 A |
| Output Capacitor | $C_{o1}C_{o2}$ | 1000 $\mu$F/250 V |
| Input Voltage | $v_s$ | 90−−264 VACrms |
| Output Voltage | $V_o$ | 380 VDC |
| Switching Frequency | $f_s$ | 100 kHz |
| Full Power | $P_o$ | 700 W |

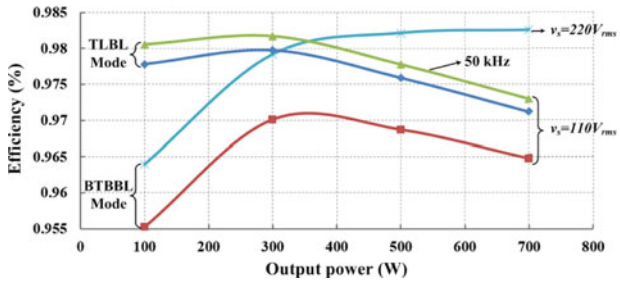


Fig. 11. Calculated efficiency curves across the output power range under different operating modes.

MOSFET losses including turn-on loss, turn-off loss, conduction loss, and capacitive loss; diode losses including capacitive loss (SiC diode is used for fast diode here), conduction loss; capacitor loss caused by the equivalent series resistor. A comprehensive loss calculation method about the traditional PFC rectifier is presented in [2], which can be used as a good reference. In [2], 1.15-mm (diameter) copper wire is used for the input inductor. The skin depth for copper wire is 0.2089 mm in the condition of 100 kHz and 20 , which means the skin effect has a great effect on the copper loss. In order to lower the skin effect, litz wire (0.1 mm $\times$ 120) is used for the inductor in the experiment prototype. Similarly, the proximity effect is also greatly reduced due to the use of litz wire. Therefore, the impact of the skin effect and proximity effect is ignored in the loss calculation.

The prototype components and parameters shown in Table I are used in the loss calculation. The switching frequency $f_s$ is 100 kHz. Based on [2], the calculated efficiency curves across the output power range are plotted in Fig. 11. From Fig. 11, it can be seen that the efficiency at 220 Vrms is much higher than that at 110 Vrms when the FMBL PFC operates in the BTBBL mode. The efficiency improvement at low-line voltage is significant after the proposed rectifier switches to the TLBL mode, especially for the light-load conditions. With the same input inductor and ripple requirement, the switching frequency in the TLBL mode can be reduced to $f_s/2$ to reduce the switching losses further. The efficiency curve with reduced switching frequency is also provided in Fig. 11.

Figs. 12 and 13 give the detailed loss distribution diagrams at the full load of both low- and high-line conditions for the FMBL PFC rectifier. Fig. 12(a) and (b) presents the loss distribution diagrams at different input voltages when the FMBL PFC rectifier works in the BTBBL mode. Comparing Fig. 12(a) with (b), the losses from the power MOSFETs at 110 Vrms account for a larger proportion than that at 220 Vrms, which is caused by the larger input current $i_L$ under low-line input. Generally, there is much difficulty in further reducing the conduction losses for the bridgeless PFC converter. Therefore, a potentially effective solution to improve the efficiency is to decrease the switching losses caused by the power MOSFETs, and three-level rectifier is a good alternative choice.

Fig. 13 gives the loss distribution diagrams at full-load and low-line condition when the FMBL PFC rectifier works in the TLBL mode. Since the switching voltage of power devices is reduced to half of the output voltage, so the switching losses and capacitive losses are lower than before. The losses from the power MOSFETs only account for 29% in Fig. 13(a). Additionally, the switching losses can be lower if the switching frequency is reduced to half of that adopted in the BTBBL mode with the same ripple requirement. Fig. 13(b) presents the corresponding loss distribution diagram after the frequency is decreased to 50 kHz.

In order to get a more intuitive comparison about loss distribution, Fig. 14 gives all the calculated device losses for three different operating modes at low-line condition: the BTBBL mode operating in 100 kHz and the TLBL modes operating

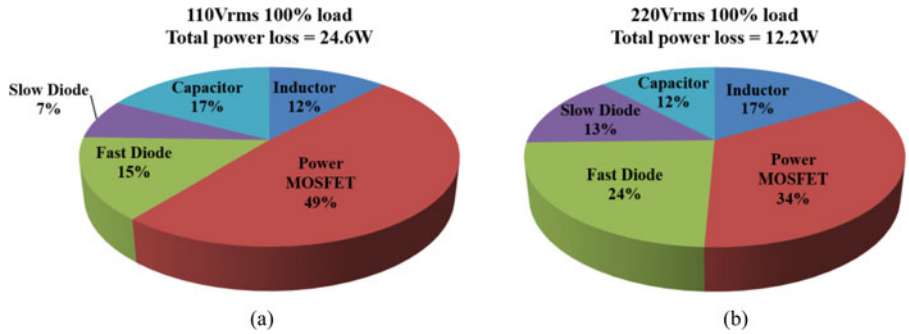


Fig. 12. Loss distribution diagrams in the BTBBL mode under different input voltages. (a) Loss distribution diagram at 110 Vrms with full load. (b) Loss distribution diagram at 220 Vrms with full load.

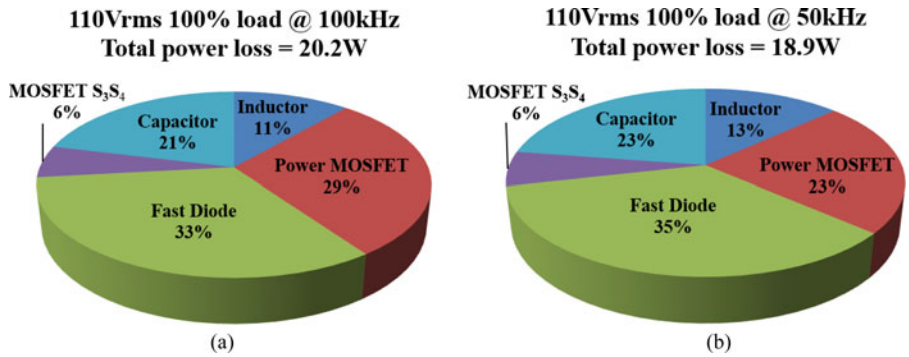


Fig. 13. Loss distribution diagrams in the TLBL mode with different switching frequencies. (a) Loss distribution diagram at 100 kHz with full load. (b) Loss distribution diagram at 50 kHz with full load.

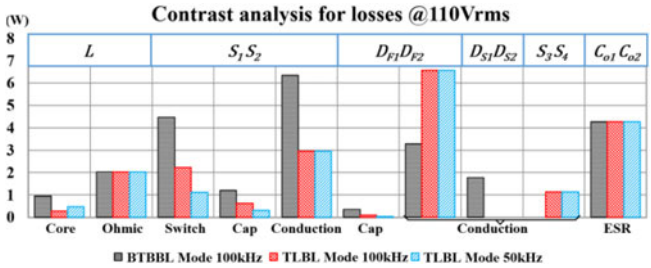


Fig. 14. Loss comparison for different modes and switching frequencies at full-load and low-line condition.

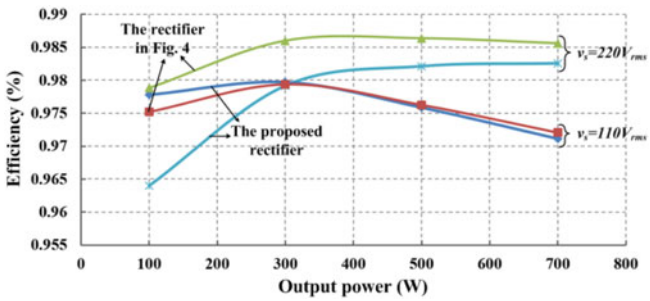


Fig. 15. Efficiency comparison between the proposed topology and the rectifier shown in Fig. 4.

in 100 and 50 kHz. From Fig. 14, the switching losses of MOSFETs decrease a lot when the TLBL mode is adopted for the same switching frequency 100 kHz. The total switching losses (including the switching loss, capacitive losses for $S_1S_2$ and $D_{F1}D_{F2}$) are much lower in the TLBL mode. The total conduction losses (including the conduction losses from $S_1--S_4$, $D_{F1}D_{F2}$, and $D_{S1}D_{S2}$) are also decreased a little. At the same time, the inductor current ripple is decreased remarkably when the FMBL PFC works in TLBL mode, so the core loss also drops a lot. In a word, the efficiency under low-input voltages is promoted significantly in the proposed flexible mode rectifier. In additional, the lower working frequency of $f_s/2$ can be used if the current ripple in TLBL mode is kept the same with that in the BTBBL mode. Although the reduction of operating frequency will lead to an increase of the core loss, the reduction in the total switching losses is larger than the increase of the core loss. So the efficiency can still be improved a little.

Finally, a comparison between the improved three-level PFC rectifier shown in Fig. 4 and the proposed FMBL PFC rectifier is presented under the frequency 100 kHz. The low-voltage MOSFETs that are identical to $S_3S_4$ in FMBL PFC are adopted for the loss calculation of the rectifier in Fig. 4. The efficiency curves of these two rectifiers are plotted in Fig. 15. Fig. 16 gives the specific loss comparison between these two topologies with both low- and high-line conditions at full load. At the low-line conditions, these two topologies have nearly identical efficiency and their loss distributions are also similar to each other. From Fig. 16(a), the FMBL PFC rectifier has lower capacitive loss since the IPW65R080CFD

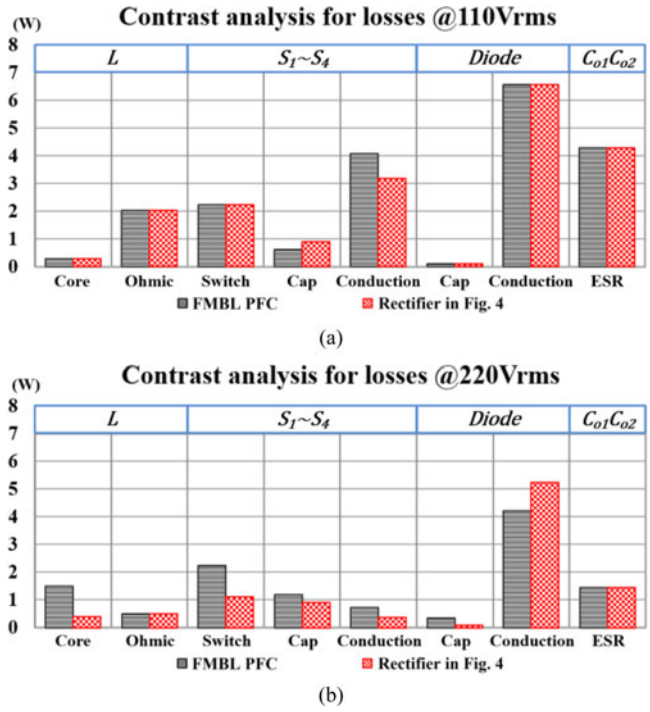


Fig. 16. Loss contrast analysis between the FMBL PFC rectifier and the rectifier shown in Fig. (a) Loss contrast at low-line full-load condition. (b) Loss contrast at high-line full-load condition.

has lower output capacitor than IPP200N25N3, but suffers from higher conduction losses due to the larger on-state resistance of IPW65R080CFD. At the high-line conditions, the FMBL PFC has larger inductor core loss and switching losses than the improved three-level converter since it operates in the BTBBL mode, so the efficiency of the FMBL PFC rectifier is significantly lower. From Fig. 16(b), it can also be noted that the total conduction losses in the FMBL PFC rectifier is lower since two slow diodes are used to conduct the current.

In summary, the proposed FMBL PFC rectifier can achieve a higher efficiency than the conventional bridgeless PFC rectifiers at low-line conditions and maintain a high efficiency at high-line conditions.

### C. Parameter Design

The proposed converter operates in a similar way with the traditional full-bridge boost PFC, so the design method used for the conventional full-bridge boost PFC can also be applied to the proposed flexible mode converter. A brief analysis about the input current ripple and output voltage ripple, which is used for designing the input inductor $L$ and the output capacitors $C_{o1}$ and $C_{o2}$, will be given.

The following ripple expression for the FMBL PFC converter can be derived:

$$\Delta i_L = \begin{cases} \frac{(V_o - v_s)v_s}{V_o}\frac{T_s}{L}, & \text{for BTBBL Mode} \\ \frac{(V_o/2 - v_s)v_s}{V_o/2}\frac{T_s}{L}, & \text{for TLBL Mode} \end{cases}. \quad (6)$$

On the basis of (6), Fig. 17 shows the input current ripples with 110-Vrms input under different modes and switching

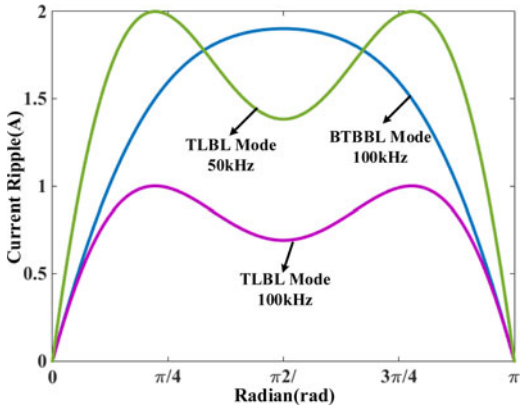


Fig. 17. Input current ripples for 110 Vrms under different topologies and switching frequencies.

frequencies. It can be seen that the maximum current ripple in the TLBL mode with 50 kHz is nearly the same as that in the BTBBL mode with 100 kHz. So the switching frequency can be reduced to increase the efficiency of the TLBL PFC converter under the same ripple requirement.

After designing the input inductor $L$, next step is to choose a proper capacitance for $C_{o1}$ and $C_{o2}$. When the FMBL PFC rectifier operates in the BTBBL mode, the capacitors $C_{o1}$ and $C_{o2}$ are in series and the voltage ripple across each capacitor is half of the total output voltage ripple. At this time, the following expression can be obtained:

$$\frac{C_o}{2}\frac{dv_o}{dt} = \frac{2P_{\text{in}}}{V_o}(\sin\omega t)^2 - I_o = -I_o\cos 2\omega t \quad (7)$$

where $P_{\text{in}}$ is the input power, $I_o$ is the dc output current, and $\omega = 2\pi f_g$ ($f_g$ is the line frequency).

From (7), the maximum voltage ripples can be derived as follows:

$$\begin{cases} \Delta v_{C_{o1}\_\max} = \Delta v_{C_{o2}\_\max} = \frac{I_o}{\omega C_o} \\ \Delta v_{o\_\max} = \frac{2I_o}{\omega C_o} \end{cases}. \quad (8)$$

When the FMBL PFC rectifier operates in the TLBL mode, one capacitor is charged by the input current during half-line cycle. At the same time, the other capacitor is discharged by the load current. For the positive half-line cycle, the currents that flow through these two capacitors are given as

$$\begin{cases} C_{o1}\frac{dv_{C_{o1}}}{dt} = \frac{2P_{in}}{V_{C_{o1}}}(\sin\omega t)^2 - I_o = I_o\,(1 - 2\cos 2\omega t) \\ C_{o2}\frac{dv_{C_{o2}}}{dt} = -I_o. \end{cases} \quad (9)$$

According to (9), Fig. 18 gives the voltage ripples across the capacitors and the maximum voltage ripples can be derived as follows:

$$\begin{cases} \Delta v_{C_{o1}\_\max} = \left(\sqrt{3} + \frac{2\pi}{3}\right)\frac{I_o}{\omega C_o} \\ \Delta v_{o\_\max} = \frac{2I_o}{\omega C_o}. \end{cases} \quad (10)$$

In the negative half-line cycle, the maximum voltage ripple $\Delta v_{C_{o2}\_\max}$ of $C_{o2}$ has the same value with $\Delta v_{C_{o1}\_\max}$.

Comparing (8) with (10), it can be seen that the total maximum output voltage ripple is the same in different operating

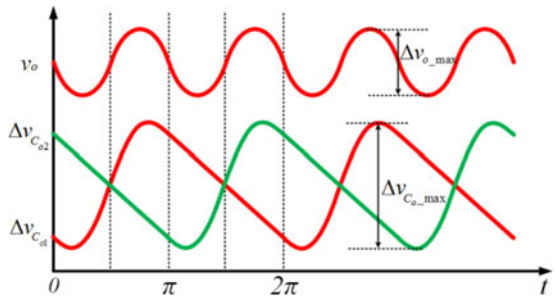


Fig. 18. Output voltage ripples of the capacitors in the TLBL mode.

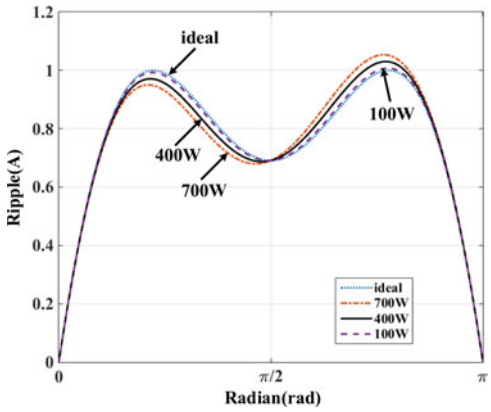


Fig. 19. Effect of capacitor voltage ripple on the input current ripple under 110 Vrms.

modes and the maximum voltage ripple for each output capacitor in the TLBL mode is much larger than that in the BTBBL mode. The amplitude of voltage ripple increases with the increase of output power. So the output capacitance can be designed based on (10) for the required voltage ripple.

The expression (6) is derived by assuming that the capacitor voltage is constant. However, the large voltage ripple in the TLBL mode may have an effect on the input current ripple. According to (9), the voltage across $C_{o1}$ during positive half-line cycle can be derived as follows:

$$v_{C_{o1}}(t) = \frac{V_o}{2} + \frac{I_o}{C_o}\left(t - \frac{\pi}{2\omega} - \frac{\sin 2\omega t}{\omega}\right), \quad 0 < \omega t < \pi. \tag{11}$$

So the accurate input current ripple is

$$\Delta i_L = \frac{4I_o v_s^2}{V_o^2 \omega C_o}\frac{T_s}{L}\left(\omega t - \frac{\pi}{2} - \sin 2\omega t\right) + \frac{(V_o/2 - v_s)\, v_s}{V_o/2}\frac{T_s}{L}, \quad 0 < \omega t < \pi. \tag{12}$$

In the TLBL mode, the second part of (12) is the same with (6) and is independent of the output power. The first part is closely related to the output power. Fig. 19 shows the difference between (6) and (12) under different output powers, which is very small. That is, (6) can be used to design the input inductor.

## IV. Experiment Result

A prototype of the FMBL PFC rectifier shown in Fig. 7 at 100 kHz 700 W is built to verify the theoretical analysis. The prototype is designed to work in a universal ac-line input. The detailed prototype components and parameters are shown in Table I. A low-voltage MOSFET named IPP200N25N3 (20 $m\Omega$ /250 V) from Infineon is selected for the bidirectional switch $S_3S_4$ since the maximum drain-source voltage across $S_3S_4$ is only half of the output voltage $V_o$. In addition, SiC diodes are adopted as the fast recovery diodes $D_{F1}$ and $D_{F2}$ to reduce the reverse-recovery current. The litz wire ($0.1\,\mathrm{mm} \times 120$) and the toroidal magnetic core (77439A7 from Magnetics) are used for the boost inductor to reduce the skin effect and the proximity effect. A MCU called TMS320F28335 from Texas Instruments is used as the controller.

### A. Experiments of Traditional BTBBL PFC

For the traditional BTBBL PFC rectifier, Fig. 20(a) and (b) presents the experiment waveforms of the output voltage $V_o$, the voltage $v_{D_{S2}}$ across the slow diode $D_{S2}$, the input current $i_L$, and the input voltage $v_s$, at full load of two rated input voltages 110 and 220 Vrms. For the convenience of viewing, the input current $i_L$ is shown in the reverse direction. In both situations, the voltage $v_{D_{S2}}$ across the slow diode remains unchanged during a half-line cycle, which is in accordance with the analysis.

Fig. 21(a) and (b) gives the voltage waveforms across the diodes in series at different input voltages. During a switching period, the voltage $v_{D_{S1}}$ stays the same and $v_{D_{F2}}$ jumps from 0 to $V_o$ quickly or vice versa. It illustrates that all of the reverse voltage is applied to the fast diode $D_{F2}$ and the slow diode $D_{S1}$ could be treated as short-circuit. At the same time, the switchover process of $v_{D_{S1}}$ near the zero point is slow for both input voltages. The input source is always directly connected to the output capacitor, so the common noise interference is low.

Fig. 22 shows the measured efficiency curves of the BTBBL PFC rectifier. As can be seen from Fig. 22, the high conversion efficiency can be achieved in the traditional BTBBL PFC rectifier at high-line conditions. When the input voltage is 110 Vrms, the measured maximum efficiency is only 96%, which is much lower than 98% at 220-Vrms input. So it is necessary to promote the conversion efficiency under the low-input voltages.Fig. 23 gives the measured power factor curves of the BTBBL PFC rectifier at different input voltages and output powers.

### B. Efficiency of FMBL PFC

In order to promote the efficiency at low-line input, the proposed FMBL PFC rectifier can be adapted to work in the TLBL mode by turning on the bidirectional switch $S_3S_4$. The switching losses in the three-level converter are much less than those in the two-level converter, so it is possible to improve the efficiency at low-input voltages. Fig. 24 (a) and (b) shows the experiment waveforms of the output voltage $V_o$, the voltage $v_{dd}$ across the bidirectional switch $S_1S_2$, the input current $i_L$, and the input voltage $v_s$ at the input voltage 110 Vrms and with switching frequency 100 and 50 kHz, separately. The voltage $v_{dd}$ presents

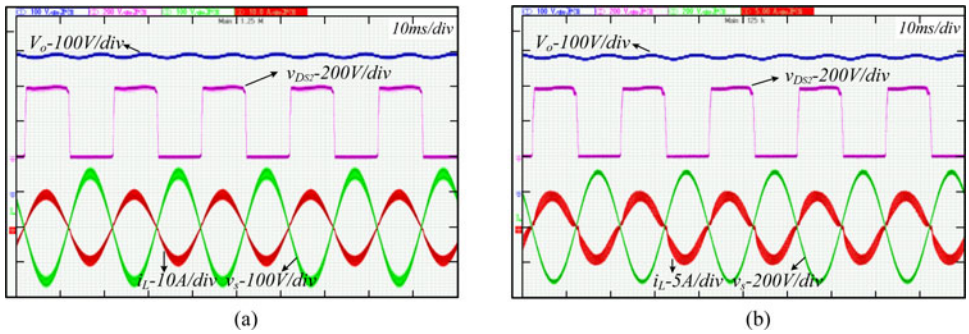


Fig. 20. Experiment waveforms of the BTBBL PFC rectifier with full load under different input voltages. (a) $V_o$, $v_{D_{S2}}$, $v_s$ and $i_L$ at $v_s = 110$ Vrms. (b) $V_o$, $v_{D_{S2}}$, $v_s$, and $i_L$ at $v_s = 220$ Vrms.

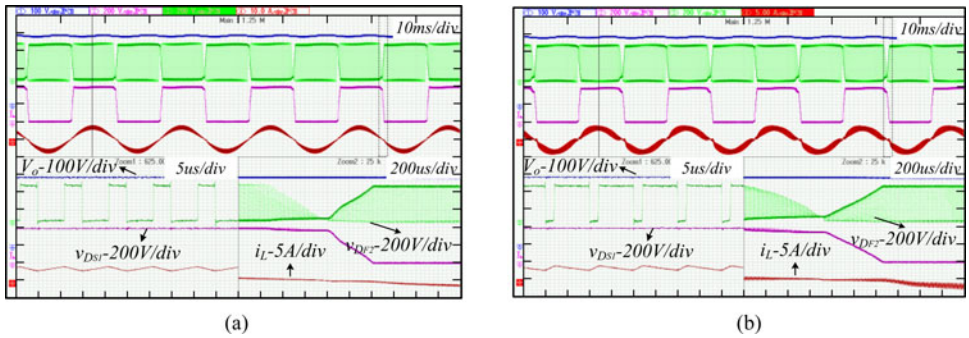


Fig. 21. Experiment waveforms under 500-W output power and different input voltages. (a) $V_o$, $v_{D_{F2}}$, $v_{D_{S1}}$, and $i_L$ at $v_s = 110$ Vrms. (b) $V_o$, $v_{D_{F2}}$, $v_{D_{S1}}$, and $i_L$ at $v_s = 220$ Vrms.

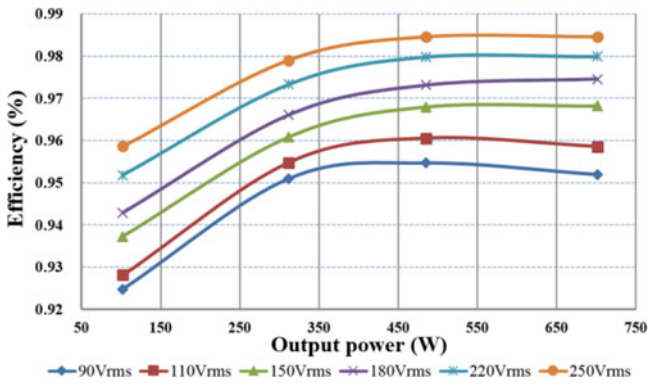


Fig. 22. Efficiency curves of the BTBBL PFC rectifier at different input voltages.

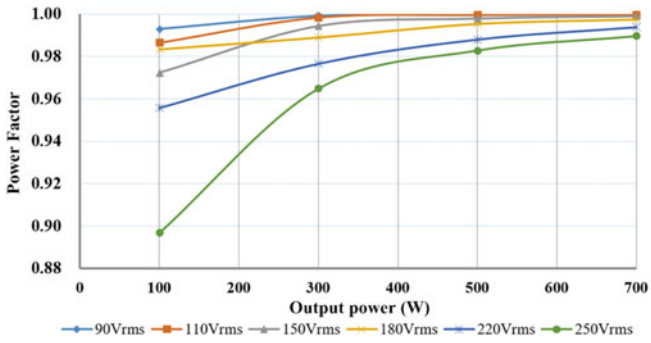


Fig. 23. Measured power factor curves of the BTBBL PFC rectifier under different input voltages and output powers.

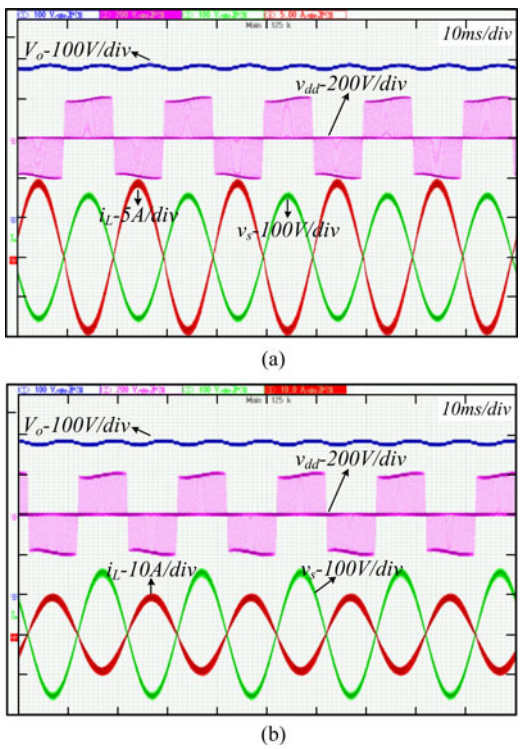


Fig. 24. Experiment waveforms of the proposed FMBL PFC rectifier working in TLBL mode under full load of 110 Vrms input and different switching frequencies. (a) $V_o$, $v_{dd}$, $v_s$, and $i_L$ at $f_s = 100$ kHz. (b) $V_o$, $v_{dd}$, $v_s$, and $i_L$ at $f_s = 50$ kHz.

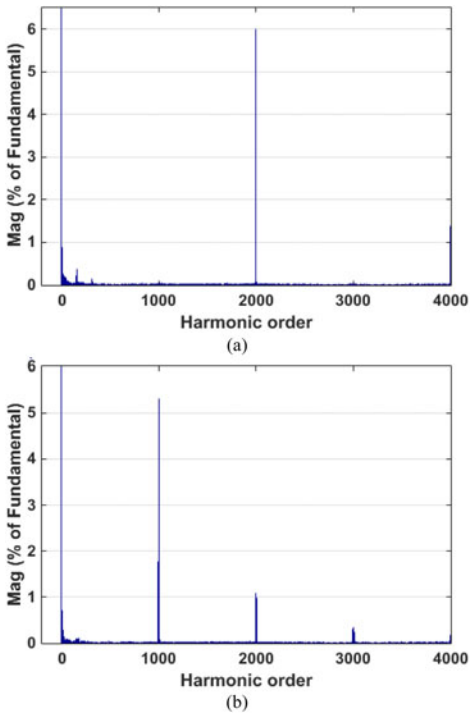


Fig. 25. FFT analysis of the input current $i_L$ with full load and 110-Vrms input. (a) BTBBL mode with $f_s = 100$ kHz. (b) TLBL mode with $f_s = 50$ kHz.

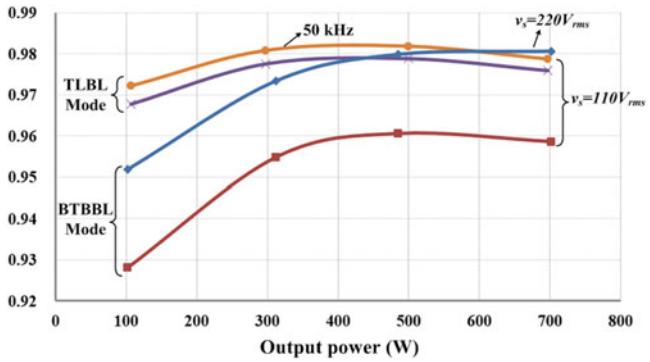


Fig. 26. Efficiency curves of the proposed FMBL PFC rectifier at low- and high-line conditions.

three levels: $-V_o/2$, 0, $V_o/2$ which is in accordance with the theoretical analysis. Furthermore, Fig. 25 gives the FFT analysis of the input current $i_L$ at different modes and switching frequencies. It can be seen that the current harmonic at 50 kHz in the TLBL mode is a little smaller than that at 100 kHz in the BTBBL mode. Therefore, the switching frequency in the TLBL mode can be reduced to $f_s/2$ for the same input current ripple requirement. However, if a *LC* filter with a transfer function $1/(s^2LC + 1)$ is used to suppress the switching harmonic, the switching frequency can only be reduced to 80 kHz for the same attenuation. In a word, the efficiency can be improved further by reducing the switching frequency when the FMBL PFC rectifier operates in the TLBL mode.

Fig. 26 gives all the measured efficiency curves of the proposed FMBL PFC rectifier at low- and high-line conditions. It is clear that the efficiency is promoted significantly when the

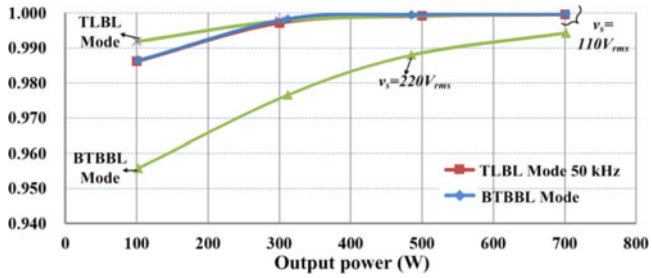


Fig. 27. Measured power factor of the TLBL PFC rectifier across the output power range with the switching frequency 100 kHz.

FMBL PFC rectifier works in the TLBL mode at the low-input voltage. A higher efficiency can be achieved when the switching frequency is reduced to 50 kHz for the same ripple requirement. These experiment results prove that the proposed topology can realize efficiency promotion by reducing the switching losses at low-line conditions. The efficiency of the FMBL PFC rectifier at high-line conditions is the same with Fig. 22 since the same topology is adopted. Therefore, the proposed FMBL PFC rectifier can achieve a higher efficiency than the conventional bridgeless PFC rectifiers at low-line conditions and maintain a high efficiency at high-line conditions.

From the efficiency curves shown in Fig. 26, the efficiency at 110 Vrms in the TLBL mode is higher than that at 220 Vrms at light-load conditions. At this time, the switching losses dominate in the total circuit losses since the input current is small. With the increase of load, the conduction losses at low-input voltages grow rapidly and become the dominant component of the total losses. The efficiency at low-input voltages starts to decrease with the increasing of load. Compared with Fig. 11, there is a distinct difference between the measured efficiencies and the calculated efficiencies under light-load conditions. The difference is mainly caused by the measurement error due to the limitation of measuring instruments. For the output power 100-W 0.005-A deviation in output current will lead to a deviation 1.9% in measured efficiency. On the other hand, the input current ripple also has a little impact on the conducting losses when the input current is small. Additionally, it is assumed that the temperature rise at all conditions is the same in the loss calculation. However, the device temperature usually is higher in the BTBBL mode with 110-Vrms input, which leads to that the measured efficiency is lower than the calculated. The calculated efficiency will agree better with the experimental ones if a more accurate loss model can be established and the more delicate instruments can be used for measurement. In general, their trends are consistent by comparing the theoretical analysis with the measured efficiency curves. Fig. 27 gives the measured power factor curves of the FMBL PFC rectifier across the output power range.

## V. Conclusion

In this paper, a novel FMBL PFC rectifier is proposed, in which the high efficiency over a wide input range can be achieved. In the proposed rectifier, a BTBBL PFC rectifier is adopted at high-line voltages and a TLBL PFC rectifier is

formed to achieve high efficiency at low-line voltages. Compared with the traditional bridgeless boost PFC rectifier, an extra low-voltage bidirectional switch (usually composed of two switches) is added, therefore the increased cost is low. At both high- and low-line conditions, the low CM noise can be achieved due to the direct connection between the input power grid and the output electrolytic capacitor during half-line cycle. The detailed principle analysis about the proposed FMBL PFC rectifier is presented. Finally, an experimental prototype is built to verify the feasibility and the effectiveness of the proposed topology.

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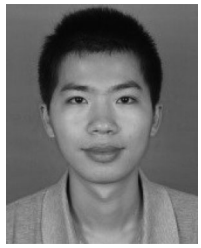

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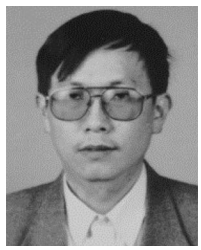

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