Letters

Fast Diagnostic Method of Open Circuit Fault for Modular Multilevel DC/DC Converter Applied in Energy Storage System

Kaitao Bi, Quntao An, *Member, IEEE*, Jiandong Duan, Li Sun, *Member, IEEE*, and Kuo Gai

***Abstract*—This letter presents a fast open circuit diagnostic method for modular multilevel DC/DC converter (MMDDC), which is applied in super capacitor energy storage system. The proposed method is derived based on the analysis of submodule output characteristics under both normal and fault conditions. For MMDDC, different types of open circuit fault are reflected by the output voltage of submodule in certain operating modes, thus a simple and effective diagnostic method by the aid of a hardware circuit and a fast fault location algorithm is proposed. The hardware circuit is responsible for detecting submodule output voltage and its output result is transmitted to a processor to accomplish the final fault diagnosis along with drive signals. The proposed approach avoids complex mathematical operations and minimizes fault diagnostic time; moreover, it can achieve fault diagnosis under a wide super capacitor operating voltage range. Finally, the proposed diagnostic method is verified experimentally based on a laboratory-scale MMDDC energy storage prototype.**

***Index Terms*—Energy storage system, fault diagnosis, modular multilevel DC/DC converter, open circuit fault.**

I. Introduction

MODULAR multilevel converter (MMC) is widely applied in high-voltage and high-power applications due to its superior control performance, flexible combination, and high-pressure characteristics [1], [3]. Since the large number of identical half bridge submodules connected in series, each submodule may be considered as a potential failure point, thus, the probability of a fault in MMC is larger than other converters with fewer IGBTs, which directly affects the safe operation of MMC application systems. Hence, rapid fault diagnosis and location is necessary to improve the security and reliability of the system.

IGBT faults can be classified as short circuit fault [4]–[8] and open circuit fault [9]–[17]. Short circuit fault is very destructive for system, which is usually caused by overcurrent. At present, most of gate drivers applied in industries have been integrated with short circuit protections, when such a fault is detected, the driver will immediately turn off IGBT. By contrast, open circuit fault is also a threat to system, and much more time is necessary to detect it. For MMC, open circuit fault can heavily distort the waveforms of voltage and current, besides, the capacitor employed by submodule is easily destroyed due to the absent of discharge circuit caused by open circuit fault. Therefore, in this letter, the diagnostic method for IGBT open circuit fault is specially considered.

Open circuit fault diagnosis has been widely studied, however, some of the proposed methods are only suitable for voltage source inverters or fixed structure converters used in specific applications [9]–[12]. Karimi *et al.* [11] proposed the method using "voltage criterion" and "time criterion" to process collector error voltage to diagnose open circuit faults for a inverter, and a fast A/D converter and FPGA were employed to reduce fault diagnosis time to 10 μs. But this method can only diagnose the fault arm without the capability of locating faults. A fast and low-cost diagnostic method based on switching function model for three-phase inverter was presented in [12]. This method is capable to use a simple hardware to detect the collector voltage of lower arm to realize fault detection and location, but it requires the supply power of system which should be larger than the detection circuit, which reduced its applications.

Fault diagnostic methods for MMC are also applicable to MMDDC because of the similar structure. Shao *et al*. [13] proposed the method using sliding mode observer to diagnose open circuit fault in MMC and the property of the same observer was improved in [14]. However, the performance of this method heavily relies on the accuracy of converter switching model. Some other fault diagnostic methods based on advanced algorithm were proposed in [15] and [16], but a certain time is essential for these methods to locate the fault submodule, which may bring potential risk to the system during location time interval. A practical way to detect faults is to add additional hall sensors in the system [17], but the unwanted sensor noises may degrade the precision of fault detection if they are not taken into consideration. Moreover, the failure of additional hall sensors has to be considered in order to ensure the reliability of system, thus special algorithm for sensor fault detection and isolation is

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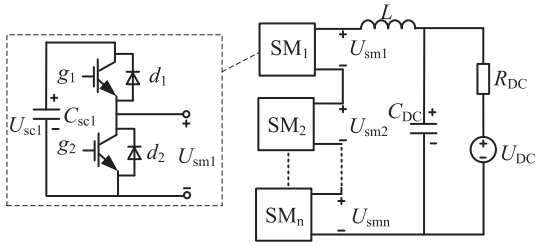

Fig. 1. Module multilevel DC/DC converter.

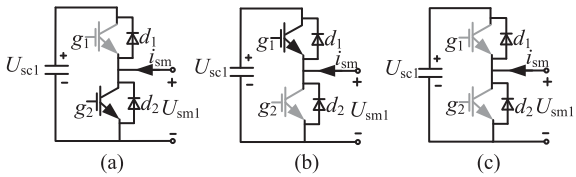

Fig. 2. Open circuit fault types: (a) open circuit fault on upper arm. (b) Open circuit fault on lower arm. (c) Open circuit fault on both arms.

inevitable [18], [19], but this may result in the system control to be more complicated.

This letter proposes a fast open circuit fault diagnostic method for MMDDC applied in super capacitor energy storage system (SESS). A simple detection circuit is used in this method to detect submodule operation condition and its output together with drive signals are input to FPGA to achieve final fault diagnosis and location. This method can not only improve fault diagnosis response but also is applicable under a wide supercapacitor voltage range. Moreover, the proposed method avoids complex mathematical operations, and is easy to be implemented.

The remainder of this letter is organized as follows: Section II presents an analysis of submodule output characteristics in MMDDC both under normal and fault conditions. The design principle of the proposed method is described in Section III. Validity of the proposed fault diagnosis is demonstrated by experimental results in Section IV. Finally, Section V concludes this paper.

II. Analysis of Submodule Output Characteristics

The structure of modular multilevel DC/DC converter [3] applied in SESS is shown in Fig. 1, which is mainly composed of identical half bridge submodules. $U_{\mathrm{smi}}\,(i = 1, 2, 3, \ldots, n)$ represents the output voltage of submodule and $U_{\mathrm{sci}}\,(i = 1, 2, 3, \ldots, n)$ denotes super capacitor voltage. In order to diagnose open circuit faults, it is essential to analyze the output characteristics of submodule both in normal and fault conditions.

As shown in Fig. 2, open circuit fault in MMDDC can be classified into three types: fault on upper arm, fault on lower arm, and fault on both arms. Define S_{1+} and S_{1-} as the drive signals of submodule 1. Ignore the effect of dead time, under normal charge and discharge conditions, when $S_{1+} = 1$ and $S_{1-} = 0$, g_1 is ON and g_2 is OFF, thus $U_{\mathrm{sm}1} = U_{\mathrm{sc}1}$, conversely, g_1 is OFF and g_2 is ON, $U_{\mathrm{sm}1} = 0$. Hence, the relationship between super capacitor voltage and submodule output voltage

TABLE I
Submodule Output Characteristics

Operation mode	S_{1+}	S_{1-}	Normal $U_{\mathrm{sm}1}$	g_1 fault $U_{\mathrm{sm}1}$	g_2 fault $U_{\mathrm{sm}1}$	g_1 g_2 fault $U_{\mathrm{sm}1}$
Charge	1	0	$U_{\mathrm{sc}1}$	$U_{\mathrm{sc}1}$	$U_{\mathrm{sc}1}$	$U_{\mathrm{sc}1}$
Charge	0	1	0	0	$\boldsymbol{U}_{sc1}$	$\boldsymbol{U}_{sc1}$
Charge	0	0	$U_{\mathrm{sc}1}$	$U_{\mathrm{sc}1}$	$U_{\mathrm{sc}1}$	$U_{\mathrm{sc}1}$
Discharge	1	0	$U_{\mathrm{sc}1}$	**0**	$U_{\mathrm{sc}1}$	**0**
Discharge	0	1	0	0	0	0
Discharge	0	0	0	0	0	0

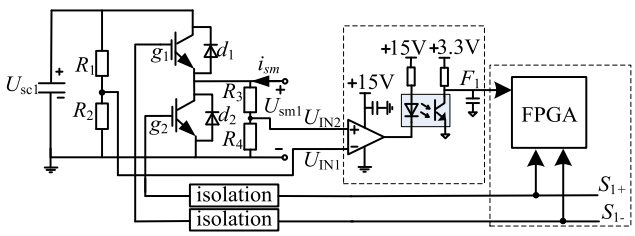

Fig. 3. Schematic of proposed open circuit diagnostic method.

is expressed as follows:

$$U_{\mathrm{sm}1} = S_{1+}U_{\mathrm{sc}1} \tag{1}$$

Under fault conditions, (1) is no longer suitable for expressing submodule output voltage. Considering open circuit fault on upper arm, as shown in Fig. 2(a). When MMDDC operates under charge mode and $S_{1+} = 1$, super capacitor is charged by the current which flows through the antiparallel diode of upper arm, thus we have $U_{\mathrm{sm}1} = U_{\mathrm{sc}1}$. When MMDDC operates under discharged mode, due to the fault on upper arm, regardless of the state of drive signals, current can only flow through d_2, thus the value of $U_{\mathrm{sm}1}$ is always 0.

When open circuit fault occurs on lower arm and both arms, submodule output voltage can be analyzed in the similar way. Table I demonstrates submodule output characteristics under both normal and fault conditions.

We can see from Table I, under charge mode, lower arm fault results in submodule output voltage variation, and upper arm fault has no effect on the converter. In contrast, under discharge mode, upper arm fault influences submodule output result and lower arm fault can be ignored. When both arms fault occurs, submodule output features are the same as single arm fault, hence it can be deal with single arm fault. So the abnormal submodule output voltage together with relevant drive signals can be adopted to diagnose open circuit faults on a particular arm.

III. Principles of the Proposed Fault Diagnostic Method

The proposed diagnostic method is shown in Fig. 3, which is composed of a detection circuit and an algorithm based on FPGA. The function of detection circuit is detecting submodule output voltage and achieving signal isolation, to achieve these objects, a comparator and a photocoupler are employed. The algorithm in FPGA accomplishes the final diagnosis using drive signals and detection circuit output result.

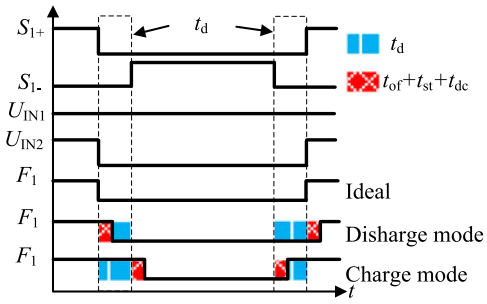

Fig. 4. Time sequence of signals.

A. Detection Circuit

Super capacitor as energy storage device has a wide operating voltage range, which may expand from zero to rated value if precharge operation is considered in actual applications, hence the detection circuit should be to work under a wide super capacitor range. Ignore the dead time, U_{IN1} and U_{IN2} under normal condition are calculated as follows:

$$U_{\mathrm{IN1}} = \frac{R_2}{R_1+R_2}U_{\mathrm{sc1}} \tag{2}$$

$$U_{\mathrm{IN2}} = \frac{R_4}{R_3+R_4}S_{1+}U_{\mathrm{sc1}}. \tag{3}$$

There are two limitations to design proper values for U_{IN1} and U_{IN2}. First, U_{IN1} and U_{IN2} have to be selected within the permitted input value of photocoupler. Second, when $S_{1+}=0$, as shown in (3), $U_{\mathrm{IN2}}=0$, the output of comparator must be a low level. When $S_{1+}=1$, U_{IN2} has to be larger than U_{IN1} to flip the comparator output to a high level, thus U_{IN1} and U_{IN2} should meet the following requirements:

$$\begin{cases} U_{\mathrm{IN2}} > U_{\mathrm{IN1}} \ (S_{1+}=1) \\ U_{\mathrm{IN2}} < U_{\mathrm{IN1}} \ (S_{1+}=0) \end{cases}. \tag{4}$$

However, due to the existence of IGBT voltage drop U_d, there should be a minimum super capacitor voltage to active the comparator. The relationship between submodule output voltage and super capacitor voltage is expressed in

$$U_{\mathrm{sc1}} = U_{\mathrm{sm1}} + U_d. \tag{5}$$

Substituting (2), (3), and (5) into (4), the lowest available super capacitor voltage U_{scmin} is shown in

$$U_{\mathrm{sc1min}} = \frac{R_4(R_1+R_2)}{R_1R_4-R_2R_3}U_d. \tag{6}$$

Therefore, the optimal values of the four sampling resistors can be derived by (2)–(4) and (6) to maximize the input voltage range of the detection circuit. The detection circuit output only reflects the operation state of submodule, hence a postprocessing has to be implemented to extract fault information.

B. Fault Diagnosis and Location Algorithm

Fig. 4 presents the time sequences of various signals in actual system. System delay time can be classified as dead time t_d, signal transmission delay t_{st}, switch on-off delay t_{of}, and detection circuit delay t_{dc}. As shown in Fig. 4, the effect of different delay times results in the value of F_1 under actual operation modes is inconsistent with ideal value, which will lead to misdiagnosis in fault postprogram processing, but this issue can be settled by delaying the drive signals in the program.

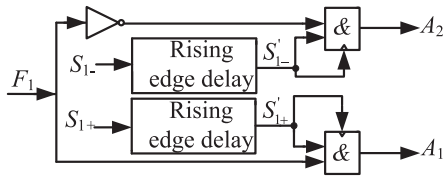

Fig. 5. Algorithm structure of fault diagnosis and location.

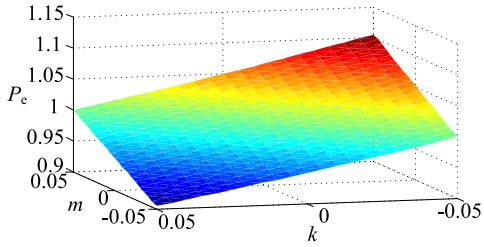

Fig. 6. Range of P_e under different precision values of sampling resistor.

The fault location algorithm completed in FPGA is shown in Fig. 5, which is composed of two parts, and they are rising edge delay and an AND gate with enable function together with data lock function.

The main goal of rising edge delay is to eliminate misdiagnosis caused by system delay time. The AND gate will be enabled by a high-level drive signal. When the AND gate output is high, it indicates that MMDDC is operating normally, and a low output indicates a fault in MMDDC. The AND gate stops working and its output is locked in the previous moment when the drive signal is turned into a low level. As shown in Fig. 5, A_1 and A_2 are the diagnosis results for upper arm and lower arm, respectively, which can be expressed as

$$A_1 = (S'_{1+}\&F_1)||(\overline{S'_{1+}}) \tag{7}$$

$$A_2 = (S'_{1-}\&\overline{F_1})||(\overline{S'_{1-}}). \tag{8}$$

C. Influence of Sampling Resistors on the Proposed Method

In actual applications, manufacturing process leads to a certain deviation in the value of sampling resistor. Hence, when the precision of sampling resistor is considered, (2) can be rewritten as follows:

$$U_{\mathrm{IN1}} = \frac{R_2(1+m)}{(R_1+R_2)(1+k)}U_{\mathrm{sc1}} \tag{9}$$

where m and k are the precision value of sampling resistor, whose values typically vary from -5%–5%. With the aid of (2) and (9), the relationship between actual sampling voltage value and theoretical design value can be obtained in (10), which is expressed as P_e, and its range is shown in Fig. 6.

$$P_e = \frac{1+m}{1+k}. \tag{10}$$

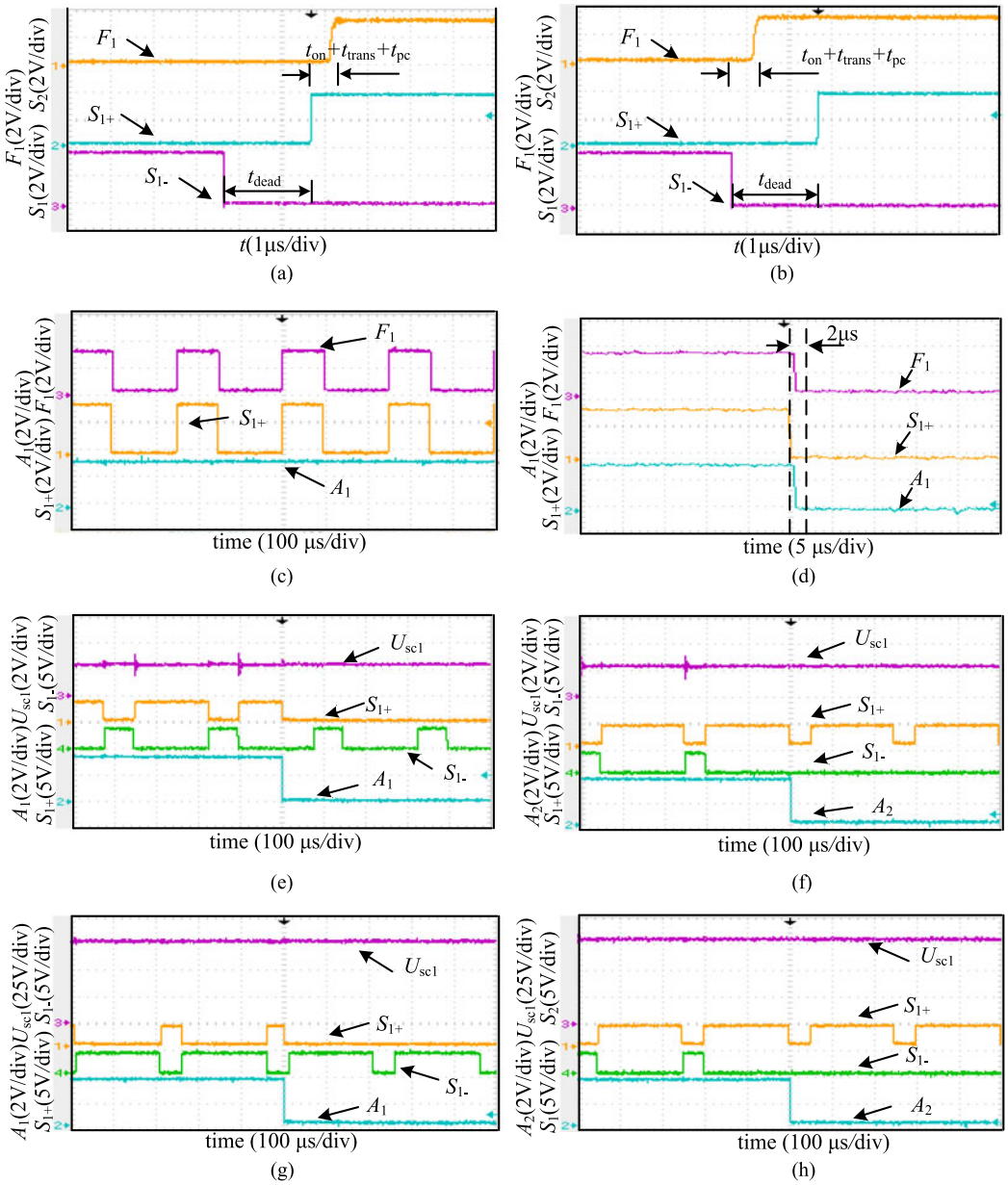

Fig. 7. Experiment results: drive signals and detection circuit output F_1: (a) under discharge mode, (b) under charge mode. (c) Signal responses under normal condition. (d) Signal responses when fault occurs on upper arm under discharge mode. (e) Upper arm fault diagnosis response under a low SC voltage. (f) Lower arm fault diagnosis response under a low SC voltage. (g) Upper arm fault diagnosis response under a high SC voltage. (h) Lower arm fault diagnosis response under a high SC voltage.

It can be seen from Fig. 6 that the maximum detection deviation of super capacitor voltage can reach 10% of theoretical value when the precision values of the two sampling resistors are 5% and −5% respectively. Hence, the maximum detection deviation of submodule output voltage value also will be 10% if the same precision sampling resistor is used. However, the voltage sampling error caused by sampling resistors can be eliminated by reasonably designed the input values of comparator. For example, when the condition of maximum detection deviation is considered, $U_{\mathrm{IN}2}$ should be designed 1.2 times larger than $U_{\mathrm{IN}1}$ so that (4) can be satisfied, thus open circuit diagnosis can always be realized without the influence of sampling resistors. If high precision resistors are adopted, the difference between $U_{\mathrm{IN}2}$ and $U_{\mathrm{IN}1}$ can be reduced.

IV. Experimental Results

In order to verify the validity of the proposed diagnostic method, an experimental prototype is built. The capacity of super capacitor is 1.42 F with 100 V rated voltage. Infineon IRFP90N20D is employed as the switch, switching frequency is set to 4 kHz and dead time is regulated to be 2 μs. According to the parameters of the selected switch, delay time in the algorithm is set to be 3.5 μs. The sampling resistor from R_1 to R_4 are chosen as: 45, 5, 86, and 14 kΩ, respectively.

Constant duty control is adopted in the experiment and experimental results are presented in Fig. 7. The effects of time delay on detection circuit output under discharge and charge mode are shown in Fig. 7(a) and (b), respectively. Fig. 7(c) shows the fault diagnostic result A_1 under normal cases, which is always a high level. The diagnostic response of upper arm fault is shown in Fig. 7(d) and the level of A_1 is inverted within 2 μs, which indicates that upper arm fault is diagnosed. Fig. 7(e)–(h) show the diagnostic results under different open circuit fault conditions, where super capacitor voltage is 2 and 75 V, respectively. These results demonstrate that the proposed diagnostic method is valid and is applicable under a wide super capacitor operating voltage range.

V. Conclusion

Open circuit fault diagnosis is necessary for power electronic system. This paper proposes a fast open circuit diagnostic method for MMDDC based on hardware detection circuit and a fast fault location approach. By properly selecting voltage sampling resistors, the detection circuit can generate an isolation signal that reflects the operation state of submodule. In order to eliminate misdiagnosis caused by system delay time and locating the fault quickly, a postprocessing fault location approach completed in FPGA is presented. A laboratory-scale energy storage system based on MMDDC is designed and comparative experimental results demonstrated that the proposed method can achieve open circuit fault diagnosis within 5 μs.

References

[1] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–14, Jan. 2015.

[2] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron*, vol. 30, no. 1, pp. 18–36, Jan. 2015.

[3] D. Montesinos-Miracle, M. Massot-Campos, J. Bergas-Jane, S. Galceran-Arellano, and A. Rufer, "Design and control of a modular multilevel DC/DC converter for regenerative applications," *IEEE Trans. Power Electron*, vol. 28, no. 8, pp. 3970–3979, Aug. 2013.

[4] V. K. Sundaramoorthy, E. Bianda, G. Knapp, and A. Heinemann, "A novel method to protect IGBT module from explosion during short-circuit in traction converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 20–24, 2015, pp. 2734–2741.

[5] M. Oinonen, M. Laitinen, and J. Kyyrä, "Current measurement and short-circuit protection of an IGBT based on module parasitics," in *Proc. 16th Eur. Conf. Power Electron. Appl.*, Aug. 26–28, 2014, pp. 1–9.

[6] X. Zhang, M. Chen, N. Zhu, and D. Xu, "A self-adaptive blanking circuit for IGBT short-circuit protection based on VCE measurement," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 4125–4131.

[7] S. Bolognani, M. Zordan, and M. Zigliotto, "Experimental fault-tolerant control of a PMSM drive," *IEEE Trans. Ind. Electron.*, vol. 47, no. 5, pp. 1134–1141, Oct. 2000.

[8] S. Karimi, A. Gaillard, P. Poure, and S. Saadate, "FPGA-Based real-time power converter failure diagnosis for wind energy conversion systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 12, pp. 4299–4308, Dec. 2008.

[9] B. Mirafzal, "Survey of fault-tolerance techniques for three-phase voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5192–5202, Oct. 2014.

[10] X. Pei, S. Nie, Y. Chen, and Y. Kang,"Open-circuit fault diagnosis and fault-tolerant strategies for full-bridge dc–dc converters," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2550–2565, May 2012.

[11] S. Karimi, A. Gaillard, and P. Poure, "FPGA-based real-time power converter failure diagnosis for wind energy conversion systems," *IEEE Trans. Power Electron.* vol. 55, no. 12, pp. 4299–4308, Dec. 2008.

[12] Q. T. An, L. Z. Sun, K. Zhao, and L. Sun, "Switching function model-based fast-diagnostic method of open-switch faults in inverters without sensors," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 119–126, Jan. 2011.

[13] S. Shao, P. Wheeler, J. Clare, and A. Watson, "Fault detection for modular multilevel converters based on sliding mode observer," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4867–4872, Nov. 2013.

[14] S. Shao, A. Watson, J. Clare, and P. Wheeler, "Robustness analysis and experimental validation of a fault detection and isolation method for the modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3794–3805, May 2016.

[15] D. Fujin, C. Zhe, M. R. Khan, and Z. Rongwu, "Fault detection and localization method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2721–2732, May 2015.

[16] B. Li *et al.*, "Fault diagnosis and tolerant control of single IGBT open-circuit failure in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3165–3176, Apr. 2016.

[17] R. Picas, J. Zaragoza, J. Pou, and S. Ceballos, "Reliable modular multilevel converter fault detection with redundant voltage sensor," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 39–51, Jan. 2017.

[18] H. Berriri, M. W. Naouar, and I. Slama-Belkhodja, "Easy and fast sensor fault detection and isolation algorithm for electrical drives," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 490–499, Feb. 2012.

[19] G. H. B. Foo, X. Zhang, and D. M. Vilathgamuwa, "A sensor fault detection and isolation method in interior permanent-magnet synchronous motor drives based on an extended kalman filter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3485–3495, Aug. 2013.