Energy Channeling LED Driver Technology to Achieve Flicker-Free Operation With True Single Stage Power Factor Correction

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***Abstract*—A conventional single stage ac–dc LED driver usually produces significant twice-line-frequency ripple current when a high power factor is achieved. The ripple current causes a lighting flicker of the LEDs. In this paper, an energy channeling ripple cancellation LED driver is proposed. It achieves true single stage power conversion, maintains a high power factor while significantly removing the twice-line-frequency ripple current – flicker free LED driving. An 8.5 W, 50 V/0.17 A Buck–Boost experimental prototype has been built to verify the proposed method.**

***Index Terms*—Energy channeling, offline LED driver, power factor correction, single-stage power conversion.**

I. Introduction

SINGLE-STAGE LED driver is a popular design choice in the industry and can usually achieve a high efficiency and a low component cost [1]–[3]. However, when a high power factor is also obtained in the offline applications, a significant twice-line-frequency ripple is produced on the LED driving voltage. Due to the very low resistance of the LED load, excessive ripple current is generated by the ripple voltage. A single-stage offline LED driver and its Usually waveforms are illustrated in Fig. 1. Usually the percentage of the ripple current is much higher than the percentage of the ripple voltage because of the low resistance LED load.

Because of the almost linear relationship between an LED current and its lighting output, a ripple LED current is proportionally presented as the same frequency lighting fluctuation – flicker. It has been suggested from IEEE PAR1789 that excessive flicker at the twice-line-frequency has the significant adverse effect to human eyes [4], [5]. In order to reduce the flicker to an acceptable level with a single-stage LED driver, usually impractically large amount of output capacitors are needed, which significantly increases the component cost and defeats the original purpose of using single-stage LED driving structure.

A practical solution to reduce flicker is by using a two-stage LED driver. A generic implementation of a two-stage LED driver is illustrated in Fig. 2. High power factor is achieved by the first stage PFC and a flicker-free LED driving performance is achieved by the second stage dc–dc converter. There are two common implementations for the two-stage LED drivers. In one implementation, the PFC can be implemented with boost topology and the dc–dc converter is implemented with LLC topology [6]–[8]. In another implementation, the PFC can be implemented by a Flyback/Buck–Boost topology and the dc–dc converter is implemented by Buck topology [9]. In general, the first implementation can achieve relatively higher efficiency but also with higher component cost. It is more suitable for high power applications, and those are not sensitive to cost. The second implementation is more suitable for below 60 W and costs sensitive applications. Although two-stage LED drivers have much higher cost and usually lower efficiency than a single-stage LED driver, they are necessary for applications that have a tight restriction on flicker.

Many innovative LED driving methods have been proposed to reduce the component cost, remove flicker, improve efficiency, or all of the above. A single stage ac–dc multiple outputs LED driver had been proposed in [10]. Power factor correction and

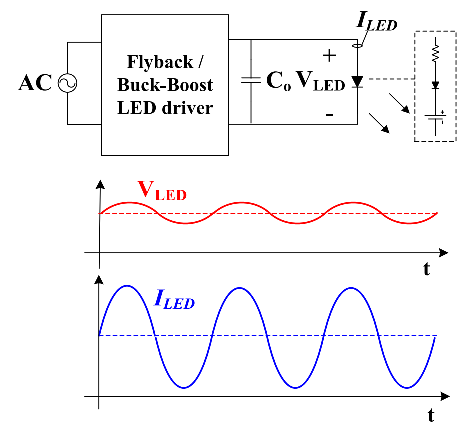

Fig. 1. Typical single-stage LED driver and its waveforms.

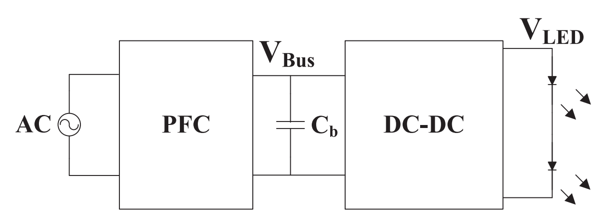

Fig. 2. Generic structure of two-stage LED Driver.

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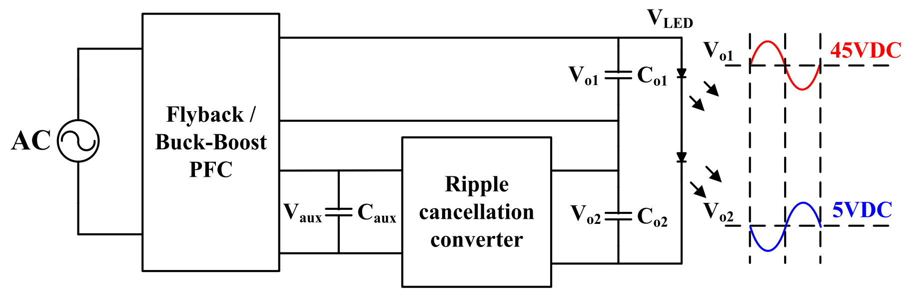


Fig. 3. Generic structure of a ripple cancellation LED Driver and its key waveforms.

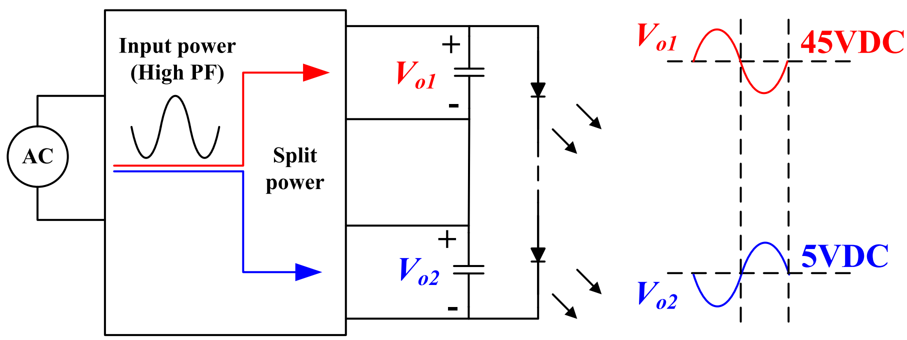


Fig. 4. Concept of the proposed energy channeling LED driver.

current balancing have been implemented with a single stage multiplexing power structure. The design achieved smaller form factor and better efficiency than the conventional current balancing methods for multiple outputs. However, this LED driving method did not include measures to solve the twice line frequency lighting flicker issue. An active energy storage method was proposed in [11] and [12]. It can achieve dc LED current driving while reducing the output capacitors. However, a considerable amount of power is converted back and forth in the system, which increases the power loss and requires a complicated, expensive bidirectional converter. A harmonic current injecting method was proposed in [13] and [14]. The LED ripple current can be reduced at the cost of reducing the power factor. It is a design tradeoff between reducing the twice-line-frequency ripple current and achieving a high power factor. A two-stage combining method was proposed in [15]. The power MOSFETs are shared between the first stage PFC and the second stage LLC converter. It can reduce the component count and, therefore, the component cost. However, neither the PFC stage nor the LLC stage can achieve optimal operation, and the operation is fairly complicated.

In order to achieve low cost and high efficiency as a single-stage LED driver and flicker-free LED driving as a two-stage LED driver, ripple cancelation LED drivers had been proposed in [16]–[22]. Fig. 3 illustrates a general implementation of a ripple cancellation LED driver.

A Flyback / Buck–Boost PFC stage produces a main output V_{o1} and an auxiliary output V_{aux}. Because of the energy imbalance between the input and the output in a half line cycle, a twice-line-frequency ripple voltage is presented on the main output V_{o1}. A ripple cancellation converter is powered by the auxiliary output V_{aux} and produces an opposite ripple voltage to cancel the twice-line-frequency ripple voltage from the main output V_{o1}. A dc LED driving voltage is, therefore, produced, and the output light is flicker free. Because the output voltage V_{o2} is much smaller than the main output V_{o1}, the power processed by the ripple cancellation converter is only a small percent of the total output power (10% or less). Therefore, the overall efficiency of the ripple cancelation LED driver is close to a single-stage LED driver and much higher than a two-stage LED driver. The component cost of the ripple cancellation LED driver is also significantly lower than that of a two-stage LED driver.

A more advantageous ripple cancellation LED driver—energy channeling LED driver was proposed in [23]. It can achieve ripple cancellation (flicker-free) LED driving without adding a ripple cancellation converter as shown in Fig. 3. Instead, the ripple cancellation voltage is generated by the same power factor correction circuit that generates the main output voltage. Therefore, the component cost is further reduced from the previously proposed ripple cancellation LED drivers. Most importantly, it achieves true single-stage power conversion. In this paper, more detailed and comprehensive operation of the energy channeling LED driver is presented.

This paper is arranged as follows. The operating principle of the proposed energy channeling LED driver is discussed in Section II. Section III discusses the special treatment for the proposed LED driver when it is operated under input voltage zero-crossing. The critical design consideration is discussed in Section IV. The experimental result is shown in Section V, and the paper is concluded in Section VI.

II. Basic Idea of Energy Channeling LED Driver

A. *Concept of the Energy Channeling LED Driver*

Fig. 4 illustrates the concept of the proposed energy channelling LED driver. It is designed to achieve a high power

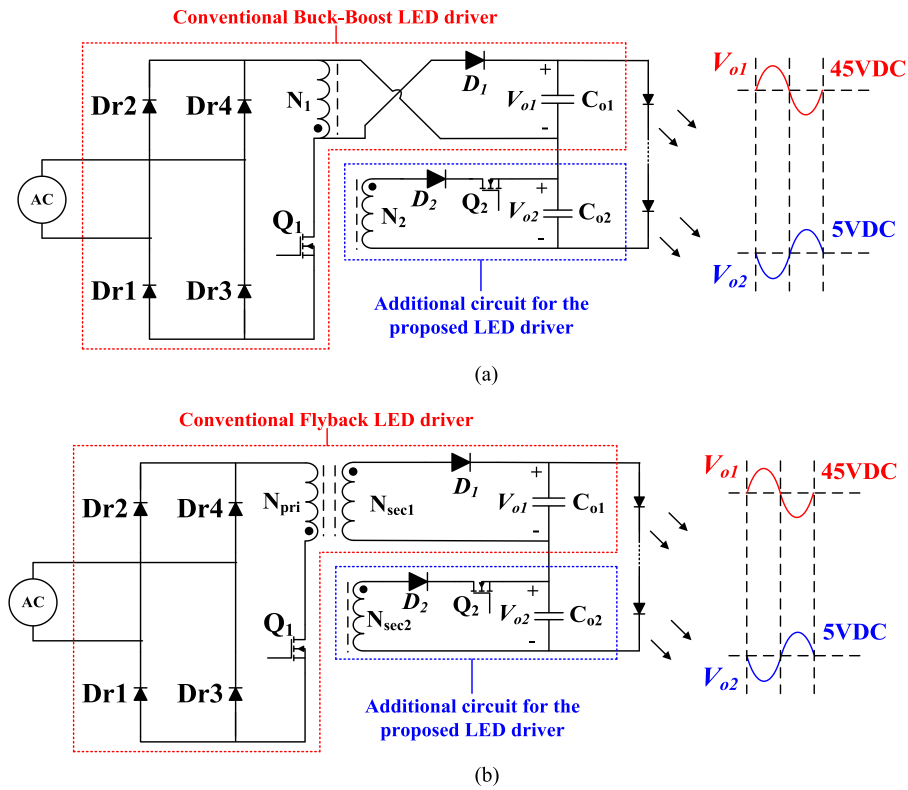


Fig. 5. Proposed energy channeling LED driver: (a) Buck–Boost topology based implementation and (b) Flyback topology-based implementation.

factor, so the input power is a sinusoidal waveform with a dc bias. The input power is split into two portions with the following strategy: the majority (90% or up in a typical design) of the input power is channeled to produce a main output V_{o1}. The remaining portion (10% or less in a typical design) of the input power is channeled to produce a much smaller output V_{o2}. For example, the output V_{o1} is averaged at 45 V while output V_{o2} is averaged at 5 V. Under this voltage ratio, the averaged input power transferred to V_{o1} and V_{o2} are 90% and 10% of the total input power, respectively. Because the input power waveform has a twice-line-frequency ripple component and the majority of the power is transferred to V_{o1}, V_{o1} has the same frequency ripple voltage. The amount of energy being channeled to V_{o2} is precisely controlled in every switching cycle in order to produce an opposite twice-line-frequency ripple voltage on V_{o2}. With V_{o1} and V_{o2} being connected in series, a dc LED voltage is produced and is used to drive the LED with ripple-free current.

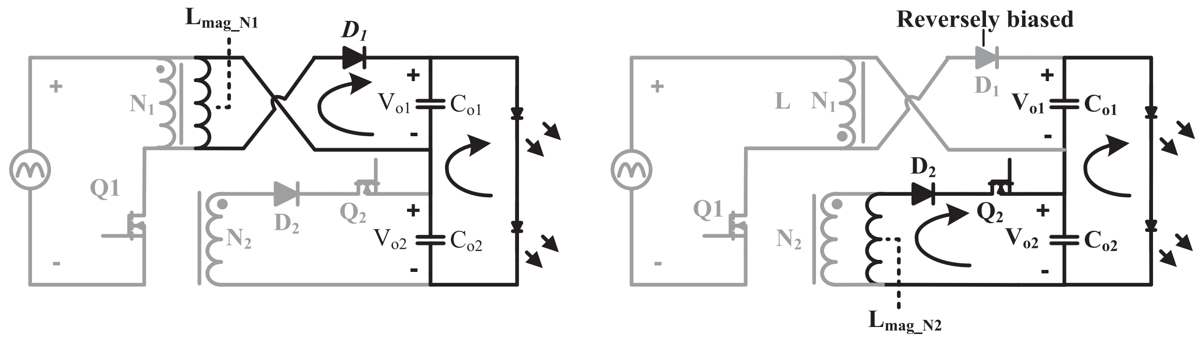
B. Circuit Implementation of the Proposed LED Driver

A Buck–Boost topology and a Flyback topology-based implementation of the proposed energy channeling LED driver are shown in Fig. 5(a) and (b). The difference between the proposed energy channeling LED driver and a conventional Buck–Boost / Flyback LED driver is highlighted. In (a), N_1 is the main winding of the inductor. By adding the winding N_2, the diode D_2, the MOSFET Q_2, and the capacitor C_{o2}, a ripple cancelation voltage V_{o2} is produced. The MOSFET Q_2 controls the inductor energy to flow to either V_{o1} or V_{o2}. After the main switching, Q_1 is turned OFF, and if Q_2 is also off, the inductor current continues to flow in winding N_1 and the inductor energy is transferred to output V_{o1}. If Q_2 is ON, the inductor current flows in winding N_2 and the inductor energy is transferred to the output V_{o2}. By controlling the pulse width of Q_2, the amount of energy being transferred to V_{o2} is precisely controlled in every switching cycle, and therefore, V_{o2} can be controlled to cancel the voltage ripple on V_{o1}. The more detailed operation will be described in the following part of this paper. The operating principle of the proposed Flyback implementation energy channeling LED driver is the same as the Buck–Boost implementation one. The energy channeling LED driving method can also be implemented on other current-fed topologies. The following discussion will base on the Buck–Boost implementation.

C. Energy Channeling Mechanism

Fig. 6 shows the concept of achieving energy channelling with the proposed LED driver. A coupled inductor with two windings is used to generate two outputs. These two outputs are connected in series as required by the proposed LED driver. The main MOSFET Q_1 is used to control the input switching current. The small MOSFET, Q_2, is used to channel energy flow and is placed in series with the V_{o2} output.

The coupled inductor is modeled as an ideal transformer with a magnetic inductor either in parallel with the winding N_1 or in parallel with the winding N_2. The magnetic inductor is energized during the on time of Q_1. After Q_1 is turned OFF, the magnetic current needs to keep flowing. In Fig. 6(a), where Q_2 is off, the magnetic current can only flow in winding N_1 and the magnetic inductor is presented as $L_{\mathrm{mag\_N1}}$. Thus, the inductor energy is transferred to the output V_{o1}. In Fig. 6(b), where Q_2 is ON, the magnetic current only flows in winding N_2 and the



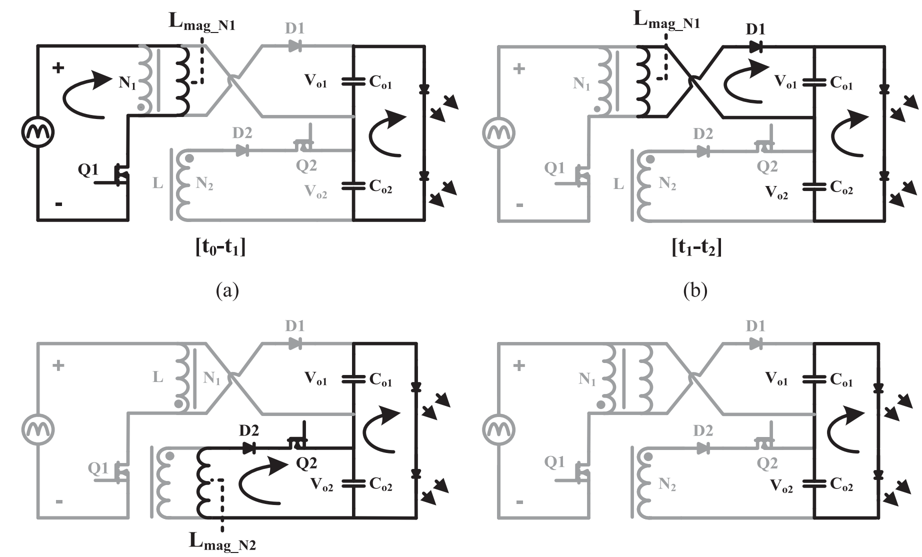
Q1 off, Q2 is off

(a)

Q1 off, Q2 is on

(b)

Fig. 6. Operating principle of the energy channeling circuit in the proposed LED driver (The dark line indicates the current flow path).



[t_0-t_1]

(a)

[t_1-t_2]

(b)

[t_2-t_3]

(c)

[t_3-t_4]

(d)

Fig. 7. One completed switching cycle operation of the proposed DCM operated Buck–Boost energy channeling LED driver (The dark line indicates the current flow path). (a) Q1 on, Q2 off, (b) Q1 off, Q2 off, (c) Q1 off, Q2 on, (d) Q1 off, Q2 on.

magnetic inductor is presented as $L_{\mathrm{mag\_N2}}$. This is achieved by mismatching the turn's ratio N_1:N$_2$ with respect to the voltage ratio $V_{o1} : V_{o2}$. The following relationship needs to be satisfied:

$$N_1 : N_2 < V_{o1} : V_{o2}. \tag{1}$$

For example, in (1), the turn's ratio $N_1 : N_2$ is 9:2 while the voltages V_{o1} and V_{o2} are 45 and 5 V, respectively (9:1). When Q_2 is ON, the voltage across the winding N_2 is clamped at 5 V (ignore the diode forward voltage drop). Because of the voltage coupling relationship, the voltage across the winding N_1 is clamped at 22.5 V. Therefore, the output diode D_1 should be reversely biased, and the inductor current only flows in winding N_2. Therefore, one design requirement is $N_1 : N_2 < V_{o1} : V_{o2}$ so that D_1 is reversely biased when Q_2 is turned ON.

D. Cycle by Cycle Operation

Fig. 7 shows a completed one switching cycle operation of the proposed Buck–Boost energy channelling LED driver. Fig. 8 shows the key switching cycle waveforms. Each switching cycle has four time intervals, and they are described as follows.

1) Interval [t_0–t_1]: A switching cycle starts from time t_0 when Q_1 is turned ON. The inductor current rises from zero, and the energy is taken from the ac input. This time interval ends at t_1 when Q_1 is turned OFF. During this time interval, the peak switching current in MOSFET Q_1, which is also the peak input switching current, can be calculated as follows:

$$I_{Q1\_pk}(t) = I_{\mathrm{in\_}pk}(t) = \frac{V_{\mathrm{in}}(t) \times T_{\mathrm{on}}}{L_{\mathrm{mag\_}N1}} \tag{2}$$

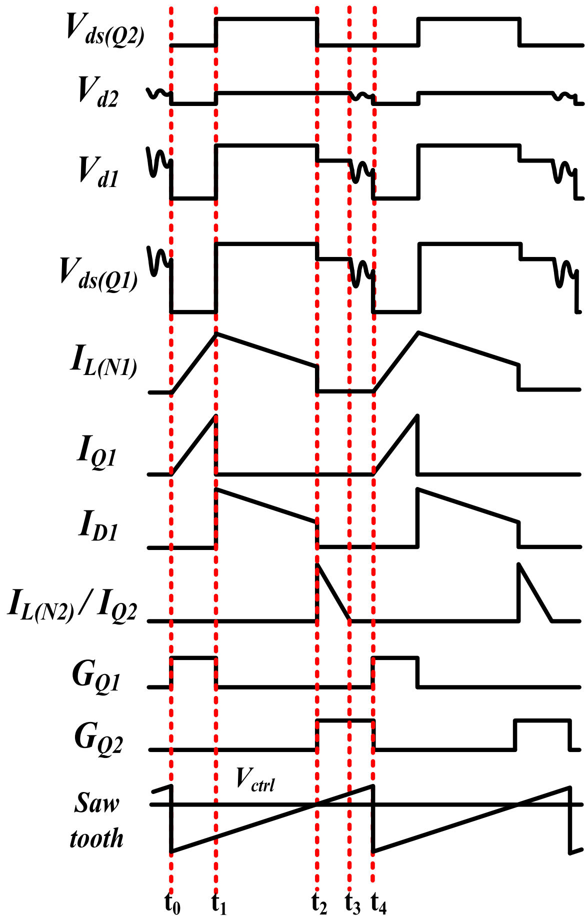


Fig. 8. Key switching cycle waveforms of the proposed DCM operated Buck–Boost energy channeling LED driver.

where T_{on} and $L_{\text{mag\_N1}}$ are the turn on time of Q_1 and the inductance of winding N_1, respectively.

The averaged input current at that switching cycle and the peak switching current can be expressed as follows:

$$I_{\text{in\_avg}}(t) = \frac{I_{\text{in\_}pk}(t) \times T_{\text{on}}}{2 \times T_s}. \tag{3}$$

The averaged input current can also be expressed as follows:

$$I_{\text{in\_avg}}(t) = \frac{I_{\text{in\_rms}}}{V_{\text{in\_rms}}} \times V_{\text{in}}(t). \tag{4}$$

Equaling the right sides of (3) and (4) yields

$$\frac{I_{\text{in\_rms}}}{V_{\text{in\_rms}}} \times V_{\text{in}}(t) = \frac{I_{\text{in\_}pk}(t) \times T_{\text{on}}}{2 \times T_s}. \tag{5}$$

Rearranging (5) yields

$$T_{\text{on}} = \frac{2 \times I_{\text{in\_rms}} \times V_{\text{in}}(t) \times T_s}{V_{\text{in\_rms}} \times I_{\text{in\_}pk}(t)}. \tag{6}$$

Substituting (6) into (2) yields

$$I_{\text{in\_}pk}(t) = V_{\text{in}}(t)\sqrt{\frac{2 \times I_{\text{in\_rms}} \times T_s}{V_{\text{in\_rms}} \times L_{\text{mag\_}N1}}}. \tag{7}$$

Also, with assuming the power conversion is lossless, the relationship between the RMS input voltage, RMS input current and the LED power can be expressed as follows:

$$I_{\text{in\_rms}} = \frac{P_{\text{LED}}}{V_{\text{in\_rms}}}. \tag{8}$$

Substituting (8) into (7) yields

$$I_{Q1\_pk}(t) = I_{\text{in\_}pk}(t) = \frac{V_{\text{in}}(t)}{V_{\text{in\_rms}}} \times \sqrt{\frac{2 \times P_{\text{LED}} \times T_s}{L_{\text{mag\_}N1}}}. \tag{9}$$

Equation (9) describes the peak switching current of Q_1 at a particular instantaneous input voltage.

Both diode D_1 and D_2 are reversely biased due to the polarity of the windings. The antiparallel diode of Q_2 is forward biased. The reverse voltages across diode D_1 and D_2 can be expressed as follows:

$$\text{During } [t_0 - t_1]:\ V_{D1\_R} = V_{\text{in}}(t) + V_{o1}(t) \tag{10}$$

$$\text{During } [t_0 - t_1]:\ V_{D2\_R} = V_{\text{in}}(t)\frac{N_2}{N_1} + V_{o2}(t). \tag{11}$$

2) Interval [t_1–t_2]: During the time interval [t_1–t_2], Q_1 is turned OFF, and Q_2 is still off. Only the circuit connecting the winding N_1, D_1, and C_{o1} provides a freewheeling loop for the inductor current. Therefore, the inductor energy is transferred to the output V_{o1} during this time interval. The peak switching current in D_1 is equal to the peak switching current in Q_1. The voltage across the MOSFET Q_1 can be expressed as follows:

$$\text{During } [t_1 - t_2]:\ V_{ds\_Q1} = V_{o1}(t) + V_{\text{in}}(t). \tag{12}$$

Because the voltage across the winding N_2 is higher than the output voltage $V_{o2}(t)$, the diode D_2 is forward biased while the body diode of Q_2 is reversely biased. The voltage across Q_2 can be expressed as follows:

$$\text{During } [t_1 - t_2]:\ V_{ds\_Q2} = V_{o1}(t)\frac{N_2}{N_1} - V_{o2}(t). \tag{13}$$

3) Interval [t_2–t_3]: Q_2 is turned ON at time t_2 when the control signal, V_{ctrl}, and the sawtooth signal cross. The inductor current commutes from the winding N_1 to the winding N_2 at t_2. This way, the remaining inductor energy is transferred to the output V_{o2}. The peak switching current in Q_2, $I_{Q2\text{\_peak}}$, can be expressed as follows:

$$I_{Q2\_\text{peak}}(t) = \frac{V_{o2}(t) \times (t_3 - t_2)}{L_{\text{mag\_}N2}}. \tag{14}$$

In (14), $L_{\text{mag\_N2}}$ is the inductance value of the winding N_2. The inductance of winding N_2 is proportional to the square of its turn's number and can be expressed as follows:

$$L_{\text{mag\_}N2} = L_{\text{mag\_}N1} \times \left(\frac{N_2}{N_1}\right)^2. \tag{15}$$

At the same time, the current flowing through Q_2 contributes to the LED current and charges the capacitor C_{o2}. Therefore, another equation can be established as follows:

$$\frac{I_{Q2\_\text{peak}}(t) \times (t_3 - t_2)}{2T_s} = I_{\text{LED}} + \frac{\Delta V_{o2}(t) \times C_{o2}}{T_s}. \tag{16}$$

In (16), T_{s} is the switching period, C_{o2} is the output capacitor of V_{o2}, and $\Delta\text{V}_{o2}(\text{t})$ is the voltage change on C_{o2} in that

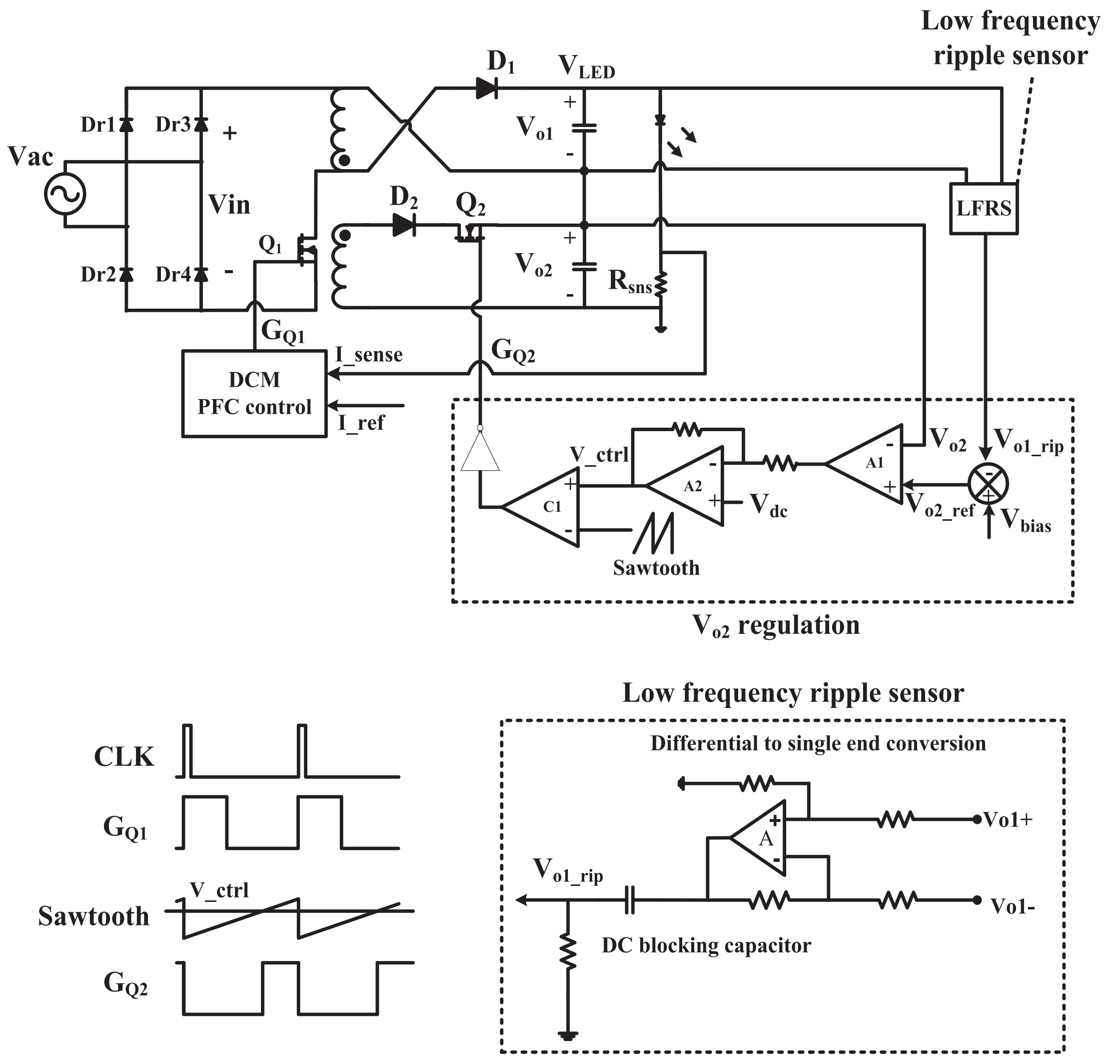


Fig. 9. Control diagram of the proposed LED Driver.

switching cycle. The term $\frac{\Delta V_{o2}(t)\times C_{o2}}{T_s}$ in (16) can be ignored in the calculation since it is much smaller than the term I_{LED}. Combining (14) and (16) yields

$$I_{Q2\_\mathrm{peak}} = \sqrt{\frac{2\times V_{o2}(t)\times I_{\mathrm{LED}}\times T_s}{L_{\mathrm{mag}\_N2}}} \tag{17}$$

$$t_3 - t_2 = \sqrt{\frac{2\times L_{\mathrm{mag}\_N2}\times I_{\mathrm{LED}}\times T_s}{V_{o2}(t)}}. \tag{18}$$

The RMS current of Q_2 in that switching cycle can be calculated as follows:

$$I_{Q2\_\mathrm{rms}} = \sqrt{\frac{(t_3-t_2)}{3T_s} I^2_{Q2\_\mathrm{peak}}}. \tag{19}$$

Substituting (18) and (19) into (17) yields

$$I_{Q2\_\mathrm{rms}} = \frac{\left(\frac{2\times L_{\mathrm{mag}\_N2}\times I_{\mathrm{LED}}\times T_s}{V_{o2}(t)}\right)^{1/4}}{\sqrt{3}} \times \sqrt{\frac{2\times V_{o2}(t)\times I_{\mathrm{LED}}}{L_{\mathrm{mag}\_N2}}}. \tag{20}$$

The voltage across MOSFET Q_1 and diode D_1 can be Expressed as follows:

$$\text{During } [t_2 - t_3]:\ V_{ds\_Q1} = V_{\mathrm{in}}(t) + V_{o2}(t)\frac{N_1}{N_2} \tag{21}$$

$$\text{During } [t_2 - t_3]:\ V_{D1\_R} = V_{o1}(t) - V_{o2}(t)\frac{N_1}{N_2}. \tag{22}$$

4) Interval [t_3–t_4]: In order to achieve a high power factor and straightforward implementation, the proposed LED driver is designed to operate under DCM. There is a short time interval [t_3–t_4] when the inductor current remains zero before the start of the next switching cycle. Q2 remains on with the proposed LED driver. Since the magnetic current is already zero, the status of Q2 is not important during the time interval [t_3–t_4]. Q2 can also be off during the time interval [t_3–t_4] if it is desired.

The aforesaid operations illustrate that the proposed LED driver achieves single stage power conversion. During the time interval [t_0-t_1], the energy is transferred from the ac source to the inductor. During the time interval [t_1-t_2], the energized inductor transfers the majority portion of its energy to the output

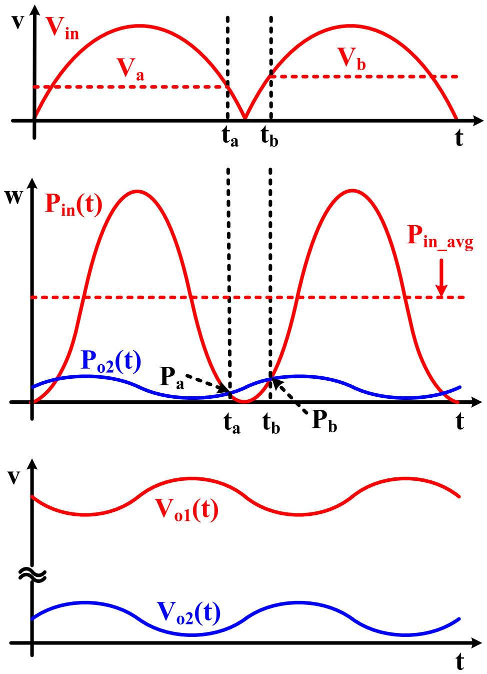


Fig. 10. Critical line frequency waveforms of the proposed LED driver.

V_{o1}. During the time interval $[t_2 - t_3]$, the inductor transfers its remaining energy to the output V_{o2}. In one switching cycle, the inductor is charged and discharged for only one time while transferring the energy from the input to the output.

E. Control Scheme

Fig. 9 shows the control diagram of the proposed Buck–Boost energy channeling LED driver. There are two control loops with the proposed LED driver: the LED current regulation loop and the output V_{o2} voltage regulation loop. A PFC controller is used to control the input current to follow the rectified input voltage (achieve high power factor) and to achieve LED current regulation. A voltage controller is used to control the output voltage V_{o2} and achieve ripple cancellation between V_{o1} and V_{o2}.

The PFC controller automatically adjusts the duty ratio of Q_1 to achieve LED current regulation. The change of the duty cycle on Q_1 leads to change of the RMS input current and eventually results in the change of the dc level of V_{o1}. The dc level of V_{o1} settles to the value that produces the exact level of LED current required by the current reference. In the control scheme, the dc level of V_{o2} is constant and does not participate in the LED current regulation.

The output V_{o2} voltage control loop works as follows. First, the twice-line-frequency ripple voltage of V_{o1}, V_{o1_rip} is sensed. The sensed ripple voltage is inverted and added with a dc bias voltage $V_{\rm bias}$. The result, which contains a reverse ripple voltage of V_{o1}, becomes the reference voltage of output V_{o2}. The voltage control loop automatically adjusts the level of $V_{\rm ctrl}$. By the comparing the sawtooth and the control signal $V_{\rm ctrl}$, the pulse width of Q_2 is precisely produced in every switching cycle. With a well-designed feedback loop, V_{o2} closely follows its reference voltage and therefore contains an opposite twice-line-frequency ripple voltage to achieve ripple cancelation. One should also note that sawtooth signal and the clock signal for the PFC controller are synchronized in every switching cycle to operate Q_2 at the correct timing.

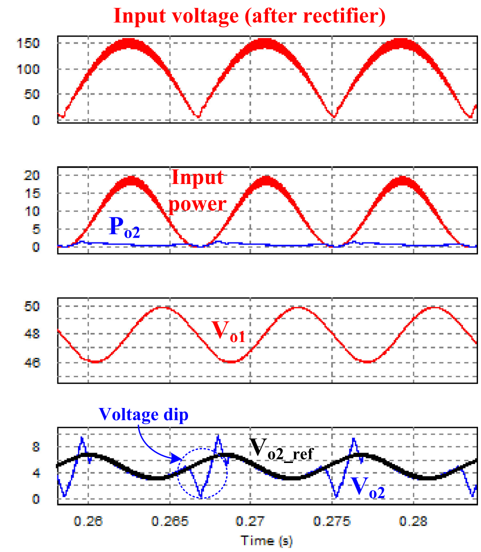


Fig. 11. Voltage dip on V_{o2} near the input voltage zero crossing.

At the startup, the PFC controller starts operating and the output V_{o1} rising from zero. V_{o1} keeps increasing until the produced averaged LED current is equal to the current reference. At the same time because V_{o2} is also zero, the voltage V_{o2} control loop forces the control signal $V_{\_\rm ctrl}$ stay at the minimum. Because of leading edge modulation, Q_2 is operated at the maximum turn on time in every switching cycle, and V_{o2} also starts rising from zero. $V_{\_\rm ctrl}$ stay at minimum and Q_2 is operated at maximum turn on time until V_{o2} is equal to its reference. The LED driver enters the stable operation when the LED current and V_{o2} are within regulation.

III. Special Treatment During Input Voltage Zero Crossing

As discussed in Section II, the energy needed to sustain V_{o2} comes from the inductor (also means from the ac input source) in every switching cycle. By carefully examining the input power waveform in Fig. 10, it can be observed that the instantaneous input power is lower than the expected output power of $V_{o2}(t)$, $P_{o2}(t)$, during the time interval $[t_a - t_b]$. The instantaneous input voltage at the time t_a and t_b are V_a and V_b, respectively. Without any techniques to address this issue, the output V_{o2} will lose regulation.

Fig. 11 verifies the above analysis with simulation. The instantaneous input power is lower than the power $P_{o2}(t)$ during the zero crossing of the input voltage. V_{o2} loses regulation and experiences a voltage dip.

In order to solve the aforesaid issue and keep V_{o2} being regulated, the instantaneous input power need to be always higher than P_{o2} (t). Different methods can be implemented to keep input power higher than $P_{o2}(t)$. One way that is easier to implement is shown in Fig. 12. Instead of allowing the rectified

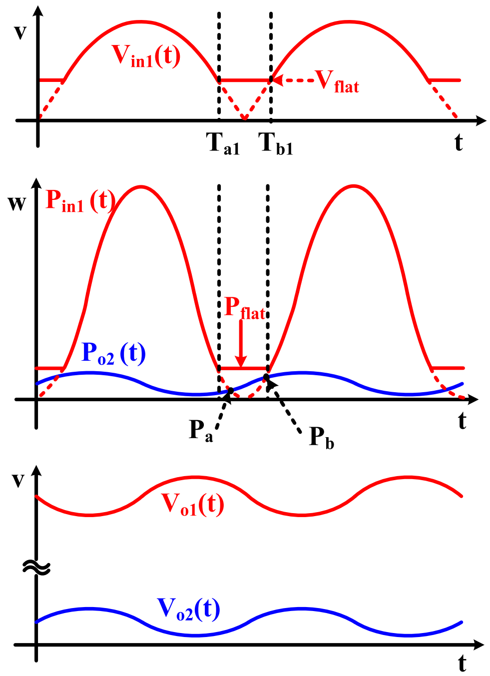


Fig. 12. Reshaping the input voltage and results in the reshaped input power.

input voltage fall to zero at the ends of a half line cycle in a conventional design, the rectified input voltage is flattened at the level $V_{\rm flat}$ during the time interval $[t_{a1}-t_{b1}]$ in a half line cycle. Because the input current follows the input voltage, the input current should also be flattened in the same time interval. Therefore, the input power also becomes flat during $[t_{a1}-t_{b1}]$. As long as the flat part, $P_{\rm flat}$, is higher than P_b, the input power is always greater than $P_{o2}(t)$, where P_b is the higher crossover point between the original input power waveform and $P_{o2}(t)$.

Flatting the input voltage (after the input bridge rectifier) can be implemented with a modification of the power stage circuit shown in Fig. 13. An auxiliary voltage $V_{\rm flat}$ is produced from another winding $N_{\rm aux}$. $V_{\rm flat}$ represents the flat part of the after rectifier input voltage. The diode D_b is used to block $V_{\rm flat}$ from the rectified ac input voltage. When the absolute value of the ac input voltage is higher than $V_{\rm flat}$, the diode D_b is reversely biased. The power delivered to the LED load is from the ac input power. When the absolute value of the ac input voltage is lower than $V_{\rm aux}$, D_b is forward biased, and the input bridge rectifier is reversely biased. The energy stored in $C_{\rm aux}$ provides the energy to V_{o2}.

Fig. 14 shows the simulation result of the modification on the power stage circuit shown in Fig. 13. During the time intervals $[t_{a1}-t_{b1}]$, the input power is flattened and kept higher than $P_{o2}(t)$. As a result, the voltage dip on V_{o2} is removed, and V_{o2} follows its reference voltage very well. During the same time interval, the energy supplying the output V_{o2} is from the capacitor $C_{\rm aux}$, which causes $V_{\rm flat}$ decrease from 41.7 to 39.5V. With $C_{\rm aux}$ being 20 μF in the simulation, the amount of energy provided by $C_{\rm aux}$ is calculated to be around 2 mJ, which contributes 3% of the total energy (or around 70 mJ) supplied to the LED load in a half line cycle. Since the winding $N_{\rm aux}$ refills the energy to capacitor $C_{\rm aux}$, $N_{\rm aux}$ does not carry significant current and very small size wire can be used to save the winding space.

As the input rectifier is reversely biased, a zero-crossing distortion is introduced for the ac input current. In order to minimize this impact, it is desirable to design $V_{\rm flat}$ as low as possible. Meanwhile, $V_{\rm flat}$ should be high enough to generate the $P_{\rm flat}$ that is no less than P_b. As shown in Fig. 11, the input voltage is equal to V_b when the input power is equal to P_b. Therefore, $V_{\rm flat}$ should be designed slightly higher than V_b. The process of deriving the voltage V_b is shown as follows.

The input voltage and the input current can be expressed as follows:

$$V_{\rm in}(t) = \sqrt{2}\times V_{\rm in\_rms}\cos(2\pi\times f_{\rm line}\times t) \tag{23}$$

$$I_{\rm in}(t) = \sqrt{2}\times I_{\rm in\_rms}\cos(2\pi\times f_{\rm line}\times t). \tag{24}$$

Therefore, the input power waveform can be expressed as follows:

$$P_{\rm in}(t) = 2V_{\rm in\_rms}\times I_{\rm in\_rms} + P_{\rm in\_avg}\cos\left(4\pi\times f_{\rm line}\times t\right) \tag{25}$$

also, we have

$$\frac{V_{\rm in\_rms}}{I_{\rm in\_rms}} = \frac{V_{\rm in}(t)}{I_{\rm in}(t)} \tag{26}$$

and

$$P_{\rm in\_avg} = V_{\rm in\_rms}\times I_{\rm in\_rms}. \tag{27}$$

Substituting (27) into (26), the relationship between input power and input voltage can be further expressed as follows:

$$P_{\rm in}(t) = \frac{V_{\rm in}(t)^2\times P_{\rm in\_avg}}{V_{\rm in\_rms}^2}. \tag{28}$$

At the same time, the ripple of the V_{o2} output power is 270° out phase of the ripple of the input power, $P_{o2}(\rm t)$ can be expressed as follows:

$$P_{o2}(t) = P_{o2\_\rm avg} + P_{o2\_\rm rip\_pp}\times\cos\left(4\pi\times f_{\rm line}\times t - \frac{3}{2}\pi\right) \tag{29}$$

where

$$P_{o2\_\rm avg} = V_{o2\_\rm avg}\times I_{\rm LED}. \tag{30}$$

And $P_{o2\_\rm rip\_pp}$ is the peak to peak ripple of the V_{o2} output power. By combining (25), (28), and (29), the mathematic expression for V_b can be solved. The output $P_{o2}(\rm t)$ is around its averaged value when $P_{o2}(\rm t)$ and $P_{\rm in}(\rm t)$ cross. As approximation, the $1.3P_{o2}$_avg can be used to substitute the left side of (28) to obtain the optimum $V_{\rm flat}$ as follows:

$$V_{\rm flat} = V_{\rm in\_rms}\times\sqrt{1.3\times\frac{V_{o2\_\rm avg}}{V_{\rm LED}}}. \tag{31}$$

As shown by (31), if $V_{o2\_avg}/{\rm V_{LED}}$ is designed to be constant, the required $V_{\rm flat}$ changes proportionally with the RMS input voltage. The maximum requirement for $V_{\rm flat}$ occurs when the RMS input voltage is at the maximum. For example, under 110-Vrms nominal input with variation from 90 to 130 Vrms, the maximum $V_{\rm flat}$ is required when the input voltage is 130 Vrms.

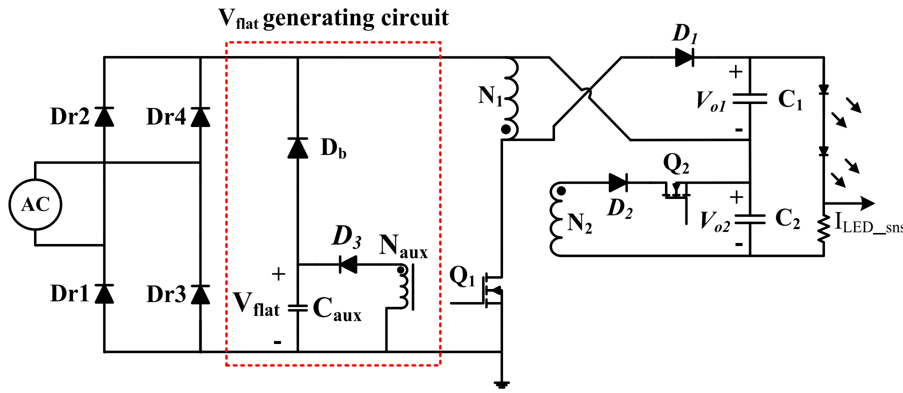


Fig. 13. Power stage of the energy channeling LED driver with the added flat input voltage V_{flat}.

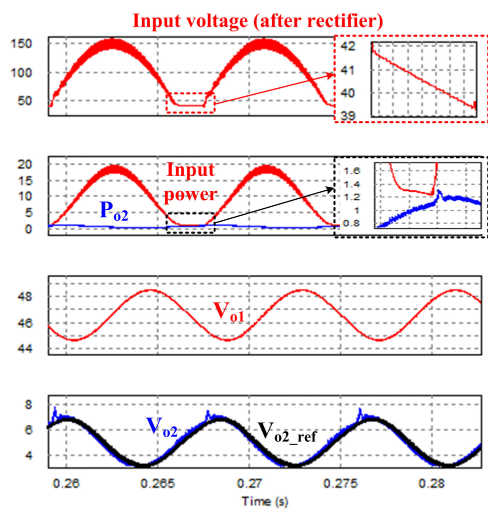


Fig. 14. Reshape the input power to remove the voltage dip on V_{o2}.

With V_{flat} being designed for 130 Vrms input, the entire operating condition can be covered. With V_{o2}_avg to be 5 V, V_{LED} to be 50 V, the voltage V_{flat} under 130 Vrms input is calculated to be around 45 V by using (31).

However, when universal ac input voltage (120/220 Vrms) is required; V_{flat} should be around 90 V for input voltage of 265 Vrms. This would be too high for 90-Vrms input. Therefore, an adaptive V_{flat} generating scheme is introduced. For example, when 110-Vrms input voltage is detected, the system will generate 45 V for V_{flat}. When 220-Vrms input voltage is detected, the system will generate 90 V for V_{flat}. The improved circuit is shown in Fig. 15.

Two levels of auxiliary voltage, V_{flat1} and V_{flat2}, can be produced by the circuit. The turns' ratio between the winding N_{aux1} and N_{aux2} is 1:1. An RMS input voltage detection circuit is used to determine whether the LED driver is connected to 220-V input voltage rail or 110-V input voltage rail. As a low-cost implementation, a resistor divider with a filter capacitor C_{rms} can also be used to control MOSFET Q_3. When 110-Vrms input voltage is detected, the comparator will keep the MOSFET Q_3 off. Therefore, the winding N_{aux2} is not working. The voltage V_{flat1} is proportional to the winding N_{aux1}. When 220-Vrms input voltage is detected, the comparator turns ON Q_3 and the winding N_{aux2} starts working. Because N_{aux1} is equal to N_{aux2}, the voltage V_{flat2} is, therefore, two times of V_{flat1} and V_{flat1} becomes idle. Fig. 16 shows the simulation results with the adaptive V_{flat} generating scheme. The flat voltage, V_{flat}, is equal to 40 V under 110-Vrms input while is equal to 80 V under 220-Vrms input.

IV. Critical Design Considerations

In the aforesaid sections, the basic working principle of the proposed energy channeling LED driver has been introduced. In this section, more detailed design considerations will be included.

A. *Pulse Width Modulation Scheme for Q2*

MOSFET Q_2 is controlled under leading edge modulation. The turn off edge of G_{Q2} is fixed at the end of the switching cycle while the turn-on edge is determined by the crossover of the saw tooth and V_{ctrl}. The inductor current commutes from winding N_1 to winding N_2 when it has already been greatly reduced from its peak. For example, 10% and 90% of the inductor energy is delivered to V_{o2} and V_{o1}, respectively in Fig. 17. It can be calculated that when applying leading edge modulation on Q_2, the peak switching current of Q_2 (with reflect to the main winding) is 31.6% of the peak inductor current.

B. *Additional Conversion Loss Minimization*

For the proposed Buck–Boost energy channeling LED driver, the operation during the time interval $[t_0 - t_1]$ and $[t_1 - t_2]$ is the same as the conventional Buck–Boost LED driver. Therefore, this part of the conversion loss will not be discussed. The different operation occurs on the time interval $[t_2 - t_3]$ and the conversion loss is identified as follows.

First, there is the conducting loss with the diode D_2 and Q_2 during the time interval $[t_2 - t_3]$. Equation (20) gives the RMS current of the D_2 and Q_2 in one switching cycle and the parameters $L_{\mathrm{mag\_N2}}$, V_{o2} and T_s affect the RMS current. Changing these parameters can reduce the RMS current in D_2 and Q_2. However, all these parameters are also restricted by the other design considerations. Changing these parameters will not benefit the overall design given the fact that less than10% of the output power is delivered through V_{o2} Therefore, in order to

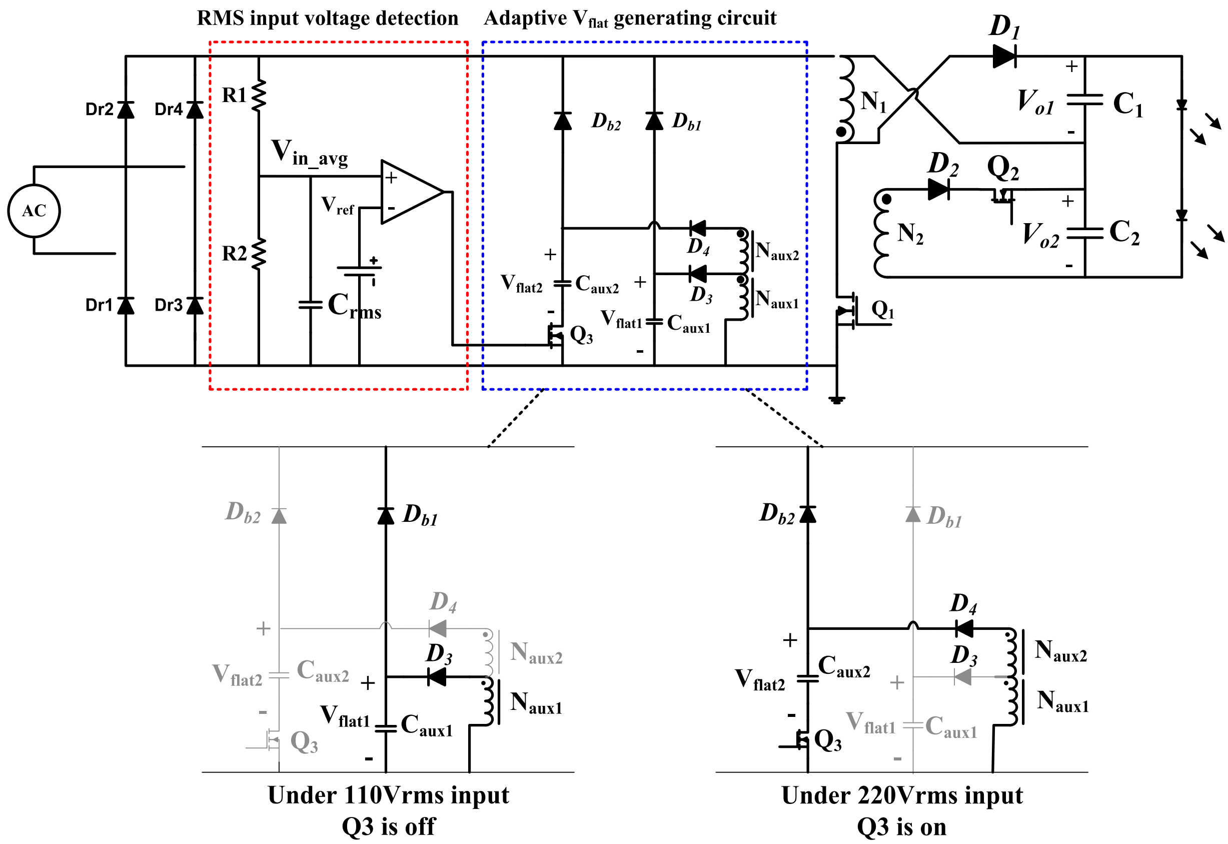


Fig. 15. Adaptive $V_{\rm flat}$ circuit to cover universal range input voltage (The darker line in the $V_{\rm aux}$ generating circuit indicates the current flow path).

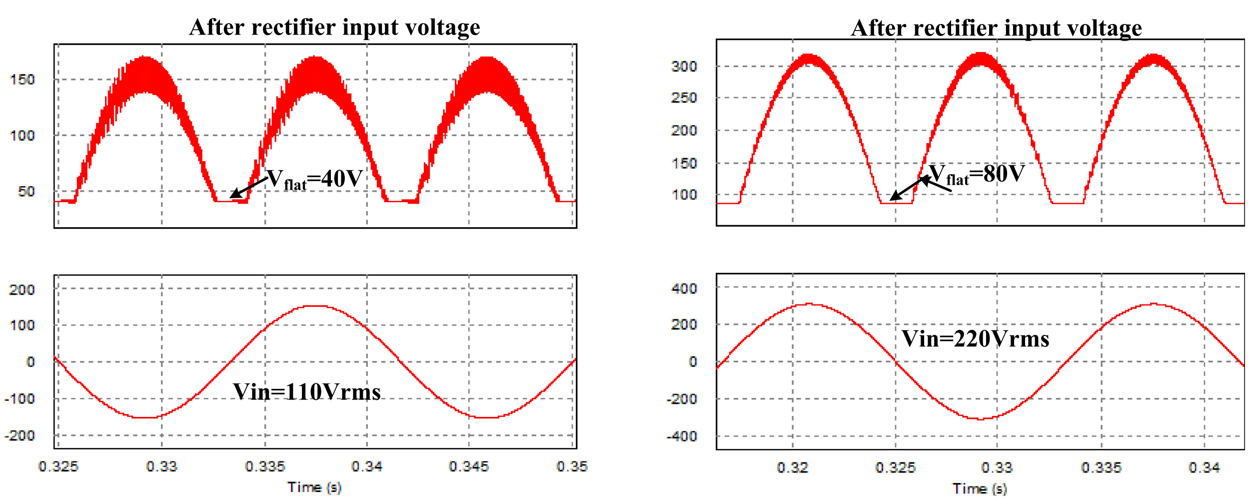


Fig. 16. Simulated key waveforms of the adaptive $V_{\rm flat}$ generating.

reduce the conduction loss, the most effective way is to use low on-resistance diode D_2 and MOSFET Q_2.

There are also switching loss during this time interval. The inductor current commutes from the winding N_1 to winding N_2 at time t_2. The diode D_2 is already forward biased before the time t_2. Therefore, the switching loss with the diode D_2 is zero. This transition is hard switching for the MOSFET Q_2 and the main output diode D_1.

For the MOSFET Q_2, the switching loss can be further divided into V-I overlap switching loss, gate charging switching loss and MOSFET output capacitor loss. For the V-I overlap loss with Q_2, the general rule applies here: minimize the turn on transition time, reduce the voltage and current stress. Equations (13) and (17) give the voltage and the current stress of Q_2 in one switching cycle. The parameters N_1:N$_2$, T_s, V_{o2}, and $L_{\rm mag\_N2}$ affect the voltage and current stress. Again, these parameters are restricted by other design considerations, and it will not effectively improve the overall efficiency by changing these parameters. However, one can reduce the current spark with Q_2 to reduce the V-I overlap switching loss. The current spark is

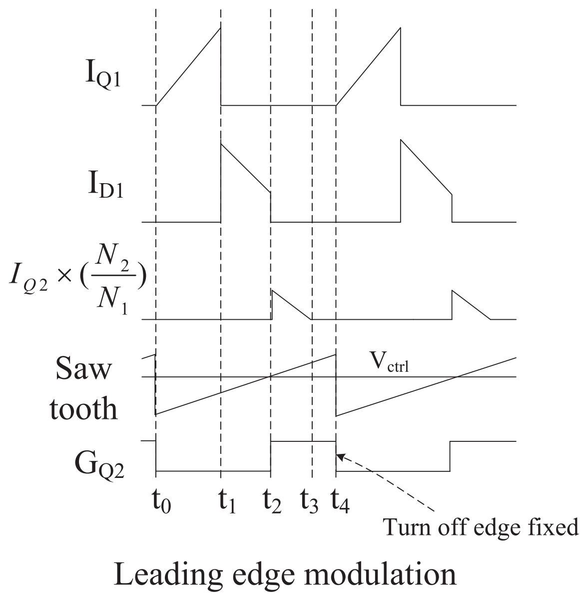


Fig. 17. Applying leading edge modulation on Q_2 ($I_{Q2} \times \frac{N_2}{N_1}$ represents the reflected current in Q_2 with respect to the main winding).

induced by the reverse recovery of the main output diode D_1. By choosing a Schottky diode for D_1, the current spark with Q_2 and the switching loss associated with the reverse recovery of D1 can be greatly avoided. For the gate charge loss and MOSFET output capacitor loss, one can select the low gate charge and low output capacitor MOSFET for Q_2.

Although generating V_{o2} introduces extra power loss, this portion can be managed to be a very small portion of the overall power loss as long as the aforesaid suggested design practice is applied.

C. Component Selection

1) Selection of Capacitor C_{o1}: The function of capacitors C_{o1} and the C_{o2} is different in the proposed LED driver. Since the majority of the input power is transferred to the output V_{o1}, the capacitor C_{o1} is used to buffer most of the energy imbalance between the input and the output in a half line cycle. The peak to peak amplitude of the V_{o1}'s twice-line-frequency ripple is directly related to the capacitance of C_{o1} and their relationship can be approximately expressed as follows:

$$V_{o1\_\mathrm{rip\_pp}} \approx \frac{I_{\mathrm{LED}}}{2 \times \pi \times f_{\mathrm{line}} \times C_{o1}} \tag{32}$$

where in (32), $V_{o1\_\mathrm{rip\_pp}}$ represents the peak to peak amplitude of V_{o1}'s twice-line-frequency ripple voltage. A smaller capacitor C_{o1} will result in a larger ripple voltage on V_{o1}. It is desirable to use a smaller C_{o1} to reduce component cost.

Although the ESR of the capacitors also produce ripple on V_{o1} (also on V_{o2}), the actual twice line frequency ripple created by the ESR is ignorable as compared to the ripple generated by the imbalanced energy between the input side and the output side in a half line cycle. Besides, the total twice line frequency ripple voltage (produced from both energy imbalance and from ESR) of V_{o1}, as a whole, is sensed by the control system. It will be cancel by the ripple voltage of V_{o2}. Therefore, the impact of the ESR is not a problem in design.

Because the ripple voltage from V_{o1} is compensated, a larger ripple voltage from V_{o1} does not have a direct impact on the output light flicker. However, it will affect the power factor performance. When the ripple voltage from V_{o1} is increased, the ripple voltage and the dc value of V_{o2} will need to be increased to achieve compensation. According to (31), V_{flat} needs also be designed with higher value when the dc value of V_{o2} is increased. By rearranging the (31), the maximum dc voltage of V_{o2} can be approximately expressed as follows:

$$V_{o2\_\mathrm{avg\_max}} = 0.59 \times \left(\frac{V_{\mathrm{flat}}}{V_{\mathrm{in\_rms}}}\right)^2 \times V_{\mathrm{LED}}. \tag{33}$$

One can design the dc voltage of V_{o2} to be 1.2 times of the peak amplitude of its ripple as shown in

$$V_{o2\_\mathrm{avg}} = 1.2 \times \left(\frac{1}{2} V_{o1\_\mathrm{rip\_pp}}\right). \tag{34}$$

Combining (32)–(34) yields

$$C_{o1\_\min} = \frac{I_{\mathrm{LED}}}{\pi \times f_{\mathrm{line}} \times 2 \times V_{\mathrm{LED}}} \times \left(\frac{V_{\mathrm{in\_rms}}}{V_{\mathrm{flat}}}\right)^2. \tag{35}$$

Therefore, when I_{LED}, V_{LED}, and V_{flat} (V_{flat} is close related to the zero-crossing distortion) are determined, the minimum capacitor C_{o1} can be selected according to (35). C_{o1} should be chosen considering both the cost as well as its impact to input current zero-cross distortion. In the experimental prototype, the C_{o1} value is chosen to be 133 μF (100 μF + 33 μF).

2) Selection of Capacitor C_{o2}: The capacitor C_{o2} is only used to filter the switching frequency ripple of the output V_{o2}. A small ceramic capacitor, in the range of approximately 10 μF, is usually enough for a low-power design.

3) Selection of Capacitor C_{aux}: During the zero crossing of the input voltage, the capacitor C_{aux} provides the energy to V_{o2}. Therefore, the voltage on C_{aux} is decreased. The capacitor C_{aux} should be designed to meet the following requirement:

$$\frac{1}{2} C_{\mathrm{aux}} V_{\mathrm{flat}}^2 - \frac{1}{2} C_{\mathrm{aux}} (V_{\mathrm{flat}} - \Delta V)^2 > E \tag{36}$$

where ΔV and E represent the voltage drop on C_{aux} and the amount of energy transferred from capacitor C_{aux} to V_{o2} in a half line cycle. E can be approximately expressed as follows:

$$E = P_{\mathrm{flat}} T_{\mathrm{flat}}. \tag{37}$$

T_{flat} represents the time that input bridge rectifier is reverse biased. It can be calculated as follows:

$$T_{\mathrm{flat}} = \frac{\arccos\left[1 - \frac{P_{\mathrm{flat}}}{P_{\mathrm{in\_avg}}}\right]}{\pi \times f_{\mathrm{line}}}. \tag{38}$$

Also, the instantaneous input voltage and the input power have the following relationship:

$$P_{\mathrm{in}}(t) = \frac{V_{\mathrm{in}}(t)^2 \times P_{\mathrm{in\_avg}}}{V_{\mathrm{in\_rms}}^2}. \tag{39}$$

Substituting the input voltage in (39) with V_{flat} yields

$$P_{\text{flat}} = \frac{V_{\text{flat}}^2 \times P_{\text{in\_avg}}}{V_{\text{in\_rms}}^2}. \tag{40}$$

Combining (36)–(38) and (40) yields

$$C_{\text{aux}} \geq \frac{2 \times V_{\text{flat}}^2 \times P_{\text{in\_avg}} \times \arccos\left[1 - \frac{V_{\text{flat}}^2}{V_{\text{in\_rms}}^2}\right]}{(2V_{\text{flat}} - \Delta V) \times \Delta V \times \pi \times f_{\text{line}} \times V_{\text{in\_rms}}^2}. \tag{41}$$

For example, under 110-*V*rms input voltage, with V_{flat} and ΔV being designed at 40 and 3 V, respectively, C_{aux} is calculated to be higher than 26 µF. Since both (37) and (40) are all approximation expression, the result that calculated with (41) is reasonably accurate.

4) Coupled Inductor Design: It is important to select the value for the magnetizing inductor (looking from ac voltage side) and the winding turns, N_1 and N_2. As the circuit operates the same as the conventional Buck–Boost LED driver from power factor correction point of view, the magnetizing inductor value can be selected in the same way as the conventional LED driver [24].

Once the magnetizing inductance is selected, N_1 can be determined based on the core size. N_2 should be chosen to meet the relationship described by (1). The turn's ratio of N_1:N$_2$ affects the voltage stresses of D_2 and Q_2 as indicated by (11) and (13). Once the inductance of the winding N_1 is determined, the turn's ratio also affects the inductance of the winding N_2. As indicated by (17), the current stresses of Q_2 and D_2 are related to the inductance of winding N_2. Therefore, the selection of N_1:N$_2$ should also consider the impact to the voltage and current stress of Q_2 and D_2. The winding N_1 and N_2 are 90 and 20 turns, respectively, in the proposed LED driver.

5) MOSFET Q1 and Diode D1: For the proposed LED driver, the voltage and current stresses for D_1 and Q_1 can be calculated the same way as in a conventional Buck–Boost converter design. Equations (10) and (12) express the current and voltage stress of D_1 and Q_1. As also shown in Fig. 18, the voltage and current stresses on Q_1 and D_1 are similar to those in a conventional single-stage LED driver design. Therefore, Q_1 and D_1 can be selected by following the general guideline used to design a conventional single-stage LED driver.

6) MOSFET Q2 and Diode D2: The current rating for Q_2 and D_2 can be chosen according to (17). Since I_{LED}, T_s, and $L_{\text{mag\_N2}}$ are fixed values in design, the peak switching current of Q_2/D$_2$ changes along with the output $V_{o2}(\text{t})$. The maximum peak switching current occurs when V_{o2} is at its maximum, which agrees with the fact that the most amount of inductor energy is needed to sustain V_{o2} when V_{o2} is at its maximum value. The voltage rating for Q_2 and D_2 can be chosen according to (11) and (13). Both the voltage and current stress of Q_2 and D_2 relies on the turn's ratio N_1:N$_2$. With the experimental prototype, N_1:N$_2$ is set to be 9:2, a reasonably small voltage and current stress of Q_2 and D_2 are obtained.

The components stresses of the proposed LED driver, as well as a conventional LED driver, are shown in Fig. 18. The voltage and current stress of Q_1, D_1 are almost the same, which is 200 V and 1.2-A peak in both designs under 110-*V*rms input. In the proposed LED driver, the voltage and current stresses of D_2 are 35 V and 1.6-A peak, respectively. The voltage and current stress of Q_2 are 8.1 V and 1.6-A peak, respectively, which are reasonably low.

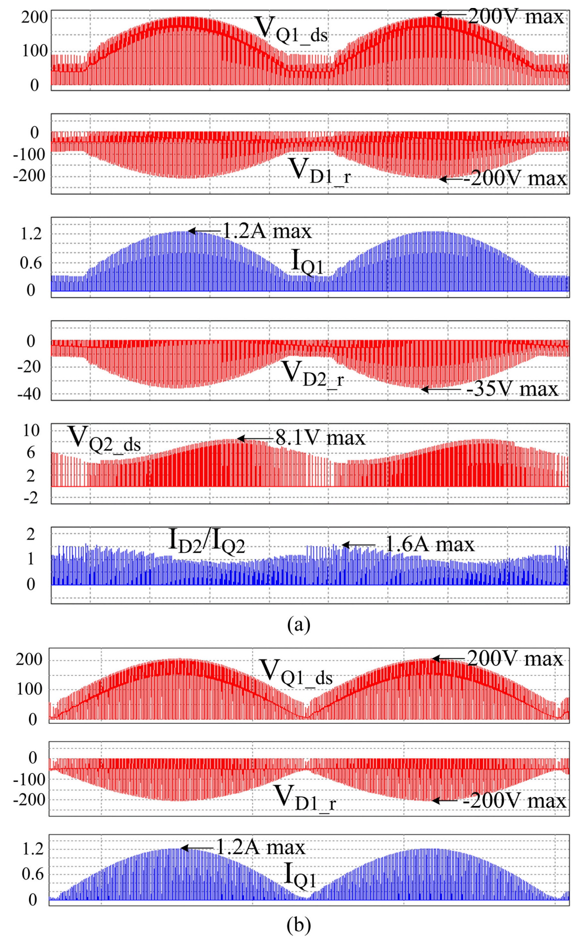


Fig. 18. Simulation result of the components voltage / current rating: (a) Proposed Buck–Boost LED driver. (b) Conventional Buck–Boost LED driver (under 110-*V*rms input).

V. Experimental Result

An 8.5 W, 50 V/0.17 A output experimental prototype is built to verify the proposed energy channeling LED driving method. Table I shows the critical component of the experimental prototype.

Fig. 19 shows the 120-Hz twice-line-frequency ripple current comparison between the proposed energy channeling LED driver and a conventional Buck–Boost LED driver. These two LED drivers are connected with the same 133 µF (100 µF + 33 µF) output capacitors and the same LED loads. Fig. 19(a) shows the key waveforms of the proposed LED driver. Ripple voltage cancelation is achieved between the main output V_{o1} and the small output V_{o2}. A dc LED voltage is produced and drive LED load with a dc LED current. The 120-Hz twice-line-frequency LED ripple current is measured to be around 20-mA peak to peak with the proposed LED driver, which is only 5.8% of the averaged 170-mA LED current. Fig. 19(b) shows the waveforms of the conventional Buck–Boost LED

TABLE I
CRITICAL CIRCUIT PARAMETERS OF THE PROPOSED BUCK–BOOST ENERGY CHANNELING LED DRIVER PROTOTYPE

Critical component	Value / PN
Output capacitor C_{o1}	ECA-1JM101 (63 V, 100 µF) ECA-1JM3301 (63 V, 33 µF)
Output capacitor C_{o2}	CL31A226MOCLNNC (16 V, 20 µF)
Coupled inductor	Ferrite core EF16 with main winding inductance 800 µH N_1:N_2:N_{aux} = 90 : 20 : 90
Main MOSFET Q1	STP3NK80Z(800 V, 2.5 A)
Controller for Q1	FL7732
Main rectifier diode D1	MURS360-E3/57T (600 V,3 A)
Energy channeling MOSFET Q2	NTD4906N (30 V,10.3 A)
Controller for Q2	Implemented with discrete components LM311 and TLV272 based on Fig. 9
Output Diode D2 for V_{o2}	SS35-E3/57T (50 V, 3 A)
Auxiliary voltage output capacitor C_{aux}	ECA-2CM470 (160 V, 47 µF)
Auxiliary voltage blocking Diode D_b	DLM10E-AT1 (400 V, 1 A)
LED load	25 LEDs connected in series Part number: LR W5AM-HZJZ-1-Z

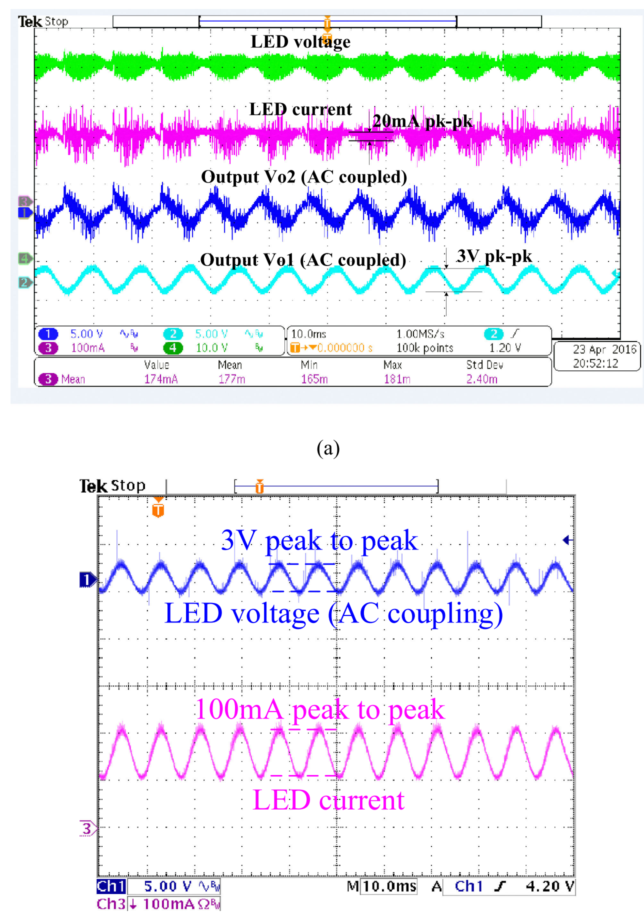
driver. A 3-V pk–pk 120-Hz twice-line-frequency LED ripple voltage is observed, which introduces a 100-mA peak to peak (29.5% of current ripple) LED ripple current. Therefore, the proposed LED driver achieves an 80% ripple current reduction (from 100 to 20 mA) in the experiment.

Fig. 20 shows the key switching waveforms of the proposed energy channeling LED driver. The switching cycle starts at time t_0. During the time interval $[t_0 - t_1]$, the main MOSFET Q_1 is on, and the inductor is charged through winding N_1.Q_1 is turned OFF at time t_1. Since Q_2 is not on during the time interval $[t_1 - t_2]$, the inductor current continues circulating in winding N_1 and transfers the energy to output V_{o1}.Q_2 is turned ON at time t_2 and the inductor current commutes immediately from winding N_1 to winding N_2. The inductor current at t_2 has already been greatly reduced from the peak value at t_1, which results in a low current stress on Q_2. The inductor current keeps decreasing in winding N_2 until it becomes zero at time t_3. In order to achieve a high power factor, the proposed LED driver operates under DCM condition and does not immediately turn on again when the inductor current drops to zero. There is a short time of turn on overlap between Q_1 and Q_2 due to the limitation of the implementation circuit. It will not impact the circuit operation since the diode D_2 is reverse biased when Q_1 is on. This overlap can also be avoided with more sophisticated circuit design.

Fig. 21 shows the rectified input voltage and the ac input current under 110-Vrms input and when the voltage V_{flat} is provided. During the time interval $[t_a - t_b]$, the rectified voltage is flat, and the ac input current becomes zero. A power factor of 0.97 has been measured with the prototype. Similar waveforms had also obtained from 220-Vrms input. A power factor of 0.93 has been measured. The power factor performance exceeds the 0.9 PF requirement for LED lighting applications.

Fig. 23 shows the waveform of adaptive V_{flat} generation. When the input voltage changes from 110-Vrms input to 220-Vrms input, V_{flat} voltage changes from 40 to 80 V, which agrees with the previous analysis.

Fig. 24 shows the dynamic LED current response of the proposed LED driver. By applying the control signal, the current sensing resistor is programmable. The LED current changes



(a)

(b)

Fig. 19. Ripple current comparison between the energy channeling LED driver and a conventional Buck–Boost LED driver with 50 V/0.17 A output. (a) Energy channeling Buck–Boost LED driver. (b) Conventional Buck–Boost LED driver.

from 100 to 170 mA in the experimental measurement and shows stable operation.

Fig. 25 shows the efficiency of the proposed Buck–Boost experimental prototype under 110 and 220-Vrms input voltage. In total, 86% and 83% efficiency are achieved at full load with 110 and 220-Vrms input, respectively. The experiment focused

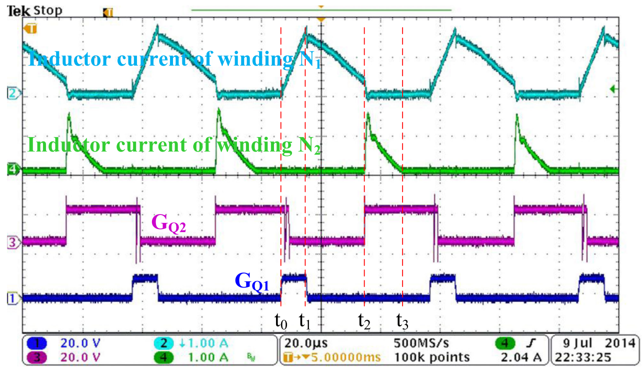


Fig. 20. Key switching cycle waveforms of the proposed energy channeling LED driver.

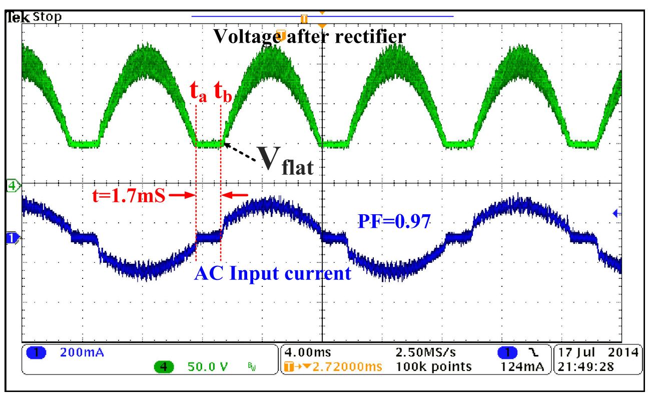


Fig. 21. 110-V input voltage (after rectifier) and ac input current waveforms when the input power is reshaped.

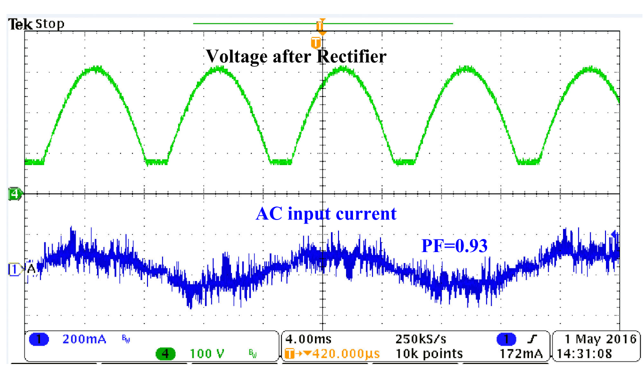


Fig. 22. 220-V input voltage (after rectifier) and ac input current waveforms when the input power is reshaped.

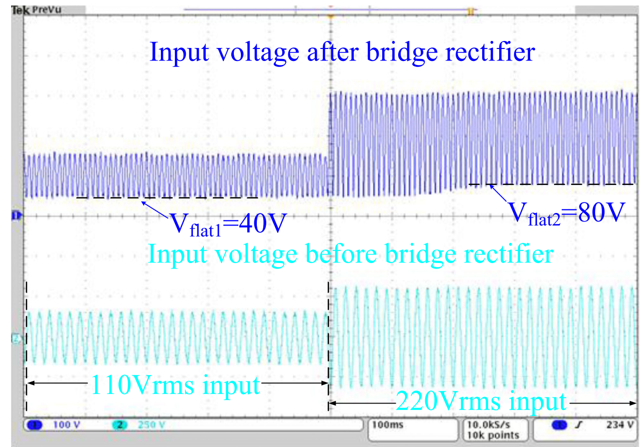


Fig. 23. Waveform of adaptive Vaux generation.

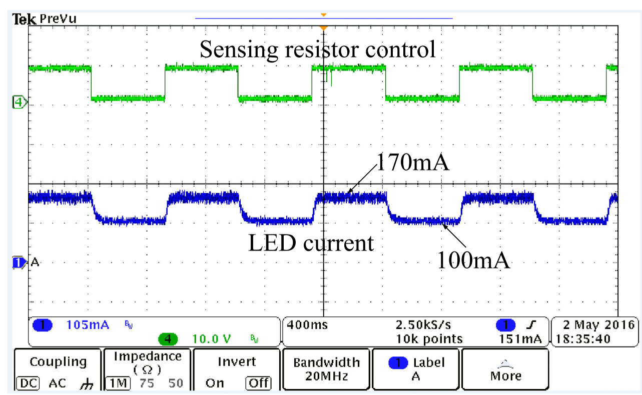


Fig. 24. Dynamic LED current response of the proposed LED driver.

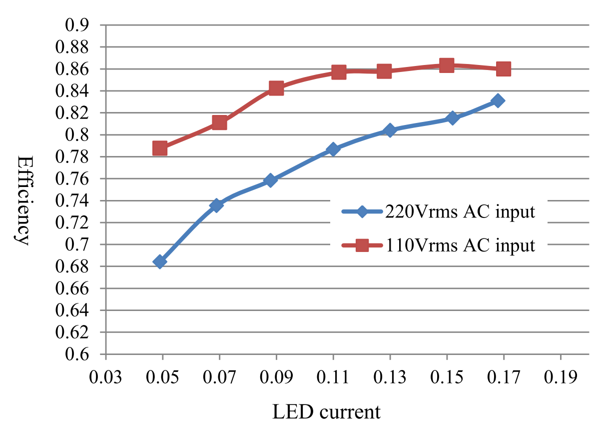


Fig. 25. Efficiency of the proposed LED driver under 110 and 220-*V*rms input voltage.

on the feasibility of the proposed LED driving method, and the efficiency can be further improved with an optimized design.

Table II shows the THD measurement of the proposed LED driver and Fig. 26 shows each order of the input current harmonic versus the IEC-61000-3-2 standard. Under 110-*V*rms input, the measured input current harmonics are within the standard limit. Under 220-*V*rms input, after ninth order, the measured harmonics are marginally within or slightly surpassed the standard limit. With a better EMI filter design, the input current harmonics under 220-*V*rms input can be managed to fall into the standard limit. Fig. 22 shows the photo of the experimental prototype.

TABLE II
THD MEASUREMENT OF THE PROPOSED LED DRIVER

Load current (mA)	Under 110 Vrms (%)	Under 220 Vrms (%)
50	17.7	23.0
70	16.9	20.4
90	18.2	18.9
110	17.1	17.5
130	16.3	15.4
150	16.4	15.6
170	17.8	15.8

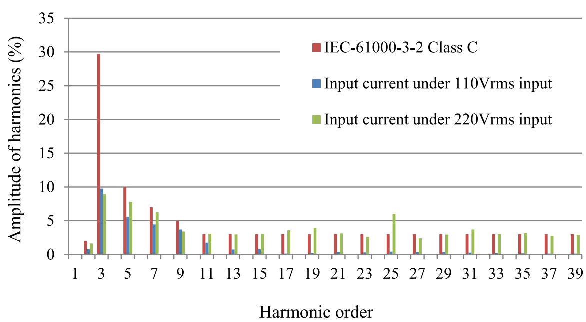


Fig. 26. Input current harmonic measurement versus IEC-61000-3-2 Class C.

Fig. 27. Photo of the experimental prototype.

VI. CONCLUSION

In this paper, the concept of energy channeling LED driver has been proposed. It is a true single-stage solution with high power factor and flicker-free LED driving performance. The input power is split into two portions to produce two output voltages. The main output provides energy storage and contains a 120-Hz twice-line-frequency ripple voltage. The auxiliary output is controlled to cancel the ripple voltage of the main output. This way, a dc LED driving voltage is produced and drives the LED load with flicker-free performance. Both simulation and experiment have been performed to verify the proposed energy channeling LED driving method. The 8.5 W, 50 V/0.17 A prototype achieves 5.8% 120-Hz twice-line-frequency ripple current, 0.97 power factor, and 86% full load efficiency under 110-*V*rms input.

REFERENCES

[1] "19-W single-stage AC/DC LED driver For T8/T10 fluorescent lamp replacement," Texas Instrument reference design, Apr. 2011.
[2] "NCL30001 high-efficiency single stage power factor correction and step-down offline LED drive," On Semiconductor datasheet, Feb. 2015.
[3] "FL7732 single-stage PFC primary-side-regulation offline LED driver," Fairchild datasheet, 2011.
[4] A. Wilkins, J. Veitch and B. Lehman, "LED lighting flicker and potential health concerns: IEEE standard PAR1789 update," in *Proc. Energy Convers. Congr. Expo.*, Sep. 2010.
[5] B. Lehman and A. J. Wilkins, "Designing to mitigate effects of flicker in led lighting: reducing risks to health and safety," *IEEE Power Electron. Mag.*, vol. 1, no. 3, pp. 18–26, Sep. 2014.
[6] " AN-9729 LED application design guide using half-bridge LLC resonant converter for 100w street lighting," Fairchild application note, Nov. 2012.
[7] "AN-1169 40V/1.4A low voltage LED Driver using IRS2548D," International Rectifier application note, May 2014.
[8] "SLUA617A A new off-line LED lighting driver solution with multi-transformer LLC control," Texas Instrument application note, Sep 2011.
[9] "AN-2150 LM3450A evaluation board," Texas Instruments application note, May 2013
[10] Y. Guo, S. Li, A. T. L. Lee, S. C. Tan, C. K. Lee, and S. Y. R. Hui, "Single-stage ac/dc single-inductor multiple-output LED drivers," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5837–5850, Aug. 2016.
[11] S. Wang *et al.*, "A flicker-free electrolytic capacitor-less AC–DC LED driver," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4540–4548, Nov. 2012.
[12] Q. C. Hu and R. Zane, "Minimizing required energy storage in off-Line LED drivers based on series-input converter modules," *IEEE Trans. Power Electron.*, vol. 26, no. 10 pp. 2887–2895, Oct. 2011.
[13] X. B. Ruan, B. B. Wang, K. Yao, and S. Wang, "Optimum injected current harmonics to minimize peak-to-average ratio of LED current for electrolytic capacitor-less AC–DC drivers," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1820–1825, Jul. 2011.
[14] B. B. Wang, X. B. Ruan, K. Yao, and M. Xu, "A method of reducing the peak-to-average ratio of LED current for electrolytic capacitor-less AC–DC drivers," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 592–601, Mar. 2010.
[15] C. A. Cheng, C. H. Chang, T. Y. Chung, and F. L. Yang, "Design and implementation of a single-stage driver for supplying an LED street-lighting module with power factor corrections," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 956–966. Feb. 2015.
[16] P. Fang, B. White, C. Fiorentino, and Y. F. Liu, "Zero ripple single stage AC-DC LED driver with unity power factor," in *Proc. Energy Convers. Congr. Expo.*, 2013, pp. 3452–3458.
[17] P. Fang and Y. F. Liu, "An electrolytic capacitor-free single stage buck-boost LED driver and its integrated solution," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2014, pp. 1394–1401.
[18] P. Fang and Y. F. Liu, "Single stage primary side controlled offline flyback LED driver with ripple cancellation," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2014, pp. 3323–3328.
[19] P. Fang, Y.-F. Liu, and P. C. Sen, "A flicker-free single-stage offline LED driver with high power factor," *IEEE J. Emerging Select. Topics Power Electron.*, vol 3, no. 3, pp. 654–665, Sep. 2015.
[20] Y. Qiu, L. Wang, H. Wang, Y.-F. Liu, and P. Sen, "Bipolar ripple cancellation method to achieve single-stage electrolytic-capacitor-less high-power LED driver," *IEEE J. Emerging Select. Topics Power Electron.*, vol. 3, no. 3, pp. 698–713, Sep. 2015.
[21] D. Camponogara *et al.*, "Capacitance reduction with an optimized converter connection applied to LED drivers," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp.184–192, Jan. 2015.
[22] D. Camponogara, G. F. Ferreira, A. Campos, M.A. Dalla Costa, and J. Garcia, "Offline LED driver for street lighting with an optimized cascade structure," *IEEE Trans. Ind. Appl.*, Vol. 49, no 6, pp. 2437–2443, Nov./Dec. 2013.
[23] P. Fang, Z.Y. Hu, and Y. F. Liu, "An energy channeling LED driver technology to achieve flicker-free operation with true single stage power factor correction," in *Proc. Appl. Power Electron. Conf. Expo.*, Mar. 2015, pp. 3353–3358.
[24] AN-5076, Design a High Power Factor Flyback Converter Using FL7733A for an LED Driver with Ultra-Wide Output Voltage, Oct. 2014.

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