Decoupled PWM Control of a Dual-Inverter Four-Level Five-Phase Drive

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***Abstract*—This paper studies pulse width modulation (PWM) techniques suitable for a four-level five-phase open-end winding (OeW) drive. The drive comprises a five-phase induction machine, supplied using two two-level voltage source inverters with isolated and unequal dc-link voltages, in the ratio 2:1. A decoupled carrier-based (CB) PWM modulation strategy, based on unequal voltage reference sharing between the two converters, is introduced in this paper. The stability of dc-link voltages in OeW drives is investigated next, using a novel analysis technique. Several modulation methods are analyzed and the results show that application of the coupled PWM technique, with carriers having in-phase disposition, leads to overcharging of the capacitor in the dc-link of the inverter intended to operate with the lower dc-link voltage. On the other hand, the proposed decoupled CB PWM scheme naturally eliminates the dc-link capacitor overcharging problem. These findings are verified experimentally, using open-loop *V/f* control. Two different decoupled CB modulation methods are compared and the best performing modulation method is selected and incorporated further into an OeW drive with field-oriented control. The presented steady state and transient experimental results demonstrate that the decoupled CB PWM technique is suitable for high-performance variable speed drive applications.**

***Index Terms*—Field-oriented control (FOC), induction motor drives, multiphase drives, open-end winding (OeW), pulse width modulation (PWM).**

I. Introduction

OPEN-END winding (OeW) drives offer a number of advantages over conventional multilevel drive systems, such as reduced component count, when compared to neutral-point clamped (NPC) and flying capacitor converters (additional diodes or capacitors are not required) [1] and an improved capability to operate under faulted conditions [2], [3]. This paper considers a five-phase OeW induction motor drive, supplied using two isolated five-phase two-level voltage source inverters (VSIs) with dc-link voltages in the ratio 2:1. Such dc-link voltages enable drive operation with output voltage waveforms equivalent to those obtainable with a four-level VSI in the single-sided supply mode [4]. Isolated dc power supplies are required in order to eliminate a path for zero-sequence current flow. This topology is aimed at high-power applications where the well-known advantages of multiphase machines and multilevel converters are of importance. OeW drives are particularly interesting for EVs/HEVs [5] and electric ship propulsion [6], [7], where use of two isolated supplies may not represent a problem. The OeW topologies have also been investigated as a means of extending the operating speed range of five-phase permanent magnet synchronous [8] and three-phase induction machine [9] drives.

The four-level OeW topology has predominantly been investigated for three-phase drives in conjunction with the space vector (SV) pulse width modulation (PWM) technique [10], [11]. A fractal-based SV PWM method with low computational requirements is proposed in [10]. It relies on the fact that a three-phase system produces simple triangular subsectors. Unfortunately, this algorithm is not applicable to the five-phase case since the system does not produce such uniformly distributed subsectors.

Regardless of the structure of the inverters, number of drive phases, and selection of carrier-based (CB) or SV PWM in implementation, modulation in an OeW drive can be such that the inverters are controlled either as a single entity or individually. The first group of modulation strategies, to which [10] belongs, is referred to here as "coupled" PWM control and it relies on already known modulation strategies for single-sided multilevel inverters, which are applied to the OeW drives after some minor modifications.

If the inverters are controlled independently, so called "decoupled" PWM control results and it requires appropriate means for overall reference sharing between the two inverters. Two decoupled SV PWM algorithms, which view the inverters as individual two-level VSIs, are discussed in [11] for a three-phase drive. Since two VSIs are supplied with dc-link voltages in the ratio 2:1, both proposed methods are based on the sharing of the overall phase voltage reference between two inverters in the same ratio. In the first approach described in [11] both VSIs have the same switching frequency, while the second method utilizes switching of the two VSIs using switching frequencies that are in the ratio 2:1 (i.e., proportional with their dc-link voltages). The second approach leads to approximately 10% reduction of switching losses and somewhat better harmonic performance.

In the case of multiphase multilevel drives, the large number of switching states and voltage vectors, discussed in [12], make the development of suitable control strategies difficult. Furthermore, some additional complexity is introduced, since more than three voltages need to be synthesized. The problem is further exacerbated by the fact that the PWM scheme has to consider more than one plane simultaneously (α–β and x–y in the case of a five-phase drive) in order to achieve optimum performance [13]. It is for these reasons that the CB PWM is considered in

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[14]–[17], as well as in this paper, as a simpler, and hence, more appropriate technique in the case of OeW multiphase drives.

The coupled phase disposition (PD) PWM, widely recognized as a superior CB PWM technique for single-sided three-phase [18] and five-phase [1] multilevel drives, is adapted to control the four-level five-phase OeW configuration in [14], [15]. As explained in [16], three carrier signals are required although each inverter is a two-level one. In [15], it is shown that the inverter dead time can lead to triggering of unwanted voltage levels which can have a detrimental impact on the drive's performance. A method to alleviate the problem is proposed in [15] and the transient and steady-state performances of the method are experimentally verified in [17].

Regardless of the number of phases, one of the major issues, associated with multilevel drives, is the dc-link capacitor voltage stability. Unbalance at this stage of power conversion means nonconstant voltage levels, which affect the modulation strategy performance. Furthermore, safety issues may arise if the dc-link capacitors are overcharged. Unfortunately, in the case of the considered OeW drive, the full four-level operation, obtainable with the coupled PD PWM, leads to the lower dc-link voltage side capacitor overcharging. Therefore, this dc-link would have to be formed using a fully controllable supply with bidirectional current flow, in order to avoid unnecessary power loss in the dynamic brake. This constraint was overcome for the three-phase case in [11], by using a suitable PWM technique, which is addressed in more detail later in the paper.

An alternative solution to the overcharging problem is given in [19], where one out of three three-phase diode rectifiers is nested within the other two. The lower dc-link voltage is formed using the nested rectifier voltage output, while the higher dc-link is formed by combining the output voltages of the other two diode rectifiers. Although this approach effectively eliminates the capacitor voltage balancing problems, it has some drawbacks. First, although the proposed circuitry relies on usage of an isolated center-tap transformer with winding turns ratio 1:2:1, isolation between two inverters is not obtained, allowing zero-sequence current circulation. This increases the harmonic distortion of produced phase voltages and currents, making a tradeoff between drive harmonic performance and lower dc-link voltage side capacitor voltage balancing. Second, this solution leads to a more complex structure with an increased component count, which is in contradiction with the primary motivation for the OeW drive development.

This paper builds on the work presented in [20], where a decoupled SV PWM algorithm is developed, which considers the four-level drive as two individual two-level inverters rather than a single four-level structure. Two decoupled modulation strategies, based on the unequal reference sharing between the modulators of the inverters (so called URS1 and URS2) are discussed in [20]. It is shown that the decoupled SV PWM methods naturally avoid the switching states that lead to the dc-link capacitor overcharging. As an alternative, a dual CB PWM scheme is developed in this paper. Contrary to the coupled CB PD PWM case, decoupled modulation algorithm for the four-level drive relies on only two carrier signals and each of them corresponds to one two-level inverter. The main contributions of the paper are as follows:

1) Proposed CB PWM is simpler to implement, when compared to the SV PWM of [20]. The developed so-called unequal reference sharing (URS) modulation methods are compared with the proportional reference sharing (PRS), proposed in [11]. Results show that URS is superior in terms of total harmonic distortion (THD) performance.
2) A novel concept of OeW drive modeling is introduced, which leads to better understanding of the dc-link voltage stability, when compared to methods in [19], [20]. Results show in which circumstances PD PWM leads to lower dc-link voltage side capacitor overcharging; on the other hand, the URS naturally keeps all dc-link voltages stable. Results of this dc-link voltage stability analysis are experimentally confirmed and they show that coupled PD PWM leads to higher power losses, when compared to the URS PWM.
3) A field-oriented control (FOC) scheme is developed, which incorporates the best performing decoupled modulation method. Dynamic performance of the OeW drive is then examined experimentally. The results show that the developed modulation technique, in addition to avoidance of the capacitor overcharging problem, ensures high dynamic performance expected from a FOC drive.

The paper is organized as follows. For the sake of clarity, Section II provides a short description of the topology under analysis. More details can be found in [14]–[17], [20]. Unequal reference sharing algorithms (URS1 and URS2), based on CB PWM, are discussed in Section III, and compared with the method introduced in [11]. It is shown that URS1 offers superior harmonic performance and so it is chosen for further analysis. In Section IV, a novel method of analyzing the dc-link voltage stability is introduced and applied to the cases of coupled (PD PWM) and decoupled (URS1 PWM) modulation methods. Section V discusses experimental results obtained with closed-loop FOC control. Conclusions are summarized in Section VI.

II. Four-Level OeW Topology

The four-level drive consists of an OeW five-phase induction machine, supplied via two isolated two-level VSIs, as shown in Fig. 1. The inverters are supplied with unequal dc-link voltages in the ratio $V_{\mathrm{dc1}} : V_{\mathrm{dc2}} = 2 : 1$, where VSI_1 is supplied from V_{dc1}, and VSI_2 is supplied from V_{dc2}. This provides an overall dc-link voltage of $V_{\mathrm{dc}} = V_{\mathrm{dc1}} + V_{\mathrm{dc2}}$. In order to demonstrate that this configuration is equivalent to the four-level drive with single-sided supply, it is sufficient to analyze so-called equivalent model [14]–[17], based on a single-phase structure, boxed within dashed line in Fig. 1. Chosen dc-link voltages are $V_{\mathrm{dc1}} = 400$ V and $V_{\mathrm{dc2}} = 200$ V, which results in the overall dc-link voltage of $V_{\mathrm{dc}} = 600$ V. Disregarding the rest of the drive and under the assumption that $v_{n1} = v_{n2}$, this model shows how the phase voltage levels are formed, with regard to switching combinations of two inverters. Using symbols in Fig. 1, switching states S_{jk}, which correspond to the *j*th VSI and *k*th phase can be defined: $S_{\mathrm{jk}} = 1$, if S_{upjk} or D_{upjk} conducts, otherwise $S_{\mathrm{jk}} = 0$. Analysis of all possible switching combinations leads to four equidistant voltage levels of $-V_{\mathrm{dc}}/3$, 0,

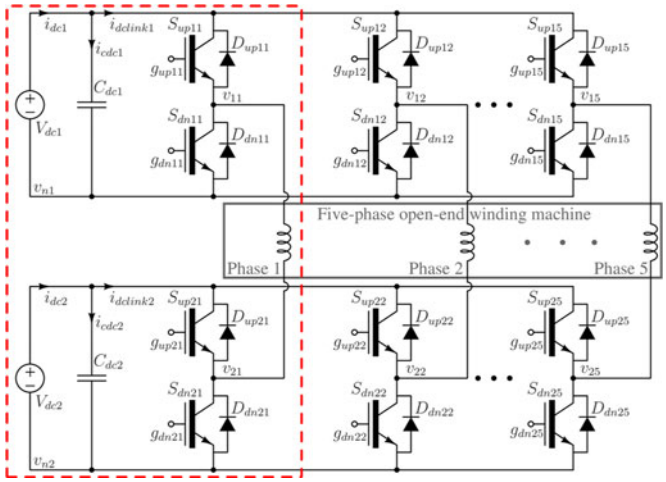

Fig. 1. Five-phase open-end winding topology with two two-level inverters. One drive's phase that represents equivalent drive model is boxed within the dashed line.

TABLE I
RELATIONSHIP BETWEEN SWITCHING STATES, LEG AND EQUIVALENT VOLTAGES OF FIG. 1

S_{1k}	S_{2k}	$v_{1k}\,[V]$	$v_{2k}\,[V]$	Equivalent $v_k\,[V]$
1	0	$V_{\rm dc1}$	0	$V_{\rm dc1}$–0 = $2/3 \cdot V_{\rm dc}$
1	1	$V_{\rm dc1}$	$V_{\rm dc2}$	$V_{\rm dc1}$–$V_{\rm dc2}$ = $1/3 \cdot V_{\rm dc}$
0	0	0	0	0–0 = 0
0	1	0	$V_{\rm dc2}$	0–$V_{\rm dc2}$ = $-1/3 \cdot V_{\rm dc}$

$V_{\rm dc}/3$, and $2V_{\rm dc}/3$, as summarized in Table I. This leads to the conclusion that the topology is equivalent to the four-level single-sided drive, with the same number of phases.

In order to determine the actual phase voltage waveform, common-mode voltage (CMV) v_{n2n1} should be taken into account. Therefore, the phase voltage waveform of phase *k* can be obtained using

$$v_k = v_{1k} - v_{2k} - v_{n2n1}. \tag{1}$$

Assuming that the sum of all phase voltages is zero, the CMV is calculated as

$$v_{n2n1} = v_{n2} - v_{n1} = \frac{1}{5}\sum_{k=1}^{5}(v_{1k} - v_{2k}). \tag{2}$$

When compared to single-sided four-level drives, topology in Fig. 1 offers lower component count per drive phase, which reduces the overall cost and potentially leads to increased power density. For example, a four-level NPC converter requires six semiconductor modules (that consist of one IGBT and one antiparallel diode) and four clamping diodes, while equivalent OeW drive can be built using only four such modules per drive phase. It follows that in the case of a five-phase drive 10 modules and 20 diodes can be saved if single-sided solution is replaced with topology in Fig. 1. Although two isolated dc sources are required, number of energy storage components is still reduced, since three capacitor banks are needed for a four-level NPC VSI, while an OeW drive requires only two.

Comparison of CB PWM and SV PWM methods shows that CB PWM can achieve the same level of performance as the SV PWM methods, i.e., increase the dc-link voltage utilization in the linear modulation region to the maximum modulation index equal to $M_{\max} = 1/\cos(\pi/10) = 1.051$ in the case of a five-phase machine [21]. This can be achieved by adding the zero-sequence injection to the sinusoidal phase voltage reference signals, calculated as

$$v_{\rm inj} = -1/2 \cdot (v_{\min} + v_{\max}) \tag{3}$$

where $v_{\max}$ and $v_{\min}$ stand for the maximum and minimum value, respectively, of the normalized phase voltage references. The final phase voltage references are generated in per unit using the following expression:

$$v_k^*(t) = M \cdot \sin(M \cdot 2 \cdot \pi \cdot f_n \cdot t - 2 \cdot \pi/5 \cdot (k-1)) + v_{\rm inj} \tag{4}$$

where $k = 1, 2, \ldots 5$, and the modulation index *M* is defined as a ratio between the reference amplitude and $V_{\rm dc}/2$. Equation (4) provides phase voltage references for variable-voltage variable-frequency control, since sine wave amplitude is normalized with *M*, as is the angular frequency as well (f_n stands for the nominal machine frequency).

III. DECOUPLED CB PWM CONTROL

As already stated, decoupled CB PWM approach results in a much reduced computational burden, when compared to the equivalent SV PWM, as the case always is [21]. Additionally, extension of a CB PWM scheme to an arbitrary number of phases is straightforward. Hence, CB PWM implementation, which considers two VSIs as separate entities, is presented in this section. The basic idea is to decompose the control of the complete system into two subproblems of lower level of complexity, by splitting the original phase voltage reference into two parts, in order to share it between individual references of the two inverters [12]. By doing so, it becomes possible to apply well-known PWM methods for two-level inverters to the two individual two-level inverters. Modulation is performed separately for v_{1k}^* and v_{2k}^*, which are voltage references for $\rm VSI_1$ and $\rm VSI_2$ leg outputs, respectively, connected to the *k*th drive phase.

The total phase voltage reference is given with (4). In order to share the phase voltage reference between two inverters while respecting the dc link voltage ratio, two additional modulation indices for $\rm VSI_1$ and $\rm VSI_2$ are introduced

$$M_1 = \begin{cases} 0 & \text{if} \quad 0 \le M < 0.35 \\ 1.5 \cdot (M - 0.35) & \text{if} \quad 0.35 \le M \le 1.05 \end{cases}$$
$$M_2 = \begin{cases} 3 \cdot M & \text{if} \quad 0 \le M < 0.35 \\ 1.05 & \text{if} \quad 0.35 \le M \le 1.05 \end{cases}. \tag{5}$$

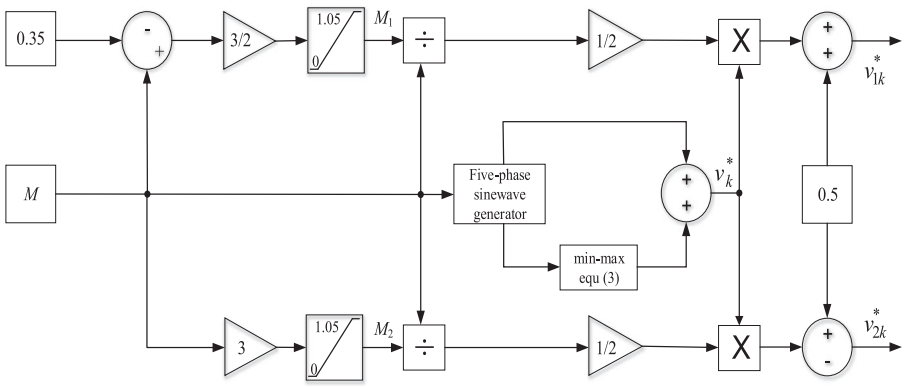

Fig. 2. Decoupled URS CB PWM algorithm block diagram.

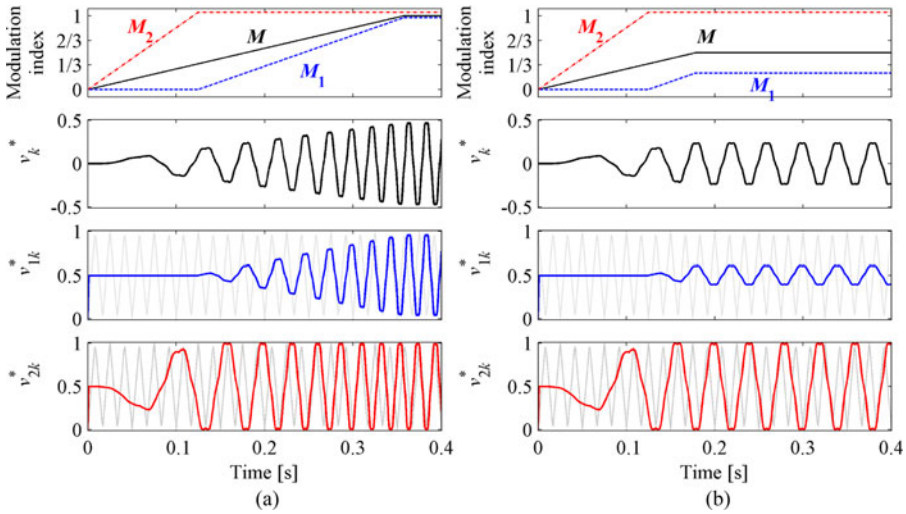

Fig. 3. Formation of the voltage references for two VSIs using algorithm of Fig. 2, for two final M values. Carrier signal frequency is reduced to 60 Hz, for better visualization. Carriers shown in (a) correspond to URS1, while for URS2 carrier signal for VSI_1 is inverted, (b). (a) URS1, final $M = 1$, (a) URS2, final $M = 0.5$.

Using (4) and (5), it is possible to form voltage references for VSI_1 and VSI_2 using

$$v^*_{1k}(t) = \tfrac{1}{2} + (M_1/M)\tfrac{1}{2}v^*_k(t)$$
$$v^*_{2k}(t) = \tfrac{1}{2} - (M_2/M)\tfrac{1}{2}v^*_k(t) \quad (6)$$

where v^*_{1k} and v^*_{2k} are the phase voltage references of the kth drive phase for VSI_1 and VSI_2, respectively. The complete modulation strategy (URS CB PWM) block diagram is shown in Fig. 2. Modulation indices of the two VSIs and voltage references, with respect to the overall modulation index and commanded phase voltage reference, are shown in Fig. 3 for the drive start-up transient with open-loop V/f = const. control. Within the scope of the decoupled modulation technique, two separate modulation methods are investigated. The first one (URS1) relies on VSI_1 and VSI_2 carrier signals with in-PD [Fig. 3(a)], while the second method (URS2) uses carrier signals with mutual phase shift of 180° [see Fig. 3(b)].

In the low modulation index range, i.e., for $0 < M < 0.35$, both URS1 and URS2 lead to the single-sided supply equivalent in terms of the operating mode. This comes from (5) and results in two-level operation, since VSI_1 holds all five leg voltages on the same voltage potential (v_{n1}), while VSI_2 operates in PWM mode. The upper border for this kind of operation is equal to $M_{\max}/3 = 0.35$, due to the dc-link voltage ratio 2:1. In the rest of the modulation index range, i.e., for $M \geq 0.35$, both inverters operate in PWM mode, which leads to multilevel modulation.

An alternative way for reference sharing, presented in [11] and termed here PRS, is based on the overall phase voltage reference sharing between two inverters in proportion to their dc-link voltages, regardless of the modulation index instantaneous value. This kind of decoupled modulation has already been investigated for the five-phase OeW drive case, but for equal dc-link voltages, in [22] where it was referred to as equal reference sharing. Again, two different carrier arrangements are possible. In the case of PRS1, carriers for VSI_1 and VSI_2 modulators are with in-PD, while phase shift of two carrier signals of 180° corresponds to PRS2. The harmonic performances of the decoupled PWM methods are compared using the THD as a figure of merit

$$\text{THD} = \sqrt{\sum_{i=2}^{K} \frac{X_i^2}{X_1^2}} \quad (7)$$

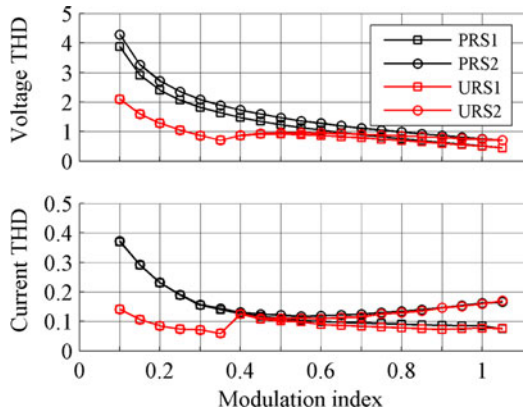

Fig. 4. Simulation results: phase voltage and phase current THD against modulation index in the case of PRS (black) lines, [11] and URS methods (red lines). Results are obtained with CB PWM.

where X_i is the rms value of the *i*th harmonic, the fundamental is denoted with X_1, and $K = 5000$. The THD is calculated for M ranging from 0.1 to 1.05 in 0.05 increments and is shown in Fig. 4 for both PRS and URS methods. Results are obtained using numerical simulation for the same simulation parameters as in [14]–[17]. Clearly, PRS methods offer inferior harmonic performance in the low modulation index range. Results obtained for $M \geq 0.35$ show that PRS1 has similar phase current harmonic performance as URS1. The same can be concluded for PRS2 and URS2. At the same time, phase voltage harmonic performance with the PRS methods is worse in the range $0.35 \leq M < 0.7$, when compared to the URS. Comparison of the two URS methods leads to a conclusion that both methods offer similar performance up to $M = 0.5$. Above this value, the URS1 offers superior performance since the current THD is much lower. Comparison of URS1 and URS2 THD(M) dependencies with those reported in [20] confirms duality between herein proposed CB PWM implementation and SV PWM schemes in [20].

IV. Capacitor Overcharging Issue

In general, a number of multilevel VSI topologies suffer from some sort of capacitor voltage balancing issue. In an OeW drive with dual two-level VSI supply capacitor overcharging would lead to constant triggering of the dynamic brake (when diode rectifiers are used) and a waste of energy. Change of the modulation strategy, i.e., software-based solution, is the least costly solution for remedying the problem. It is demonstrated in [20] that coupled PD PWM leads to the lower dc-link voltage capacitor becoming overcharged, if unequal dc-link voltages are used. Simulations are used to show the overcharging of the dc-link and identify the deleterious voltage vectors which cause this phenomenon. In this paper, the same phenomenon is addressed using a different approach. The complete analysis of dc-link capacitor charging and discharging processes is performed using only the first Kirchhoff's law. Impacts of drive parameters and modulation strategy on the dc-link capacitor voltages are analyzed using a simplified and then linearized drive model, which does not include PWM and relies on sinusoidal approximation (i.e., only the fundamental is considered and higher order harmonic content is neglected).

First, let us assume that dc sources in Fig. 1 are current unidirectional, which means that i_{dc1} and i_{dc2} can only be positive. For the purpose of this analysis, voltages across dc-link capacitors C_{dc1} and C_{dc2} (see Fig. 1) are denoted with v_{cdc1} and v_{cdc2}, respectively, indicating that they are treated as time-dependent variable voltages. Using the first Kirchhoff's law, on the upper dc-link contours, which include all upper inverter leg nodes in Fig. 1, one can write

$$\begin{aligned} i_{\mathrm{cdc1}}(t) &= i_{\mathrm{dc1}}(t) - i_{\mathrm{dclink1}}(t) \\ i_{\mathrm{cdc2}}(t) &= i_{\mathrm{dc2}}(t) - i_{\mathrm{dclink2}}(t). \end{aligned} \tag{8}$$

Currents i_{dclink1} and i_{dclink2} can be calculated using the switching states of the semiconductors, defined in Section II. Hence

$$\begin{aligned} i_{\mathrm{dclink1}}(t) &= \sum_{k=1}^{5} (S_{1k}(t) \cdot i_k(t)) \\ i_{\mathrm{dclink2}}(t) &= -\sum_{k=1}^{5} (S_{2k}(t) \cdot i_k(t)). \end{aligned} \tag{9}$$

Using correlation between capacitor voltage and current, in which capacitor and dc-link currents are eliminated using (8) and (9), one has

$$\begin{aligned} v_{\mathrm{cdc1}}(t_2) &= \frac{1}{C_{\mathrm{dc1}}} \int_{t1}^{t2} \left(i_{\mathrm{dc1}}(t) - \sum_{k=1}^{5} S_{1k}(t) \cdot i_k(t) \right) \cdot \mathrm{d}t \\ &\quad + v_{\mathrm{cdc1}}(t_1) \\ v_{\mathrm{cdc2}}(t_2) &= \frac{1}{C_{\mathrm{dc2}}} \int_{t1}^{t2} \left(i_{\mathrm{dc2}}(t) + \sum_{k=1}^{5} S_{2k}(t) \cdot i_k(t) \right) \cdot \mathrm{d}t \\ &\quad + v_{\mathrm{cdc2}}(t_1) \end{aligned} \tag{10}$$

where $v_{\mathrm{dc1}}(t_1)$ and $v_{\mathrm{dc2}}(t_1)$ are initial conditions at $t = t_1$. Equation (10) shows that the capacitor voltage remains constant only if the integral value is zero. Since i_{dc1} and i_{dc2} cannot be negative, voltages v_{cdc1} and v_{cdc2} can only be constant if i_{dclink1} and i_{dclink2} are positive. However, if for any reason i_{dclink1} and/or i_{dclink2} are negative, some additional charge will be added to the dc-link capacitors, even if the corresponding dc source current is equal to zero. Hence, it seems sufficient to analyze i_{dclink1} and i_{dclink2}, in order to understand what conditions, if any, lead to the dc-link capacitor overcharging problem. Although i_{dclink1} and i_{dclink2} are not constant in time, their mean values over one fundamental period should be positive, if dc-link capacitor voltage levels are to be constant. The next step in the analysis is simplification of the drive model, in order to identify what drive parameters have impact on i_{dclink1} and i_{dclink2} mean values. Therefore, phase currents are assumed to be $i_k(t) = I_m \cdot \sin(2 \cdot \pi \cdot M \cdot f_n \cdot t - 2 \cdot \pi/5 \cdot (k-1) - \phi)$, i.e., purely sinusoidal. Here, I_m stands for expected phase current amplitude and k is the phase number. In order to simplify calculations, $I_m = 1$ A is used. Phase angle, calculated with respect to the corresponding phase voltage, is denoted by ϕ. Phase voltage

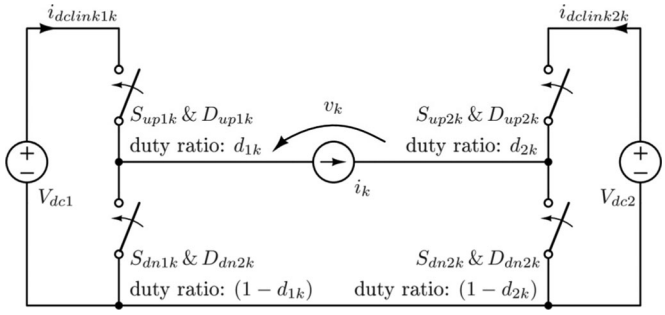

Fig. 5. Equivalent drive model under the sinusoidal phase current approximation.

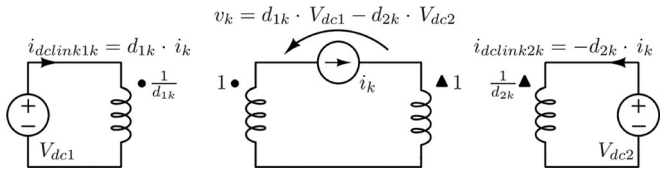

Fig. 6. Linearized drive equivalent model under the sinusoidal phase current approximation.

references of (4), but without min–max injection, are considered in further analysis for simplicity.

Based on the phase voltage reference and modulation algorithms, duty cycles of $S_{\mathrm{up}1k}$, $D_{\mathrm{up}1k}$, $S_{\mathrm{up}2k}$, and $D_{\mathrm{up}2k}$ are defined as their conduction time normalized with the switching period. All semiconductor devices are considered as ideal (no dead time) and very high switching frequency is assumed, so that switching effects can be ignored. This enables further simplification of the circuit, where each IGBT and corresponding antiparallel diode pair can be considered as an ideal switch, so that a single duty cycle parameter can be assigned to $S_{\mathrm{up}1k}$ and $D_{\mathrm{up}1k}$, referred to as d_{1k}. The same applies to $S_{\mathrm{up}2k}$ and $D_{\mathrm{up}2k}$ pair, which together form S_{2k} switch that has duty cycle d_{2k}. The final equivalent model under sinusoidal approximation is shown in Fig. 5. Duty cycle becomes a continuous time domain function, determined by the modulation strategy algorithm. Since all switching effects are eliminated from the analysis, while phase current is purely sinusoidal, this also means that there are no ac components in the CMV. The CMV has a nonzero dc component [17], which is disregarded in Fig. 5. The model in Fig. 5 assumes that phase currents are always sinusoidal, regardless of the modulation of the inverters, which means that dc CMV component has no impact on the analysis. The same can be concluded for all dc voltages in the simplified model ($V_{\mathrm{dc}1}$ and $V_{\mathrm{dc}2}$ are shown only to give the meaning of $i_{\mathrm{dclink}1k}$ and $i_{\mathrm{dclink}2k}$ currents). Since all parameters and variables in the above described model are piecewise linear functions, the circuit in Fig. 5 can be represented in linear form, shown in Fig. 6. Two ideal transformers are used to model the relations between the three drive stages: VSI_1, machine, and VSI_2.

Numbers of turns of individual windings are related to duty cycles of two inverters. The aim of this model is to provide insight into the phase current and modulation strategy influence on dc-link voltage balancing. From this point of view, it is practical to consider phase currents and phase voltage references as system inputs, while dc-link currents are treated as system outputs.

TABLE II
DUTY CYCLE EXPRESSIONS FOR COUPLED PD MODULATION

Condition	$d_{1k}(t)$	$d_{2k}(t)$
$l_1 \le v_k^*(t) \le l_2$	0	$3(l_2 - v_k^*(t))$
$l_2 \le v_k^*(t) \le l_3$	$3(v_k^*(t) - l_2)$	$3(v_k^*(t) - l_2)$
$l_3 \le v_k^*(t) \le l_4$	1	$3(l_4 - v_k^*(t))$

The PD PWM scheme, as an example of a coupled PWM method, is analyzed first. Having in mind basic principles of CB PWM and the inverters' operation defined in [14], [16], [17], duty ratios in Figs. 5 and 6 can be analytically expressed, using phase voltage reference and equivalent voltage levels ($l_1 = 0$, $l_2 = 1/3$, $l_3 = 2/3$, and $l_4 = 1$). These voltage levels define the codomains of the three carrier signals in the case of PD PWM. Any duty cycle in the circuit may take instantaneous value between 0 and 1. However, since phase voltage reference and carriers do not have the same amplitude and range, some numerical manipulations of the phase voltage reference are needed, in order to obtain duty cycles in the expected range. In order to eliminate the offset introduced by carriers' minimal value different from 0, one has to subtract the lower reference zone border from v_k^*, in the corresponding reference zone (for example, if the reference belongs to the reference zone 2, i.e., it is between l_2 and l_3, then $v_k^* - l_2$ has to be used in further calculations). Second, negation in the final expressions in [14], [16], [17] means that the phase voltage reference has to be subtracted from the upper voltage level that defines that reference zone. Finally, the span of the reference zone versus the overall phase voltage reference range defines a multiplication factor, which ensures that the overall duty cycle range is between 0 and 1. The complete list of expressions for duty cycles is provided in Table II for the coupled PD modulation.

Using the expressions for phase current and duty cycles, contributions of the *k*th drive phase to $i_{\mathrm{dclink}1}$ and $i_{\mathrm{dclink}2}$ can be calculated, based on the model in Fig. 6. Resulting waveforms are shown in Fig. 7, for different modulation indices and phase angles, for the first drive phase. Horizontal (blue) lines in the top subplot represent reference zone borders (l_1, l_2, l_3, and l_4), which at the same time define minimum and maximum values of the three carrier signals. The upper two subplots represent model inputs, i.e., v_k^* (for $k = 1$) and i_1, which is shown for three different values of power factor angle ϕ. Contributions of the *k*th drive phase to $i_{\mathrm{dclink}1}$ and $i_{\mathrm{dclink}2}$ are

$$\begin{aligned} i_{\mathrm{dclink}1k}(t) &= d_{1k}(t) \cdot i_k(t) \\ i_{\mathrm{dclink}2k}(t) &= -d_{2k}(t) \cdot i_k(t). \end{aligned} \tag{11}$$

These are considered as final model outputs, shown in the bottom two subplots in Fig. 7. Obtained waveforms show that phase shift between i_k and v_k^* has a strong influence on $i_{\mathrm{dclink}1k}$ and $i_{\mathrm{dclink}2k}$. This comes from the fact that duty cycles d_{1k}

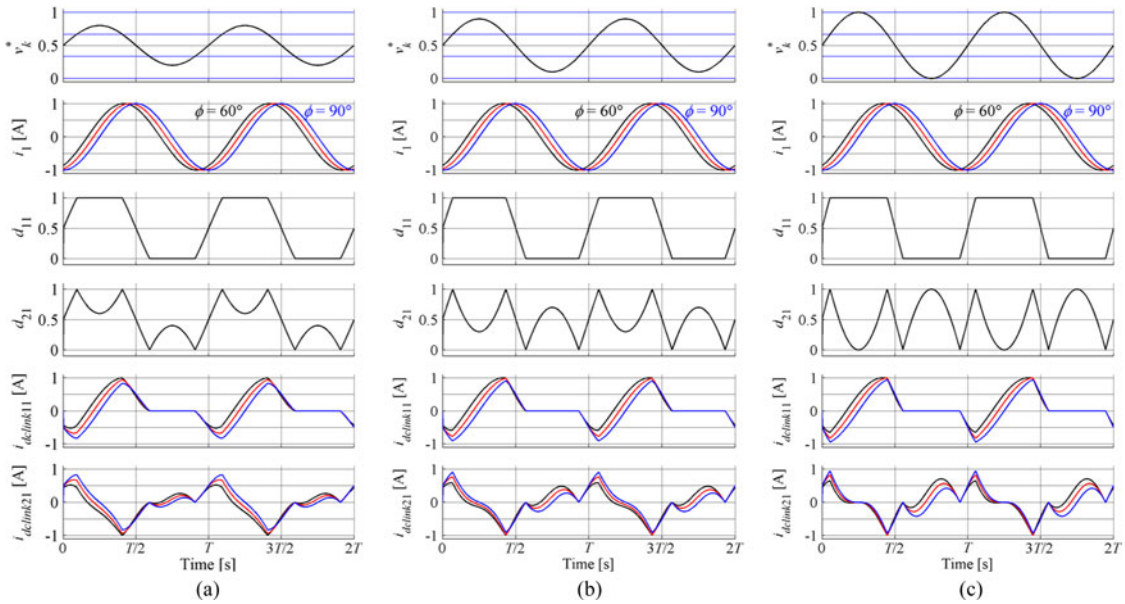

Fig. 7. Waveforms obtained using the model in Fig. 6 and coupled (PD) modulation for $\phi = 60$, 75° and 90° (black, red, and blue lines, respectively) and (a) $M = 0.6$, (b) $M = 0.8$, and (c) $M = 1$.

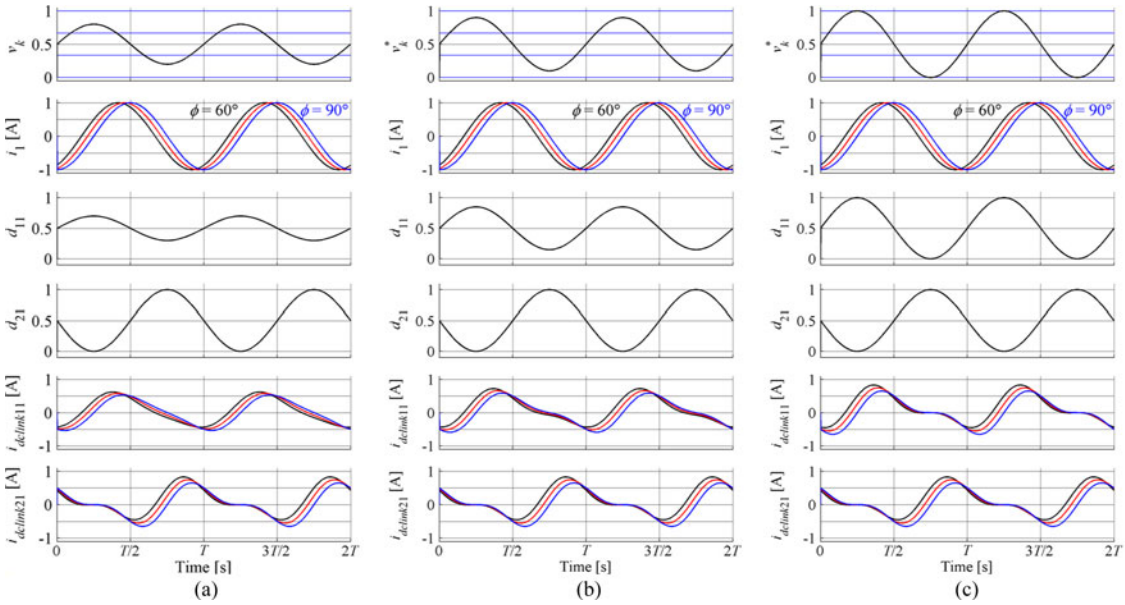

Fig. 8. Waveforms obtained using the model in Fig. 6 and decoupled (URS1) modulation for $\phi = 60$, 75° and 90° (black, red, and blue lines, respectively) and (a) $M = 0.6$, (b) $M = 0.8$, and (c) $M = 1$.

and d_{2k} are determined using v_k^* only (Table II), while the final dc-link currents are influenced by i_k as well. It can be seen that $\phi < 90°$ always results in longer positive intervals than negative ones, which means that the drive takes current from the VSI_1 dc source. On the lower dc-link voltage side, the phase current is around its peak values when v_k^* belongs to reference zone 2, where ϕ has very little impact on $i_{\text{dclink2}k}$, while its influence is more apparent when v_k^* is in reference zones 1 and 3. Fig. 7 shows that the modulation index has a strong influence on $i_{\text{dclink2}k}$ with longer negative intervals than positive ones when $M = 0.6$.

The same analysis can be performed for the decoupled modulation case. Due to the simpler modulation algorithm and carrier arrangements, shown in Fig. 3, expressions for d_{1k} and d_{2k} are equal to VSI_1 and VSI_2 phase voltage references. Obtained waveforms are shown in Fig. 8 and indicate that there are no values of ϕ and M that lead to the overcharging of the dc-link capacitors since the dc-link current waveforms never have longer negative intervals than positive ones. In order to further verify observations from Figs. 7 and 8, analysis of mean values is performed next, in order to find under which conditions the drive operates with $i_{\text{dclink2}} > 0$.

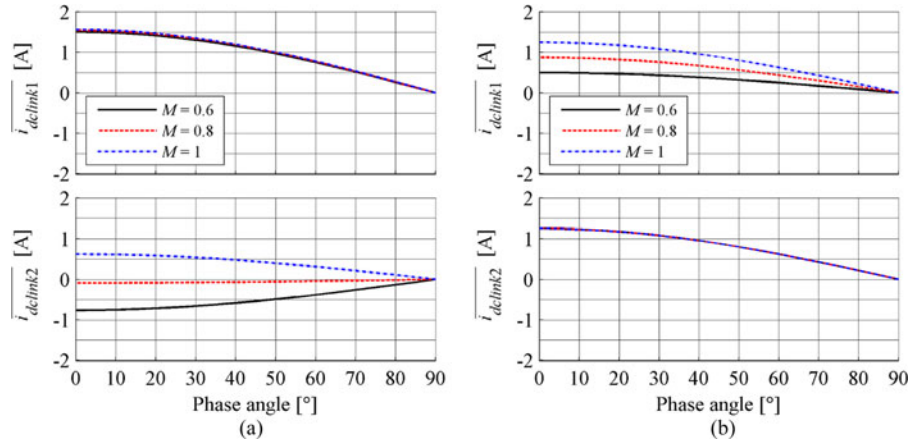

Fig. 9. Phase angle influence on the dc-link current mean values with (a) coupled PD and (b) decoupled URS1 modulation.

The final step in this analysis is to find the mean values of dc-link currents i_{dclink1} and i_{dclink2}. For this purpose, a numerical integration is performed over one fundamental period. First, the mean values of the first drive phase contribution are calculated based on (11) and final result is obtained under the assumption that the drive is symmetrical, i.e., that every drive phase gives the same contribution to i_{dclink1} and i_{dclink2} mean values. The final dependencies are shown in Fig. 9, for the two modulation methods under analysis, where the bar over the symbols signifies the mean value of the current.

Fig. 9(a) shows that for any ϕ and M set of values VSI_1 has positive dc-link current mean value, while dc-link current of VSI_2 has a negative mean value for $0.33 < M < 0.825$. The lower border ($M = 0.33$) represents the minimal M for which drive operates in the four-level mode (using both VSIs, as defined in [16], [17]), when min–max injection is not applied (as the case is in this analysis). The upper border is determined by the numerical iterative analysis of dc-link current mean value sign with respect to M and ϕ. Obtained results lead to several important conclusions, which can be applied to the real drive case. The phase angle has influence only on the amount of charge that is going to be added to C_{dc2}, but not on the dc-link current sign, which depends on M only. Negative dc-link current on VSI_2 side suggests that the inverter has the opposite power flow in the case of PD PWM, which leads to accumulation of the electric charge in C_{dc2} if unidirectional current dc sources are used for dc-link formation, and hence unwanted operation of the dynamic brake. In the case of URS1, both VSIs have positive dc-link current mean values in all conditions. VSI_2 now processes the same current, since M_2 in (5) is always constant in multilevel operation range.

These findings are verified experimentally, using open-loop $V/f =$ const. control for both coupled PD and decoupled URS1 PWM. Results are shown in Fig. 10. To avoid undesirable operation of the dynamic brake, a controllable four-quadrant voltage source was used in the experiment when the drive was modulated with coupled PD PWM. Modulation index was linearly increased from 0 to 1. Zero-sequence injection is now applied.

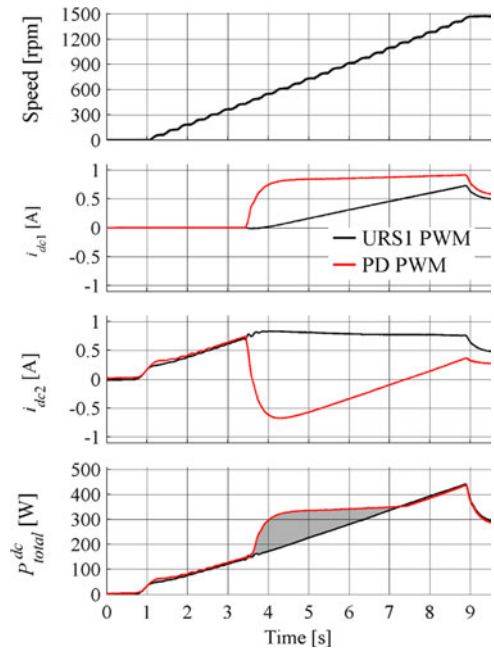

Fig. 10. Experimental results: dc-source currents and total drive power during $V/f =$ const. acceleration, for coupled PD PWM and decoupled URS1 PWM.

Motor reference speed during acceleration is shown in the upper-most plot in Fig. 10. Other signals in Fig. 10 are highly filtered, in order to eliminate switching ripple and electromagnetic interference noise. Due to the hardware configuration, it is only possible to measure i_{dc1} and i_{dc2} since dc-link voltage capacitors are incorporated within the inverters. This does not impact on the validity of the analysis, since the voltage sources keep dc-link voltages constant and measurements of their output currents (i_{dc1} and i_{dc2}) provide all the needed information. For both modulation strategies, i_{dc1} is zero for two-level modulation, since only VSI_2 is operational. In this range ($M < 0.35$), VSI_2 operates with positive dc source current which means that it sources power to the drive. In multilevel regime, URS1 PWM results in both i_{dc1} and i_{dc2} being positive, meaning that the overall drive power is formed by combination of V_{dc1} and V_{dc2}.

Coupled PD PWM, however, leads to negative i_{dc2} in the first part of the multilevel range. Gray area between two curves in the bottom subplot in Fig. 10 shows an additional energy loss, caused by overcharging mechanism in the case of PD PWM. This energy would have to be dissipated on the braking resistor in standard drive systems with dynamic braking, in order to maintain optimal four-level modulation and stable dc-link voltages at the same time. Since the lower dc-link voltage inverter is supplied from the controllable dc source, this means that total dc source power in Fig. 10 is calculated as

$$P_{\mathrm{total}}^{\mathrm{dc}} = \begin{cases} \overline{v_{\mathrm{dc1}}(t)\cdot i_{\mathrm{dc1}}(t)} + \overline{v_{\mathrm{dc2}}(t)\cdot i_{\mathrm{dc2}}(t)} & \text{if} \quad i_{\mathrm{dc2}}(t) > 0 \\ \overline{v_{\mathrm{dc1}}(t)\cdot i_{\mathrm{dc1}}(t)} & \text{if} \quad i_{\mathrm{dc2}}(t) \le 0 \end{cases} \tag{12}$$

where the bar over the symbol represents again the mean value over one fundamental period. In the case when both inverters supply the power to the drive, that is, when both dc source currents are always positive, (12) gives the sum of their powers. However, when one of the dc source currents is negative, the total power (i.e., the drive power plus the overcharging power) is sourced from the dc source with positive output current. Since previous analysis showed that this can be the case only with VSI_2, calculation in (12) is based on the analysis of i_{dc2} sign only. This finding is in agreement with previous analysis of the idealized drive model. Fig. 10 leads to the conclusion that coupled PD PWM scheme causes additional energy losses, when compared to the decoupled URS1 PWM.

V. Experimental Verification of Decoupled CB PWM in Closed-Loop Control

The prior analysis shows that URS1 has a better harmonic performance, when compared to the other decoupled modulation methods (see Fig. 4), while it naturally keeps dc-link voltages stable in the whole operation range (see Fig. 10). Consequently, standard three-phase diode rectifiers are now used to obtain dc-link voltages. Isolation between VSI_1 and VSI_2 is provided by means of an isolation transformer, while two auto-transformers are used in order to adjust dc-link voltages to desired levels, 400 and 200 V for VSI_1 and VSI_2, respectively. Experimental results are obtained using two custom built five-phase two-level VSIs and a four-pole five-phase induction motor, as shown in Fig. 11 (the same system, with the exception of the rectifier for the 200 V dc-link, was also used to produce results in Fig. 10). The inverters are controlled using a dSPACE DS1006 processor board, connected to the VSIs via a dSPACE DS5101 digital waveform unit. The switching frequencies of both VSIs equal 2 kHz. The phase and leg voltages are measured using high voltage differential probes P5205A, while the phase current is measured using a high-performance current probe TCP0030.

The steady state and dynamic performance of the decoupled modulation algorithm under FOC is evaluated. Indirect rotor flux-oriented control is implemented to control the speed of the five-phase induction motor, as discussed in [17]. The algorithm is shown in the form of a block diagram in Fig. 12(a) and power invariant transformation is used. The control inputs are measured values of rotor speed ω, position θ and phase currents

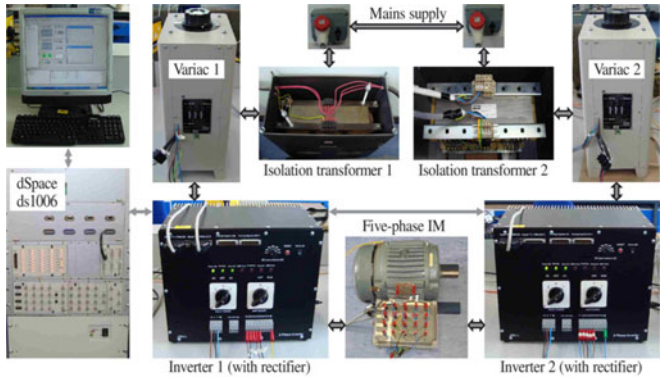

Fig. 11. Experimental setup.

i_k and references for speed ω^* and i_d current component i_d^*. As with three-phase machines, only two current components (i_d, i_q) are required for independent torque and flux control if the multiphase machine has nearly sinusoidal magneto-motive force distribution, as the case is here. However, additional current PI controllers are introduced in order to suppress unwanted nontorque producing harmonics in the *x*–*y* plane, which are mainly introduced by the inverter dead time.

The current control scheme is based on a multiple reference frame structure [17] using PI controllers in several synchronous reference frames in parallel. The method separately controls two of the most dominant current harmonics. This solution requires two pairs of PI controllers, in order to suppress x and y components that correspond to the dead-time induced third and seventh harmonics. The current control structure is depicted in Fig. 12(b). Current components labeled with i_{x3}, i_{y3}, i_{x7} and i_{y7} are obtained with additional rotational transformations that rotate the second plane with $-3\cdot\omega_e$ and $7\cdot\omega_e$, where ω_e is the rotor flux SV electrical angular speed. In this way, obtained i_{x3}, i_{y3}, i_{x7}, and i_{y7} are dc and almost constant, with a small ripple that comes from higher current harmonics, which have amplitudes much lower than the original third and seventh harmonics.

The oscilloscope screen shots (see Fig. 13) show, from top to bottom, the VSI_2 leg voltage v_{21} (CH1), VSI_1 leg voltage v_{11} (CH2), machine phase voltage v_1 (CH3), and the stator current i_1 (CH4) for three different modulation index values in steady-state operation. When $M < 0.35$, drive operates in two-level mode with only the VSI_2 switching, which is in agreement with (5) and Fig. 2. Hence, the machine phase voltage waveform is the same as for a five-phase two-level converter with an effective dc-link voltage of 200 V. Having in mind that all five drive phases are controlled in the same manner, it is clear that VSI_1 forms a star connection on its side of the OeW. In the case of multilevel operation, i.e., $M = 0.5$ and $M = 1$, the drive utilizes both inverters, so the effective dc-link voltage is 600 V. The different dc-link voltages and the switching of both inverters are clearly visible, as is the resulting four-level phase voltage. The obtained waveforms are the same as in [20] where, however, SV PWM was used; hence, the same harmonic performance is achieved but using this time much simpler URS implementation, based on the CB PWM.

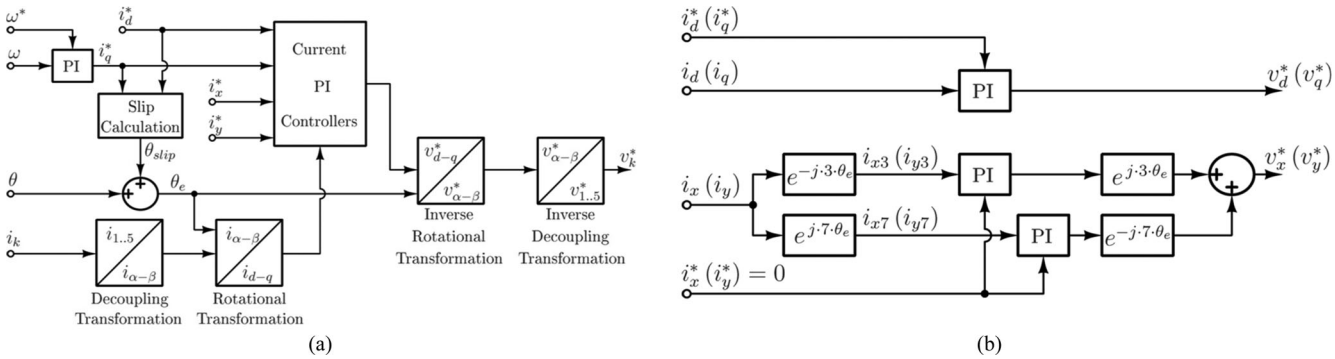

Fig. 12. (a) Rotor flux oriented control algorithm and (b) closed-loop current control algorithm.

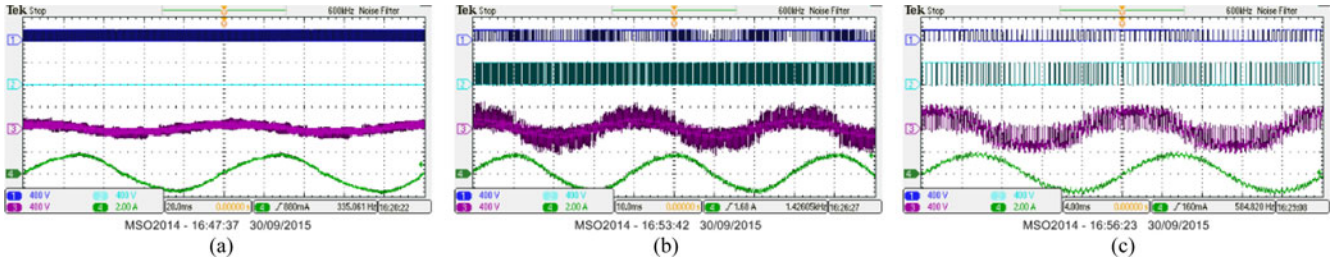

Fig. 13. Experimental results: waveforms with URS1 PWM with (a) $M = 0.2$, (b) $M = 0.5$, and (c) $M = 1$. CH1: v_{21}, 400 V/div; CH2: v_{11}, 400 V/div; CH3: v_1, 400 V/div, and CH4: i_1, 2 A/div.

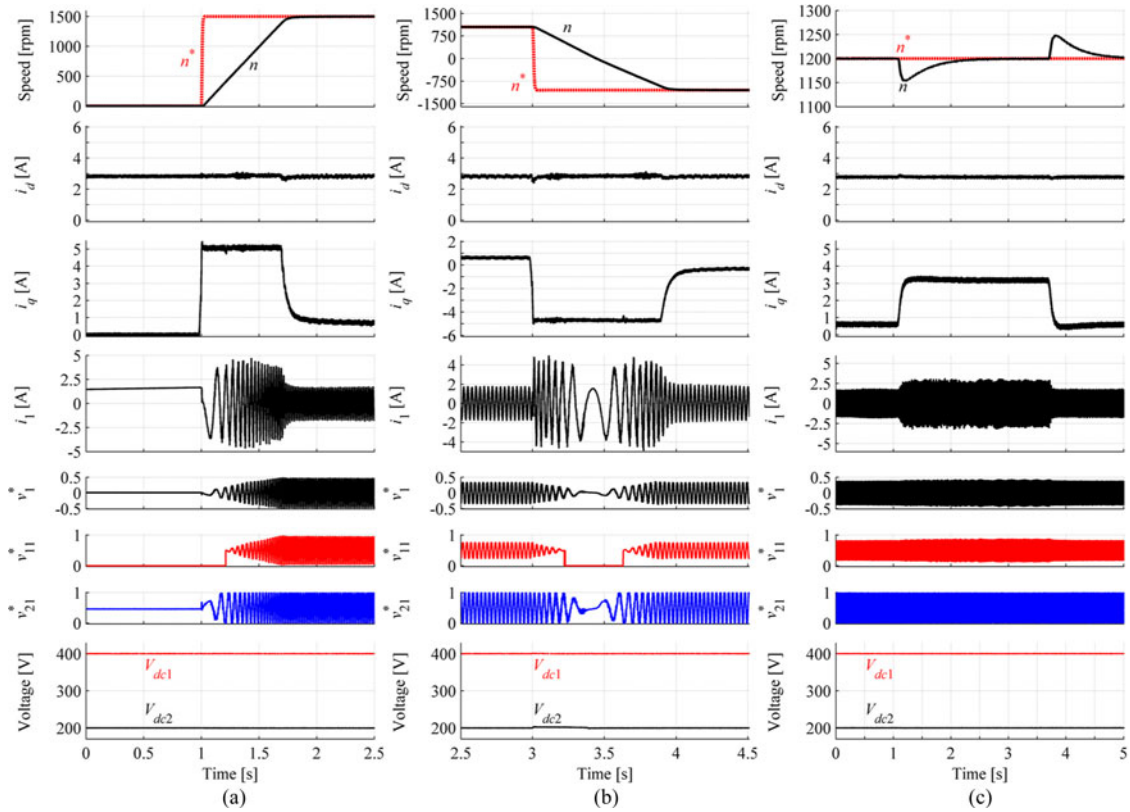

Fig. 14. FOC response with URS1 PWM: (a) acceleration from 0 to 1500 r/min, (b) reversal from 1050 to −1050 r/min, and (c) load application/removal at $n =$ 1200 r/min. Top to bottom: drive speed, i_d, i_q, i_1 v_1^*, v_{11}^*, v_{21}^*, and dc-link voltages.

The dynamic performance of the FOC is presented in Fig. 14. In Fig. 14(a), the speed reference n^* (in r/min) is stepped from 0 to 1500 r/min at $t = 0.5$ s. As expected, the q-axis current reference i_q^* almost immediately steps to its maximum (5 A) value and remains there until the reference speed has been met. The measured q-axis current (i_q) tracks the reference closely. Fig. 14(a) also demonstrates that both dc-link voltages remain constant throughout the entire transient and in the final steady state. Acceleration from 0 to 1500 r/min shows that in the range $0 \leq n < 525$ r/min, $v_{11}^* = 0$, meaning that the VSI_1 forms a star connection at its side of the windings, as explained in Section III. At the same time, VSI_2 operates in PWM mode. For $n \geq 525$ rpm (i.e., $M \geq 0.35$) v_{21}^* has constant amplitude. A speed reversal transient (1050 to -1050 r/min) is presented in Fig. 14(b). Once again, a typical FOC response is observed. As the drive transits through the region when $M < 0.35$, i.e., from 3.25 to 3.6 s, VSI_1 is deactivated, forming again a star point on one side of the machine. Small perturbation in the trace of the lower dc-link capacitor voltage is caused by the electric braking during reversal and it triggers operation of the dynamic brake.

Finally, the response of the drive to step loading and unloading is depicted in Fig. 14(c). Again, the dynamic performance of the drive is excellent with the q-axis current tracking the reference. Disturbance rejection is very fast, as an expectation is with FOC. Presented results clearly demonstrate that the decoupled modulation method does not have a negative impact on the dynamic performance of the drive.

VI. Conclusion

A four-level five-phase OeW drive is analyzed in this paper. The topology employs two isolated dc-link voltages in the ratio 2:1. First, a decoupled modulation scheme, based on the previously developed URS algorithm for an SV PWM algorithm, is developed in conjunction with CB PWM. The stability of dc-link voltages is addressed next, as one of the most important figures of merit for all multilevel drives. A novel approach to the analysis is introduced and applied to the previously widely investigated coupled PD PWM. It is shown that the coupled PD PWM strategy is susceptible to the lower voltage dc-link capacitor overcharging. The same analysis, conducted in conjunction with the decoupled URS method, shows that it is capable of naturally keeping all dc-link voltages stable, in all conditions. These findings are verified experimentally, based on an observation of the dc-link currents during drive acceleration and comparison of energy losses in the cases when coupled PD PWM and decoupled URS1 PWM schemes are used. Hence, decoupled modulation is more suitable for variable speed drives and this PWM method is therefore selected for use in a closed-loop field-oriented controlled drive. The transient performance of the drive is evaluated next. Excellent quality of the dynamic performance is achieved, as evidenced with the experimental results for starting, reversal, and step loading/unloading transients. It can be therefore concluded that OeW drives, controlled using FOC and the proposed modulation technique, are suitable for high-performance drive applications.

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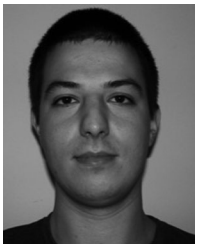

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