Current-Fed Multilevel Converters: An Overview of Circuit Topologies, Modulation Techniques, and Applications

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***Abstract*—Multilevel converters (MLCs) have emerged as standard power electronic converters in high power as well as quality demanding applications. They are classified into current-fed MLCs and voltage-fed MLCs. Voltage-fed MLCs have widely researched whereas the current-fed MLCs are the recent topic of research. Based on the principle of duality between voltage and current sources, several current-fed MLCs analogous to voltage-fed MLCs have been identified. Current-fed MLCs offer several advantages in terms of high power capability, transformerless operation, short-circuit protection, and excellent quality of output current waveform. The goal of this paper is: 1) to present review of circuit topologies, modulation schemes, and applications of current-fed MLCs; and 2) to review an emerging low-device switching frequency modulation technique known as synchronous optimal pulsewidth modulation for current-fed MLCs. The circuit configuration and advantages of each topology along with various modulation techniques are discussed in detail. Compared to voltage-fed MLCs, the operation of current-fed MLCs need to satisfy additional switching constraints. A survey of classical methods for realization of these operational constraints has been done and a new generalized method has been proposed. Finally, future scope of research has been presented to encourage further development of topologies and modulation techniques for current-fed MLCs.**

***Index Terms*—Current-fed multilevel converters, low switching frequency modulation techniques, modulation techniques, solar power integration, synchronous optimal pulsewidth modulation (SOP).**

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NOMENCLATURE

S	Number of sub-converters (CSI H-Bridge or CSI with inductors).
L	Number of current levels.
m	modulation index.
P	Number of polygonal sides of space vector diagram.
I_{dc}	Input dc-current for multilevel converter.
N	Number of switching angels.
d	distortion factor.
α_i	switching angles for $i = 1, 2, \ldots, N$.
h	harmonic content.
m	amplitude modulation index.
i_h	RMS of harmonic current.
$i_{h,six-step}$	RMS of harmonic current of six-step operation.
$S(i)$	slope of level transition.
f_s	switching frequency.
f_1	fundamental frequency.

LIST OF ABBREVIATIONS

CHB	Cascaded H-bridge.
CSI	Current source inverter.
FACTS	Flexible AC transmission system.
FC	Flying capacitor.
HVDC	High-voltage direct current.
IGBT	Insulated-gate bipolar transistor.
IGCT	Integrated gate-commutated thyristor.
MCSC	Multilevel current source converter.
MLC	Multilevel converters.
MMC	Modular multilevel converter.
MOSFET	Metal-oxide-semiconductor field-effect transistor.
NPC	Neutral-point-clamped.
PWM	Pulse width modulation.
SHE	Selective harmonic elimination.
SOP	Synchronous optimal pulse width modulation.
SVM	Space vector modulation.
STATCOM	Static compensator.
VSI	Voltage source inverter.
THD	Total harmonic distortion.

I. INTRODUCTION

THE research on multilevel converters (MLCs) began with introduction of three-level neutral-point-clamped (3L-NPC) converter in 1980s [1]. Depending on the input source,

MLCs can be categorized as voltage-fed MLCs and current-fed MLCs. In voltage-fed MLCs, the output voltage waveforms contain multilevel structure, whereas the current-fed MLCs generate multilevel structure in the output current waveforms [2]. The topologies of voltage-fed MLCs such as NPC, flying capacitor (FC), cascaded H-bridge (CHB), active NPC and modular multilevel converters (MMC), have been extensively studied in the last few decades [3]. Many of these topologies have been commercialized by number of companies and thus, it can be said that they have reached a mature stage [4].

On the other hand, current source converters (CSCs) have been found as better option in various applications. Though CSC has slow dynamic response, they have found in application such as high power drives for fan in which fast dynamic response is not needed. For high power drives, it provides advantages of inherent four quadrant operation. Especially the regeneration mode of operation is so important in which the polarity of voltage at the converter will be reversed to transfer power back to source. For operating this mode CSC does not require any additional circuit [5]. Moreover the inductors in the CSC provide longer lifetime compared to capacitors as in VSC.

Another notable advantage of CSCs is that it provides short circuit protection to drives as the dc link reactor limits the rate of rise of current and, hence, it improves the reliability of the drive [6]. In case of low voltage applications such as fuel cells and solar photovoltaic (PV), CSC provides inherent voltage boosting capability as the inductors in the circuit help in stepping up voltage. Moreover, the direct current control property of CSC enables grid integration without any ac current feedback control [7]. In case of high-voltage direct current (HVDC) system, the short-circuit protection is major concern and also it requires converter that provides higher mean time between failure (MTBF). The inductors in CSC can with-stand high voltage ripple without affecting its performance and hardly suffer from degradation. Hence, the CSC provides longer MTBF which suits for HVDC application. Most of the installed HVDC systems are CSCs because of SCR semiconductors which are higher power and voltage ratings compared to VSCs. Various fully controllable CSCs have also been found in HVDC and FACTS applications [8]. CSC also provides advantages such as independent control of the active and reactive power, the converter can be operated in weak grids or with passive loads and ac-side filters can be eliminated due to low harmonic distortion [8]. Because of these various advantages and applications of CSC, researchers have focused on developing multilevel topologies for CSC in recent years.

The basic advantage of multilevel operation with CSC topologies is high operating current capability with low or medium current semiconductor devices. Vazquez *et al.* surveyed the current-fed MLC topologies and classified them into embedded, two-stage and paralleled MLCs [9]. The embedded current-fed MLCs are suitable for high current and high power applications such as super-conductive magnetic energy storage (SMES) [10]. The paralleled current-fed MLCs with several current sources are recommended for high-power ac drives [11]. The two-stage current-fed MLCs achieve smooth input current with less number of semiconductor devices and they are more attractive power electronic converters for solar power integration [12]. Even though few converters have been identified in [9], for researchers to understand and to develop new current-fed MLCs, there is a need of complete survey of existing current-source MLCs, modulation of these classical MLCs and their applications. Hence, the contribution of this paper are as follows.

1) *Identification and classification of CS MLC topologies:* Provides a detailed discussion of all existing current-fed MLC topologies that are derived using duality principle from voltage fed MLCs. Highlighting their issues in the operation and listing out various suggested solutions.
2) *Conversion methods:* The modulation of current-fed MLC is not straightforward as compared to voltage-fed MLC. The modulation techniques are required to satisfy set of operation constraints such as continuous path for input current and output current should be defined in order to modulate the current-fed MLCs. To achieve these constraints there is need of additional conversion method in the modulation process. This paper surveys various classical conversion methods developed for CSC and also proposes a generic conversion method which can be applied for reference based modulation technique.
3) *Modulation techniques:* This paper surveys various classical modulation techniques that utilize different conversion methods. In addition, this paper also reviews the modified synchronous optimal pulse width modulation (SOP) technique for CS MLC that utilizes the proposed conversion method for operating current fed MLCs. The SOP state-of-the-art has been so far applied only on voltage-fed MLCs.

The contents of this paper are organized as follows: topologies of current-fed MLCs are described in Section II. Several modulation techniques have been discussed and compared in Section III. Applications of current-fed MLCs are explored in Section IV and finally, the future scope of research to further enhance current-fed MLCs is suggested in Section V.

II. Topologies and Classification

Current-fed MLC topologies utilize combination of multiple inductors for splitting input current into equal parts for achieving current multilevel with the help of power semiconductor devices. Usage of current-fed MLC has been started with thyristor-based paralleled CSI at the late 1970s by Nabae *et al.* [13]. Pulse width modulation (PWM)-based higher level current-fed MLC has been identified for SMES application in [14]. Later, this topology has been referred as single-rated inductor current-fed MLC [15]. Following this, a generalized current-fed MLC topology has been proposed [16], which is referred as embedded current-fed MLC in [17]. Recently, current-fed MLCs have been derived from classical voltage-fed MLCs such as CHB, FC, and NPC topologies, based on principle of duality [15]. In addition, several other current-fed MLC topologies have been found through literature study. The classification of various current-fed MLC topologies is shown in Fig. 1 and more details about each topology will be given next.

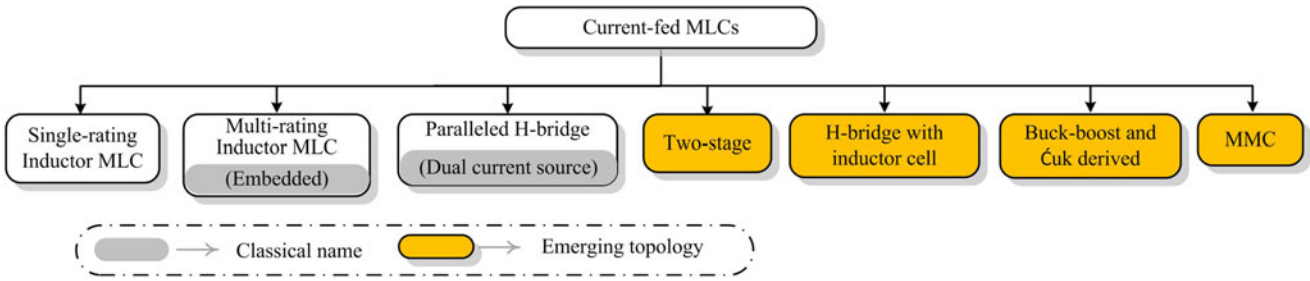

Fig. 1. Classification of current-fed MLC topologies.

The current-fed MLC topologies are operated from either single source or multiple sources. The topologies of single-rating inductor, multi-rating inductor, and paralleled H-bridge current-fed MLC topologies are obtained from classical voltage-fed MLCs by using principle of duality. These topologies are suitable for applications such as active filter [18], power converters for grid-connected PV panels [19], fuel-cell power grid integration [20], wind energy conversion [21], SMES [14], [22], AC motor drives [23], and HVDC applications [24]. A detailed discussion about various current-fed MLCs including emerging topologies is given next.

A. Single-Rating Inductor MLC

A seven-level (7L) topology of single-rating inductor MLC is shown in Fig. 2(a) and it consists of three modules for producing 7Ls ($\pm I_{\rm dc}$, $\pm\frac{2I_{\rm dc}}{3}$, $\pm\frac{I_{\rm dc}}{3}$, and 0) in the output current waveform. It could be extended to any number of output current levels by adding more modules. If the number of modules in the converter is denoted as S, then the output current will have $2{*}S{+}1$ levels. Because of this modularity nature, this topology has been treated as MMC in [25]. However, it differs from conventional voltage-fed MMC in terms that these modules share load current equally among modules irrespective of modulation index whereas in the voltage-fed MMC the load current is shared by few modules and the remaining modules are stopped at lower modulation range [26].

Each module in the single-rating inductor MLC contains three phase legs with top and bottom inductors, and each leg has one top and bottom semiconductor devices. The inductors reduce the current ripple of the module and also provides equal impedance among phases. The diodes are connected in series with switches to provide unidirectional current flow and bipolar voltage blocking capability. The converter has been named as single-rating inductor Multilevel current source converter (MCSC) by Zhihong Bai because input dc current is distributed equally among the inductors and, hence, all the inductors are of same current rating [15]. This converter is identified as dual of voltage-fed diode-clamped MLC. If the five-level (5L) configuration of this topology with the fully controlled switches are replaced by half-controlled thyristors then the topology resembles multiple current source inverter invented by Nabae in 1977 [13] and later in 1995 Uchino has patented this topology which has gate turn-off thyristors (GTO) [27]. The notable advantages of the single-rating inductor topology are increased current capacity, reduction of conduction losses as the current through devices are reduced, meeting harmonic standards without the need of expensive filters, etc. [14].

The major issue with this converter is balancing inductors currents of modules otherwise the unequal current increases the output total harmonic distortion (THD) and introduces low-order harmonics which require higher value of capacitor for filtering them out. A carrier-phase-shift modulation technique can be adopted to overcome this issue by swapping carrier waves on consecutive fundamental cycles [28]. However, this approach cannot be applied for higher levels as the increase in number of levels results in increased swapping periods. In [29], a vector-based inductor current balancing has been achieved for 5L converter by utilizing redundant vectors, however, this methodology increases the complexity for higher levels as the number of redundant vectors is increased. The module current balancing control methodology approached by these modulation techniques is focused on controlling current flowing in the top inductor with the assumption that both the top and bottom inductor current are same. However, the imbalance in inductor currents within a module has been studied in [30], and proposed a novel method for balancing inductor currents. This method utilizes zero vectors for balancing when there is a deviation in the inductor currents and output filter capacitor voltage. This also brings additional damping for the resonance raised from inductor–capacitor filter. The another limitation with the single-rating inductor MLC topology is the more number of inductors and, hence, the size of converter will be bulkier. The inductors count within a module cannot be reduced in order to keep the advantage of power balancing. Palaniappan *et al.* have suggested improvement of 5L configuration of this topology by wounding two top inductors in one core and two bottom inductors in another core which was termed as interphase inductors as shown in Fig. 2(b) [31]. These interphase reactors on single-rating inductor MLC help in reducing the overall size of the converter by four times [32]. In normal scenario, the inductors in the modules face the switching frequency of the semiconductor but with this interphase reactors the switching frequency faced by the module inductors get twice and, hence, the overall volume is reduced [33].

B. Multi-rating Inductor MLC

The multi-rating inductor shown in Fig. 3(b) is identified as a dual of FC voltage-fed MLC [15]. This converter

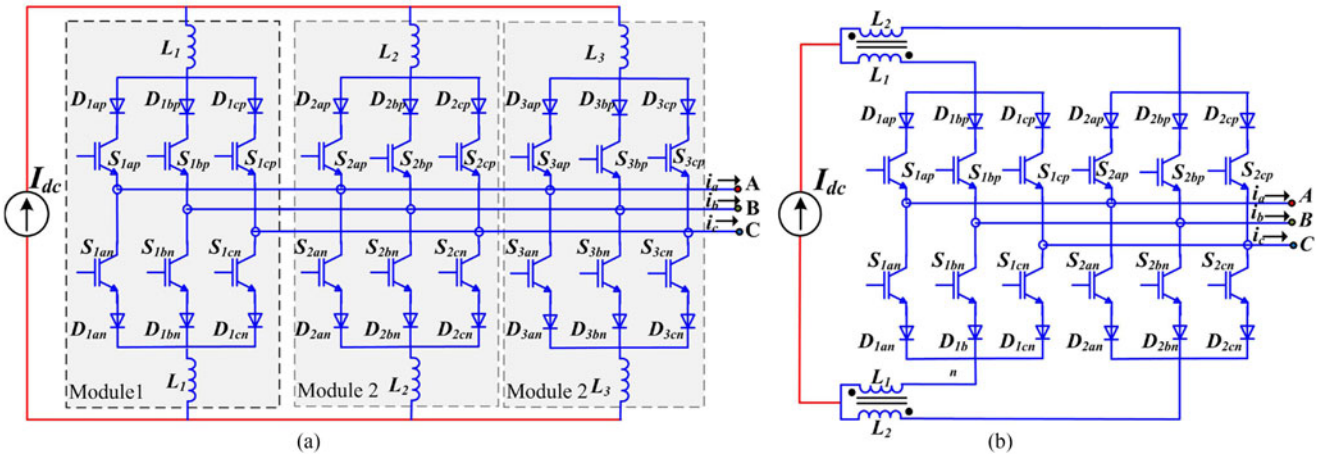

Fig. 2. Single-rating inductor MLC. (a) 7L inverter (b) 5L inverter with interphase inductors.

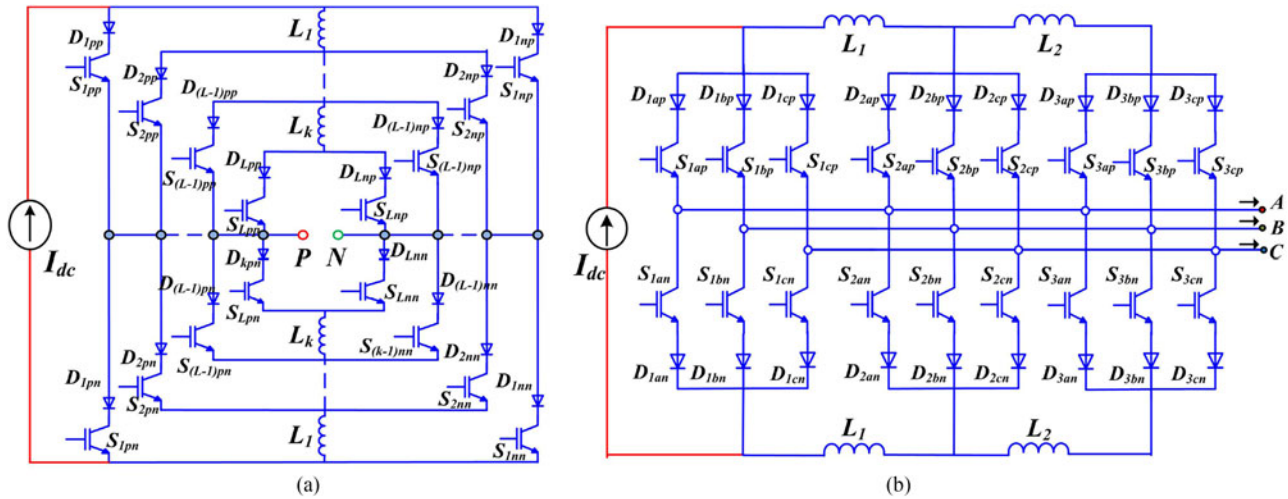

Fig. 3. Multi-rating inductor MLC. (a) Single phase (embedded). (b) Three phase.

has been derived from parallel commutation cells identified for dc–dc converters by making use of inductors as current sources [34].

The two sets of parallel commutation cells are reoriented and one set is connected to positive rail and another one for negative rail to derive single-phase multilevel current source inverter [16]. The single phase multi-rating inductor MLC is also named as embedded MLC as in [9] and the arrangement of inductors with semiconductor devices is shown in Fig. 3(a). The topology utilizes intermediate inductors that split input current into multiple currents at different magnitude, thus avoiding the need for isolation coupling transformer [35]. The converter can be operated at low-frequency modulation to achieve an output current with some harmonic elimination. To make sure there is equal current distribution among switches, the duty cycle and resistance of semiconductor devices has to be same. To ensure this requirement, two switching strategy has been identified in [16]. One is symmetric switching strategy which operates the semiconductor devices with 50% duty cycle and achieves the current balance within two cycles. However, if this strategy applied for higher level converters then the inductors current ripple will increase which may cause the imbalance in the current among semiconductor devices. This has been avoided using asymmetric switching strategy which provides unequal duty cycle among semiconductor devices and achieves current balancing within a fundamental period [16]. This strategies ensure current balancing under open-loop condition, however, for higher levels of this topology, it needs higher computation in identifying the balancing situation. In [10], a generic combination strategy has been framed for single-phase multi-rating inductor MLC for L-level which utilizes four steps to achieve zero inductor voltage, 50% conduction period of each switch, and minimum current ripple on inductors [16]. The four steps involve determination number of combinations (2^{L-1}), populating states of switches that are connected to output phase terminal (S_{ipn}, S_{ipp}, where $i = 1, 2, 3, \ldots, L$) for each combination, identifying output current and voltage states, and finally the combination sequences with minimum frequency is selected with a computation algorithm. The three phase version of this multi-rating inductor has been developed in [36] and the topology is shown in Fig. 3(b), which can produce 3^{2*L} number of switching combinations.

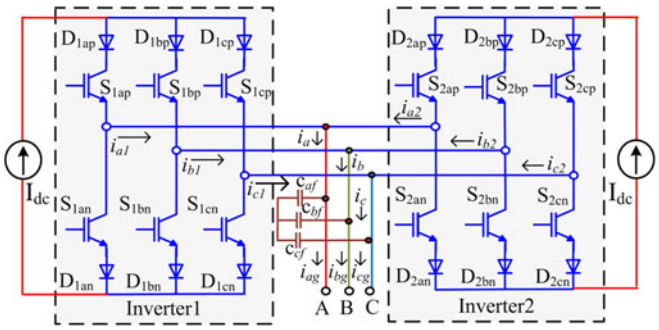

Fig. 4. Paralleled H-bridge MLC.

Similar to single-phase version of multi-rating MLC, the inductor current balancing is one of the key issue in the three phase version of multi-rating inductor MLC. Though the fundamental frequency switching method explains about the inductor current balancing based on developing combination table, the dynamic performance study performed in [37] shows that a slight variation in the resistances of the inductor will cause imbalance and it requires load impedance domination to nullify the effect of differences in resistance of the inductors. The another way to avoid the effect of inductor resistance mismatch is either by choosing appropriate modulation technique or by developing closed-loop techniques [37]. Since this topology is a dual of FC voltage-fed MLC, the natural current balancing approach by a carrier phase-shift method has been applied and verified in [37]. In [38], a closed-loop control is proposed by utilizing redundant switching states for balancing the inductor currents. The voltage across intermediate inductors is fed back to the controller for determining the state selection. In case of converter modulated with Space vector modulation (SVM), a vector-based current balancing is achieved in [39] by choosing zero vector based on the polarity of the voltage across intermediate inductor. Another notable issue in the multi-rating converter is the number of semiconductor devices, a modified version of this topology has been proposed in [40] for achieving same performance of conventional multi-rated converter at the cost of increased current rating of few semiconductor devices.

C. Paralleled H-Bridge MLC

The first type of paralleled H-bridge MLC was introduced by Palaniappan during 1979 using thyristors and called it as dual CSC for ac drives applications [31]. Later, it is identified as dual of voltage-fed CHB VMLC [15]. It could also be observed from Fig. 4 that the paralleled H-bridge topology MLC resembles the single-rated MLC. However, it differs in the sense of independent current sources whereas single-rating MLC uses single dc source and, hence, the parallel H-bridge MLC does not face circulating current and current imbalance issues [21]. However, deriving multiple current sources is another complex task. Especially in drive applications, these dc current sources need to be obtained from multiple current source rectifiers with phase-shift transformer. Hence, equal dc currents can be obtained by controlling the rectifier which avoids imbalance issue and also the inverters can be operated with fixed gating patterns [41]. This combination of rectifier and parallel inverters have been treated as modular CSC, however, for consistency in nomenclature this topology is referred as parallel H-bridge MLC in this paper. The complete switching operation of 5L-paralleled H-Bridge converter can be referred from [42]. A 7L converter of this topology has been suggested for super high-power ac drives (>20 MW) as in [43], in which multiple dc current sources are obtained through 18 pulse transformer with identical SCR rectifiers.

Another well-known resources of multiple current sources are solar PV application, and parallel H-bridge MLC is a suitable candidate for this application [44]–[46]. However, the PV sources produce unequal dc currents due to partial shading and varying insolation. Under such variation, the parallel H-bridge output current will have low-order harmonics. To handle unequal currents a closed-loop controller with modulation strategy is needed for keeping output ac current within required THD standards [45]. In [44], the combined current control with *dq*-frame control strategy using carrier-phase-shift-modulation technique has been approached to handle unequal currents. This control strategy has achieved seventh-order harmonic elimination, better output quality waveforms even at low switching frequency with inexpensive capacitive filter [46]. In another paper [45], space vector-based strategy has been approached to operate converter under unequal input currents. In this approach, two methods of selecting switching state vectors has been obtained and the low-frequency pulsation in the dc-link voltage has been eliminated for achieving better THD. Another notable issue with this converter topology is the resonance due to inductor and filter capacitor which will introduce the lower order harmonics in the output current. The resonant issue has been overcome in [47], by introducing active damping in the controller design using a virtual resistor.

The main disadvantage of this topology is the requirement of many isolated dc-current sources in terms of ac drive applications. This results in bulky, complex, bigger inductors, and high-cost isolation transformers [48]. However, in case of solar applications, the space is not constraint and also there is no need for transformers as the solar power is obtained through multiple PV sources. For ac drive application, Kwak and Toliyat have proposed a modified version of this topology by replacing one PWM CSI module by load-commutated inverter (LCI) module [49]. The modified topology combines semi controlled LCI as one module and fully controlled GTO inverter as another module. By doing so, the advantage of soft switching in LCI module is achieved and in addition the combination has also reduced the filter size and overall cost.

D. Emerging Multilevel Topologies

Developing new current-fed multilevel topologies has become main focus by various researchers for reducing the number of passive and active devices, to apply duality principle in obtaining current-fed MLC from well-established voltage fed MLCs and also to increase the reliability of the converter [50].

1) Two-Stage MLC: One of the emerging topology is a two-stage MLC which is also named as boost MLC. The single-phase configuration of this topology is shown in Fig. 5(a). It is made

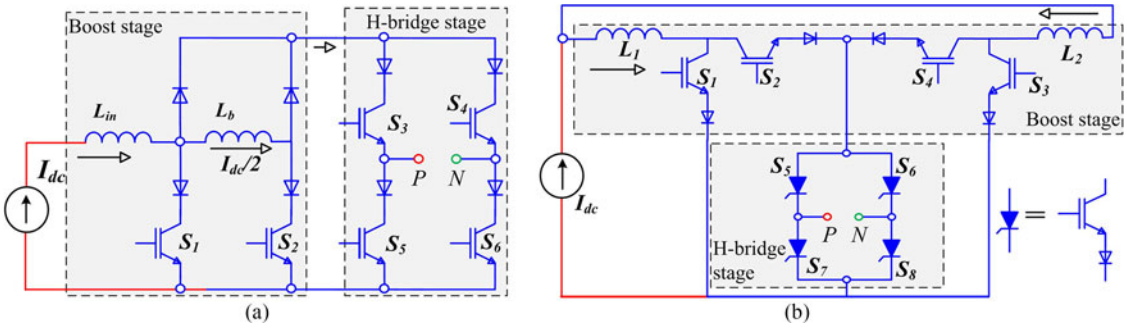

Fig. 5. Two-stage current-fed MLC. (a) Boost stage using multi-rated cell. (b) Boost stage using single rated cell.

up of a three-level dc–dc boost converter stage with four semiconductor devices and an H-bridge inverter stage. The boost stage is operated at designed switching frequency whereas the H-bridge is operated at fundamental frequency [12]. The intermediate current levels are achieved by the inductors and they help in balancing the different current levels. The topology has been introduced by Yu using the generic multilevel inductor cells [51]. As explained in Section II-B that multi-rated MLC also have been derived using multilevel inductor cells. In case of multi-rated MLC topology, to make a generic L-level it requires 2* $(L-1)$ semiconductor devices and $(n-3)$ current sharing inductors, whereas with the two-stage MLC topology only $(L+3)$ semiconductor devices and $\frac{L-3}{2}$ current sharing inductors are needed [51]. A detailed modes of operation of two-stage MLC can be referred from [52]. To further reduce the number of switches in the converter by half in number, the top switches in the boosting stage of the topology can be replaced by power diodes [50]. The mathematical derivation for the design of the intermediate inductors for 7L two-stage converter can be referred from [50]. It shows that the value of main inductor (connected to dc side) depends on the inverter fundamental frequency, whereas the intermediate inductors value depends on switching frequency. In [53], the boost stage of two-stage MLC has been achieved by single-rated 3L current cell instead of multi-rated inductor cell and the diodes are replaced by semiconductor switches as shown in Fig. 5(b).

2) H-Bridge With Inductor Cell MLC: Another emerging topology, which has been recently proposed based on common emitter arrangement with inductor cells is shown in Fig. 6. Common emitter arrangement of switches reduces the number of driver circuits [54]. By incorporating this advantage, Naguchi and Suroso have developed the H-bridge with inductor cell topology by introducing inductors as dc current sources in the common emitter configuration. The CSI H-bridge acts as the main inverter of the topology followed by parallel connection of single or more inductor cells which act as auxiliary circuits. Each cell is composed of an inductor with four unidirectional semiconductor devices [55]. If number of level is represented as L-level and number of auxiliary inductor cells is represented as N_{cell} then the relationship is given by $L=(2^{N+1}+1)$ and the current flowing in the inductor cell i is given by $\frac{I_{\text{dc}}}{2^i}$, where $i=1,2,\ldots,L$. Due to this modularity nature, the topology has been classified as hybrid MMC in [25]. The major operational difference between this topology and rest of the topologies discussed so far, is that the inductors in the cell have three states such as charging (positive current slope), discharging (negative current slope), and constant current circulation (inductors shorted) whereas the other topologies have only charging or discharging states. The modes of operation can be referred from [48]. The additional advantage of this topology are smaller di/dt, reduced output filter size, small value of inductors compared to multi-rating inductor and single-rating inductor MLCs and avoidance of isolated gate driver due to common emitter configuration [48].

3) Buck–Boost and Ćuk Derived CS-MLC: Buck–boost derived 5L CSI is shown in Fig. 7(a). Unlike other current-source MLCs which are aiming at voltage boost, this converter employs buck–boost technique to realize low voltage output. The buck–boost derived converter utilizes voltage source and two inductors with two CSIs to achieve multilevel in the output current waveform. Additional semiconductor devices S_W and $S_{W'}$ are employed to effectively isolate the input dc rails from unnecessary circulating currents between CSIs [56]. The topologies discussed so far face difficulties in maintaining a constant output voltage if the input side voltage rises or lowers. However, with the buck–boost topology this difficulty can be overcome as it can operate with wide voltage-conversion range with minimal number of components. In addition to this, the topology has natural balancing of dc-link inductor currents within each switching cycle without additional hardwares [57]. With the alternative phase opposition disposition (APOD) modulation, the shoot through path is achieved during which one of the inductor free wheels and the other one can charged through source [56]. This helps in reducing the component count by removing the semiconductor device $S_{W'}$ and the modified topology is shown in Fig. 7(b). The input current in the buck–boost 5L CSI is of discontinuous nature and, hence, in order to maintain smooth input current a current-source version has been suggested as shown in Fig. 8(a). This topology is named as Ćuk-derived 5L CSI and it differs from buck–boost derived topology by replacing the voltage source by the current source and an ac capacitor [56]. The operating principle and switching patterns of both buck–boost derived and ćuk-derived 5L CSIs are similar except that inductive charging energy is derived through capacitor C in case of Ćuk-derived topology. Detailed switching operation and mathematical analysis can be referred from [57].

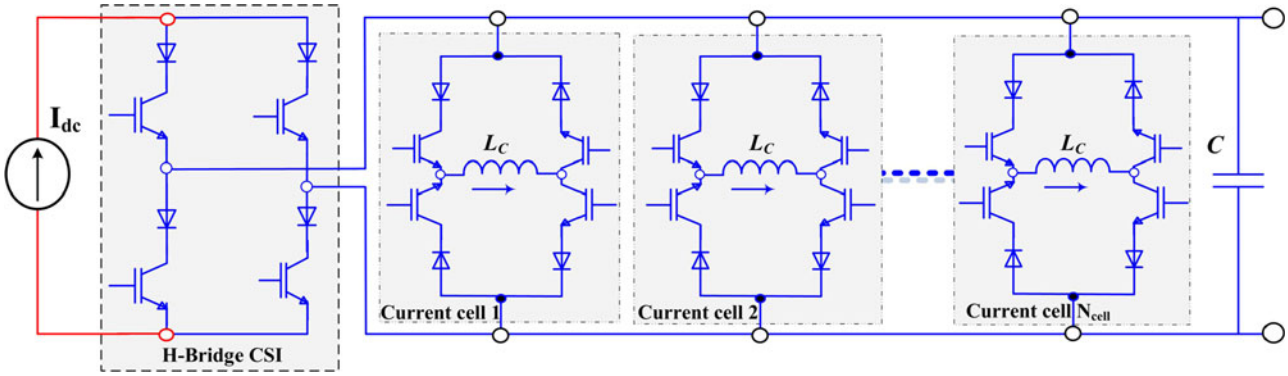

Fig. 6. H-bridge with inductor cells.

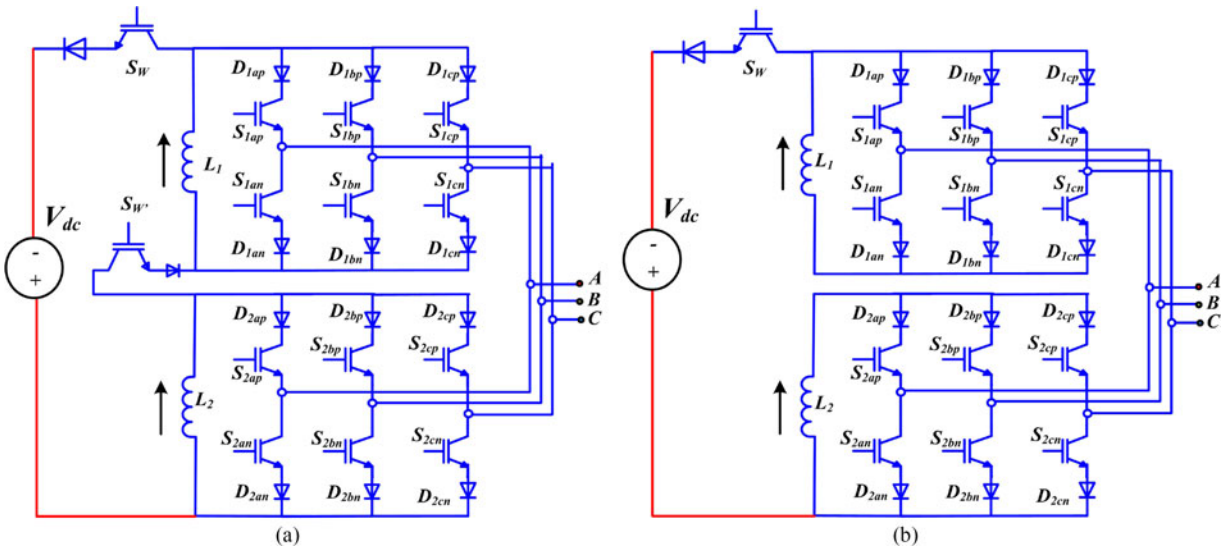

Fig. 7. Buck-boost derived 5L CSI (a) with two switch arrangement. (b) with reduced component count.

4) Modular Multilevel Converter: MMC has been in the recent research trend and it has received high attention from academia as well as from industry [58]. Current source MMC has been proposed recently by Liang *et al.* [25]. In general, the circuit configuration of MMC has three arm-legs for three phase and each leg has two arms one for positive rail and another for negative rail. The arm comprises of several modular cells to produce multilevel output waveform. In case of voltage fed MMC, the modular cells are made of capacitor and semiconductor device combinations, and they are connected in series to produce multilevel voltage. In other words, connecting modular cells made of inductors and semiconductor devices in parallel on each arms produces multilevel current waveform. The MMC topology with the inductor modular cells is shown in Fig. 8(b) [25]. The basic inductor-based modular cells such as half-bridge cell and full-bridge cell are shown in Fig. 8(b) and these cells are inserted or bypassed in each arm of the converter to control the output current. A detailed analysis and operation of the current source MMC can be referred from [24].

The dangerous fault that could happen for current source MLC is open-circuit fault which is common for all current source topologies, especially in the modular topology its possibility of occurrence is high due to more inductors. This could be avoided by modifying the inductor cells with antiparallel connection of press-pack diodes or thyristors to provide emergency current path during short interval of time [59]. Another common issue that could be faced by current-fed MLC listed in Sections II-A to II-C on high-voltage application is that semiconductor devices have to face full ac voltage. In [59], this issue has been overcome by the voltage scaling methodology for current source MMC by modifying the modular cells to have both inductor and capacitor. Circulating current is a commonly found issue in MMC, in case of current source MMC this is caused by the ripple current in the sub-module inductor. Bhesaniya and Shukla have proposed inductance selection method on current-fed MMC which ensures the minimization of inductor ripple current [24] and thereby it reduces the circulating current.

E. Comparison of Topologies

The overall comparison with advantages and challenges of the presented topologies is shown in Table I. Since some of the emerging topologies are only applicable for single-phase

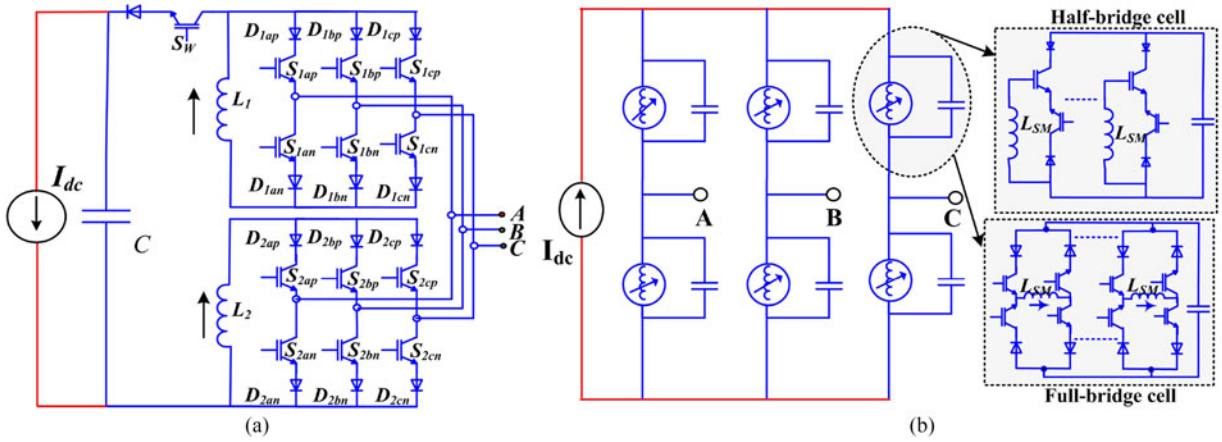

Fig. 8. Emerging topologies. (a) Ćuk derived 5L CSI. (b) Current-fed MMC.

TABLE I
SUMMARY OF CHARACTERISTICS OF SURVEYED CURRENT-FED MULTILEVEL TOPOLOGIES

Topology	Single-Rating Inductor	Multi-Rating Inductor	Paralleled H bridge	Two stage MCSC	H-Bridge with inductor cell	Buck Boost and Ćuk derived	MMC
Advantages	-Modularity	-Modularity	-No imbalance issue	-less device counts	-Smaller inductor value	-Wide voltage range	-Modularity
	-Simple structure	-Simple structure	-No sharing inductors	-Dual frequency	-Less driver circuits	-Self current balancing	-High power capability
		-No passive elements in modules		-Less inductor count	-Less inductor count		
Challenges/cons	-current imbalance	-current imbalance	-multiple sources	-current imbalance	-high current rated inductor	-current imbalance	-more components
	-circulating current	-circulating current	-unequal input currents	-limited levels	-controller to maintain cell currents	-high current rated device	-high cost and volume
Inductor count	$L-1$	$L-3$	no sharing inductors	$(L-3)/2$	$\log_2(L-1)-1$	$(L-1)/2$	$4(L-1)$
(if $L=5$)	(4)	(2)	no sharing inductors	(1)	(1)	(2)	(16)
switch count	$2(L-1)$	$2(L-1)$	$2(L-1)$	4+(L-1)/2	$4\log_2(L-1)$	$5(L-1)/2$	$8(L-1)$
(if $L=5$)	(8)	(8)	(8)	(6)	(8)	(10)	(32)
Max. inductor rating	$2I_{\rm dc}/(L-1)$	$I_{\rm dc}(L-3)/(L-1)$	$2I_{\rm dc}/(L-1)$	$I_{\rm dc}(L-3)/(L-1)$	$I_{\rm dc}/2$	$I_{\rm dc}/(1-$ duty-ratio)	$I_{\rm dc}/(L+1)$
($L=5$,duty-ratio $=0.75$)	$(I_{\rm dc}/2)$	$(I_{\rm dc}/2)$	$(I_{\rm dc}/2)$	$(I_{\rm dc}/2)$	$(I_{\rm dc}/2)$	$(4I_{\rm dc})$	$(I_{\rm dc}/6)$
Inductor size	L_{100}, L_{fsw}	L_{100}	L_{fsw}	L_{100}	L_{fsw}	L_{fsw}	L_{100}
DC Sources	1	1	$(L-1)/2$	1	1	1	1
Semiconductor devices	IGBT, MOSFET, SiC diodes	IGBT, MOSFET	GTO, IGBT	MOSFET, IGBT	MOSFET	IGBT	IGBT
Application	SMES, ac drives L_{100} −100 s of mH	SMES L_{fsw} −freq. dependent	PV, ac drives	PV, Wind	PV	SMES	STATCOM

operation, the comparison table is made based on single phase version of the presented topologies. The details related to the inductors are formulated by only considering sharing inductors or cell inductors. The input side inductors are not included since they are found in all the current-fed converters.

It could be observed that the classical topologies such as single-rating inductor, multi-rating inductor, and parallel H-bridge are utilizing same number of semiconductor devices for obtaining L levels in the output current waveform. This is because all three are H-bridge modules based inversion. For single-rating inductor and multi-rating inductor topologies, current balancing is the main challenge for the inverter operation [30], [35]. The sharing inductors in the modules are in the order of 100 s of mH to reduce low-frequency ripple in the module currents [16], [28]. However, for single-rating inductor MLC, the ripple current amplitude is half that of multi-rating inductor MLC for same values of sharing inductors. This is because the low-frequency ripple current flows through four sharing inductors in 5L single-rating inductor MLC whereas in case of 5L multi-rating inductor only two inductors appear in the current path. The low-frequency ripple issue can be eliminated in single-rating inductor topology by utilizing interphase trans-

formers and with that inductances size depend only on switching frequency [33]. In case of parallel H-bridge, the dc input current ripple is controlled by the dc–dc converter or current-source rectifier at the front end. In case of rectifier-based input dc source, the inductor size will be of the order of 100 s of mH whereas in case of dc–dc converter the input inductor size is decided by the switching frequency [49], [60]. Two-stage MLC also utilizes large inductors since the switching operation of the single-phase H-bridge introduces second-order frequency ripple in the input current [12]. For MMC topology, the cell inductors act as storage element and the size of the submodule inductor $L_{\rm SM}$ is decided by the amount of energy need to be stored in the submodule. The value can be calculated as [24]

$$L_{\rm SM} = \frac{\triangle E}{2N_{SM} i_L^2 \triangle i_L} \tag{1}$$

where $\triangle E$ represents the peak-to-peak energy variation in the arm, $\triangle i_L$ represents per-unit current ripple in the submodule inductor, $N_{\rm SM}$ represents number of submodules per arm, i_L is the inductor $L_{\rm SM}$ current, and the value of $L_{\rm SM}$ will be in the order of 100 s of mH. In case of buck–boost derived and H-bridge with inductor cell converters, the inductors values are dependent on the switching frequency of the converter [48], [57].

The size and volume of the converter can be analyzed by considering parameters such as the number of devices, number of sharing inductors, current rating of the inductors, and value of the inductor. With the advanced development in the semiconductor devices, the insulated-gate bipolar transistor (IGBT)/metal-oxide-semiconductor field-effect transistor (MOSFET) devices are available in different configurations such as three-phase bridge, single-phase bridge, half bridge, etc. The size of these package modules are more compact and, hence, in the overall converter size, the devices size is minimal when compared to the inductor size. For current-fed converters, the size of the inductors decide the overall size of the converter. From the Table I, it could be observed that the MMC topology is having more number of inductors as well as the values of inductors are in the order of 100 s of mH and, hence, the MMC is larger in size among all the topologies. Single-rating inductor is the next topology with higher number of inductors and the inductors sizes are also in the order of 100 s of mH, however, 28.2% volume can be reduced if interphase transformers replace the inductors. Multi-Rating inductor MLC and buck–boost derived MLC have same number of inductors but buck–boost derived value depends on switching frequency and, hence, the converter volume can be reduced. Even though parallel H-bridge has no sharing inductors but it needs multiple dc sources which makes it the largest among other converters. Two-stage and H-bridge with inductor-cell MLC topologies achieve required current level using single sharing inductor, however, the two-stage inductor value is larger compared to the H-bridge.

The current-fed multilevel topologies utilize fully controllable switches in order to achieve the better quality waveforms. The reverse voltage blockage capability and unidirectional current flow are the minimum criteria for semiconductor devices selection. A series diode with IGBT or MOSFET device can achieve the reverse voltage blocking at the expense of losses and cost. The semiconductor devices such as reverse block (RB) IGBTs and integrated gate-commutated thyristors allow reverse voltage blocking operation and, hence, the series diodes can be avoided [61].

III. Modulation Techniques

The aim of the modulation techniques for current-fed MLCs is to produce stepped waveform for given operational condition (frequency, amplitude, and phase fundamental component) and also to minimize the input current ripple. Other criteria of modulation technique include achieving current balance between multiple inductors [26], minimizing the harmonic distortion of output current [62], maintaining equal distribution of power losses among modules or semiconductor devices, and so on [63]. The modulation techniques that are widely used in voltage-fed MLC have been modified and proposed for current source MLCs. Compared to voltage-fed MLCs, modulation of current-fed MLC needs to satisfy additional set of constraints, hence an extra conversion method need to be included in order to implement the constraints. The various conversion methods are surveyed and are explained in this section. This section also explains how these methods are extended to multilevel operation from CSI operation. In addition, a generic conversion method for realizing the operational constraints on current-fed MLC is proposed in this paper. Finally, various modulation schemes that utilize these conversion method is discussed in detail.

A. Realization of Operational Constraint

The minimum requirement of the switching states of the CSC is to ensure the following constraints [64].

1) Continuous path for input dc current $I_{\rm dc}$: Since the converter are connected to constant current sources, it is required to maintain continuous path for the input current. Otherwise, it results in high voltage spikes across the devices.
2) Output ac current should be defined by converter and not by the load: In voltage source inverters, the output voltage waveform is decided by the switching operation of the converter whereas the fundamental magnitude of output current is decided by the load. However, in case of current source inverters the output current should be decided by the converter operation and not by the load.

For single-phase converter, achieving these constraints is straightforward but for three-phase converters, it requires special conversion technique. The conventional methods used for achieving these constraints on three-phase topologies are given next.

1) Tri-Logic Conversion: Tri-logic conversion is a two-stage method for incorporating the operational constraints on switching pulses. The conversion is an indirect way of achieving constraints by using bi-logic signals from VSI PWM techniques. The name tri-logic depicts that there are three output currents levels, they are $+1$, -1, 0 for each phase variable $Y_\phi(t), (\phi = a, b, c)$. The method involves two stage conversion, in the first stage the bi-logic pulses (± 1) for each phase are

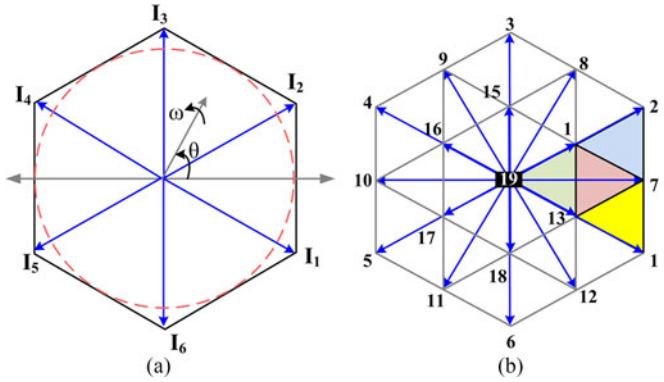

Fig. 9. Space vectors for (a) CSI operation and (b) 5L operation

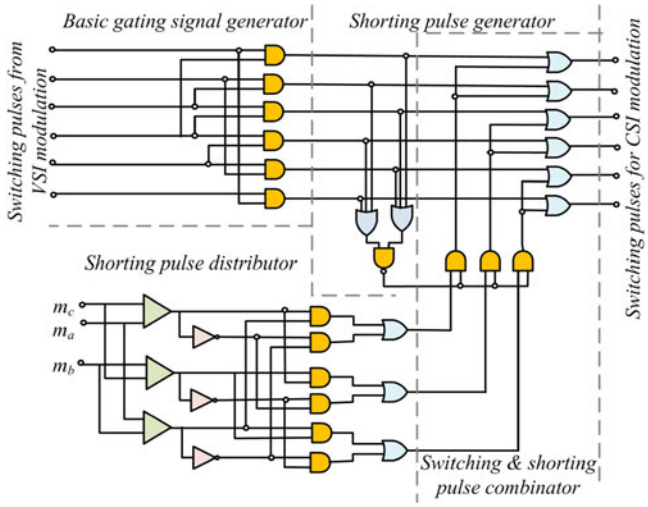

Fig. 10. Logical circuit based conversion.

obtained as $X_\phi(t)$ by comparing a triangular carrier wave with sinusoidal wave. These bi-logic pulses are converted into tri-logic pulses using a linear mapping as follows [65]:

$$\begin{bmatrix} Y_a(t) \\ Y_b(t) \\ Y_c(t) \end{bmatrix} = \frac{1}{2}[C] \begin{bmatrix} X_a(t) \\ X_b(t) \\ X_c(t) \end{bmatrix}; C = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}. \quad (2)$$

The basic requirement for this conversion is that it needs carrier-based modulation in order to obtain bi-logic signals. For extending this conversion technique to multilevel operation, the bi-logic outputs for each carrier wave should be converted to tri-logic level. For example, in single-rating inductor MLC, each module can be treated as single CSI and, hence, dedicated bi-logic signals can be obtained using conventional carrier-phase-shifted sinusoidal (CPS)-PWM for each module which can be converted to tri-logic signals [26].

2) SVM-Based Conversion: The space vector-based realization of CSI operational constraints involves identifying switching combinations that satisfy operational constraints and creating space vectors. Since this method is dependent on the switching combination, it is required to derive all the switching combinations. For single current source inverter, the space vector with switching states are given in the Fig. 9(a). Extension of this method for multilevel operation is straightforward, as it just increases in the number of state vectors as the switching combinations increase with number of levels as shown in Fig. 9(b). There are 81 feasible switching combinations with 19 state vectors which can be identified for 5L CSI [66], and for 7L inverter there are 343 switching combinations and 37 state vectors [67]. As the complexity of identifying switching combination and modulation of the state vectors are difficult for higher levels, the MLC with highest level using space vector method found through literature is a 7L MLC.

3) Trapezoidal Carrier: Trapezoidal is a direct conversion method that utilizes a modified carrier wave to compare with trapezoidal modulation wave to obtain gating pulses for operating CSI. The modified carrier waveform is obtained by resetting triangular carrier wave for the period 60° to 120° as well as 180° to 360° to zero [64]. The comparison of these waveforms can be referred from [64]. This method can be extended for multilevel by modifying all the carrier waveforms for the period 60° to 120° and 180° to 360° as explained and, then, comparing them with trapezoidal modulation signal for producing multilevel waveforms [43].

4) Logic Circuit-Based Conversion: This conversion method has been identified for selective harmonic elimination (SHE)-based modulation of CSI [68]. This method involves four step of operation to realize constraint on the converter. The four steps are *basic gating signal generator*, *shorting pulse distributor*, *shorting pulse generator*, and *shorting and switching pulse combinator* as shown in Fig. 10. The basic gating signal generator maps switching pulses generated from voltage source modulation to basic gating pulses of CSI using switching combination table. These generated CSI basic gating pulses are then used for generating shorting pulses. The shorting pulse distributor creates distributing signals by using three-phase modulation signals. In the last step of conversion, both basic switching pulses and shorting pulses are combined to create gating pulses required for operating CSI [68]. Multilevel operation using this method can be achieved by having dedicated logical circuit for each CSI module in the case of single-rating inductor MLC.

5) Proposed Conversion Method: In this paper, a new technique which resembles the tri-logic methodology has been proposed, however, the proposed method treats a reference multilevel waveform as a base whereas the tri-logic utilizes bi-logic signals as base. In this method, a reference waveform without any constraints will be considered and it will be phase shifted by 120° to obtain a five-level waveform [69]. Unlike tri-logic conversion which depends on bi-logic outputs, this method is so generic that any level of waveform can be converted to constraint current source reference signal. The objective of this conversion method is to derive realizable waveform from any quasi-sine reference wave in order to include the operational constraints mentioned in Section III-A, while keeping the main objective of the reference waveform. Let's consider that a 5L CSI is needed to be obtained by using this conversion method. The switching combination can be referred from Table II. It shows at any instant of time, the sum of three-phase output current levels should be

TABLE II
SWITCHING STATES AND OUTPUT CURRENT OF 5L CSI

$State$	I_a	I_b	I_c
1	0	0	0
2	0	$I_{\rm dc}$	$-I_{\rm dc}$
3	0	$2I_{\rm dc}$	$-2I_{\rm dc}$
4	0	$-I_{\rm dc}$	$I_{\rm dc}$
5	0	$-2I_{\rm dc}$	$2I_{\rm dc}$
6	$I_{\rm dc}$	0	$-I_{\rm dc}$
7	$I_{\rm dc}$	$I_{\rm dc}$	$-2I_{\rm dc}$
8	$I_{\rm dc}$	$-I_{\rm dc}$	0
9	$I_{\rm dc}$	$-2I_{\rm dc}$	$I_{\rm dc}$
10	$2I_{\rm dc}$	0	$-2I_{\rm dc}$
11	$2I_{\rm dc}$	$-I_{\rm dc}$	$-I_{\rm dc}$
12	$2I_{\rm dc}$	$-2I_{\rm dc}$	0
13	$-I_{\rm dc}$	0	$I_{\rm dc}$
14	$-I_{\rm dc}$	$I_{\rm dc}$	0
15	$-I_{\rm dc}$	$2I_{\rm dc}$	$-I_{\rm dc}$
16	$-I_{\rm dc}$	$-I_{\rm dc}$	$2I_{\rm dc}$
17	$-2I_{\rm dc}$	0	$2I_{\rm dc}$
18	$-2I_{\rm dc}$	$I_{\rm dc}$	$I_{\rm dc}$
19	$-2I_{\rm dc}$	$2I_{\rm dc}$	0

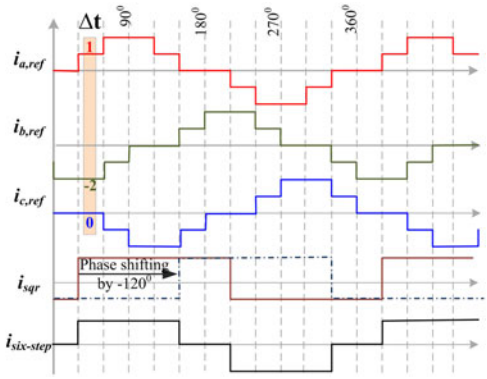

Fig. 11. Reference waveforms considered for analyzing conversion method.

zero. For example, the inverter needs to be modulated to produce three-phase 5L output current waveforms, $i_{a,\rm ref}$, $i_{b,\rm ref}$, and $i_{c,\rm ref}$, as shown in Fig. 11. The equation that governs the constraint is given by,

$$i_{a,\rm ref} + i_{b,\rm ref} + i_{c,\rm ref} = 0 \tag{3}$$

where, $i_{a,\rm ref}$, $i_{b,\rm ref}$, and $i_{c,\rm ref}$ are reference currents for three phases with 120° rotation. Consider a small time interval Δt as shown in Fig. 11, the sum of these three waveforms during this interval gives a nonzero value -1. Therefore, these references cannot be utilized for operating 5L CSI. Fourier-series analysis demonstrates that the sum of three waveforms with 120° phase shift will have only harmonic that are multiples of 3 $(3, 6, 9, 12, ..)$. Hence, in order to satisfy (3), the current reference should not contain harmonics order that are multiples of 3. Elimination of these harmonics on any quasi reference waveform can be achieved by delaying it to 120° and subtracting the delayed signal from actual waveform. For example, consider square wave $i_{\rm sqr}$ as reference, it is then phase shifted by 120° as shown in Fig. 11, and subtracted with actual waveform to obtain reference signal, $i_{\rm six-step}$. The resultant waveform is a 3L waveform without multiples of three harmonic content and it can be directly utilized as a reference signal for 3L CSI to produce maximum fundamental ($m = 1$). It could be observed that $i_{\rm six-step}$ is a 3L reference signal obtained from 2L square waveform. Similarly, if this conversion technique applied on 3L reference waveform the resultant waveform will be a 5L reference signal, and so on. Hence, for the topology under study that is 5L CSI, this conversion method requires a 3L optimal switching angles.

B. Multicarrier Sinusoidal PWM

Multicarrier sinusoidal PWM requires more than one carrier waveforms for comparing with the modulation signals to produce the multilevel waveforms. Multicarrier sinusoidal PWM techniques are of two basic types they are carrier level-shifted sinusoidal PWM (CLS-PWM and CPS-PWM. The CLS-PWM is further categorized into phase disposition (PD), phase opposition disposition (POD) and APOD methods. The more details about these methods can be seen in [70] and they have been successfully utilized for voltage-fed MLC topologies [71]. These modulation technique is generic in the sense it can be applied for all the CS MLC topologies discussed in Section II but it needs additional bi-logic to tri-logic conversion stage. However, in case of trapezoidal-based modulation which is explained in Section III-A3, the tri-logic conversion are not required as the comparison of carrier with trapezoidal directly produces gating pulses to operate current-fed MLCs [43]. From the literature, it has been found that current-fed MLCs are mostly modulated with a carrier-phase-shift modulation technique as in [26], [37], [57], [72]–[74]. To operate an L-level converter, it requires $(L-1)/2$ carrier waveforms. The carrier waveforms need to be phase shifted between each other by an angle of θ_d which is given by [37]

$$\theta_d = \frac{2\pi}{k_c * \frac{L-1}{2}} \tag{4}$$

where k_c is the ratio of carrier waveform frequency to modulation signal frequency. The harmonic frequencies of output current under this modulation technique are function of carrier frequency. Hence, the carrier frequency need to be higher for shifting the harmonics to higher frequency [74]. The PD technique has also been utilized to operate single-rated CS-MLC [75]. The advantage of using CPS-PWM is that it produce inherent current balancing between modules in case of single-rated MLC and multi-rating MLC [35].

C. Space Vector Modulation

Unlike carrier-based sinusoidal PWM technique for multilevel CSI, SVM modulation directly controls the output current and it does not require special conversion method as discussed in Section III-A2. The operation of SVM technique involves synthesizing a reference vector i^* from a sampling interval using inverter state vectors as shown in Fig. 9(b). Within one period of sampling time, the inverter is operated in the three set of state vectors. The time average value of these vectors operation ensures the magnitude and phase of reference vector has been

achieved by the current-fed MLC. The formula for computing the time interval (also called as dwell time) of state vectors are not unique for all sectors. This dwell time calculation and a detailed explanation on achieving space vectors for arbitrary reference can be referred in [76] for 5L and in [67] for 7L.

Considering 5L space vectors as shown in Fig. 9(b), there are 19 vectors which are classified as zero, small, medium, and large vectors based on their length. Zero, small, and medium vectors have redundant states whereas the large vectors have only one possible combination. These redundancies are utilized for multiple purposes such as balancing the module currents in case of single-rating inductor MLC [66], reducing low-frequency ripple in dc-link voltages in case of multi-rating inductor MLC [45], reduced switching transition and achieving zero average flux in case of interphase transformers-based MLC [33]. However, for operating single-rating inductor MLC topology zero and small vectors redundancies are not preferred because they increase switching frequency and energy loss [64]. Whereas for parallel H-bridge this limitation is not applied since it uses independent equal current sources. If the dc input currents are not equal, then the redundancies in the space vectors are lost which result in increase in the switching state vectors from 19 to 49 state vectors. Vekhande *et al.* has formulated the space vector diagram for two unequal input current conditions [45]. The first condition states that the smaller current among the two should atleast greater than half of the largest and in the second condition smallest current is lesser than half of the largest current. In [45], two strategies are developed for selection of redundant state vectors and the strategy that reduces the low-frequency ripple of dc-link voltage under unequal condition is analyzed.

To achieve better THD in the output current waveform, the space vector should rotate in perfect circular shape as shown in dotted-red line as in Fig. 9(a). For achieving the circular motion inverter needs higher switching frequency, however, lower order harmonics still exists with SVM in a small degree. A 12-sided polygon space vector representation has been used for current-fed MLC topology to eliminate lower order harmonics [77]. Multisided is possible by combining one or more MLCs. This 12-sided space representation has been first introduced in voltage-fed inverters for driving split-phase induction motor [78]–[80]. It can be extended to multisided polygon. The multisided space vector can be obtained by combining $(P/6)$ number of six-sided space vectors with phase shift of $(2\pi/P)$ radians and time shift of $(2\pi/P)$, where P is the number of polygonal sides of a space vector diagram. Also, it should be ensured that fundamental component of output current from each MLCs that are combined should be same. For example, to obtain 12-sided polygon space vector, 3L current-fed MLC and 5L current-fed MLC should be combined with input currents equal to I_{in} and $I_{\text{in}}/\sqrt{3}$, respectively [81]. Similarly, to achieve 18-sided polygon space vector, 3L current-fed MLC and two 7L current-fed MLCs should be connected in parallel with input current magnitude equal to I_{in}, $I_{\text{in}}/\sqrt{7}$, and $2I_{\text{in}}/\sqrt{7}$, respectively. The space vector diagram of 12-sided polygon and 18-sided polygon are shown in Fig. 12(a) and (b), respectively. The space vector diagram of 12-sided polygon is framed by combining the 3L space vector and 5L space vector as shown in Fig. 12(a). It could be

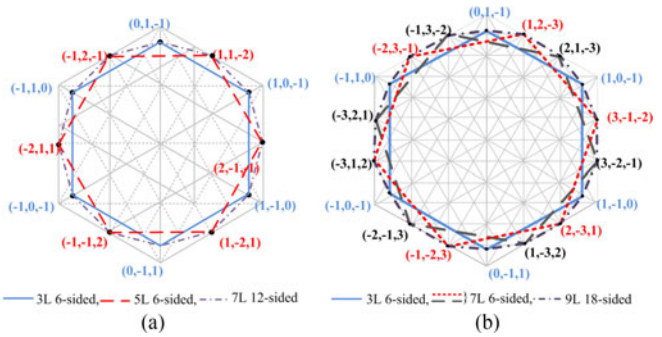

Fig. 12. Space vector diagrams for MLCs. (a) 12-sided polygon space phasor diagram. (b) 18-sided polygon space phasor diagram.

observed that 5L space vector polygon is rotated by 30°. Similar observations can be made for 18 sided polygon from Fig. 12(b).

D. Selective Harmonic Elimination

SHE modulation is one of the classical modulation technique developed to achieve low device switching frequency modulation in high power applications. SHE modulation is based on offline computation which has ability to eliminate low-order harmonics in the converter output currents. In general, SHE method involves utilizing a predefined current waveform with N switching angles $\alpha_1, \alpha_2, \ldots, \alpha_N$ for eliminating N-1 harmonics. For MLC operation, a multilevel SHE (MSHE) method has been invented. As per MSHE method, N_S number of switching angles are assigned per module of a L-level converter to eliminate $\frac{(L-1)}{2}(N_S - 1)$ harmonics. For example, in 5L single-rating MLC three switching angles are assigned for each module for eliminating (5–1) * (3–1)/2 = 4 harmonics (5th, 7th, 11th, 13th) using the MSHE modulation [41]. MSHE modulation technique has been demonstrated for 5L current-fed MLC with device switching frequency limited to four times that of fundamental frequency [82]. For a three-phase MLC, the logic circuits conversion method mentioned in Section III-A4 have been utilized in order to incorporate CSI operational constraint. However, that size of the logical circuits increases with the number of levels.

E. Hybrid Modulation

Hybrid modulation technique combines two or more modulation techniques to generate switching signals. For example, a hybrid modulation technique that combines SVM with PD CLS-PWM technique has been demonstrated for multi-rating inductor MLC topology is shown in Fig. 3. This hybrid modulation technique uses two stages of mapping in order to obtain the modulating signals. The voltage-fed switching states are identified from PD modulation and, then, it is mapped to equivalent current-fed multilevel space vectors [39]. The mapping stages of hybrid modulation has been shown in Fig. 13. For example, consider the switching signals S_a, S_b, and S_c within the dotted lines as shown in Fig. 13. These switching states are obtained by comparing three phase modulation signals S_{ma}, S_{mb}, and S_{mc} with the level shifted carrier waveforms. The switching

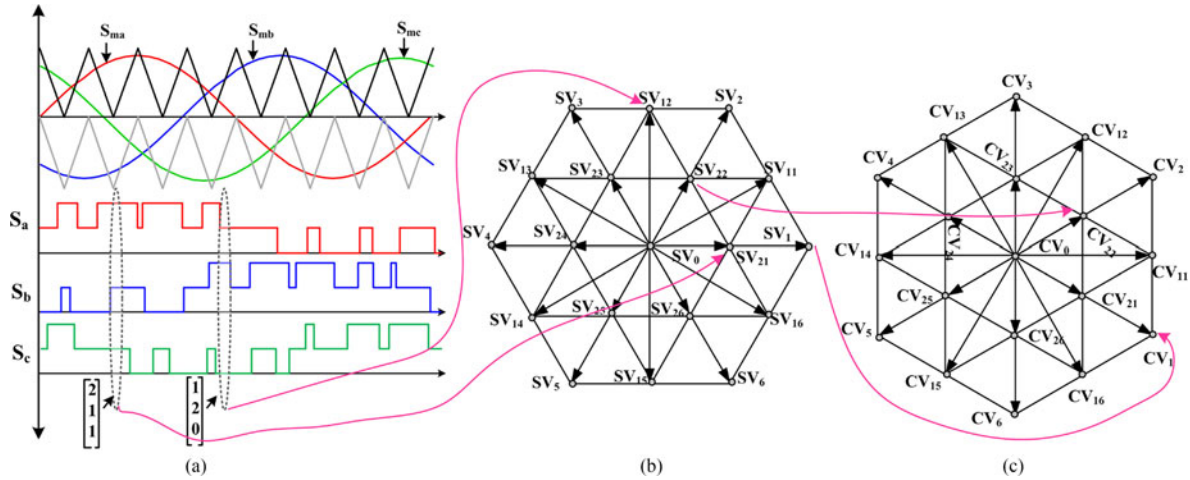

Fig. 13. Hybrid modulation POD and SVM pattern. (a) POD modulation and carrier comparison. (b) 3L voltage source space vector diagram. (c) 5L current source space vector diagram.

state combination of these signals within the dotted line is (2, 1, 1) which can be referred as space vector SV_{21} in voltage space vector. The equivalent current space vector to this voltage space vector is CV_{21} and this current source space vector is selected during the dotted-line time interval for the operation of the converter. With this technique, harmonic distortion of output has been reduced and also current balance between the modules has also been achieved [83].

F. Proposed Modified SOP

SOP technique is a combination of synchronous PWM and optimization. A generalized methodology has been developed for voltage-fed MLCs with any number of voltage levels [84]. Synchronous refers to the ratio of switching frequency f_s to operating frequency f_1 is an integer and by doing so the sub-harmonics can be eliminated [85]. The step by step procedure of classical SOP technique can be referred in [84]. In short, SOP technique determines number of switching angles for each steady-state operating point and, then, optimization is performed to obtain switching angles that minimize the harmonic distortion of output current. At the last step of SOP, the optimal switching angles are assigned to each semiconductor device to realize optimal current waveforms based on a systematic procedure. The classical SOP technique cannot be directly applied for CSI and it needs some modification to include the operational constraints mentioned in Section III-A. One possible option is, to modify the last step of SOP technique to convert optimal switching angles into constraint optimal switching angles using conversion method explained in Section III-A5.

Parallel H-bridge 5L CS MLC is considered for proposing SOP modulation technique. As per conversion method discussed III-A5, it requires 3L reference waveform for producing 5L constraint current waveform. Consider 3L reference current waveform i_{3L} shown in Fig. 14 with switching angles at α_1 to α_6 in a quarter period. In general half-wave and quarter-wave symmetries is introduced in the switching pattern to eliminate all even-order harmonics. Using the proposed conversion method,

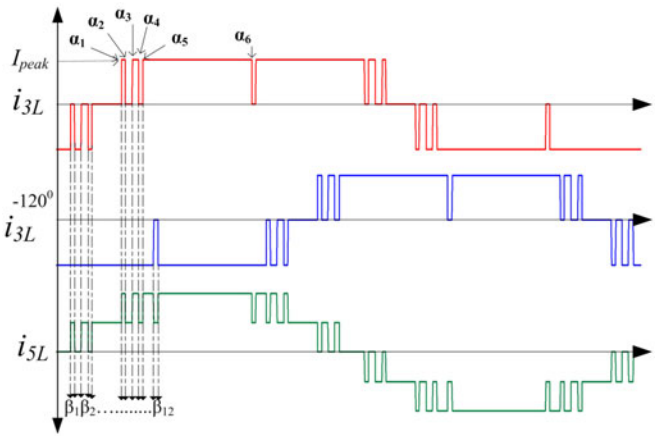

Fig. 14. 3L and 5L waveforms with optimal switching angles.

the resultant 5L reference is derived as shown in Fig. 14. As per the definition of the proposed conversion technique i_{3L} waveform which has unconstraint optimal angles (α_1 to α_6) is phase shifted by 120° to obtain $i_{3L}^{-120^\circ}$ as shown in Fig. 14, then these two waveforms are subtracted to obtain 5L waveform i_{5L} with optimal angles (β_1 to β_{12}) that satisfy operational constraints of 5L CSI. The resultant angles can be utilized for the operation of the 5L CSI.

1) Optimization of Switching Angles: The optimization of switching angles aims at minimizing the harmonic distortion of predetermined N number of switching angles for each steady-state operating point (m, N). For evaluating the switching patterns, distortion factor d is chosen as the objective function. Using Fourier analysis, the final expression for distortion factor of the 3L waveform can be obtained as [86]

$$d = \frac{i_{h,3L}}{i_{h,\text{sqr}}} = \frac{\sqrt{\sum_k \frac{1}{k^2}\left(\sum_{i=1}^{N_\alpha} s(i)\cos(k\alpha_i)\right)^2}}{\sqrt{\sum_k \frac{1}{k^2}}} \quad (5)$$

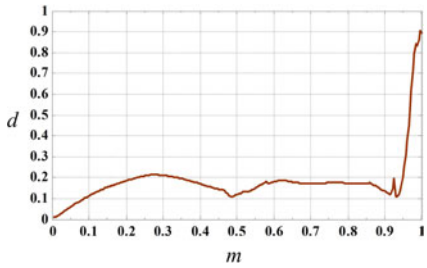

Fig. 15. 5L optimization results: modulation index versus distortion factor.

where k represents harmonic order, $i_{h,3L}$ represents the total harmonic content of 3L reference current i_{3L} at a given operating point, $i_{h,\text{sqr}}$ represents the total harmonic content of square waveform i_{sqr} in Fig. 11, and $s(i)$ represents the slopes of switching transients at switching angles α_i, $s(i)=(-1)^{i+1}$ for 3L waveform. Using the conversion method current i_{3L} can be converted in to i_{5L} as shown in Fig. 14 and the current i_{sqr} will become $i_{\text{six}-\text{step}}$ as shown in Fig. 11. From mathematical analysis, it can be obtained that the total harmonic distortion of i_{5L} and $i_{\text{six}-\text{step}}$ are calculated as $\sqrt{3}i_{h,3L}$, and $\sqrt{3}i_{h,\text{sqr}}$ respectively. The distortion faction d for the 5L waveform i_{5L} is given by

$$d = \frac{i_{h,5L}}{i_{h,\text{six-step}}} = \frac{i_{h,3L}}{i_{h,\text{sqr}}}. \tag{6}$$

Hence, the distortion factor is unchanged with the conversion method. To obtain the desired fundamental amplitude of inverter output current, the switching angles should satisfy the following equality constraint:

$$m = \frac{i_{1,3L}}{i_{1,\text{sqr}}} = \left(\sum_{i=1}^{N_\alpha} s(i)\cos(k\alpha_i)\right). \tag{7}$$

From (5), it should be noted that, d is dependent only on k, $s(i)$, and α_i. The goal of optimization is to determine optimal switching angles to minimize the value of d. The optimization algorithm is implemented in MATLAB using gradient method "FMINCON." The gradient method identifies the switching angles $\alpha_i (i = 1 \text{ to N})$ which minimize the objective function d. The distortion factors obtained using optimization have been plotted against each operating point $0 < m < 1$ in Fig. 15. It should be observed that distortion factor approached unity at $m = 1$. This is because inverter output will be similar to six-step waveform $i_{\text{six}-\text{step}}$ shown in Fig. 11.

2) Experimental Results: The proposed SOP technique has been verified on a low-power prototype on 5L current source MLC. The experimental results of the 5L inverter connected to RL load for different points are shown in Fig. 16. The waveforms of inverter output currents and their fast Fourier transform (FFT) spectrum are shown for different modulation indexes with device switching frequency of 350 Hz. It could be noticed from the FFT spectrum that the lower order harmonic components such as 7th, 13th and 17th of the inverter output current are infinitesimal compared to the amplitude of fundamental. It should also be noticed that the even-order harmonic and third-order harmonic components are eliminated. The THD of the filtered currents are obtained as 1.36%, 1.93%, and 2.79% for modulation indexes $m = 0.9294$, $m = 0.749$, and $m = 0.5216$, respectively, and these values are well below ($< 5\%$) the PV grid integration standards.

G. Comparison of Modulation Techniques

The comparison of the modulation techniques that are discussed so far is listed in Table III. It could be observed that multicarrier SPWM technique has been applied to all presented topologies especially in case of topologies that require natural current balancing. Since the carrier-based modulation utilizes dedicated carrier waveform for each modules, this technique can be easily applied for higher level (48L) converters [14]. On the other hand, SVM modulation technique is based on vector-based modulation which provides better dynamic performance among the presented techniques. It involves formulation of all switching combination for identifying the state vectors. In addition, SVM also provides high degree of freedom to directly choose vectors at any instant of time. This allows the usage of redundant switching states to achieve different objectives such as reducing switching transition, balancing of module currents in case of single-rating inductor and handling unequal input currents in case of paralleled-H bridge [33], [45]. The number of switching combination is very high for higher level converter topologies and, hence, the usage of SVM technique is limited only upto 7L operation [67]. High power conversion is one of the main advantage of MLC as it helps in reducing the current rating of the semiconductor devices. For high power conversion, low device switching frequency is preferred in order to reduce the switching losses and to minimize the cooling requirement of the converter. But low-frequency operation using multicarrier modulation or SVM modulation introduces the lower order frequency components in the output current which results in higher THD. This can be overcome by modulating the converter using SHE technique. It utilizes offline computation to obtain the switching angles that eliminate lower order harmonics in the current waveform [41]. However, in SHE-PWM, elimination of harmonics distributes the energy present in the eliminated harmonics to noneliminated harmonics and increases their magnitudes. Hence, SHE-PWM may not leads to the best performance [70].

The proposed modified SOP technique aims at overall reduction of THD and, hence, it provides better performance compared to SHE-PWM. SOP is also an offline computation technique that finds global optimal angles for achieving multilevel operation at the least possible THD. In addition to achieving reduced THD, SOP can also be formulated to find optimal angles that can shift the lower-order harmonic to higher order. The comparison of harmonic spectrum resulted from SOP and CPS-PWM as shown in Fig. 17 shows that the lower order harmonic are minimized and total harmonic content is reduced in SOP. By doing so the output capacitor size can be reduced. The modified SOP technique can be combined with a closed-loop controller such as stator flux trajectory tracking control or MPC technique to achieve better dynamic performance [87]. With the

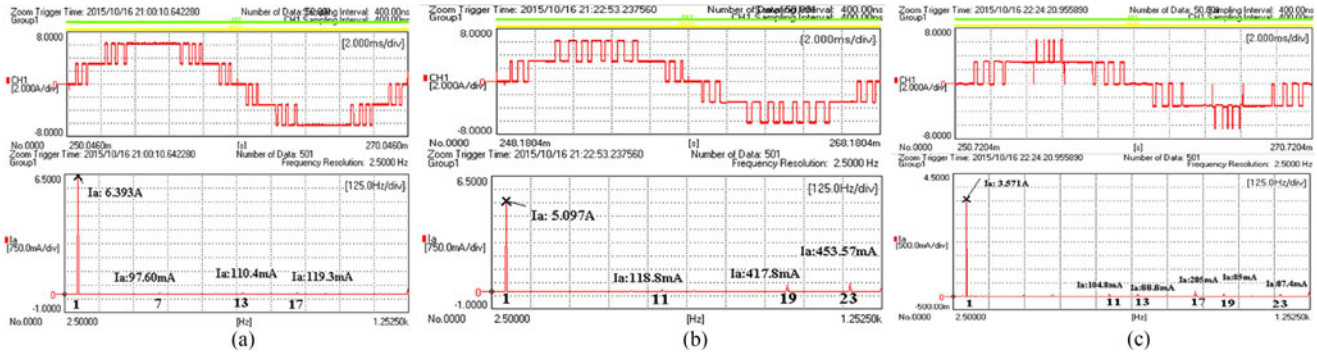

Fig. 16. Inverter output current of 5L CSI with SOP for modulation index (a) $m = 0.9294$, (b) $m = 0.749$, (c) $m = 0.5216$.

TABLE III
COMPARISON OF MODULATION TECHNIQUES FOR CURRENT-FED MLCS

Modulation Technique	Power Range	Frequency Range	Topology	Multi levels
Multi-carrier SPWM	10 kW to few MW	$high$	All[1] [2] [3] [4] [5] [6] [7]	$\geq 3L$
SVM	10 kW to few MW	$high$	Single-rating inductor[8], Paralleled H-bridge[9]	3L to 7L
SHE	10 kW to 10 MW	low	H-bridge paralleled[10], Two-stage[11]	$\geq 3L$
Hybrid	1kW to 10 kW	low / $high$	Multi-rating inductor[12]	$\geq 3L$
References	[1] [30], [2] [35], [7] [24],	[8] [29],	[3] [44], [4] [50], [9] [45], [10] [89],	[5] [48], [6] [57], [11] [10], [12] [39]

low: < 1 kHZ $high$: > 1 kHZ

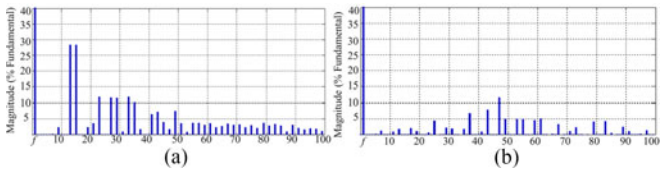

Fig. 17. Spectrum comparison of 5L CSI with (a) CPS-PWM (b) SOP.

stator flux control and SOP technique the converters will able to provide harmonic minimization even during transient periods [88]. Hence, the contributions of the proposed technique for the current-fed MLCs are that it 1) enables high power conversion due to low device frequency operation, 2) reduces the converter size by reducing both cooling requirement and output filter size, and 3) better quality of output waveforms without compromising on device switching frequency.

IV. APPLICATIONS

Current source multilevel would be a smart choice for application with low-voltage and high-current requirement like fuel cells and solar energy. The major advantages of current-fed MLC topologies such as inherent voltage boosting, continuous input current, and less distorted ac output currents, makes it a suitable converter for various applications such as solar power integration, HVDC transmission, fuel cell energy systems and superconducting magnetic energy storage (SMES). More details about these applications are given next.

A. Energy Generation

The growing energy demand across the globe paved way for search in renewable energy sources for electric power generation. Applications of MLC in the renewable energy generation and integration have been widely researched for the past few years [4]. Among the various renewable energy resources, hydrogen fuel cells found to be one of the more efficient solution to produce electricity and it provides energy continuously throughout the day. Traditionally fuel cell to grid interface is achieved using front end dc–dc boost converter with VSI which together can be replaced by single stage multilevel CSI. The CSI MLC can perform both maximum power point tracking as well as grid integration. In [90], the single-rating inductor MLC has been proposed as single-stage conversion of power from fuel-cell to grid for providing active power, compensating power factor, and greatly reducing the line current harmonic content to meet the grid standards.

Another easily available form of renewable resource is the solar energy and it has seen exponential growth recent years due to the reduction in cost of PV panels. Power generation from solar using large scale PV plants has reached up to 550 MW [91]. In general, large scale PV power plants utilize centralized configuration or multistring configuration for grid integration. Until now, the topologies of voltage-fed MLCs have been widely investigated for solar power integration [4]. However, current-fed MLC topologies would be more attractive for solar power integration due to their inherent boosting nature, direct output current control capability, longer lifetime of storage elements and also due to current source nature of PV panel output [16]. In [45], the topology of paralleled H-bridge MLC has been proposed using multi-string configuration and dc-dc module-integrated configuration with centralized inverter as shown in Fig. 18(a) and 18(b), respectively. In both schemes, the PV modules or the PV strings can be operated independently at their maximum power point. The current-fed MLC reduces system size as well as weight, as it requires smaller storage elements on dc side [60]. In addition, paralleled H-bridge MLC provides advantages such as high-quality output waveforms even with low switching frequency and inexpensive capacitor filters [46],

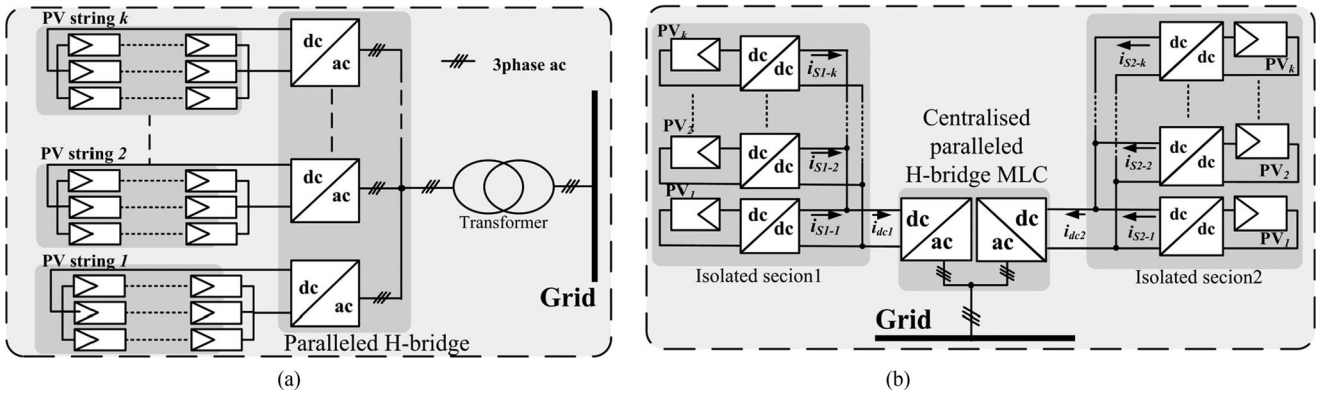

Fig. 18. Paralleled H-bridge MLC based PV grid integration configurations. (a) Multistring, (b) Module-integrated dc–dc converter with centralized inverter.

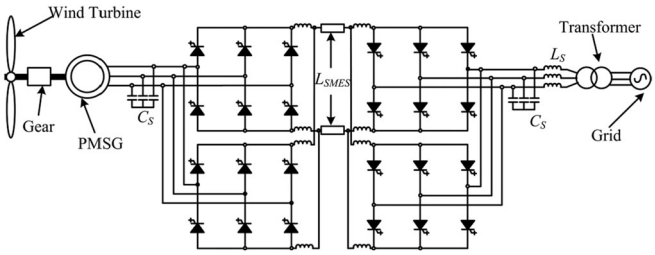

Fig. 19. Wind and SMES energy conversion system.

and continual power conversion even in case of failure of one of the inverter [67]. The emerging topology that is two stage MLC that provides better efficiency, reduced harmonic distortion, and natural short-circuit protection has been proposed by Barbosa *et al.* for residential PV to grid integration [92].

In the wind power generation, inclusion of SMES improves the generation by smoothening the irregular wind power, increases the transient stability of wind power system, enhances the wind power absorption and increases the system operating efficiency [93]. This hybrid energy conversion system provides low voltage ride through capability. However, SMES is high inductance and its current magnitude changes at some time. In such system, single-rating inductor MLC enables smooth and direct current control capability, hence, enables better overall energy conversion system as in [94]. The configuration of wind and SMES energy conversion system with back-to-back single-rating inductor MLC is shown in Fig. 19.

B. High-Voltage Direct Current

HVDC transmission system is proven to be highly efficient for transmitting very high powers over long distances compared to ac transmission systems. The major advantages of HVDC are higher controllability, less acoustic noise and less electromagnetic interference. For HVDC applications various voltage-fed MMC topologies has been researched by stating many advantages such as scalability to various power level, lower switching frequency operation, reduced harmonics, and reduced stress on each device. However, voltage-fed MMC requires additional protection method for tolerating external dc short-circuit fault. Whereas current-fed converters have inherent dc short-circuit tolerance and, hence, thyristor-based line commutated converters (LCC) are widely used for HVDC transmission. However, the limitation of LCC is large capacitor and filter banks and lack of restoring the system without relying on external energy sources. In [24], a current source MMC converter has been studied for STATCOM operation under different operating conditions such as capacitive mode, inductive mode, and also with dc short circuit fault. The dynamic response showed at each condition, current-fed MMC proves that it can tolerate dc short circuit fault. The design of sub-modules in MMC with the arm capacitors greatly reduces the filter size and, hence, the current source MMC is found to be better candidature for HVDC and FACTS applications. The research on HVDC tapping which benefits power supply to isolated rural and small urban communities located besides the HVDC lines. A shunt tapping method employing current source MLC has been described for tapping 110 kV ac from 500 kV dc as in [95]. In this innovative tapping method, the current source modules are connected in series and harmonic elimination achieved at 50 Hz using time shifting and zig–zag transformer. The current source MMC-based HVDC tapping reduces the filter cost and provides immunity from commutation failure.

C. AC Drives

For high-power drives, the current-source inverters technology is well suited and it is estimated that 700 units of large CSI-fed drives are produced worldwide per annum [96]. The requirements of medium voltage ac drives are four quadrant operation, low current ripple, low dv/dt, and fault tolerant capability [97]. Current-fed MLCs offer high dynamic performance for motor drives and are capable of handling high power in the range of MW. Attempts have been made by researchers to utilize current-fed MLC topologies for medium voltage ac drives [47], [98]. To increase the power ratings of CSI fed-drives single rating MLC has been suggested for power rating upto 10 MW [76]. The issue in multilevel CSI fed drives is that they have output capacitors which can resonates with inductor of ac drives. Hence, a proper controller design is required to operate the MLC for avoiding resonance [47]. Modern

electrical propulsion are aiming to produce energy efficient and environment friendly by using permanent magnet synchronous machines (PMSM) as motor-based drive system. The interphase reactor suggested in Section II-A provides multilevel operation using simple converter structure with reduced size. This converter has been proposed for operation of electrical propulsion system with 12-kW PMSM and it has produced efficiency of 94% for different speeds [98].

V. Trend and Future Scope of Research

The current-fed MLC was identified in the late 1970, however, LCI and PWM CSI converters have occupied various applications. MLCs have emerged as advanced power converters due to the advancement on semiconductor device for the past few decade. The topologies of current-fed MLCs are obtained from well-established voltage-fed MLCs by utilizing the duality principle. Since very few research works have been carried out in the current-fed multilevel technology, hence, there are various challenges for further development of this technology. This section discusses trend and future scope of research on current-fed MLCs.

Important aspect that has been considered by the researchers on developing the topologies is the size and weight reduction. Since the inductors occupy the major portion of the converter and this is why H-bridge with inductor cell topology has been introduced which aimed at reducing the number of inductors as shown in Table I. Introducing topologies that reduces inductor size and count will be trend that is expected to continue in the next years. Switching and conduction losses are another key aspect which contribute the converter efficiency. The silicon carbide (SiC) diodes can be utilized as series diodes with IGBT/MOSFET device [99] to reduce the loses and, hence, they have been used for single-rating inductor MLC as in [33]. The replacement of IGBT and series diode by RB-IGBT will also improve the converter efficiency and this will be the further development on multilevel current-fed converter technology. Another key aspect in attaining efficiency is the harmonic generated by the converter. The developed multilevel topologies achieves better THD than 2L topology, however, there is still room for further improvement. The multilevel topology can be made to achieve better THD by increasing the number of levels but it increases the device count, imbalance issue and complexity of the modulation. Also, based on the literature survey it has been found that most of these topologies are modulated with carrier-phase-shift modulation. Hence, there is a need for developing modulation technologies that focus on achieving better THD of the converter. Limited study or even very minor study on modulation techniques such as SHE is performed on current-fed MLCs. In addition, several emerging modulation techniques such as nearest level control and model predictive control have not been applied for current-fed MLC topologies [100]–[102]. Thus, there exist scope for further developing and enhancing these current-fed MLC topologies. Introduction of current source based MMC for STATCOM has enabled path for researchers for developing new topologies of MMC [24].

VI. Conclusion

The multilevel operation of CSCs provides advantages such as high current operation, reliability, ripple-free current, and high performance. This paper has provided review of various classical as well as emerging topologies of current-fed MLC topologies by highlighting merits and demerits of each topology. Modulation of current-fed MLC requires additional conversion stage compared to voltage-fed MLCs. This paper has covered most of the classical conversion technique for realizing operational constraints on CSI and how these methodologies are extended to current-fed MLCs. A generic conversion method has been proposed which can be utilized for any reference-based modulation techniques. In addition, the paper has also surveyed about existing modulation techniques for current-fed MLCs and proposed an emerging modulation technique named SOP for low-device switching frequency operation. Finally, several prospective applications for current-fed MLC topologies have been presented. Being an emerging topic for research, there exists huge scope of research to further develop new topologies and modulation techniques for these topologies.

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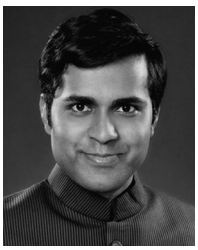

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