An Embedded Closed-Loop Fault-Tolerant Control Scheme for Nonredundant VSI-Fed Induction Motor Drives

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***Abstract*—The nonredundant voltage-source inverter, which exploits the possibility of minimum additional components for reconfiguration and operation, is a promising solution to manage faults in one inverter leg. However, control schemes at prefault and postfault conditions are always designed, separately making it hard for control scheme adaptation from normal to fault tolerant. In order to achieve smooth transitions from prefault to postfault, an embeddable fault-tolerant method based on predictive torque control (PTC) is proposed. A generalized voltage vectors, switching command, and cost function accounting for both healthy and faulty conditions are introduced to carry out a general control scheme. A novel fault-diagnosis method based on probability density analysis of the sampling currents is presented for open-circuit fault isolation under PTC scheme. Seamless likely and rapid transient processes from fault occurrence to postfault operation are achieved. Experimental results have demonstrated that the proposed scheme can make power switch fault easily managed by the controller itself.**

***Index Terms*—Fault diagnosis, fault tolerant, induction motor drive, probability.**

I. Introduction

THE induction motors are definitely one of the most used electric machines in the industrial world. However, in most industrial and manufacturing processes, electric drive systems are exposed to rigor operating conditions, which may lead to many faults essentially related to the induction motor and inverter. Recent survey shows that about 38% of the faults in variable-speed drive are due to the semiconductor power device failure [1]. The semiconductor power device is considered to be the most fragile component of electric drives.

Once a fault occurs in a single-semiconductor power device, the system operation must be halted. In critical applications where continuous operation is of essential importance, such as military, financial markets, and hospitals, halt of the system could lead to immeasurable economic losses.

Manuscript received December 9, 2015; revised April 1, 2016; accepted June 13, 2016. Date of publication June 21, 2016; date of current version February 2, 2017. This work was supported by the National Natural Science Foundation of China under Grant 61573159 and Grant 61273174. Recommended for publication by Associate Editor J. R. Espinoza.

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Digital Object Identifier 10.1109/TPEL.2016.2582834

Therefore, demand to prevent unscheduled shutdown is growing largely, which has promoted the development of real-time fault detection and fault-tolerant methodologies. As for fault-tolerant operation, numerous works have been developed and published in the past literature [2]–[17]. Based on whether redundant power switches are required, these methods can be classified into two categories: redundant and nonredundant fault-tolerant strategies. For the redundant solution, the main approaches are to add redundant switches or legs in parallel or series connection to main legs [5]–[10]. However, these solutions are always expensive and volume consuming. On the contrary, the nonredundant topologies exploiting the possibility of minimum additional components for reconfiguration and operation, either by capacitor midpoint connection [11]–[14] or by sharing converter leg [15]–[17], have attracted a lot of interests. However, smooth transitions from prefault to postfault operations are barely considered in these papers. This makes it hard for the control-software adaptation after fault [3]. Among the motor drive control strategies, predictive torque control (PTC), without modulator and axes transformation, is a promising alternative solution for fault-tolerant adaptation [18], [19].

In order to make a suitable reaction to a converter fault, the primary process is detection of the fault and its isolation. Many research works concerning the subject of open-circuit fault diagnosis in the motor drive systems are published in the literature [20]–[23]. However, PTC is a closed-loop control scheme without modulator and axes transformation. Therefore, current-based fault-diagnosis methods designed for open-loop control schemes such as scalar (v/f) control are not quite effective [24], together with ones which need axes transformation [22], [25]. Therefore, new fault-diagnosis method for PTC must be developed.

The semiconductor power device fault can be either open-circuit faults or short-circuit ones. In the case of short-circuit fault, the entire leg of the inverter is disconnected due to the intervention of fast fuses or another protection [3]. There will be no current flowing through the faulty leg. In this case, the fault-diagnosis and fault-tolerant operations are the same as that of the open-circuit fault. Therefore, only open-circuit fault is discussed in this paper.

In this paper, a novel fault-diagnosis scheme based on probability density analysis of the sampling currents is proposed for the PTC scheme. Variation and skewness of the sampled phase

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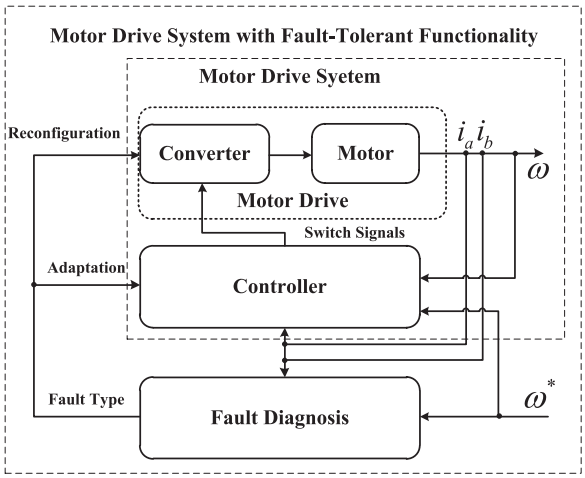

Fig. 1. Fault-tolerant motor drive systems.

currents in a period are utilized for fault isolation. A generalized voltage model for prefault and postfault is developed, and the flexible PTC employed makes it very easy for prefault and postfault software adaptation. The proposed fault-diagnosis and fault-tolerant scheme can be easily embedded within the normal control system and implemented by a single microprocessor. The transition from prefault to postfault operations with fault diagnosis is experimentally verified and discussed.

This paper is organized as follows. A novel open-phase fault-diagnosis method based on probability density analysis of the sampling currents is explained in Section II. In Section III, the model of nonredundant inverter and the induction motor is illustrated. The embedded fault-tolerant algorithm is discussed in Section IV. Section V shows the fully experimental results. And finally, conclusions are drawn in Section VI.

II. Fault-Diagnosis Algorithm Based on Probability Density Analysis

A. Motor Drives With Fault-Diagnosis Unit

The structure of motor drives combined with fault-diagnosis unit is depicted in Fig. 1. The three-phase currents and the measured speed of the induction motors are applied to the control unit to generate for "ON" and "OFF" states for the insulated-gate bipolar transistors (IGBTs). On the other hand, the inverter three-phase currents and the speed reference are fed to the fault-diagnosis unit to monitor the converter health condition. Fault diagnostic signal "fault type," which represents the fault isolation, is obtained by the proposed diagnostic method. Since the fault-diagnosis unit is independent to the control unit, it can be embedded into the control algorithm without major modification. The topology of the fault-tolerant inverter is shown in Fig. 2. The primary switches are IGBTs with antiparallel freewheeling diodes. Additional triacs are added for fault-tolerant operations.

B. Definition of Current Probability Density

In discrete motor drive control system with a sampling period of T_s, the three phase currents fedback to the controller are sets

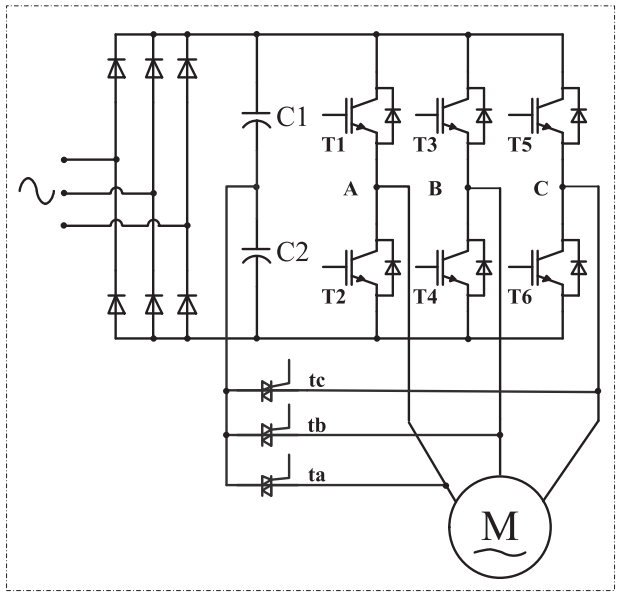

Fig. 2. Nonredundant fault-tolerant inverter topology.

of discrete values. These signals have similar electrical characteristics in a current period due to the symmetrical topology. Each current signal is similar to each other with a 120° phase difference. Therefore, the three-phase current has a same statistical characteristics in a current period. The current probability density is defined here as the probability of sampled current point falling within a particular range of values in a current period.

Based on the probability density analysis, how far a set of currents is spread out can be characterized by the variance. Mathematically, variance can be expressed as

$$\mathrm{Var}_x = \sigma^2 = E(X^2) - \mu^2, x \in \{a, b, c\} \tag{1}$$

where X is the sampled current, μ is the mean of X, $E(X^2)$ is the mean of X^2, and σ is the standard deviation.

The asymmetry of probability distribution of a real-valued variable can be characterized as skewness. For example, data samples with negative skewness tend to have the mass of the distribution concentrated on the right, whereas datasets with positive skewness tend to have the mass of the distribution concentrated on the left.

The skewness can be expressed as

$$\gamma_x = E\left[\left(\frac{X-\mu}{\sigma}\right)^3\right], \quad x \in \{a, b, c\}. \tag{2}$$

In order to reduce the computation burden for implementation, (2) can be simplified as

$$\gamma_x = \frac{E(X^3) - 3\mu\sigma^2 - \mu^3}{\sigma^3}. \tag{3}$$

These characteristics can be used to locate the fault since the variance and skewness of the current are very different in healthy and faulty conditions. Sliding window with a length of one current period is designed for online fault isolation because current samples during a period contain the health condition of the inverter. The window length can also be selected as times of a current period. However, this will increase the computational

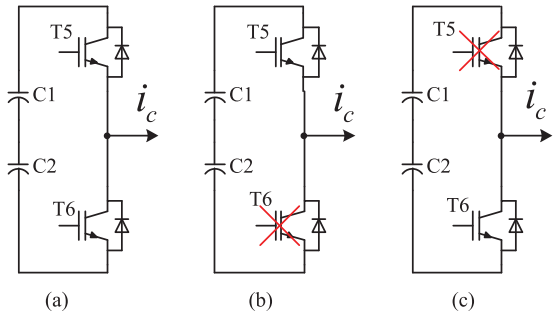

Fig. 3. Basic configuration of leg "c." (a) Normal conditions. (b) T6 fails. (c) T5 fails.

burden and the time for fault diagnose. Therefore, the window length is selected as one current period.

The windows length L can be expressed as

$$L = \frac{60}{9.55pT_s\omega^*} \tag{4}$$

where p is the number of pole pairs, ω^* is the speed reference (rad/s), and T_s is the sampling period.

C. Probability Density Analysis in Healthy and Faulty Conditions

The topology of three-phase voltage-source inverter is shown in Fig. 2. It is composed of six transistors. Each of them is antiparallelled with a diode. Var_x is chosen to monitor the inverter health condition.

It is obvious that the inverter output currents are periodic under healthy and faulty conditions in open-loop or closed-loop systems. In healthy conditions, the three-phase current has almost a same distribution, whereas in faulty conditions, the faulty phase current has a more centralized distribution.

Taking phase "c" as example, there are three conditions for leg "c." When the leg is under healthy condition as shown in Fig. 3(a), the output current is positive as the upper transistor is ON, whereas the output current is negative as the lower one is ON. When T6 fails as shown in Fig. 3(b), the output current is positive as the upper transistor is ON, whereas the output current is closed to zero as the lower transistor is ON. When T5 fails as shown in Fig. 3(c), the output current is closed to zero as the upper transistor is ON, whereas the output current is negative as the lower one is ON.

It is obvious that the three-phase current has almost a homogeneous distribution from $-I_{\max}$ to $I_{\max}$ in healthy condition. While in faulty condition, the faulty leg current has a centralized distribution with mass of current sampling point falls around zero. For example, output current of the faulty leg has a centralized distribution from 0 to $I_{\max}$ if T6 fails in comparison with that of other legs. Output current of the faulty leg has a more centralized distribution around 0 if both T5 and T6 fail in comparison with that of other legs.

D. Fault Isolation

Therefore, the faulty leg current has a smaller variance in comparison with the other two phase currents. Since the variance is related to the load, then the relative variance is utilized for fault isolation. It can be defined as

$$\varepsilon_x = \frac{\text{Var}_x}{\max\{\text{Var}_a, \text{Var}_b, \text{Var}_c\}}, \quad x \in \{a, b, c\} \tag{5}$$

where $\max\{\text{Var}_a, \text{Var}_b, \text{Var}_c\}$ denotes the maximum value among three-phase current variance.

The fault isolation at legs can be denoted as

$$f_l = \begin{cases} 0, & \text{if } \varepsilon_x \approx \varepsilon_y \approx \varepsilon_z \approx 1 \\ 1, & \text{if } \begin{cases} \text{th}_{f1} < \varepsilon_x < \text{th}_{f2} \\ \varepsilon_y > \text{th}_{f2}, \varepsilon_z > \text{th}_{f2}; \end{cases} \\ 2, & \text{if } \begin{cases} \varepsilon_x < \text{th}_{f1} \\ \varepsilon_y > \text{th}_{f2}, \varepsilon_z > \text{th}_{f2}; \end{cases} \end{cases} \tag{6}$$

where $x, y, z \in \{a, b, c\}$ and $x \neq y \neq z$, and th_f is the threshold level for fault isolation. $f_l = 0$ denotes the converter is in healthy condition, $f_l = 1$ denotes one-switch fault in a leg, and $f_l = 2$ denotes two-switch fault in a leg.

If the lower transistor fails, faulty leg current has a centralized distribution from 0 to $I_{\max}$ with mass of current sampling point falls around zero. The mass of the distribution is concentrated on the left. Whereas if the upper transistor fails, faulty leg current has a centralized distribution from $-I_{\max}$ to 0 with mass of current sampling point falls around zero. The mass of the distribution is concentrated on the right.

The faulty transistor

$$f_s = \begin{cases} 1, & \text{if } \gamma_x < 0 \\ 0, & \text{if } \gamma_x > 0 \end{cases} \tag{7}$$

$f_s = 1$ denotes the upper switch faults and $f_s = 0$ denotes the lower switch faults.

The final fault diagnostic table based on the probability density analysis is showed in Table I.

III. Model of the Nonredundant Inverter and IM

In this section, a generalized voltage vectors and the switching combinations accounting for both healthy and faulty conditions are introduced.

A. Voltage Vector

A general model for leg voltages for both healthy and faulty conditions is given as

$$\begin{cases} \text{for : healthy case} \rightarrow v_{xo} = s_x \cdot v_{c1} + (s_x - 1) \cdot v_{c2} \\ \text{for : faulty case} \rightarrow v_{xo} = 0 \end{cases} \tag{8}$$

where v_{c1} and v_{c2} are the upper and lower capacitor voltage, $x \in \{a, b, c\}$.

Applying Kirchhoff voltage law, the sum of phase voltage is zero, given as $v_{\text{an}} + v_{\text{bn}} + v_{cn} = 0$. Therefore, the phase voltage of the induction motor drive for both healthy and faulty

TABLE I
FAULT DIAGNOSTIC TABLE

State	Variation	Skewness	Faulty switch	Fault type
Healthy	$\varepsilon_a \approx \varepsilon_b \approx \varepsilon_c \approx 1$		No	0
Faulty	$\text{th}_{f1} < \varepsilon_a < \text{th}_{f2}, \varepsilon_b > \text{th}_{f2}, \varepsilon_c > \text{th}_{f2}$	$\gamma_a < 0$	T1	1
		$\gamma_a > 0$	T2	2
	$\varepsilon_a < \text{th}_{f1}, \varepsilon_b > \text{th}_{f2}, \varepsilon_c > \text{th}_{f2}$		T1T2	3
	$\text{th}_{f1} < \varepsilon_b < \text{th}_{f2}, \varepsilon_a > \text{th}_{f2}, \varepsilon_c > \text{th}_{f2}$	$\gamma_b < 0$	T3	4
		$\gamma_b > 0$	T4	5
	$\varepsilon_b < \text{th}_{f1}, \varepsilon_b > \text{th}_{f2}, \varepsilon_c > \text{th}_{f2}$		T3T4	6
	$\text{th}_{f1} < \varepsilon_c < \text{th}_{f2}, \varepsilon_a > \text{th}_{f2}, \varepsilon_c > \text{th}_{f2}$	$\gamma_c < 0$	T5	7
		$\gamma_c > 0$	T6	8
	$\varepsilon_c < \text{th}_{f1}, \varepsilon_a > \text{th}_{f2}, \varepsilon_b > \text{th}_{f2}$		T5T6	9

mode can be given as

$$\begin{aligned} v_{\text{an}} &= (2v_{\text{ao}} - v_{bo} - v_{co})/3 \\ v_{\text{bn}} &= (2v_{\text{bo}} - v_{\text{ao}} - v_{\text{co}})/3 \\ v_{\text{cn}} &= (2v_{\text{co}} - v_{\text{ao}} - v_{\text{bo}})/3. \end{aligned} \tag{9}$$

The voltage vector of the induction motor drive for both healthy and faulty modes can be obtained by the Clarke transform

$$v_s = v_{\text{an}} + j \cdot (v_{\text{an}} + 2v_{\text{bn}}) \cdot \sqrt{3}/3. \tag{10}$$

B. Switching Combinations

For convenient analysis, the switch does not include switch nonideal behavior, so the healthy leg switching states can be denoted as binary states variables S_1, S_2, and S_3. Binary "1" indicates the "ON" state of the upper switch and "OFF" state of the lower switch while binary "0" indicates the "ON" state of the lower switch and "OFF" state of the upper switch. In faulty mode, two switches are usually forbidden simultaneously to isolate the faulty leg, denoted as S_z.

After fault, the number of switching combinations is reduced from eight to four. For the inverter in healthy and faulty mode, the switching commands are given as

$$\begin{cases} \text{for : healthy case} \rightarrow \text{S} = \begin{bmatrix} S_1 & S_2 & S_3 \end{bmatrix}^{\text{T}} \\ \text{for: leg} - \text{a fault} \rightarrow \text{S} = \begin{bmatrix} S_z & S_1 & S_2 \end{bmatrix}^{\text{T}} \\ \text{for: leg} - \text{b fault} \rightarrow \text{S} = \begin{bmatrix} S_1 & S_z & S_2 \end{bmatrix}^{\text{T}} \\ \text{for: leg} - \text{c fault} \rightarrow \text{S} = \begin{bmatrix} S_1 & S_2 & S_z \end{bmatrix}^{\text{T}}. \end{cases} \tag{11}$$

C. Induction Motor Model

The state equations of an induction machine in stationary frame can be expressed as [26]

$$\dot{x} = Ax + Bv_s \tag{12}$$

where $x = \begin{bmatrix} i_s & \psi_s \end{bmatrix}^{\text{T}}$, $B = \begin{bmatrix} \lambda L_r & 0 \end{bmatrix}^{\text{T}}$,

$$A = \begin{bmatrix} -\lambda(R_s L_r + R_r L_s) + j\omega_r & \lambda(R_r - j\omega_r L_r) \\ -R_s & 0 \end{bmatrix}$$

and L_s, L_r, L_m, R_s, and R_r are the stator inductance, rotor inductance, mutual inductance, stator resistance, and rotor resistance, respectively. i_s, ψ_s, v_s, and ω are stator current, stator flux, stator voltage, and rotor speed, respectively. $\lambda = 1\,(L_s L_r - L_m^2)$.

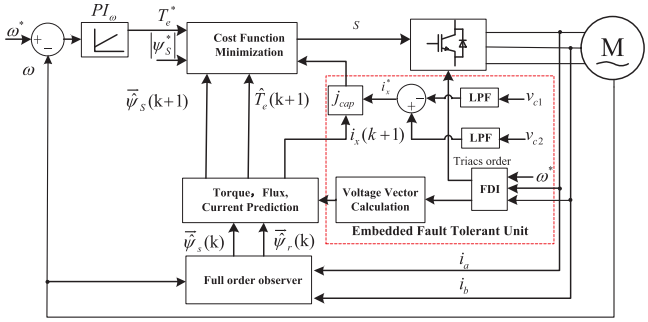

Fig. 4. Control diagram of the embedded fault-tolerant motor drive.

In digital implementation of the model-predictive control, (12) must be discreted to predict torque and stator flux for a single voltage vector. First-order Euler method is a simple way to discrete the (12). The discrete induction machine equation employed in this paper can be expressed as

$$x(k+1) = (1 + AT_s)x(k) + Bv_s. \tag{13}$$

The control variables stator flux magnitude and torque can be expressed using vector dot and cross products

$$\begin{aligned} |\psi_s(k+1)| &= \sqrt{\psi_s(k+1) \cdot \psi_s(k+1)} \\ T_e(k+1) &= (3\,2)p\psi_s(k+1) \times i_s(k+1). \end{aligned} \tag{14}$$

IV. EMBEDDED FAULT-TOLERANT ALGORITHM

The control diagram of the embedded fault-tolerant algorithm is shown in Fig. 4, which is mainly composed of the following parts: fault diagnosis, voltage vector calculation, stator flux estimation, flux and torque prediction, triacs order generation, capacitor voltage deviation suppression, and cost function minimization. The torque reference is obtained by an outer-loop proportional-integral (PI) controller. The embedded fault-tolerant unit is shown at the dashed box in Fig. 4, which is composed of the following three parts: fault diagnosis, voltage vector calculation, and capacitor voltage deviation suppression. It can be easily embedded into the control scheme. The detailed introduction of each part will be elaborated in the following text.

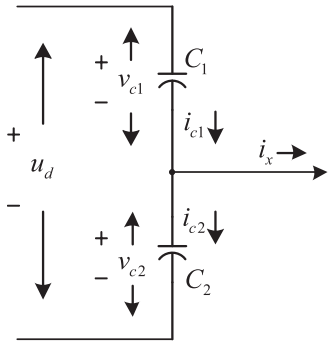

Fig. 5. Capacitor current path.

A. Full-Order Observer

In order to get higher accuracy information of the stator flux, a closed-loop full order observer is employed in this paper. It has some robustness against machine parameter variations. The full-order observer can be expressed mathematically as [27]

$$\dot{\hat{x}} = A\hat{x} + Bv_s + G(i_s - \hat{i}_s) \tag{15}$$

where $\hat{x} = \left[\hat{i}_s \ \hat{\psi}_s\right]^{\mathrm{T}}$ are observer state variables denoting the estimated stator current and estimated stator flux, respectively.

The observer gain $G = [2g \ g \ \lambda L_r]^{\mathrm{T}}$ is employed in this paper to improve the stability of observer, where g is a negative gain. More details concerning this observer can be found in [27].

B. Suppression of Capacitor Voltage Deviation

After fault, the motor phase with faulty switch is connected to the capacitor midpoint as shown in Fig. 2. The phase current flowing through the capacitor keeps charging and discharging the upper and lower capacitor. The capacitor voltages inevitably fluctuate and it will deviate to the opposite direction if the imbalance current flows during speed variation or load disturbance. Suppressing deviation of capacitor voltages can improve the dc voltage utilization after fault [11]. Although capacitor voltage deviation was achieved in [11], implementation of the algorithm is relatively complicated. It requires two healthy leg currents making it hard to be embedded into the normal control algorithm. Therefore, a compact method is proposed to improve the control performance of the motor drive at fault mode.

The current path of the two capacitor is shown in Fig. 5. Applying Kirchhoff's current law, the capacitor currents are shown as

$$i_{c1} - i_{c2} = C_1\frac{dv_{c1}}{dt} - C_2\frac{dv_{c2}}{dt} = i_x \tag{16}$$

where i_{c1} and i_{c2} are the upper and lower capacitor current, and $C_1 = C_2 = C$ are the upper and lower capacitance value, respectively. i_x is the phase current corresponding to faulty leg.

Therefore, the dynamic equation for capacitor voltage deviation can be expressed as

$$C\frac{d(v_{c1} - v_{c2})}{dt} = i_x. \tag{17}$$

After the transient state, dc current $\bar{i}_x$ can be introduced into the i_x. Then, the analytical solution of (17) is

$$v_{c1}(t) - v_{c2}(t) = \frac{1}{C}\int (i_x + \bar{i}_x)dt + v_{c1}(0) - v_{c2}(0). \tag{18}$$

When $\bar{i}_x$ is positive, the upper capacitor is in charge mode, its voltage deviates to a higher value. When the lower capacitor is in the discharge mode, its voltage deviates to a lower value and *vice versa*. It reveals that the capacitor voltage deviation can be eliminated by injecting a proper dc component into current i_x.

The transfer function of capacitor voltage suppression can be given as

$$G_c = \frac{v_{c1} - v_{c2}}{\bar{i}_x} = \frac{1}{Cs}. \tag{19}$$

The capacitor voltages v_{c1} and v_{c2} are measured in real time and the difference of the capacitor voltage is extracted from the low-pass filter (LPF). Therefore, the cost function component of capacitor voltage deviation can be expressed as

$$j_{\mathrm{cap}} = \frac{\left(i^*_{\mathrm{cap}} - i_p(k+1)\right)^2}{I^2_{\mathrm{nom}}} \tag{20}$$

where $i^*_{\mathrm{cap}} = k_p(\bar{v}_{c2} - \bar{v}_{c1})$, $\bar{v}_{c1}$ and $\bar{v}_{c2}$ are the filtered upper and lower capacitor voltage, and k_p is a constant coefficient with a value of 1. I_{nom} is the maximum allowed phase current.

The general model for capacitor voltage deviation suppression by applying different predictive current is given as

$$\begin{cases} \text{for : healthy case} \rightarrow i_p(k+1) = i^*_{\mathrm{cap}} \\ \text{for : faulty case} \rightarrow i_p(k+1) = i_x(k+1), \end{cases} x \in \{a, b, c\}. \tag{21}$$

C. Cost Function Design

In healthy mode, the cost function showed in Fig. 4 is usually used as the criterion to select the best voltage vector [28]

$$j_m = \frac{1}{T^2_{e,\mathrm{nom}}}\left(T^*_e - \hat{T}_e(k+1)\right)^2 + \frac{\lambda_f}{\psi^2_{s,\mathrm{nom}}}\left(\psi^*_s - |\hat{\psi}_s(k+1)|\right)^2 \tag{22}$$

where λ_f stands for a flux weighting factor and subscript nom represents for the nominal (rated) value. The λ_f is primarily set to 1 and adjusts experimentally. $\hat{T}_e(k+1)$ and $\hat{\psi}_s(k+1)$ are the predicted torque and stator flux at time instant $k+1$, respectively.

In faulty mode, the voltage deviation suppression component should be added to the cost function. Then, the general cost function for prefault and postfault is given as

$$J = j_m + \lambda_{\mathrm{cap}} j_{\mathrm{cap}} \tag{23}$$

where λ_{cap} denotes weighting factor of the capacitor voltage deviation term. The λ_{cap} is primarily set to 1 and also adjusts experimentally.

As it can be seen in (14) and (20), torque, stator flux, and capacitor current predictions can be written in terms of the inverter voltage $v_s(k)$. This implies that seven different sets of predictions are obtained for the normal operation and four different sets of predictions are obtained for the fault-tolerant operation.

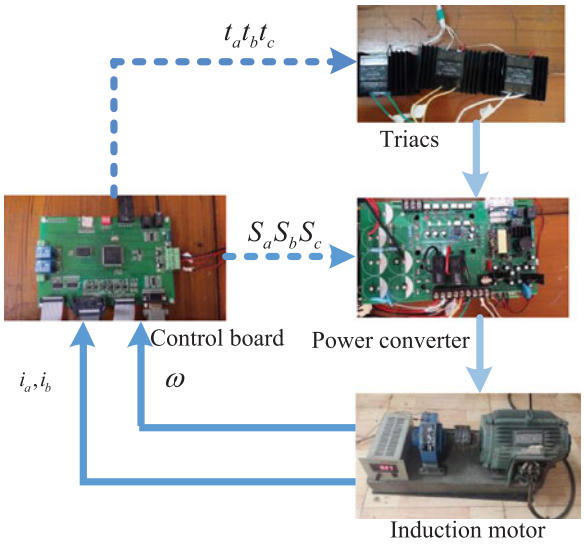

Fig. 6. Experimental setup.

TABLE II
PARAMETERS

Parameter	Value	Parameter	Value
R_s	2.804 Ω	P_{nom}	2.2 kW
R_r	2.178 Ω	ω_{nom}	1430 r/min
L_s	330.03 mH	i_{nom}	4.9 A
L_r	330.03 mH	T_{eN}	14 N·m
L_m	319.7 mH	ψ_{sN}	0.6 Wb
p	2	u_d	540 V

Switching state selection is made by means of a cost function which corresponds to a comparison between references to their predicted values. The cost function is evaluated for every prediction and the voltage vector that produces the lowest cost function value is selected. The optimization times are eight in normal mode, while they are four in fault-tolerant mode. The cost function is valid for all operating conditions with the modification made by (21).

D. Emembedded Fault-Tolerant Unit

In order to make the software adaptation simple and compact for the fault-tolerant operation, the fault-tolerant unit is designed relatively independent to the control scheme, as shown in Fig. 4. During healthy and faulty mode operation, (8) and (11) are adopted for voltage calculation and switching pattern selection. Equation (23) is adopted for cost function optimization. The control schemes at prefault and postfault conditions are merged into one scheme.

The triacs order produced by fault-diagnosis unit is utilized to reconfigure the topology. For example, if leg-C fails, t_c is fired to connect the faulty phase to the capacitor midpoint. The subscript x denotes the faulty leg. It is determined by the fault diagnose unit. Applying the proposed software adaptation and hardware reconfiguration method, the proposed scheme can make the power switch fault easily managed by the controller itself.

V. Experimental Results

Although the fault-diagnosis and embedded fault-tolerant algorithm have been first verified using numerical simulations, all the following analyses are based entirely on the experimental results, since a better representation of the control performance is given in the presence of model uncertainty, measurement noise, inverter dead time, etc.

A test bench composed of a 32-bit floating DSP TMS320F28335 controller and an IPM (PM25RSB120) converter has been set up to verify the effectiveness of the proposed fault-diagnosis and embedded fault-tolerant control strategy. The fault-tolerant converter is consisted of an IPM converter and additional Triacs, as shown in Fig. 6. Open-circuit fault emulation has been realized by permanently inhibiting the gating signal of the corresponding transistor. The triacs is utilized to reconnect the faulted phase to the dc-link midpoint. An induction motor parameters are given in Table II and a magnetic powder brake has been utilized as a load. Sampling frequency is set to 25 kHz and the converter dead time is 3.6 μs. Computation delay compensation [29] usually utilized in PTC is also applied in the experimental implementation. The proposed scheme is validated to be effective at a large amount of operating point; only selective results are presented in the paper.

th_{f2} is a threshold that is used to detect single-switch fault. Single transistor open-circuit fault will cause no more than two times relative variance between the remaining healthy legs current and more than two times relative variance between the fault leg current and the healthy ones. Therefore, th_{f2} should be set to around 0.5. Lower value of th_{f2} will decrease the false alarm caused by diode stream and transient disturbance. However, it will increase the detection time.

th_{f1} is a threshold that is used to detect entire-leg fault. Its value should be lower than 0.1 for double-transistor open-circuit fault in the same leg will cause more centralized distribution around 0. The variance of the faulty leg current is very small in comparison with the healthy one. Therefore, th_{f1} should be set to around 0.1. Similarly, lower value of th_{f1} will decrease the false alarm caused by diode stream and transient disturbance. However, it will increase the detection time.

The threshold th_{f1} and th_{f2} is set to 0.1 and 0.5 in this paper, respectively. The weighting factors are tuning experimentally, λ_f is set to 8, and λ_{cap} is set to 0.012.

A. Fault Detection Results

Experimental results of a single fault (T6 fails) without fault-tolerant operation are shown in Figs. 7 and 8. Fig. 7 shows the performance of speed, torque, stator flux, and three-phase current during healthy and faulty condition. The significant deterioration in performance is shown in faulty conditions. Fig. 8 shows the proposed fault-diagnosis method; when a fault occurs, three variations of the phase currents are not approximately equal again. Their values deviate from one. The relative variation of the faulty phase current ε_c drops to a lower value of about 0.2, which is higher than th_{f1} and lower than th_{f2}. Relative variations of other phase currents ε_a and ε_b are higher than th_{f2}. Then, a fault is detected. According to the skewness of the

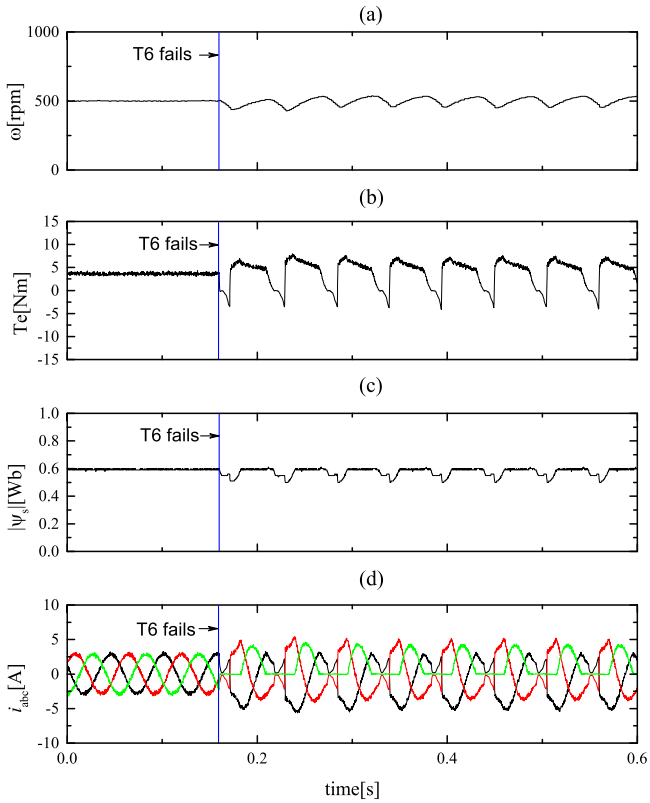

Fig. 7. Control performance when T6 fails with 30% rated load torque at 500 r/min without fault-tolerant operation. (a) Speed. (b) Estimated torque. (c) Stator flux. (d) Stator current.

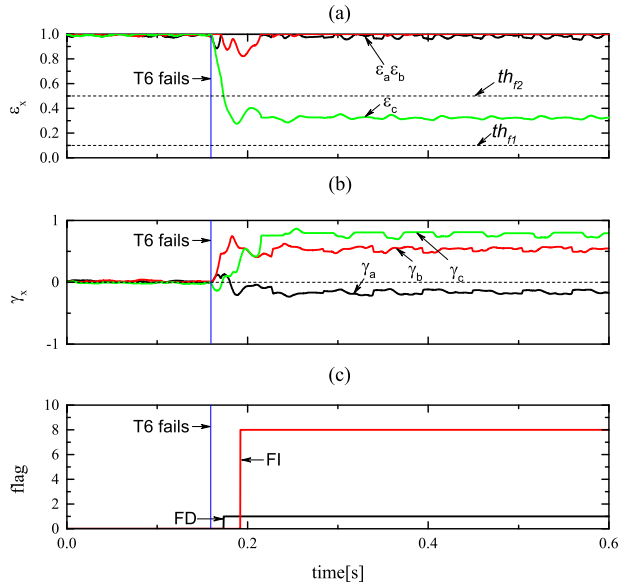

Fig. 8. Fault diagnostic process when T6 fails with 30% rated load torque at 500 r/min without fault-tolerant operation. (a) Variation (b) Skewness. (c) Fault detection and fault isolation flag.

faulty phase currents $\gamma_c > 0$, the faulty switch or switches can be isolated by looking up Table I.

Experimental results of multiple fault in the same leg (T5T6) without fault-tolerant operation are shown in Figs. 9 and 10. Fig. 9 shows the performance of speed, torque, stator flux, and three-phase current during healthy and faulty condition. The significant deterioration in performance is shown in two-switch faulty conditions. Fig. 10 shows the proposed fault-diagnosis method; when the fault occurred, three variations of the phase currents were not approximately equal again. Their values deviated from one and relative variation of the faulty phase current ε_c drops to a value of about 0, which is lower than th_{f1}. Then, a fault is detected. The faulty switch or switches can be isolated by looking up Table I. Other faults cases can be detected and isolated in the same way.

In order to clarify the concept of the proposed fault diagnose algorithm, the probability density of the phase current in one current cycle is shown in Fig. 11. Three different cases are discussed separately.

1) Three legs of the inverter operate normally: The current flowing across each phase can circulate during the whole wave and the three-phase current has almost a homogeneous distribution as shown in Fig. 11(a).
2) An open-circuit fault only in one switch: The current flowing across the faulty phase can circulate only during half wave. The faulty phase current has a centralized distribution as shown in Fig. 11(b). It is also shown that the faulty switch is the upper one. The mass of current sampling point falls around zero and the mass of the distribution is concentrated on the right. Remaining healthy leg currents have almost a same homogeneous distribution.
3) In the case of short-circuit fault, the entire leg of the inverter is disconnected due to the intervention of fast fuses or another protection. The leg with faulty switches is cut off from the converter. The motor becomes single phase operating and the current flowing across the faulty phase is zero. In the case of open-circuit fault, the current corresponding to the faulty leg is supposed to be highly pulsating due to the conducting of the healthy legs and the freewheeling diodes. However, this highly pulsating current is attenuated by the large inductance of the motor. Actually, current flowing through the freewheeling diodes is almost zero in open-circuit fault condition. In these cases, the faulty phase current has a more centralized distribution as shown in Fig. 11(c). Remaining healthy leg currents have almost a same homogeneousbr distribution.

B. Fault-Tolerant Results

To continue the operation of the faulted inverter, the hardware reconfiguration and software adaptation are conducted after the fault isolation. The control performance of the transient during the transition from normal operation to single- and two-switch fault mode operations is shown in Figs. 12 and 13, respectively. In single-switch fault case, the transient from prefault to postfault takes about 40ms during the operation, while in the two-switch fault case, the transient takes about 30 ms during the operation. Although the speed must be derated due to the halved voltage utilization factor after hardware reconfiguration, the fault-tolerant algorithm can achieve almost the same torque,

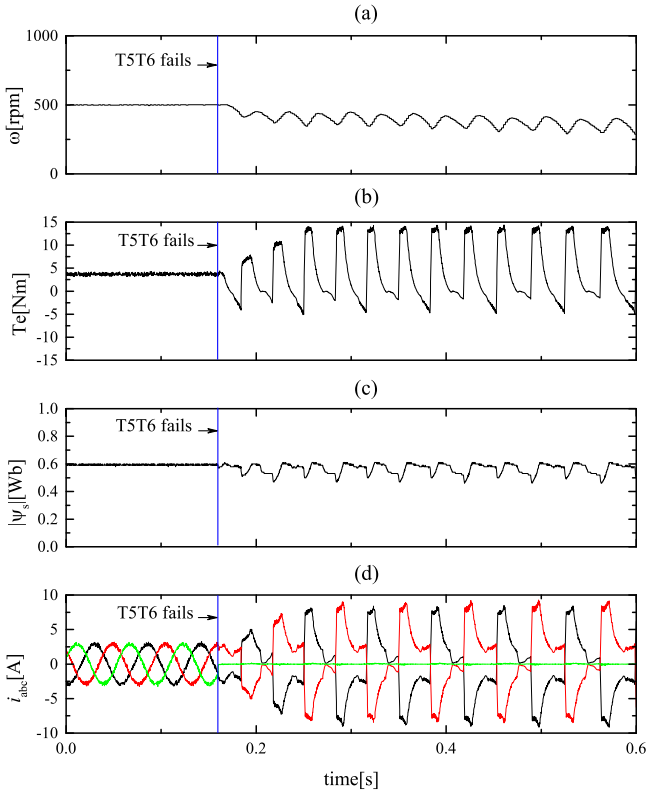

Fig. 9. Control performance when T5T6 fails with 30% rated load torque at 500 r/min without fault-tolerant operation. (a) Speed. (b) Estimated torque. (c) Stator flux. (d) Stator current.

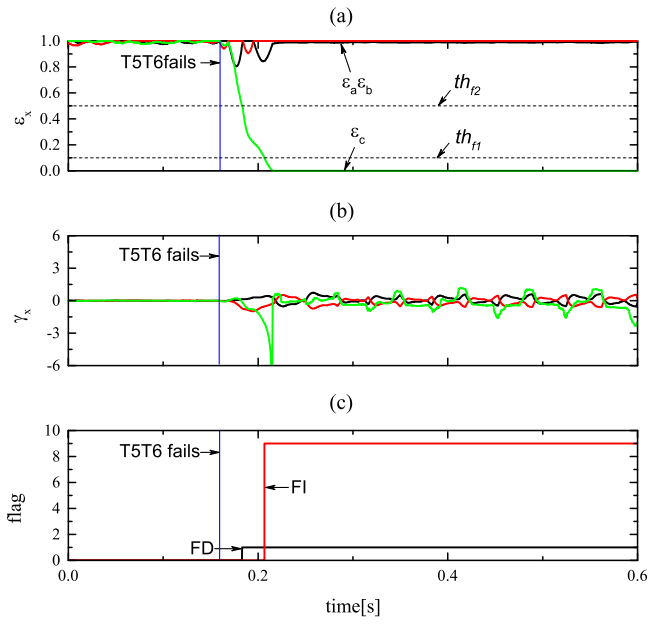

Fig. 10. Fault diagnostic process when T5T6 fails with 30% rated load torque at 500 r/min without fault-tolerant operation. (a) Variation. (b) Skewness. (c) Fault detection and fault isolation flag.

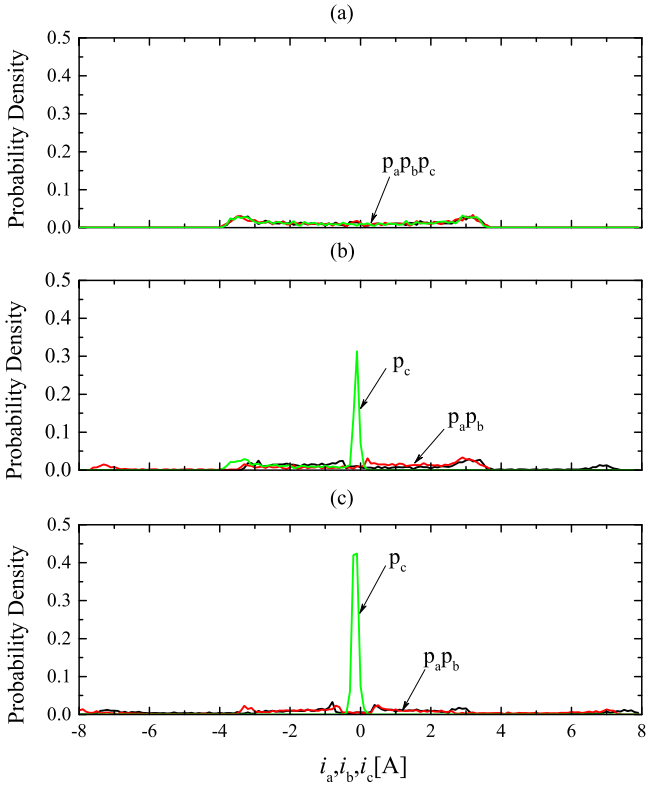

Fig. 11. Output current probability density in different cases. (a) Healthy case. (b) One switch fault. (c) Entire leg fault.

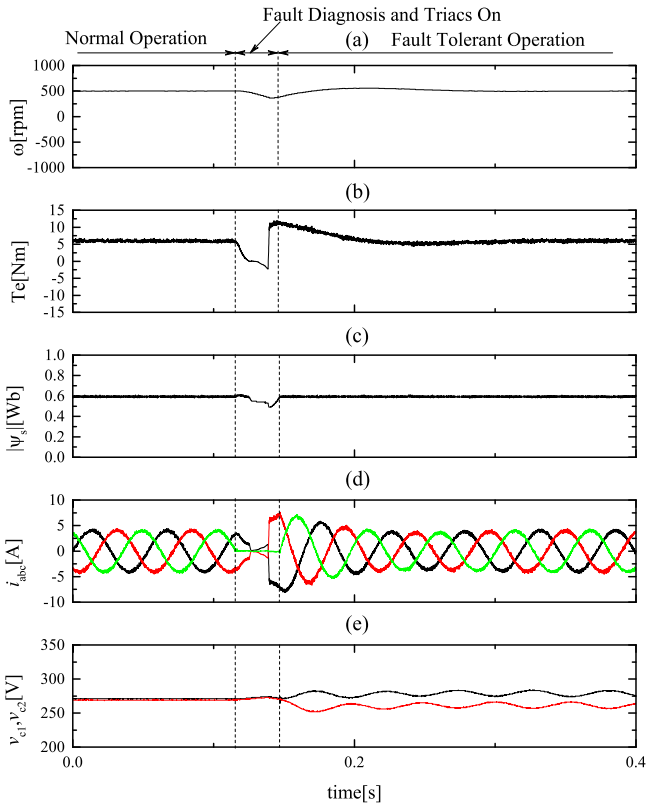

Fig. 12. Control performance during the transition from normal operation to the faulty mode operations when T6 fails. (a) Speed. (b) Estimated torque. (c) Stator flux. (d) Stator current. (e) Capacitor voltages.

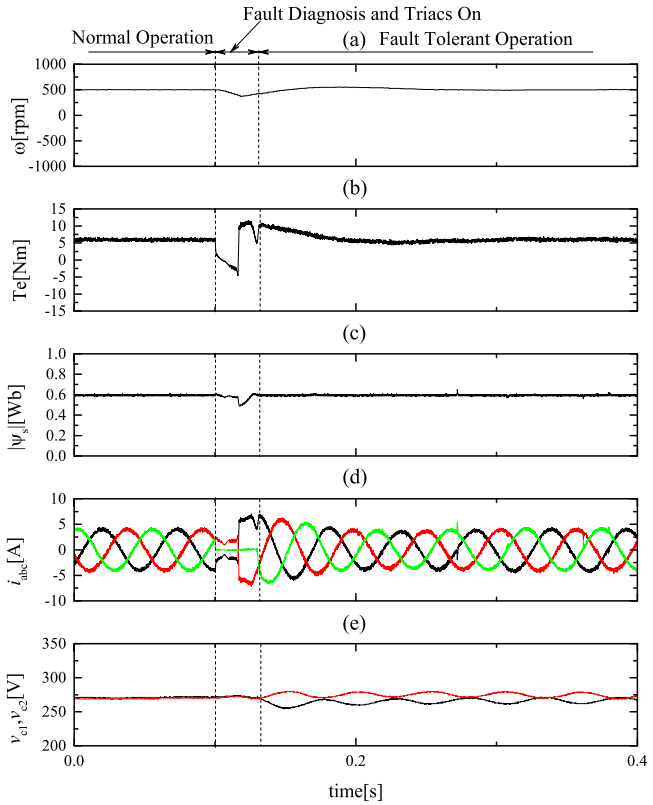

Fig. 13. Control performance during the transition from normal operations to the faulty mode operation when T5T6 fails. (a) Speed. (b) Estimated torque. (c) Stator flux. (d) Stator current. (e) Capacitor voltages.

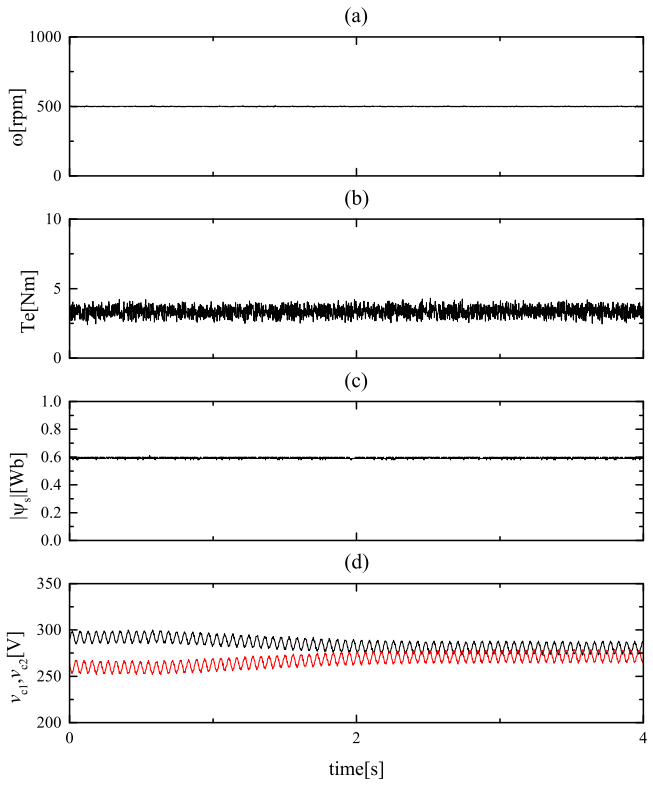

Fig. 14. Control performance at the fault-tolerant mode during capacitor voltage deviation suppression term applied. (a) Speed. (b) Estimated torque. (c) Stator flux. (d) Capacitor voltages.

stator flux, and current performance at normal condition. It is clear to see that the fluctuation and deviation of the capacitor voltages are presented after hardware reconfiguration in both cases.

Fig. 14 displays the control performance at the fault-tolerant mode during the capacitor voltage deviation suppression term applied. As shown in Fig. 14, when the proposed strategy is applied at 0.6 s, the voltage offset across the two capacitor introduced by the speed variation is eliminated at 2.6 s. During the transient, the performance of speed, torque, and stator flux is barely affected.

VI. Conclusion

This paper has presented a comprehensive embedded fault-tolerant algorithm for induction motor drives. A novel fault-diagnosis algorithm for PTC scheme based on probability density analysis is proposed to isolate the fault. A generalized voltage model, switching combination, and cost function for prefault and postfault are developed for compact software adaptation. The flexible control structure of the PTC can make the proposed fault-diagnosis and fault-tolerant control scheme easily embedded within the normal control scheme. In this way, the control schemes at prefault and postfault are merged into one. This makes fault-tolerant operation of practical interests. Experimental results have shown that the seamless likely and rapid transient processes from fault occurrence to postfault operation are achieved.

With the proposed embedded fault-tolerant algorithm, induction motor drives can manage the power switch fault itself without significantly changing the control scheme. The proposed scheme has been found an easy and compact solution for applications where continuously operation is of great importance.

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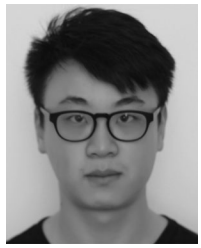

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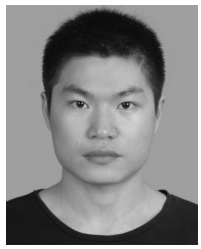

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