An AC–DC LED Driver With a Two-Parallel Inverted Buck Topology for Reducing the Light Flicker in Lighting Applications to Low-Risk Levels

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***Abstract*—This paper presents an ac–dc LED driver that consists of two-parallel inverted buck converters. To buffer the twice-line-frequency energy, one inverted buck converter (also known as a floating buck converter) conveys energy to a storage capacitor, simultaneously performing the power factor correction. The other inverted buck converter regulates the LED current to maintain a constant brightness in the LEDs for reducing the light flicker to low-risk levels. The proposed architecture reduces the voltage stress and the size of the storage capacitor, enabling the use of a film capacitor instead of an electrolytic capacitor. Considering the power factor and the flicker standards, a design procedure to achieve a high power factor, while minimizing the storage capacitance and the LED current ripple, is presented. A prototype of the proposed LED driver has been implemented with an on-chip controller IC fabricated in a 0.35-μm CMOS process and its functionality and performance have been verified experimentally. It demonstrates a power factor of 0.94 and a peak power efficiency of 85.4% with an LED current ripple of 6.5%, while delivering 15 W to the LEDs.**

***Index Terms*—AC–DC, digital pulse width modulators (DPWM), flicker, floating buck, inverted buck, LED driver, light-emitting diodes (LEDs), power factor correction (PFC).**

I. Introduction

LIGHT-EMITTING diodes (LEDs) have been replacing traditional light sources like incandescent and fluorescent lamps in many lighting applications because LEDs have a wide color gamut, a high luminous efficacy, a long lifetime, and are environment friendly [1]–[4]. Most state-of-the-art LED drivers utilizing an offline ac voltage source employ power factor correction (PFC) circuits to comply with standards like the IEC61000-3-2 [5] and the ENERGY STAR [6], which specifies that the power factor (PF) should be higher than 0.9 for commercial applications and 0.7 for residential applications. To meet these requirements, conventional single-stage LED drivers with PFC circuits that reduced the number of discrete components using simple structures with reduced costs and small form factors were reported in [7]–[9].

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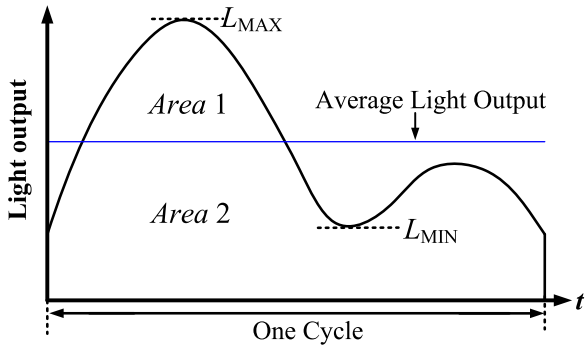

Fig. 1. Periodic waveform of the light output in one cycle [12].

However, the single-stage LED drivers in [7]–[9] exhibit light flicker that varies at twice the ac-line frequency because they mainly focus on the PFC function only, and, therefore, have a large LED current ripple. Although light flicker at frequencies above 70 Hz is typically invisible to most people, it may induce harmful biological effects including headache, fatigue, eyestrain, and even epileptic seizures [10], [11]. According to [12], there are two common ways to measure flicker, the Flicker Index and the Percent Flicker. With reference to Fig. 1, the Flicker Index and Percent Flicker (also known as Modulation (%)) can be expressed as

$$\text{Flicker Index} = \frac{\text{Area1}}{\text{Area1} + \text{Area2}} \tag{1}$$

$$\text{Percent Flicker} = 100 \times \frac{L_{\text{MAX}} - L_{\text{MIN}}}{L_{\text{MAX}} + L_{\text{MIN}}}. \tag{2}$$

Studies in [13] and [14] indicate the permissible flicker in terms of the Flicker Index or the Percent Flicker by collecting experimental data from previous flicker studies. The IEEE standard 1789-2015 in [15] provides the recommended practices for modulating current in high-brightness LEDs. According to [13] and [15], in LED lighting applications with flicker frequencies above 90 Hz, Percent Flicker for low-risk level should satisfy the following:

$$\text{Percent Flicker} \left(= \text{Mod\%} \right) < 0.08 \times f_{\text{FLICKER}} \tag{3}$$

where f_{FLICKER} is the frequency of the flickering light. For example, a Percent Flicker of less than 9.6% is acceptable if f_{FLICKER} is 120 Hz. The relationship between the Percent Flicker and

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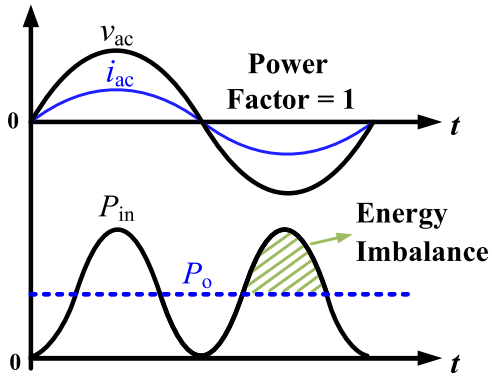

Fig. 2. Waveforms of an ac–dc LED driver with a constant output power when the power factor is unity.

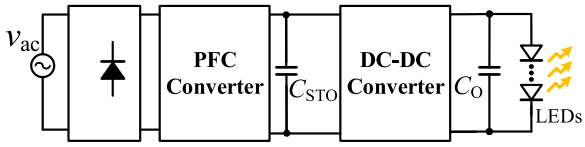

Fig. 3. Conventional two-stage ac–dc LED driver consisting of a first-stage PFC converter and a second-stage dc–dc converter.

the Flicker Index is discussed in [14], where the recommended Flicker Index is

$$\text{Flicker Index} \leq 0.1 \text{ (when } f_{\text{FLICKER}} = 100 \text{ Hz)}. \quad (4)$$

A Flicker Index of 0.1 is equivalent to a Percent Flicker of 20% and 30% for a square and sinusoidal light output, respectively.

Fig. 2 depicts the waveforms of an ac–dc LED driver with a constant output power, when the input PF is unity. The input power (P_{in}) at twice the line frequency has a pulsating waveform that periodically changes above or below the constant output power (P_{o}). Hence, a storage capacitor as an energy buffer is required to balance out the instantaneous power differences between P_{in} and P_{o}. Fig. 3 illustrates the architecture of a conventional two-stage ac–dc LED driver with a storage capacitor (C_{STO}) [16]–[19]. Although this approach offers a near unity PF and a precisely regulated output voltage, it would be generally more difficult to achieve a high-conversion efficiency with the two-stage architecture unless an optimized control in each stage is applied, although efficiencies up to 95% have been reported. Furthermore, this architecture requires several components relatively, resulting in large sizes and considerable costs [20]–[22].

To achieve a high PF and reduce the output LED current ripple, several methods have been proposed [21]–[37]. The first approach is to inject odd-harmonic signals like the third and the fifth harmonics [22]–[24] or the third harmonic only [25], [26] to the input current for reducing the input current pulsation, sacrificing the input PF down to 0.9. While the previous studies in [22], [23], and [25] show a reduction in the size of the capacitors, recent studies in [24] and [26] consider the output light flicker characteristics. Although this approach enables the single-stage architecture without the use of C_{STO}, the study in [24] requires a large output capacitor of 500 μF for the output power of 20 W to ensure a Percent Flicker less than 40%.

The second approach is to employ a parallel [21], [27]–[30] or a series [31]–[35] ripple cancellation converter (RCC). In [21] and [27]–[30], a bidirectional converter is used as an active power filter and is placed in parallel with the LED load that is directly connected to the PFC stage, for controlling the LED current ripple. While this method can achieve a dc LED current and significantly reduce the size of the output and storage capacitors, approximately 32% of the output power is converted three times before it is delivered to the output, incurring a power loss [31]–[33]. In [31]–[35], on the other hand, the output of the RCC is connected in series with the output of the PFC stage, and the LED load is connected in parallel with the two series-connected output capacitors. The series RCC topology can provide a higher power efficiency than the parallel RCC topology because it further reduces the proportion of the output power converted more than once. In [31] and [32], for example, 90% of the output power is directly delivered by the PFC stage, while 10% of the output power is converted twice before being delivered to the output.

Another approach with an ac–dc power conversion architecture consisting of two stacked energy-storage capacitors across the rectifier output and two inverted resonant buck converters is proposed in [36]. Although the stacked architecture needs an additional power combing converter composed of a switched capacitor circuit, this architecture is suitable for high-frequency operations at 3–10 MHz, enabling the use of two 0.8-μH inductors for an LED power of 30 W. An average current modulation method for a single-stage LED driver is proposed in [37], where the LED load is connected in series with a modulation switch for pulsed current driving. To achieve a constant average level of the LED current in each modulation cycle, the duty cycle of the switch is controlled according to the pulsating output voltage level. In [38], an ac–dc converter with a parallel PFC scheme is proposed. An isolated full-bridge boost converter is employed for the main power stage where 68% of the input power is directly delivered to the output, and the remaining 32% of the power is stored in a storage capacitor. A forward converter is placed in parallel with the boost converter and is used for the auxiliary power stage that provides the necessary power for dc output power by using the storage capacitor as its input source. Although only 32% of the power must be processed twice before being delivered to the output, this architecture requires two isolation transformers that are relatively complex and expensive.

In this paper, we propose an ac–dc LED driver consisting of two parallel inverted buck converters for reducing the light flicker to low-risk levels. To handle the power differences between the twice-line-frequency input power and the constant LED power, one inverted buck converter conveys energy from the ac source to a storage capacitor, simultaneously performing the PFC operation. The other inverted buck converter supplies constant current to the LEDs to maintain a constant brightness. The proposed architecture can achieve an input PF higher than 0.9. Although the proposed approach offers a lower PF than the conventional two-stage approach with a boost PFC converter [16]–[19], the proposed architecture with two inverted buck converters in parallel significantly reduces the average voltage of C_{STO} to 56.5 V at the input voltage of 110 V_{rms}, whereas the average voltage of C_{STO} in the two-stage must be higher than

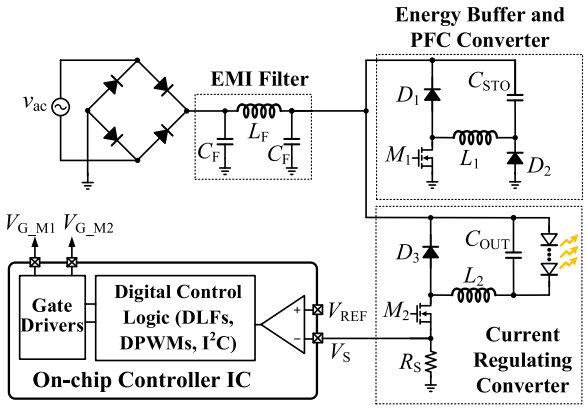

Fig. 4. Overall architecture of the proposed ac–dc LED driver with two-parallel inverted buck converters.

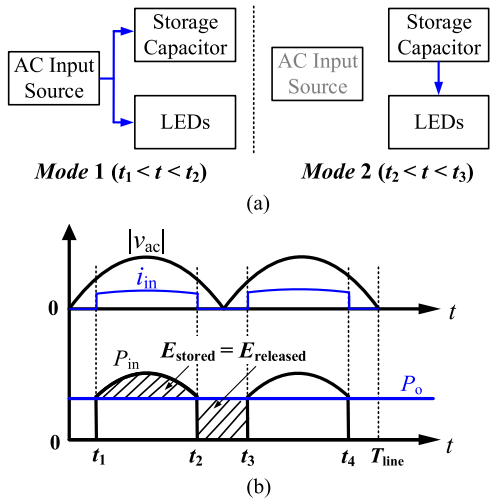

Fig. 5. (a) Energy flow concept and (b) input and output waveforms of the proposed LED driver with two alternating operating modes.

155 V. Moreover, the size of $C_{\rm STO}$ is reduced because less than 30% of the output power is initially stored in $C_{\rm STO}$ and then delivered to the LED load. Thus, the reduced voltage stress and size of $C_{\rm STO}$ enables ceramic or film capacitors to be utilized instead of electrolytic capacitors that have lifetime constraints.

In addition, the two inverted buck converters have a low-side switch that reduces the design complexity of the gate driver circuit. Whereas the second approach employing an RCC [21], [27]–[35] requires a transformer or coupled inductor with several other components, the proposed architecture provides a low-cost solution and simple design for low-power LED lighting applications. The rest of this paper is organized as follows: Section II presents the system architecture and operation principle of the proposed LED driver. Section III discusses the design considerations for achieving a high PF and efficiency, and describes the design procedure of the proposed LED driver. Section IV summarizes the experimental results of the prototype LED driver.

II. Proposed System Architecture and Operation Principle

A. Overall Architecture

Fig. 4 illustrates the overall architecture of the proposed LED driver that consists of a full-bridge rectifier, an EMI filter, two parallel inverted buck converters, and an on-chip controller IC. The upper inverted buck converter composed of M_1, L_1, D_1, D_2, and $C_{\rm STO}$ performs the PFC function while simultaneously transmitting energy from an ac source to a storage capacitor $C_{\rm STO}$ to buffer the instantaneous power differences between the input power and the output LED power. The other inverted buck converter consisting of M_2, L_2, D_3, and $C_{\rm OUT}$ regulates the output current to maintain the brightness of the LEDs to reduce light flicker. The EMI filter suppresses electrical noises from the ac source and the switching circuits, and shapes the ac input current for the PFC.

The duty cycle of the switches $\rm M_1$ and $\rm M_2$ are controlled by a digital control logic composed of programmable digital-loop filters and digital pulse width modulators (DPWMs). For a 10-bit DPWM, the upper 6-bit resolution is realized by a counter-based DPWM and the lower 4-bit resolution is obtained by a phase interpolator circuit to improve the input clock frequency requirement [39]. For example, if the input clock frequency is 64 MHz, the output switching frequency is 1 MHz.

Inverted buck converters (also known as floating buck converters) have been widely used as current regulators in dc–dc [40], [41] and ac–dc LED drivers [8], [9], [19], [36]. While the traditional buck converter with a high-side switch requires additional bootstrapping circuits, the inverted buck converter with a low-side NFET can be easily driven by a gate driver circuit. Therefore, the proposed ac–dc LED driver with two inverted buck converters in parallel can be cost effective because of a reduced component count [40]. Furthermore, as an inverted buck converter has a floating output voltage, the voltage stress of $C_{\rm STO}$ can be greatly reduced if the voltage across $C_{\rm STO}$ is well regulated by the controller circuit. Hence, ceramic or film capacitors can be employed for $C_{\rm STO}$ in place of electrolytic capacitors.

B. Operation Principle

Fig. 5 (a) depicts the concept of energy flow in the proposed architecture with two alternating operating modes, *Mode* 1 and *Mode* 2; Fig. 5 (b) illustrates its theoretical input and output power waveforms. The energies stored and released by the storage capacitor, indicated as $E_{\rm stored}$ and $E_{\rm released}$, respectively, can be expressed as

$$E_{\rm stored} = \int_{t_1}^{t_2} (P_{\rm in}(t) - P_o)dt \tag{5}$$

$$E_{\rm released} = \int_{t_2}^{t_3} P_o dt = P_o \times (t_3 - t_2). \tag{6}$$

During *Mode* 1, energy from the ac-input source is delivered to both the LEDs and the storage capacitor. During *Mode* 2, the stored energy $E_{\rm stored}$ is transferred to the LEDs without the help of the ac source. Therefore, the LED load has a constant

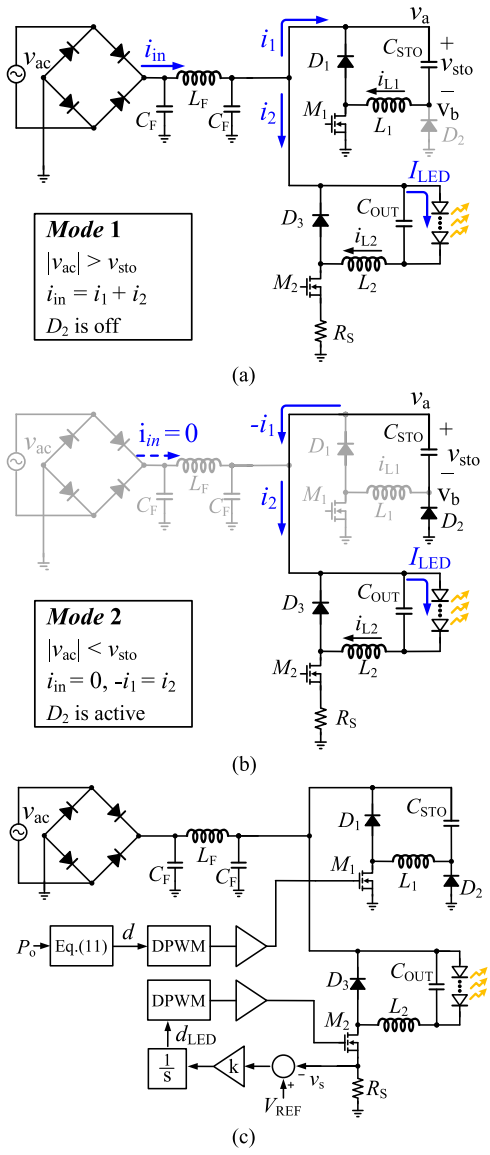

Fig. 6. Operating modes: (a) *Mode* 1 when $|v_{ac}| > v_{sto}$ and (b) *Mode* 2 when $|v_{ac}| < v_{sto}$; and (c) the block diagram of the proposed LED driver with a two-parallel inverted buck topology.

output current regardless of the mode of operation. The detailed explanation for each mode of operation is as follows.

1) Mode 1: when $|v_{ac}| > v_{sto} (t_1 < t < t_2)$*:* Fig. 6 illustrates the operating modes and the block diagram of the proposed LED driver with two parallel inverted buck converters, and Fig. 7 shows its theoretical voltage and current waveforms. The two operating modes alternate according to the voltage relationship between the ac-input voltage (v_{ac}) and the voltage across C_{STO}, denoted as v_{sto}. During *Mode* 1 when $|v_{ac}| > v_{sto}$, the input voltage and current can be expressed as

$$v_{ac}(t) = V_m \sin wt \tag{7}$$

$$i_{in} = i_1 + i_2 \tag{8}$$

where i_1 and i_2 are input currents of the two inverted buck converters, respectively. As shown in Fig. 6(a), the input current

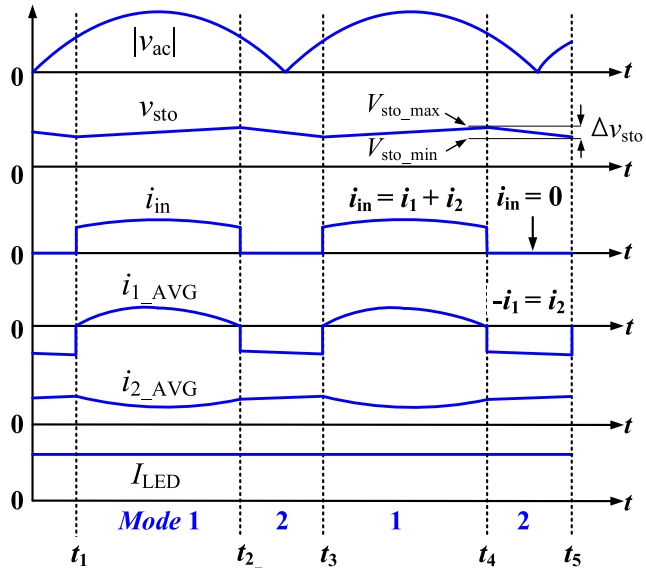

Fig. 7. Theoretical voltage and current waveforms of the proposed LED driver.

(i_{in}) can be expressed as the sum of i_1 and i_2 because the two inverted buck converters operate separately in *Mode* 1.

The lower inverted buck converter regulates the current flowing through the LEDs regardless of the two operating modes to provide a constant current to the LEDs. This regulating converter operates in a fixed-frequency continuous-conduction mode (CCM) to reduce the output voltage ripple. As shown in Fig. 6 (c), the duty cycle (D_{LED}) of switch M_2 is controlled by the feedback loop to achieve the desired LED current. If we assume that the power efficiency of the current regulating converter is 100%, the averaged current (i_{2_AVG}), flowing into the regulating converter in one switching cycle can be expressed as

$$i_{2\_AVG}(t) = \frac{P_o}{V_m |\sin wt|}. \tag{9}$$

As shown in Fig. 7, (i_{2_AVG}) is inversely proportional to the ac-input voltage (v_{ac}), i.e., an additional PFC circuit is required for a high PF. Therefore, the other inverted buck converter is employed for the PFC function and placed in parallel with the current regulating converter. Although employing a bidirectional boost converter instead of an inverted buck converter is a possible approach that applies to the energy flow concept shown in Fig. 5, the one buck and one boost approach requires higher voltage stress in C_{STO}; i.e., v_{sto} should be higher than the ac-input voltage.

To achieve a high PF, the upper inverted buck converter shown in Fig. 6 (a) operates in a discontinuous-conduction mode (DCM) with a fixed duty cycle (D) and the diode D_2 is always off during *Mode* 1. As shown in Fig. 6 (c), the duty cycle D of power switch M_1 is obtained from (11) and programmed to the digital control logic through an interintegrated circuit (I^2C) interface. Although the buck PFC converter with a clipped-sinusoidal input current usually has a lower PF than the boost PFC converter, it can achieve a PF ranging from 0.82 to 0.98 and meet the harmonic requirements (IEC61000-3-2) [42]–[44]. Besides,

its low-output voltage permits the use of lower voltage-rated semiconductor devices and capacitors [42]–[44]. The averaged current (i_{1_AVG}) flowing into the buck PFC converter operating in a DCM can be expressed as

$$i_{1\_\mathrm{AVG}}(t) = \frac{D^2}{2L_1 f_{\mathrm{sw}}}(V_{\mathrm{m}}\,|\sin wt| - v_{\mathrm{sto}}(t)) \tag{10}$$

where D is the duty cycle of the power switch M_1 and f_{sw} is the switching frequency of the buck PFC converter [42]. It is noted that i_{1_AVG} shown in Fig. 7 is proportional to the voltage difference between the input voltage (v_{ac}) and the output voltage (v_{sto}). Inserting (9) and (10) into (8), the input current (i_{in}) is obtained as

$$i_{\mathrm{in}}(t) = \frac{D^2}{2L1 f\mathrm{sw}}(V_{\mathrm{m}}\,|\sin wt| - v_{\mathrm{sto}}(t)) + \frac{P_{\mathrm{o}}}{V_{\mathrm{m}}\,|\sin wt|} \tag{11}$$

where the input current (i_1) of the PFC converter cancels out the input current (i_2) of the regulating converter.

Furthermore, the PFC converter also stores energy in C_{STO} to buffer the twice-line-frequency energy. Because this converter does not have a load to consume the output power, the energy charged onto the inductor (L_1) by the ac input source is stored in C_{STO}. Consequently, the storage capacitor voltage (v_{sto}) shown in Fig. 7 increases until it enters *Mode* 2 and can be expressed as

$$v_{\mathrm{sto}}(t) = V_{\mathrm{sto\_min}} + \frac{1}{C_{\mathrm{STO}}}\int_{t1}^{t} i_{\mathrm{L1}}(t)dt, (t_1 < t < t_2). \tag{12}$$

By using the minimum and maximum voltage values of the storage capacitor, the stored energy E_{stored} is expressed as

$$\begin{aligned} E_{\mathrm{stored}} &= \frac{C_{\mathrm{STO}}}{2}({V_{\mathrm{sto\_max}}}^2 - {V_{\mathrm{sto\_min}}}^2) \\ &= C_{\mathrm{STO}} \cdot \Delta v_{\mathrm{sto}} \cdot V_{\mathrm{sto\_AVG}} \end{aligned} \tag{13}$$

where $\Delta v_{\mathrm{sto}}{=}V_{\mathrm{sto\_max}}{-}V_{\mathrm{sto\_min}}$ and $V_{\mathrm{sto\_AVG}}$ is the average voltage of v_{sto} across C_{STO}.

As the inverted buck converter has a floating output voltage, the positive terminal voltage (v_{a}) of C_{STO} is equal to $|v_{\mathrm{ac}}|$ in *Mode* 1 and the negative terminal voltage (v_{b}) can be expressed as

$$v_b(t) = |v_{\mathrm{ac}}(t)| - v_{\mathrm{sto}}(t). \tag{14}$$

As the voltage level of $|v_{\mathrm{ac}}|$ decreases, v_{b} also decreases and approaches ground. When $|v_{\mathrm{ac}}|$ falls below $v_{\mathrm{sto},}$ v_{b} becomes negative. Consequently, a transition from *Mode* 1 to *Mode* 2 occurs when diode D_2 becomes active and starts conducting.

2) Mode 2: When $|v_{\mathrm{ac}}| < v_{\mathrm{sto}}(t_2 < t < t_3)$*:* As illustrated in Fig. 6 (b), the full-bridge rectifier is off and the PFC converter is idle because v_{sto} is higher than $|v_{\mathrm{ac}}|$. Thus, the input current (i_{in}) and the current (i_2) flowing into the lower inverted buck converter are

$$i_{\mathrm{in}} = 0 \text{ and } i_2 = -i_1. \tag{15}$$

The storage capacitor C_{STO} operates like a ground-connected capacitor and acts as an energy source for the regulating converter. When the switch M_2 is on, the diode D_2 turns on and the energy stored in C_{STO} during *Mode* 1 is delivered to the LEDs. Hence, v_{sto} decreases until it enters *Mode* 1, whereas the averaged current (i_{2_AVG}) increases because the input current of the regulating converter is inversely proportional to the input voltage. Similar to the derivation of (9) in *Mode* 1, v_{sto} and i_{2_AVG} as shown in Fig. 7, can be expressed as

$$i_{2\_\mathrm{AVG}}(t) = \frac{P_{\mathrm{o}}}{v_{\mathrm{sto}}(t)} \tag{16}$$

where

$$v_{\mathrm{sto}}(t) = V_{\mathrm{sto\_max}} - \frac{1}{C_{\mathrm{STO}}}\int_{t2}^{t} i_2(t)dt, (t_2 < t < t_3). \tag{17}$$

Here, the voltage v_{sto} on the storage capacitor should be higher than the output voltage across the LED load for the buck operation, i.e., $V_{\mathrm{sto\_min}} > V_{\mathrm{out}}$.

In the following ac cycle, when the ac-input voltage increases above v_{sto}, the full-bridge rectifier is turned on, the diode D_2 is off and *Mode* 1 starts again. It is noted that the input voltage of the regulating converter is v_{ac} in *Mode* 1 and v_{sto} in *Mode* 2. Hence, the input voltage level is continuous because mode changes occur when the two voltages (v_{ac} and v_{sto}) have the same voltage level. Therefore, the regulating converter can supply a dc current to the LEDs without causing a fluctuation in I_{LED} during the transition period between the two operating modes.

Although the proposed LED driver does not have the dimming function, the proposed architecture could accommodate analog dimming operation. The regulating buck converter can adjust the continuous value of the LED current while changing the dimming level of LEDs by setting the reference voltage (V_{REF}) shown in Fig. 6 (c). Owing to the P_{o} variations with the dimming of LEDs, the level of v_{sto} varies because the amount of energy stored and released by C_{STO} is proportional to P_{o}. Therefore, the duty cycle D of M_1 in the PFC converter must be controlled by a feedback loop to maintain v_{sto} in the proper operating range during the dimming operation. If the feedback loop for the dimming operation is added to the controller IC, we expect that analog dimming would be possible in this approach.

III. Design of the Proposed Topology

A. Design Considerations for Deciding the Storage Capacitor Voltage

The line input current (i_{in}) consists of two current components (i_1 and i_2) that flow into the respective inverted buck converters in *Mode* 1. By substituting $a_1 = \frac{D^2}{2L1 f\mathrm{sw}}$ into (11), the input current is rearranged as

$$i_{\mathrm{in}}(t) = a_1(V_{\mathrm{m}}\,|\sin wt| - v_{\mathrm{sto}}(t)) + \frac{P_{\mathrm{o}}}{V_{\mathrm{m}}\,|\sin wt|}. \tag{18}$$

The input current waveform is determined by the design parameter (a_1), the storage capacitor voltage (v_{sto}), and the output power (P_{o}). As described in Section II, the storage capacitor voltage (v_{sto}) increases in *Mode* 1, whereas it decreases in *Mode* 2. The average voltage of v_{sto} settles to a certain value where the stored energy (E_{stored}) in C_{STO} is equal to the released energy (E_{released}) for the LED load. Fig. 8 describes

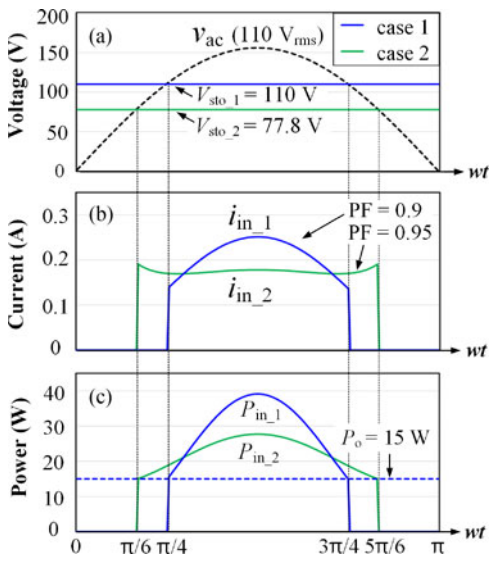

Fig. 8. Waveforms of the respective (b) input currents ($i_{\text{in\_1}}$ and $i_{\text{in\_2}}$) and (c) the input powers ($P_{\text{in\_1}}$ and $P_{\text{in\_2}}$) depending upon (a) the voltage across the storage capacitors ($V_{\text{sto\_1}}$: 110 V and $V_{\text{sto\_2}}$: 77.8 V), respectively.

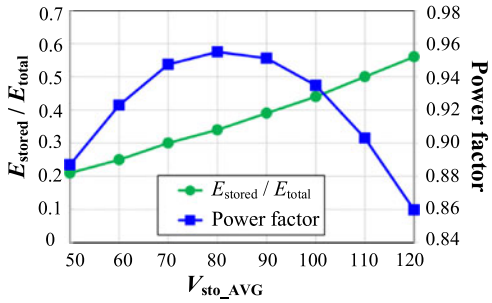

Fig. 9. Stored energy ratio ($E_{\text{stored}}/E_{\text{total}}$) and power factor with respect to the average values of the storage capacitor voltage, when the input voltage is 110 V_{rms}.

the variations in the waveforms of the respective input currents ($i_{\text{in\_1}}$ and $i_{\text{in\_2}}$) and the input powers ($P_{\text{in\_1}}$ and $P_{\text{in\_2}}$) depending upon the voltage across the storage capacitors ($V_{\text{sto\_1}}$: 110 V and $V_{\text{sto\_2}}$: 77.8 V), respectively. Here, the output power (P_{o}) is 15 W; it is assumed that V_{sto_1} and V_{sto_2} are constant and the power conversion efficiency is 100%. The conduction periods of $i_{\text{in\_1}}$ and $i_{\text{in\_2}}$ are 1/2 and 2/3, respectively, of a half-line cycle, as they are decided by the voltage levels of $V_{\text{sto\_1}}$ and $V_{\text{sto\_2}}$, respectively. In other words, the stored energy ratio ($E_{\text{stored}}/E_{\text{total}}$) is 1/2 in *case* 1 and 1/3 in *case* 2, where E_{total} is the total input energy for one half-line cycle. Therefore, as shown in Fig. 8 (c), the input power ($P_{\text{in\_1}}$) is higher than $P_{\text{in\_2}}$ for most of the conduction period so that more energy is stored in C_{STO}. As shown in Fig. 8 (b), compared to $i_{\text{in\_2}}$, it should be noted that $i_{\text{in\_1}}$ leads to a lower PF of 0.9 owing to a shorter conduction period, although its waveform is more similar to the line voltage.

Fig. 9 plots the stored energy ratio ($E_{\text{stored}}/E_{\text{total}}$) and the PF with respect to the average values of the storage capacitor voltage denoted as $V_{\text{sto\_AVG}}$, when the output power is 15 W and the input voltage is 110 V_{rms}, where it is assumed that the efficiency is 100% and v_{sto} has a constant value of $V_{\text{sto\_AVG}}$. The stored energy ratio ($E_{\text{stored}}/E_{\text{total}}$) increases from 0.21 to 0.56 with the voltage level of $V_{\text{sto\_AVG}}$ that decides the length of the *Mode* 2 period, where the LED load is driven by the stored energy E_{stored} in the storage capacitor. Minimizing $E_{\text{stored}}/E_{\text{total}}$ is desirable for improving the efficiency of the proposed LED driver because E_{stored} is the energy that is converted twice before it is finally delivered to the LED load. Moreover, according to (13), the voltage stress and the size of the storage capacitor can be reduced if E_{stored} is decreased.

As $V_{\text{sto\_AVG}}$ increases from 50 to 120 V, the values of the PF increase from 0.89 to 0.95 until $V_{\text{sto\_AVG}}$ is 80 V and then they decrease from 0.95 to 0.86. When $V_{\text{sto\_AVG}}$ is below 80 V, the input PF is primarily influenced by the amplitude of the input current component for the PFC. However, when $V_{\text{sto\_AVG}}$ is above 80 V, the PF is degraded by the reduced conduction time of the input current. For a PF greater than 0.9, to comply with the ENERGY STAR standards [6], the possible voltage range of $V_{\text{sto\_AVG}}$ is 55–110 V, in this example. Therefore, a design tradeoff between minimizing $E_{\text{stored}}/\text{E}_{\text{total}}$ and achieving a high PF needs to be considered when deciding the storage capacitor voltage.

B. Analysis of the Proposed LED Driver With Line-Voltage Variations

The graphs of the PF and $E_{\text{stored}}/\text{E}_{\text{total}}$ plotted in Fig. 9 maintain the same shape as the line voltage varies. However, the values of $V_{\text{sto\_AVG}}$ shown on the *x*-axis vary proportionally with the line voltage because the conduction time of the input current is decided by $V_{\text{sto\_AVG}}$; i.e., the operating mode changes when $V_{\text{m}}\sin wt = v_{\text{sto}}$. According to (11), with line-voltage variations, the two current components of the input current (i_{in}) increase or decrease in opposite directions because the buck PFC converter operates with a fixed duty cycle (*D*). In other words, the stored energy ratio ($E_{\text{stored}}/E_{\text{total}}$) and the ratio of $V_{\text{sto\_AVG}}/V_{\text{in,rms}}$ increase with the line voltage.

To handle line-voltage variations ranging from 80 to 132 V_{rms}, $V_{\text{sto\_AVG}}$ must be maintained within a voltage range from $V_{\text{in,rms}}/2$ to $V_{\text{in,rms}}$ for PF $>$ 0.9, which is equivalent to $E_{\text{stored}}/E_{\text{total}}$ being 0.23–0.5. For example, $V_{\text{sto\_AVG}}$ must be less than 132 V for $E_{\text{stored}}/E_{\text{total}} < 0.5$ when the input voltage is 132 V_{rms}. On the other hand, $V_{\text{sto\_AVG}}$ must be higher than 40 V for $E_{\text{stored}}/E_{\text{total}} > 0.23$ when the input voltage is 80 V_{rms}. Here, $V_{\text{sto\_min}} > V_{\text{out}}$ must be satisfied for proper operation of the LED driver. If $V_{\text{sto\_AVG}}$ becomes too low, i.e., $V_{\text{sto\_min}} > V_{\text{out}}$ cannot be satisfied, the Percent Flicker increases because the LED load cannot be fully driven by C_{STO} during *Mode* 2.

The input voltage range of the proposed LED driver can be derived by calculating the stored energy (E_{stored}) for a half-line cycle when the stored energy ratio ($E_{\text{stored}}/E_{\text{total}}$) is 0.23 and 0.5. For simplicity of analysis, it is assumed that the efficiency is 100% and v_{sto} has a constant value of $V_{\text{sto\_AVG}}$ that is higher than V_{out}. According to Fig. 9, the two cases can be summarized as follows.

1) When $V_{\mathrm{m}} = V_{\mathrm{m\_min}}$

$$E_{\mathrm{stored1}}/E_{\mathrm{total}} = 0.23 \text{ and } V_{\mathrm{sto\_AVG1}} = 0.5 \times (V_{\mathrm{m\_min}}/\sqrt{2}).$$

2) When $V_{\mathrm{m}} = V_{\mathrm{m\_max}}$

$$E_{\mathrm{stored2}}/E_{\mathrm{total}} = 0.5 \text{ and } V_{\mathrm{sto\_AVG2}} = V_{\mathrm{m\_max}}/\sqrt{2}$$

where $V_{\mathrm{m\_min}}$ and $V_{\mathrm{m\_max}}$ are the minimum and maximum amplitudes, respectively, of the input voltage in each case. Because the total input energy (E_{total}) is equal in each case, the relationship between E_{stored1} and E_{stored2} is

$$E_{\mathrm{stored1}} = (0.23/0.5) \times E_{\mathrm{stored2}}. \tag{19}$$

Because E_{stored} is the input power of the PFC buck converter, it can be expressed as

$$E_{\mathrm{stored}} = \int_{t_1}^{t_2} v_{\mathrm{ac}}(t) \times i_1(t) dt. \tag{20}$$

By substituting $v_{\mathrm{ac}}(t)$ with (7) and $i_1(\mathrm{t})$ with (10), E_{stored1} is derived as

$$\begin{aligned} E_{\mathrm{stored1}} &= \int_{t_1}^{t_2} (V_{\mathrm{m\_min}} \sin wt) \\ &\quad \times \frac{D^2}{2L_1 f_{\mathrm{sw}}} (V_{\mathrm{m\_min}} \sin wt - V_{\mathrm{sto\_AVG1}}) dt \\ &= \frac{D^2 V_{\mathrm{m\_min}^2}}{2L_1 f_{\mathrm{sw}}} \int_{t_1}^{t_2} \sin wt \\ &\quad \times \left(\sin wt - \frac{V_{\mathrm{sto\_AVG1}}}{V_{\mathrm{m\_min}}} \right) dt \end{aligned} \tag{21}$$

where $t_1 = 0.115 \times (T_{\mathrm{line}}/2)$ and $t_2 = (1\,0.115) \times (T_{\mathrm{line}}/2)$. In the same manner, E_{stored2} is obtained as

$$\begin{aligned} E_{\mathrm{stored2}} &= \frac{D^2 V_{\mathrm{m\_max}^2}}{2L_1 f_{\mathrm{sw}}} \int_{t_1}^{t_2} \sin wt \\ &\quad \times \left(\sin wt - \frac{V_{\mathrm{sto\_AVG2}}}{V_{\mathrm{m\_max}}} \right) dt \end{aligned} \tag{22}$$

where $t_1 = 0.25 \times (T_{\mathrm{line}}/2)$ and $t_2 = (10.25) \times (T_{\mathrm{line}}/2)$. By inserting (21) and (22) into (19) and calculating the integral values, the ratio of $V_{\mathrm{m\_max}}/\mathrm{V_{m\_min}}$ is derived as

$$\begin{aligned} 2.33\mathrm{e}-3 \times V_{\mathrm{m\_min}^2} &= 0.46 \times 7.57\mathrm{e}-4 \times V_{\mathrm{m\_max}^2} \\ \frac{V_{\mathrm{m\_max}}}{V_{\mathrm{m\_min}}} &= 2.59. \end{aligned} \tag{23}$$

Thus, if the proposed LED driver is designed to have $E_{\mathrm{stored}}/E_{\mathrm{total}} = 0.23$ at the input voltage of 80 $\mathrm{V_{rms}}$, it can operate with an input voltage of up to 207 V_{rms}, where $E_{\mathrm{stored}}/E_{\mathrm{total}} = 0.5$.

C. Design of the Inverted Buck Converter for PFC and Energy Buffering

Based on these considerations, the design procedure for the inverted buck converter for PFC and energy buffering is presented. The target value of $V_{\mathrm{sto\_AVG}}$ at the input voltage of 80 $\mathrm{V_{rms}}$ is set as 50 V to satisfy $V_{\mathrm{sto\_min}} > V_{\mathrm{out}}$, where V_{out} is approximately 43 V at the LED current of 350 mA for an output power of 15 W in our design. Here, the input PF is 0.945 and $E_{\mathrm{stored}}/E_{\mathrm{total}}$ is 0.291 according to Fig. 9. When the range of $E_{\mathrm{stored}}/E_{\mathrm{total}}$ is reduced to 0.291–0.5, the ratio of $V_{\mathrm{m\_max}}/V_{\mathrm{m\_min}}$ is obtained as 2.08 by using (19)–(23), i.e., the allowed input voltage range is 80–166 $\mathrm{V_{rms}}$ when the target value of $V_{\mathrm{sto\_AVG}}$ is chosen as 50 V at the input voltage of 80 $\mathrm{V_{rms}}$. Thus, the proposed LED driver can handle the 110 $\mathrm{V_{rms}}$ line voltage variation ranging from 80 to 132 $\mathrm{V_{rms}}$, as plotted in Fig. 10 where the range of $E_{\mathrm{stored}}/E_{\mathrm{total}}$ is 0.291–0.437 and the PF is higher than 0.9.

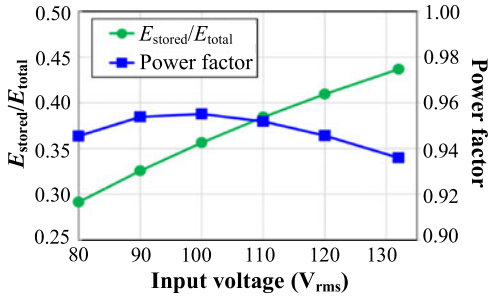

Fig. 10. Stored energy ratio $(E_{\mathrm{stored}}/E_{\mathrm{total}})$ and PF with respect to an input voltage ranging from 80 to 132 $\mathrm{V_{rms}}$.

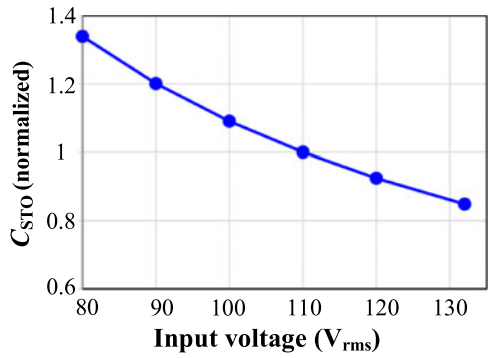

Fig. 11. Required size of C_{STO} with a constant Δv_{sto} with respect to an input voltage ranging from 80 to 132 $\mathrm{V_{rms}}$.

By rearranging (13), the storage capacitance is obtained as

$$C_{\mathrm{STO}} = \frac{E_{\mathrm{stored}}}{\Delta v_{\mathrm{sto}} \cdot V_{\mathrm{sto\_AVG}}}. \tag{24}$$

As plotted in Fig. 11, the worst case in terms of the size of C_{STO} is when the line voltage is at the minimum voltage of 80 $\mathrm{V_{rms}}$. This is because $V_{\mathrm{sto\_AVG}}$ increases faster than E_{stored} as the line voltage increases according to the data in Figs. 9 and 10. The estimated value of C_{STO} at the minimum line voltage of 80 $\mathrm{V_{rms}}$ is 33.9% higher than that of C_{STO} at the line voltage of 110 $\mathrm{V_{rms}}$. Moreover, when the input voltage is 80 $\mathrm{V_{rms}}$, $V_{\mathrm{sto\_AVG}}$ has its minimum value, and the allowed Δv_{sto} is reduced because $V_{\mathrm{sto\_min}} > V_{\mathrm{out}}$ must be satisfied. Thus, the required capacitance of C_{STO} is determined by the minimum input voltage of 80 $\mathrm{V_{rms}}$, as plotted in Fig. 12. Because the maximum allowable Δv_{sto} is 14 V when V_{out} is about 43 V, and the capacitance for C_{STO} calculated with (24) is 52.5 μF.

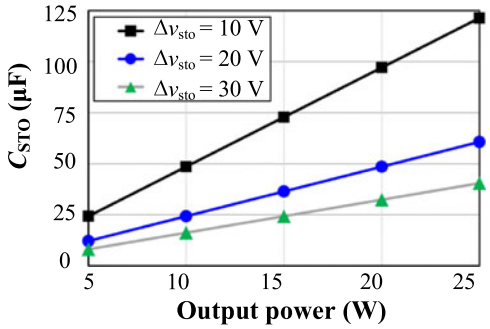

Fig. 12. Required capacitance for C_{STO} with respect to the output power, when $V_{\mathrm{sto\_AVG}}$ is 50 V and the input voltage is 80 V_{rms}.

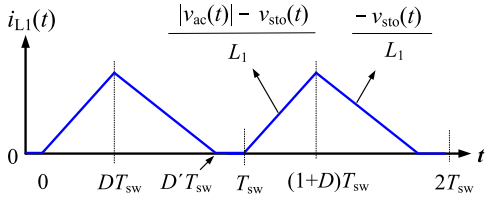

Fig. 13. Inductor current waveform of the buck PFC converter operating in a DCM.

According to Figs. 9 and 10, when the input voltage is 132 V_{rms}, $E_{\mathrm{stored}}/E_{\mathrm{total}}$ is 0.437 and the corresponding $V_{\mathrm{sto\_AVG}}$ is 118.3 V with Δv_{sto} of 8.8 V, i.e., the maximum voltage rating on C_{STO} is approximately 123 V. Therefore, for the design margin, we used a 68-μF 250-V film capacitor for C_{STO}. This can be replaced by a capacitor with a lower voltage rating (e.g., 160 V).

The buck PFC converter with no load operates in a DCM with a fixed duty cycle (D). Fig. 13 shows the waveform of the inductor current I_{L1} in the DCM where $D'T_{\mathrm{sw}} < T_{\mathrm{sw}}$. The boundary condition between the CCM and DCM operation is

$$\frac{|v_{\mathrm{ac}}(t)| - v_{\mathrm{sto}}(t)}{L_1} DT_{\mathrm{sw}} + \frac{-v_{\mathrm{sto}}(t)}{L_1}(1-D)T_{\mathrm{sw}} = 0 \quad (25)$$

where the duty cycle (D) is derived as

$$D = \frac{v_{\mathrm{sto}}(t)}{|v_{\mathrm{ac}}(t)|} \text{ (for the boundary condition)}$$

$$D < \frac{v_{\mathrm{sto}}(t)}{|v_{\mathrm{ac}}(t)|} \text{ (for the DCM)}. \quad (26)$$

In our design, the duty cycle (D) should be less than 0.32 to operate in a DCM. The value of the duty cycle (D) can be calculated by $D = \sqrt{2 \cdot a_1 \cdot L_1 \cdot f_{\mathrm{sw}}}$, derived from (18). The design parameter a_1 is obtained as 1.49e−3 when it is assumed that the efficiency is 100%. The switching frequency (f_{sw}) of the PFC converter is chosen as 1 MHz to reduce the inductance (L_1) that is selected as 22 μH. Because the proposed LED driver handles the relatively low power level, the frequency of 1 MHz is selected as a tradeoff**.** Consequently, the calculated value of D is 0.256 that satisfies the DCM operation condition of (26).

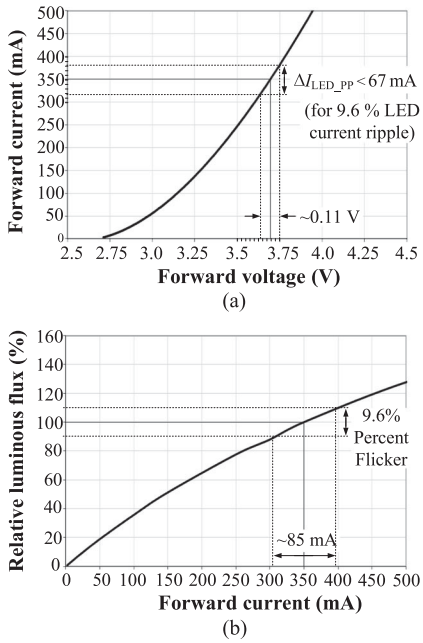

Fig. 14. Characteristics of the CREE XLamp MX-3 LED: (a) voltage versus current and (b) current versus relative luminous flux [45].

D. Design of the Inverted Buck Converter for LED Current Regulation

When deciding the design parameters of the inverted buck converter for regulating the LED current, the output voltage and current ripples should be considered for reducing output light flicker. As described in Section I, the Percent Flicker should be less than 9.6% at 120 Hz to be considered as low-risk levels, obtained by using (3). Fig. 14 shows the characteristics of the CREE XLamp MX-3 LED that is employed as the LED load in this study [45]. Although the LED current is 350 mA at 3.7 V at 25 ºC, and 14 series-connected LEDs were required for an output power of 15 W due to the forward voltage variation. Referring to Fig. 14(b), the peak-to-peak LED current ripple should be less than approximately 85 mA for a Percent Flicker below 9.6%. To provide a design margin, the limit of the peak-to-peak current ripple is set to 67 mA that is equivalent to an LED current ripple of 9.6%, when I_{LED} is 350 mA. Consequently, the corresponding peak-to-peak voltage ripple in Fig. 14(a) is around 0.11 V that is approximately 1.54 V for 14 LEDs.

The inverted buck converter for regulating the LED current operates in a CCM and its output voltage and inductor current waveforms are shown in Fig. 15. The output voltage ripple ($\Delta \mathrm{v_{out}}$) is expressed as

$$\Delta v_{\mathrm{out}} = \frac{1}{C_{\mathrm{OUT}}} \int_{t_1}^{t_2} i_{\mathrm{L2}}(t) - I_{\mathrm{LED}}\, dt \approx \frac{\Delta i_{\mathrm{L2}}}{8 \cdot C_{\mathrm{OUT}} \cdot f_{\mathrm{sw}}} \quad (27)$$

where the inductor current ripple (Δi_{L2}) is

$$\Delta i_{\mathrm{L2}} = \frac{V_{\mathrm{out}} \cdot (1 - D_{\mathrm{LED}})}{L_2 \cdot f_{\mathrm{sw}}} \quad (28)$$

wherein D_{LED} is the duty cycle of the low-side switch. By inserting (28) into (27), the output capacitance C_{OUT} is derived

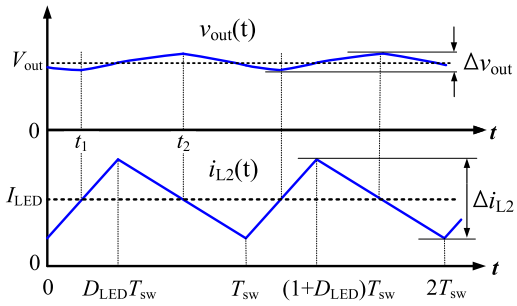

Fig. 15. Waveforms of the output voltage and the inductor current of the regulating converter operating in a CCM.

as

$$C_{\mathrm{OUT}} = \frac{V_{\mathrm{out}} \cdot (1 - D_{\mathrm{LED}})}{8 \cdot \Delta v_{\mathrm{out}} \cdot L_2 \cdot f_{\mathrm{sw}^2}}. \tag{29}$$

By using the CCM operating condition $(2 \times I_{\mathrm{LED}} > \Delta i_{\mathrm{L2}})$, the range of the inductance L_2 is derived as

$$L_2 > \frac{V_{\mathrm{out}} \cdot (1 - D_{\mathrm{LED}})}{2 \cdot I_{\mathrm{LED}} \cdot f_{\mathrm{sw}}}. \tag{30}$$

As the input voltage level of the regulating converter varies according to time, the duty cycle (D_{LED}) is controlled by the feedback loop to deliver constant currents to the LED load. Consequently, the inductor current ripple (Δi_{L2}) and the output voltage ripple $(\Delta v_{\mathrm{out}})$ vary with the input voltage level. According to (27) and (28), the largest values of Δi_{L2} and Δv_{out} is obtained when D_{LED} has a minimum value, i.e., the ac-input voltage has its peak value. Here, the minimum value of D_{LED} is obtained as $V_{\mathrm{out}}/V_{\mathrm{m}} = 0.23$, when V_{out} is approximately 43 V and the input voltage is 132 V_{rms}; the switching frequency (f_{sw}) is selected as 1 MHz to reduce the inductance (L_2). For the CCM operation, the inductance (L_2) obtained using (30) should be higher than 47.3 μH. By selecting a value of 68 μH as L_2, the required output capacitance C_{OUT} obtained using (29) is 0.04 μF, when the output voltage ripple $(\Delta v_{\mathrm{out}})$ is 1.32 V for an LED current ripple of 9.6%. For the design margin, the output capacitance C_{OUT} is selected as 0.47 μF.

IV. Experimental Results

A prototype of the proposed LED driver has been implemented using discrete passive components, power transistors, and an on-chip controller IC fabricated in a 0.35-μm CMOS process. Fig. 16 shows the photograph of the prototype board and its components are listed in Table I. The photograph of the controller IC is shown in Fig. 17 and its characteristics are summarized in Table II. The controller IC consumes 50 mW from a 5-V dc power supply. The prototype LED driver is powered by an ac power supply (Kikusui, PCR500M) and tested at the input voltage of 80–132 V_{rms}. A laptop computer is used to configure the programmable parameters in the digital control logic through an I^2C interface. The voltages and currents are measured using an oscilloscope (Tektronix, DPO5104); the power and the PF are measured using a power meter (Voltech, PM6000).

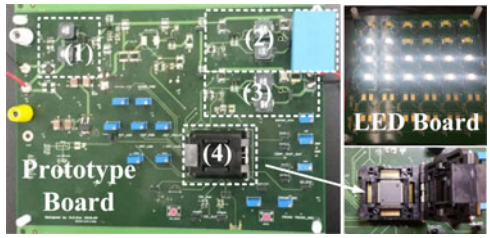

Fig. 16. Prototype board of the proposed LED driver: (1) full-bridge rectifier and EMI filter, (2) inverted buck converter for the PFC and energy buffering, (3) inverted buck converter for the LED current regulation, and (4) prototype controller IC mounted on a socket.

TABLE I
List of Components Used in the Prototype LED Driver

Component	Description	Part number
LEDs	3.7 V, 0.35 A	MX3AWT-A1
L_1	22 μH, 5.3 A	7447709220
L_2	68 μH, 3.2 A	7447709680
L_{F}	100 μH, 2.5 A	7447709101
C_{OUT}	0.47 μF, 250 V, ceramic	GRM55DR72E474KW01L
C_{STO}	68 μF, 250 V, film	B32526R3686K
C_{F}	15 nF, 250 V, ceramic	C2012X7R2E153K125AA
R_{S}	Sensing resistor, 0.5 Ω	CSR1206FKR500
D_1–D_3	Schottcky, 200 V, 2 A	STPS2200UF
Rectifier	Full bridge, 400 V, 1 A	DSRHD04-13
M_1, M_2	MOSFET N-CH, 200 V, 7 A	BSZ22DN20NS3 G
LDO	3.3 V, 0.3 A	TPS7A6550QKVURQ1

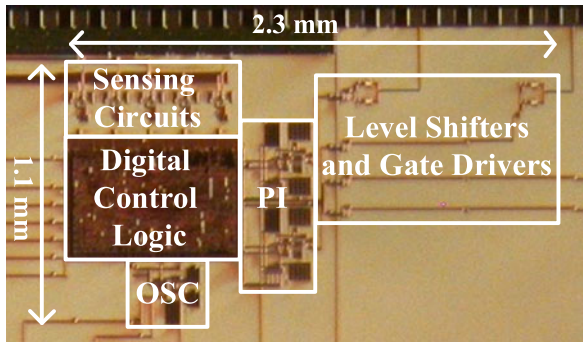

Fig. 17. Photograph of the implemented controller IC.

Fig. 18 shows the measured waveforms of the critical nodes in the proposed LED driver, when delivering 15 W to the LEDs. Fig. 18 (a) depicts the ac-input voltage and current (v_{ac} and i_{in}); the storage capacitor voltage (v_{sto}) and the positive and negative terminal voltages (v_a and v_b) of v_{sto}. According to the two alternating operating modes, v_{sto} settles to an average voltage of 86.8 V with a ripple voltage of 10.5 V. The measured minimum $V_{\mathrm{sto\_AVG}}$ for PF > 0.9 is 56.5 V that is very close to the theoretical limit of 55 V when the input voltage is 110 V_{rms}, as described in Section III. According to [46], IEC 61000-3-2 requires that the third- and fifth-harmonic currents shall not exceed 86% and 61% of the fundamental current, respectively, for the lighting equipment with an input power lower than or equal to 25 W. Because the measured third and fifth harmonics of

TABLE II
CHARACTERISTICS OF THE PROTOTYPE CONTROLLER IC

Process technology	0.35-μm CMOS
Supply voltage	3.3 V (Core), 5 V (IO)
Oscillator frequency range	6.4–64 MHz
Output switching frequency (f_{sw})	0.1–1 MHz
Power consumption	33 mW (3.3 V)
(at $f_{sw} = 1$MHz)	17 mW (5 V)
Active area	2.3 x 1.1 mm^2

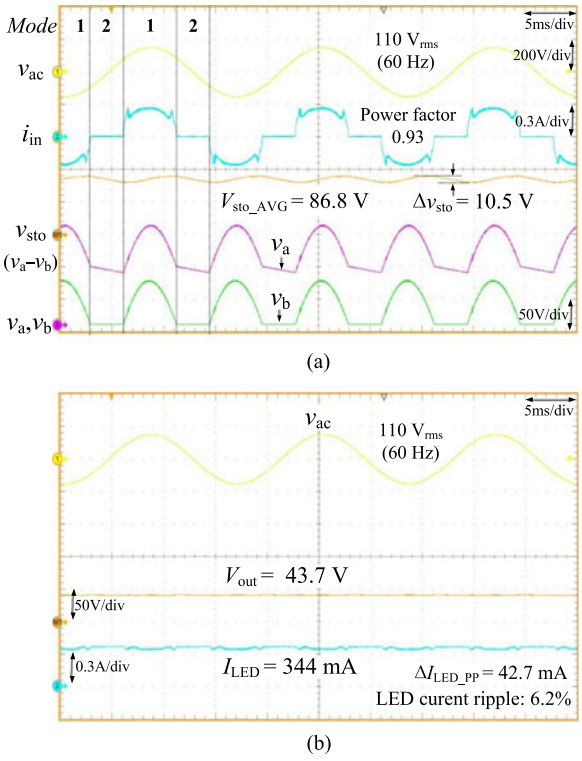

Fig. 18. Measured waveforms of the proposed ac–dc LED driver with a two-parallel inverted buck topology: (a) the ac input voltage and current ($v_{\rm ac}$ and $i_{\rm in}$); the storage capacitor voltage ($v_{\rm sto}$) and its positive and negative terminal voltages (v_a and v_b), (b) output voltage ($v_{\rm out}$) and the LED current ($i_{\rm LED}$).

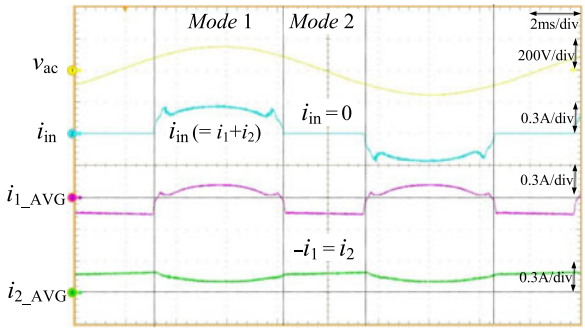

Fig. 19. Measured waveforms of the ac input voltage and current ($v_{\rm ac}$ and $i_{\rm in}$), and the currents flowing into the respective inverted buck converters, (i_1 and i_2).

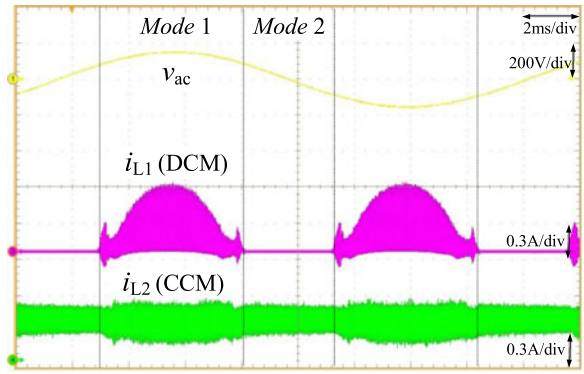

Fig. 20. Measured waveforms of the ac input voltage and the currents flowing through the inductors ($i_{\rm L1}$: PFC converter, $i_{\rm L2}$: regulating converter).

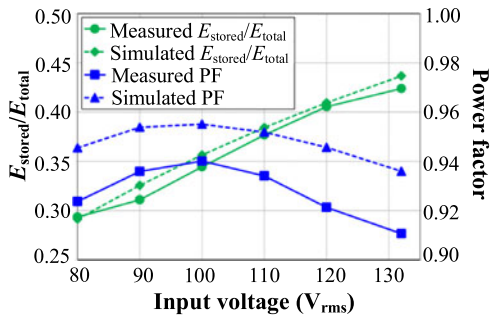

Fig. 21. Measured PF and stored energy ratio ($E_{\rm stored}/E_{\rm total}$) of the proposed LED driver.

the input current ($i_{\rm in}$) are 21.7% and 17.0% of the fundamental current, respectively, our solution is compliant with some residential LED bulbs and office LED tubes of power less than 25 W. Fig. 18 (b) shows the output voltage and the LED current. Regardless of the operating modes, $I_{\rm LED}$ is regulated to 344 mA and the peak-to-peak current ripple ($\Delta I_{\rm LED\_PP}$) is 42.7 mA that is equivalent to an LED current ripple of 6.2%.

Fig. 19 shows the measured waveforms of the ac-input voltage and current ($v_{\rm ac}$ and $i_{\rm in}$) with a PF of 0.93 and the currents flowing into each inverted buck converter (i_1 and i_2). These waveforms demonstrate that the two converters operating separately, regulate the LED current, and perform the PFC function in *Mode* 1; the stored energy in the storage capacitor is delivered to the LEDs without drawing current from the ac input source in *Mode* 2. Fig. 20 shows that the waveforms of the inductor currents ($i_{\rm L1}$ and $i_{\rm L2}$) indicate the DCM operation of the PFC converter and the CCM operation of the regulating converter, respectively.

Fig. 21 plots the measured PF and stored energy ratio ($E_{\rm stored}/E_{\rm total}$) of the prototype LED driver with an input voltage ranging from 80 to 132 $V_{\rm rms}$, where the peak PF is 0.94. Although the PF is slightly reduced, the graphs of the measured PF and $E_{\rm stored}/E_{\rm total}$ have similar shapes compared to the simulated data in Fig. 10. Fig. 22 plots the measured power efficiency, where the peak efficiency is 85.4%. Fig. 23 plots the 120-Hz LED current ripple of the proposed LED driver, where the peak LED current ripple is 6.5%, equivalent to a Percent

TABLE III
PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART AC–DC LED DRIVERS

Topology	ECCE 2015 [15] Cascaded boost PFC + dc–dc LLC	TPEL 2015 [23] Flyback with harmonic current injection	TPEL 2016 [25] Boost with harmonic current injection	TPEL 2014 [28] Flyback with a parallel RCC	JESTPE 2015[32] Buck-boost with a series RCC	This work Two-parallel inverted buck
Input voltage	90–264 V_{rms}	120 V_{rms}	90–265 V_{rms}	90–264 V_{rms}	110–230 V_{rms}	80–132 V_{rms}
Output voltage	43 V	35 V	420 V	48 V	50 V	43.7 V
Max. output power	150.1 W	20 W	20 W	33.6 W	10 W	15.3 W
Switching frequency	140 kHz	30 KHz	120 kHz	140 kHz	N/A	1 MHz
Inductor	350 μH, 33, 16.5 μH	1.2 mH	1.1 mH	30 μH, 1.2 mH	0.99 mH	22 μH, 68 μH
Output capacitor	10 μF (N/A)	500 μF (N/A)	8.8 μF (film)	0.47 μF (N/A)	4.7 μF, 60 μF (ceramic)	0.47 μF (ceramic)
Storage capacitor	30 μF (N/A)	No use	No use	4.7 μF (N/A)	20 μF (ceramic)	68 μF (film)
PF	0.97–0.99	> 0.9	0.91	0.99	0.9–0.99	0.91–0.94
Peak efficiency	90.4%	N/A	N/A	87%	87%	85.4%
LED current ripple (120 Hz)	18.8%	N/A	10%	8%	5.5%	6.5%
Percent Flicker(1)	N/A	38%	N/A	8.7% (est.)	4.9% (est.)	5.5% (est.)

(1) Estimated values are obtained by using the characteristic graph (forward current versus relative luminous flux) in each LED datasheet.

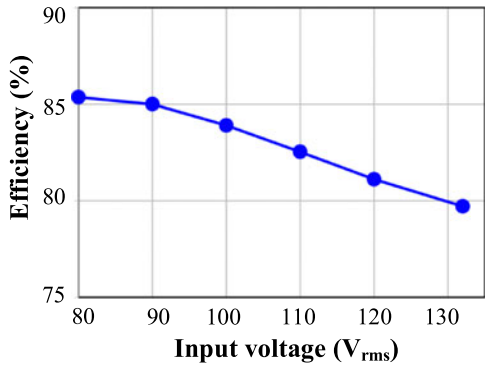

Fig. 22. Measured power efficiency of the proposed LED driver.

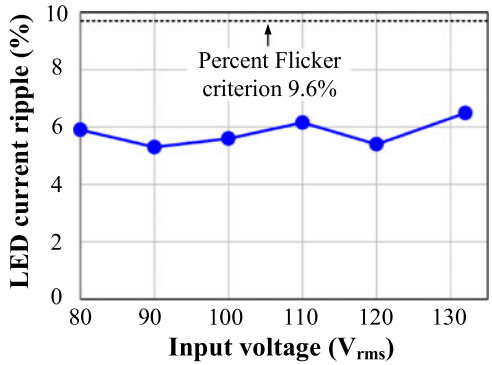

Fig. 23. Measured 120-Hz LED current ripple of the proposed LED driver.

Flicker less than 9.6%. Table III summarizes the performance of the proposed prototype LED driver in comparison with recent works. Because the required size of $C_{\rm STO}$ depends on the input voltage range of the proposed LED driver, a relatively larger capacitance of 68 μF is employed for $C_{\rm STO}$ to handle the line voltage variations ranging from 80 to 132 $V_{\rm rms}$. However, if we reduce the design margin of the input voltage range, the size of $C_{\rm STO}$ can be reduced. For example, $C_{\rm STO}$ can be reduced to 20 μF when the input voltage range is 100–132 $V_{\rm rms}$.

V. CONCLUSION

An ac–dc LED driver that can drive the LEDs with the low-risk levels of flicker has been presented in this study. A two-parallel inverted buck topology is proposed to achieve a high PF and a low LED current ripple. The PFC converter buffers the twice-the-line-frequency energy, while simultaneously performing the PFC function and the regulating converter provides a constant current to the LEDs. Further, the proposed architecture reduces the voltage stress and size of the storage capacitor; thereby, a film capacitor can be used instead of the limited lifetime electrolytic capacitor. The relationship between the input PF and the stored energy ratio in accordance with the storage capacitor voltage, to achieve a high PF and efficiency, is discussed in this study. A 15-W prototype LED driver has been implemented and tested to validate the design of the proposed ac–dc LED driver, exhibiting a PF of 0.94 and a power efficiency of 85.4%.

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