Active Current Source IGBT Gate Drive With Closed-Loop di/dt and dv/dt Control

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***Abstract*—This paper proposes an active current source gate drive (ACSD) method based on voltage controlled current source(VCCS) feedback control strategy for high-power IGBTs. Unlike the common voltage source gate drive, the proposed ACSD method provides constant drive current to charge and discharge an IGBT. With a large gate drive current, high switching speed and low switching losses can be achieved in a power converter. However, a high-current/voltage overshoot occurs. To solve this problem, a feedback current proportional to the di/dt or dv/dt signal is generated to the IGBT gate. Thus, direct control of the net gate drive current is produced. Then, the current/voltage overshoot is controlled with little sacrifice in switching time, and the switching losses are lower than that with the conventional gate drive method operating simply by gate resistance switchover. The operation principle and circuit implementation of the proposed ACSD method are presented. The experimental results from a 1200 V/800 A IGBT module verify the performance of the proposed method.**

***Index Terms*—Active current source gate drive (ACSD), current overshoot, IGBT, switching losses, voltage overshoot.**

I. Introduction

INSULATED gate bipolar transistors (IGBTs) are widely employed in high-power converters as the dominant switching devices. Fast switching speed, low electrical stresses, low power losses, and high reliability requirements for IGBT devices stand out in industrial applications especially in extreme working conditions. Optimized control on IGBT switching transients helps to meet these requirements and make maximum utilization of IGBTs. And much IGBT gate drive research has been performed to control IGBT switching transients [1]–[35].

The conventional gate drive (CGD) method controls IGBT switching transients by changing the gate drive resistance or voltage [1]–[5]. With high gate resistance or low gate voltage, the IGBT switching speed slows down, whence the collector current overshoot at turn-on decreases. However, this method is not effective to control the voltage overshoot of the latest developed trench IGBT devices at turn-off as mentioned in [6] and [32] because of the carrier streaming effect [7]. It also results in high switching losses and turn-on/off delay time.

To overcome the drawbacks of the CGD method, many active gate drive (AGD) methods have been proposed [8]–[35], which can be roughly divided into four types as follows.

The first type is a multistep method that changes the gate resistance or voltage at different stages during switching transients [8]–[15]. To regulate the current/voltage overshoot, during the current rising or falling stage, the gate resistance is switched to a high value [8] or the gate voltage is dropped to a low value [9]–[11]. In the literature [12]–[14], the Miller plateau stage is detected, then extra current is generated to control the gate current. This decreases the turn-on losses and the turn-off delay time. A detection circuit is always necessary to detect these stages in a switching transient, which is sensitive to noise. The increased control complexity and related cost are also challenges in practical applications [8], [14].

The second type is an active voltage clamping method [16]–[19]. Once the collector–emitter voltage at turn-off exceeds a clamping voltage, extra current through the clamping device will be injected to the gate to regulate the gate drive voltage. This controls the collector–emitter voltage overshoot. However, such methods suffer from high power losses of the clamping devices and the overshoot current caused by the reverse recovery of the freewheeling diode at turn-on is not controlled.

The third type is a direct voltage trajectory control method [20]–[25]. Either a collector–emitter voltage or gate–emitter voltage reference is used to control the switch voltage trajectory. In [20]–[23], the collector–emitter voltage is sensed by a passive network and then compared with the preset reference to generate an error signal, which is regulated by a fast operational amplifier to drive the gate. This controls the collector–emitter voltage gradient and overshoot. The reference generation circuits are complex and need to be adjusted for various IGBT operation conditions. And the turn-on transient is not controlled. Grbovic *et al.* [24], [25] present a feed-forward control method with a simple circuit to control the gate-emitter voltage trajectory. No active or passive feedback and current measurement circuits are needed, which makes the gate drive robust and reliable. This method is effective in limiting the current overshoot at turn-on, but the turn-on delay time remains high due to low gate voltage rising gradient. And the turn-off transient is not controlled.

The last type is a feedback control method [26]–[35]. Unlike the third type methods, the fourth type methods only detect

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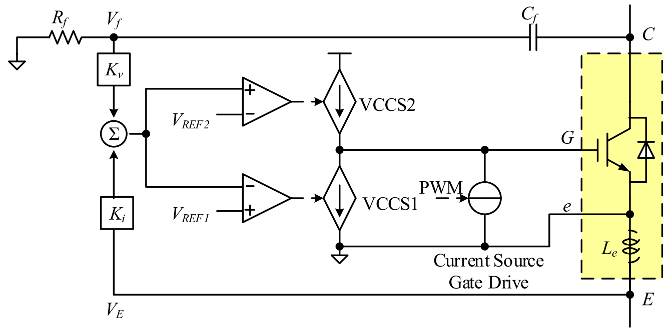

Fig. 1. Circuit diagram of the proposed ACSD method.

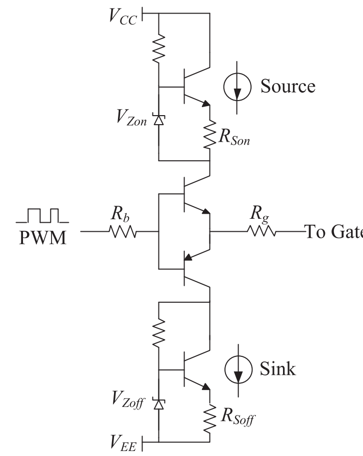

Fig. 2. Circuit implementation of the constant current source.

the collector current or collector–emitter voltage rising/falling stages rather than track the collector–emitter voltage waveforms throughout the whole switching transients. Dang, Kuhn, and Mertens [27] present a digital control method to adjust the gate drive current by sensing the IGBT current and voltage waveforms to control $\mathrm{di/dt}$ or $\mathrm{dv/dt}$. Closed loop gate drive voltage control methods based on $\mathrm{di/dt}$ or $\mathrm{dv/dt}$ feedback have been proposed in references [29]–[32]. These methods have full $\mathrm{di/dt}$ or $\mathrm{dv/dt}$ control and achieve small turn-on/off delay time. But high-speed operational amplifiers or A/D and D/A circuits are usually required, which are sensitive to electromagnetic field noise produced in the high-power converters. Moreover, with the development of the IGBT manufacture technology, the switching speed is continuously increasing, bringing additional challenges to the control loop design and delay compensation.

The active IGBT gate drive (AGD) methods considered are mainly based on voltage source, and some issues are still not well solved, such as high switching losses, complex circuit implementation (also high cost), inability to control overshoot at turn-on or turn-off transient. To solve the aforementioned issues, in this paper, an active current source gate drive (ACSD) method for high-power IGBTs is proposed. A linear current source circuit achieves constant gate drive current and fast switching speed, and the $\mathrm{di/dt}$ or $\mathrm{dv/dt}$ signal is sensed to regulate the gate drive current via a fast voltage controlled current source (VCCS). Compared with the previous works on IGBT gate drive, the proposed method can effectively control switching stresses at both turn-on and turn-off, with little sacrifice in switching time, and the switching losses are lower. Furthermore, the feedback response speed is fast, resulting in excellent control effectiveness. The detailed operation principle and circuit implementation will be discussed in the next sections. Experimental results based on the double pulse test verify the effectiveness of the proposed method.

II. Operation Principle of the Proposed ACSD Method

In this section, the circuit implementation and operation principle of the proposed ACSD method will be presented. The ACSD circuit basically has three parts as shown in Fig. 1:

1) a constant current source to supply large gate drive current based on PWM signal;
2) simple circuits to detect the $\mathrm{di/dt}$ and $\mathrm{dv/dt}$ signal; and
3) voltage controlled current source circuits (VCCS1 and VCCS2) to generate feedback current to the gate terminal.

No digital devices are used in the detection circuits and the delay of the VCCS circuits is small. Therefore, the dynamic response speed is fast and no calibration or adjustment circuit is required for the $\mathrm{di/dt}$ and $\mathrm{dv/dt}$ signal detection circuits.

The $\mathrm{di/dt}$ signal is detected across the parasitic inductance between the power emitter and the Kelvin gate drive emitter of the IGBT module, which is L_e in Fig. 1. The detected voltage is

$$V_E = -L_e * \mathrm{di/dt}. \tag{1}$$

The $\mathrm{dv/dt}$ signal V_f is detected by a high-voltage ceramic capacitor C_f and a resistor R_f. The voltage signal V_f input to the voltage controlled current source (VCCS2) can be calculated as

$$V_f = R_f * C_f * \mathrm{dv/dt}. \tag{2}$$

When $\mathrm{di/dt}$ or $\mathrm{dv/dt}$ is detected, VCCS1/VCCS2 generates extra current to the IGBT gate terminal, which adjusts the net gate drive current and then $\mathrm{di/dt}$ or $\mathrm{dv/dt}$ is controlled. VCCS1 and VCCS2 operate during turn-on and turn-off, respectively, as shown in Fig. 1. With the $\mathrm{di/dt}$ and $\mathrm{dv/dt}$ feedback signals, the collector current slew rate $\mathrm{di/dt}$ is controlled. As a result, the reverse recovery current of the freewheeling diode and the collector–emitter voltage overshoot are regulated. The detailed operation principle of the proposed ACSD method follows.

A. Constant Current Source

The proposed gate drive adopts the constant current source shown in Fig. 2 to supply stable gate drive current I_{gon} or I_{goff}, calculated as follows:

$$I_g = \frac{V_Z - V_{\mathrm{BE}}}{R_S} \tag{3}$$

where V_Z is the Zener diode breakdown voltage V_{Zon} and V_{Zoff}, and V_{BE} is the BJT base–emitter voltage drop. R_{Son} and R_{Soff} are used to regulate the gate drive current at turn-on and turn-off, respectively.

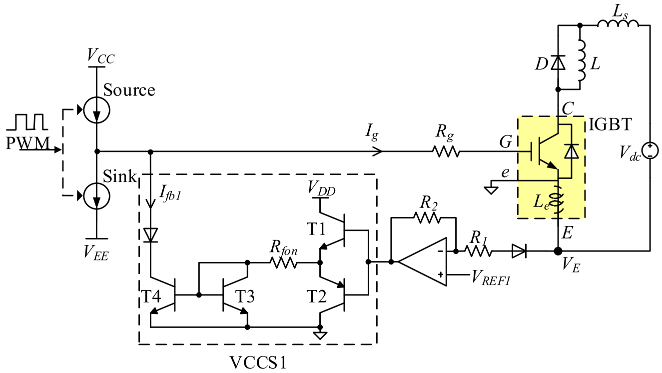

Fig. 3. Circuit diagram of the proposed feedback control at turn-on.

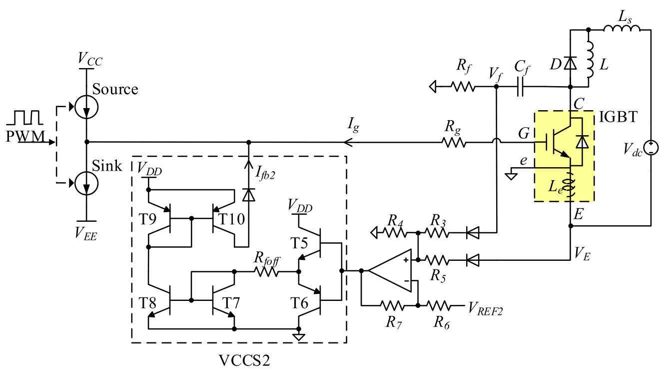

Fig. 4. Circuit diagram of the proposed feedback control at turn-off.

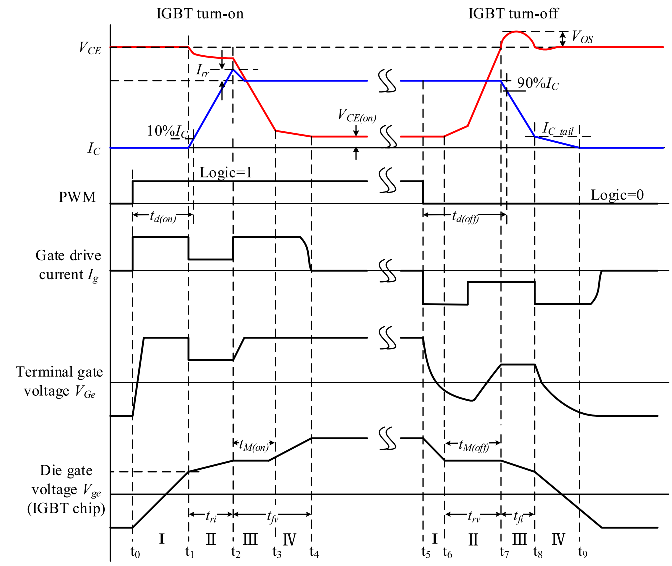

Fig. 5. Theoretical IGBT switching transient waveforms with the proposed ACSD method.

In the CGD method with a voltage source, the gate drive current drops quickly as the gate terminal voltage rises. This prolongs the switching time and increases the switching losses. However, with the proposed current source gate drive method, the gate drive current is almost constant during the whole switching transients, significantly reducing the switching time and losses [36].

To ensure a stable gate drive current, the supply voltage for the current source should be higher than the steady-state gate drive voltage clamped by the amplitude of the PWM signal, which is 15 V for turn-on and -9 V for turn-off. Here, 24 and -10 V are used for $V_{\rm CC}$ and $V_{\rm EE}$ shown in Fig. 2, respectively.

B. Feedback Control at Turn-On

Although effective in reducing the turn-on time and switching losses, a large gate drive current can cause a high collector current overshoot. To limit this overshoot, a VCCS feedback control strategy is proposed. This strategy will be analyzed for an IGBT in a switching leg with inductive load. The circuit diagram and theoretical waveforms of the proposed feedback control strategy at turn-on are shown in Figs. 3 and 5, respectively. The feedback circuit is composed of a voltage amplifier and a voltage controlled current source (VCCS1). The voltage amplifier compares the ${\rm d}i/{\rm d}t$ feedback signal to a reference $V_{\rm REF1}$ and generates an error signal, which is fed to a buffer stage consisting of T1 and T2 to drive a current mirror, extracting a feedback current from the gate. Then, the gate drive current is regulated and the collector current rising gradient *di/dt* is limited. The value of $V_{\rm REF1}$ is dependent on the working conditions of IGBTs. For example, when the operating voltage of an IGBT device is much lower than its breakdown voltage, high ${\rm d}i/{\rm d}t$ and related high current overshoot will not damage the IGBT device. Then, $V_{\rm REF1}$ can be large and the VCCS1 does not work during switching transients. For simplicity, the reference voltage $V_{\rm REF1}$ is set to zero. Since VCCS1 is a current mirror, it has fast response speed, which is very critical to achieve good control performance. From engineering point of view, the response time of the feedback circuits should be less than one-tenth of the collector current rising/falling time. The response time of VCCS1 and VCCS2 is around 10 to 20 ns, quite small compared with the current rising/falling time in hundreds nanoseconds. The test results are given in Figs. 8 and 9. In Fig. 3, $V_{\rm DD}$ for VCCS1 is 18 V and the gate resistance R_g is very small for the current source gate drive, typically 0.1 Ω. In order to facilitate the analysis and design, the turn-on transient can be divided into four stages as shown in Fig. 5.

Stage I $[\mathbf{t_0} - \mathbf{t_1}]$: The PWM signal goes to high at t_0 to turn on the IGBT. Then, a constant gate drive current $I_{\rm gon}$ is generated to charge the gate–emitter capacitor $C_{\rm ge}$ and the gate terminal voltage $V_{\rm Ge}$ increases. Large $I_{\rm gon}$ results in short turn-on delay time. The actual gate voltage at IGBT chip side ($V_{\rm ge}$) is different from the gate terminal voltage because of the internal parasitic parameters, such as parasitic inductance and internal gate resistance.

Stage II $[\mathbf{t_1} - \mathbf{t_2}]$: When the die gate voltage $V_{\rm ge}$ reaches the turn-on threshold voltage $V_{\rm TH}$ at t_1, the IGBT turns on and the collector current I_C begins to rise. The ${\rm d}i/{\rm d}t$ signal is sensed across the parasitic inductance existing between the signal emitter and the power emitter of the IGBT module as given in (1). This signal is compared with a reference $V_{\rm REF1}$

and the error signal is applied to a current mirror to extract extra current from the gate terminal as shown in Fig. 3. Then, the net gate drive current is regulated. The feedback current expression is given as

$$\begin{cases} I_{\mathrm{fb1}} = \frac{V_E * K_{i1} - V_{\mathrm{BE,T1}} - V_{\mathrm{BE,T3}}}{R_{\mathrm{fon}}} \\ K_{i1} = -R_2/R_1 \end{cases} \tag{4}$$

where $V_{\mathrm{BE,T1}}$ and $V_{\mathrm{BE,T3}}$ are the base–emitter voltage drops of BJTs T1 and T3, respectively, which are about 0.7 V, quite small compared with $V_E * K_{i1}$. So (4) can be simplified to

$$I_{\mathrm{fb1}} \approx \frac{V_E * K_{i1}}{R_{\mathrm{fon}}}. \tag{5}$$

When the controlled collector current slope is steady, the relationship between $\mathrm{di/dt}$ and the parameters setup at turn-on can be expressed as

$$\begin{cases} \frac{\mathrm{di}_C}{\mathrm{dt}}|_{\mathrm{on}} = g_m * \frac{\mathrm{dV_{ge}}}{\mathrm{dt}} \\ I_{\mathrm{gon}} - I_{\mathrm{fb1}} = C_{\mathrm{ies}} * \frac{\mathrm{dV_{ge}}}{\mathrm{dt}} \end{cases} \tag{6}$$

where g_m is IGBT transconductance and C_{ies} is the input capacitance. From (6), we get

$$\frac{\mathrm{di}_C}{\mathrm{dt}}|_{\mathrm{on}} = \frac{g_m}{C_{\mathrm{ies}}} * (I_{\mathrm{gon}} - I_{\mathrm{fb1}}). \tag{7}$$

From (1) and (5), we get

$$I_{fb1} = \frac{L_e * (-K_{i1})}{R_{fon}} * \frac{di_C}{dt}|_{\mathrm{on}}. \tag{8}$$

From (7) and (8), the $\mathrm{di}_C/\mathrm{dt}$ can be expressed as the following equation:

$$\frac{\mathrm{di}_C}{\mathrm{dt}}|_{\mathrm{on}} = \frac{I_{\mathrm{gon}}}{\frac{C_{\mathrm{ies}}}{g_m} + \frac{L_e*(-K_{i1})}{R_{\mathrm{fon}}}}. \tag{9}$$

In an IGBT, $C_{\mathrm{ies}}/\mathrm{g_m}$ is usually far smaller than $L_e*(-K_{i1})/\mathrm{R_{fon}}$, then $\mathrm{di/dt}$ is mainly determined by the gate drive current I_{gon} and the feedback resistance R_{fon}, thus $\mathrm{di/dt}$ can be effectively controlled by varying R_{fon}. The feedback parameters can be designed referring to (9). The power loss during this current rising stage is defined as E_{ri}, which is related to the current rising slew rate.

Stage III $[\mathbf{t_2} - \mathbf{t_3}]$: When the current rising stage is finished at t_2, V_{CE} begins to decrease. During this stage, $\mathrm{di/dt}$ is small and does not affect the steady-state gate drive current, so a fast switching speed can be achieved. The power loss during this voltage falling stage is defined as E_{fv}.

Stage IV $[\mathbf{t_3} - \mathbf{t_4}]$: When V_{CE} falls to a small value, the gate–collector capacitance C_{gc} increases quickly. V_{ge} rises continuously to its steady-state value and V_{CE} decreases to its steady state on-state voltage. The power loss during this voltage tail stage is defined as E_{vtail}.

C. Feedback Control at Turn-Off

Similarly, a feedback control circuit limits the collector–emitter voltage overshoot at turn-off. The circuit diagram is shown in Fig. 4, and the theoretical waveforms are shown in Fig. 5. The design of V_{REF2} is similar to V_{REF1} discussed in Section IV-B. It is set to zero in this work for simplicity. The feedback control circuit at turn-off is similar to that at turn-on. The main difference is that the $\mathrm{dv/dt}$ signal is detected to control V_{CE} rising gradient at turn-off. With the development of IGBT manufacture technology, the turn-off speed is getting faster and faster without compromising the on-state voltage. And high $\mathrm{di/dt}$ results in high collector–emitter voltage overshoot caused by the parasitic inductance in the circuit. Furthermore, due to inevitable parasitic parameters existing within IGBT devices such as parasitic inductance and internal gate resistance, there is certain delay time between the gate drive signal and the actual gate voltage applied to the IGBT chip, which is comparable to the current falling time during the turn-off transient in hundreds nanoseconds. Therefore, it is challenging to control $\mathrm{di/dt}$ at turn-off by $\mathrm{di/dt}$ feedback control alone. Thus, leading phase compensation is usually required for stable operation. Additionally, low $\mathrm{dv/dt}$ guarantees the MOSFET current of the IGBT keeping flowing, which can be controlled by gate drive circuit [7]. Therefore, the $\mathrm{dv/dt}$ signal feedback control is necessary to effectively control $\mathrm{di/dt}$ at turn-off.

When the $\mathrm{dv/dt}$ or $\mathrm{di/dt}$ signal is detected, an extra current is injected into the gate, so that the net gate drive current can be adjusted. Both the collector–emitter voltage slope and the collector current slope are controlled with the proposed feedback control method. The turn-off transient is divided into four stages to explain the operation principle of the proposed feedback control strategy.

Stage I $[\mathbf{t_5} - \mathbf{t_6}]$: The PWM signal goes to low at t_5 to turn off the IGBT under test. A constant gate drive current I_{goff} discharges the gate–emitter capacitance C_{ge} and the gate terminal voltage decreases. During this stage, the IGBT is still on, and the power losses are mainly conduction losses. The on-state voltage slightly increases due to the decreased gate drive voltage.

Stage II $[\mathbf{t_6} - \mathbf{t_7}]$: When V_{ge} decreases to the Miller plateau, the collector–emitter voltage V_{CE} begins to increase. As the gate-collector capacitance C_{gc} is nonlinearly, V_{CE} increases slowly initially and then increases quickly when C_{gc} decreases to a small value. The power loss during this voltage rising stage is defined as E_{rv}.

When the $\mathrm{dv/dt}$ signal V_f is detected, VCCS2 injects extra feedback current into the gate to reduce the net gate drive current. The feedback current I_{fb2} can be calculated as follows:

$$\begin{cases} I_{\mathrm{fb2}} = \frac{V_f * K_v - V_{\mathrm{BE,T5}} - V_{\mathrm{BE,T7}}}{R_{\mathrm{foff}}} \approx \frac{V_f * K_v}{R_{\mathrm{foff}}} \\ K_v = \frac{R_6 + R_7}{R_6} \cdot \frac{R_4}{R_3 + R_4} \end{cases} \tag{10}$$

where $V_{\mathrm{BE,T5}}$ and $V_{\mathrm{BE,T7}}$ are the base–emitter voltage drops of T5 and T7, respectively, which being much smaller than $V_f * \mathrm{K_v}$, are neglected.

According to (2) and (10), the increment of $\mathrm{dv/dt}$ leads to a larger I_{fb2}, which will decrease I_g as shown in Fig. 4. A smaller I_g can reduce $\mathrm{dv/dt}$, thus *dv/dt* is limited.

Stage III $[\mathbf{t_7} - \mathbf{t_8}]$: Once V_{CE} reaches the dc bus voltage, I_C starts to decrease. The collector current falling slope $\mathrm{di/dt}$ can be sensed by the parasitic inductance between the signal emitter and the power emitter of the IGBT module. The feedback current I_{fb3} to the gate terminal generated by VCCS2 is calculated as follows:

$$\begin{cases} I_{\text{fb3}} = \dfrac{V_E * K_{i2} - V_{\text{BE,T5}} - V_{\text{BE,T7}}}{R_{\text{foff}}} \approx \dfrac{V_E * K_{i2}}{R_{\text{foff}}} \\ K_{i2} = \dfrac{R_6 + R_7}{R_6} \cdot \dfrac{R_4}{R_5 + R_4} \end{cases}. \quad (11)$$

I_{fb3} is proportional to $\mathrm{di/dt}$, and similar to the Stage II, it limits $\mathrm{di/dt}$.

The calculation of $\mathrm{di/dt}$ at turn-off is similar to that at turn-on, namely

$$\frac{\mathrm{d}i_C}{\mathrm{dt}}\Big|_{\text{off}} = \frac{I_{\text{goff}}}{\frac{C_{\text{ies}}}{g_m} + \frac{L_e * K_{i2}}{R_{\text{foff}}}}. \quad (12)$$

According to (12), $\mathrm{di/dt}$ can be controlled by R_{foff}. The power loss during this current falling stage is defined as E_{fi}.

Stage IV [$\mathbf{t_8 - t_9}$]: This is the IGBT tail current stage. V_{ge} drops to the steady off-state voltage and I_C decreases gradually to zero. The power loss during this tail current stage is defined as E_{itail}. The tail current is mainly determined by the IGBT device minority carrier properties, which are usually not affected by the gate drive signal at this stage.

In the proposed ACSD method, VCCS1 is used to control the $\mathrm{di/dt}$ at turn-on transient, and VCCS2 is used to control the $\mathrm{di/dt}$ at turn-off transient. In a phase-leg configuration, when the lower IGBT turns on, the upper switch will have a negative $\mathrm{di/dt}$ signal and a positive $\mathrm{dv/dt}$ signal. Then, the VCCS1 of the upper IGBT gate driver will extract a current from the gate, and the VCCS2 of the upper IGBT gate driver will inject a current into the gate. The upper IGBT gate voltage may fluctuate due to this cross-talk interference. There is similar cross-talk interference when the lower IGBT turns off. To prevent such cross-talk interference, VCCS1 and VCCS2 of the lower IGBT gate driver are only enabled when the gate drive signal becomes high, and they are disabled when the gate drive signal for the upper IGBT becomes high. For VCCS1 and VCCS2 of the upper IGBT gate driver, it is similar.

III. Experimental Verification

The double pulse test method is used to evaluate the performance of the proposed ACSD method. The circuit and a photograph of the test setup are shown in Figs. 6 and 7, respectively. An Infineon 1200 V/800 A dual-IGBT module FF800R12KE3 is the device under test. The lower IGBT serves as the switch and the upper one serves as the freewheeling diode. The inductive load is a 60-μH air core inductor. The dc bus voltage V_{dc} is 600 V and the load current is 600 A, which is sensed by a compact current transformer (CT) with 1:10 current gain and then measured by the current monitor model 411 from Pearson with 20-MHz bandwidth. L_S represents the lumped main circuit parasitic inductance. The parasitic inductance between the power emitter and the Kelvin gate drive emitter of the IGBT module, L_e, is marked in Fig. 7, which is around 16 nH. The

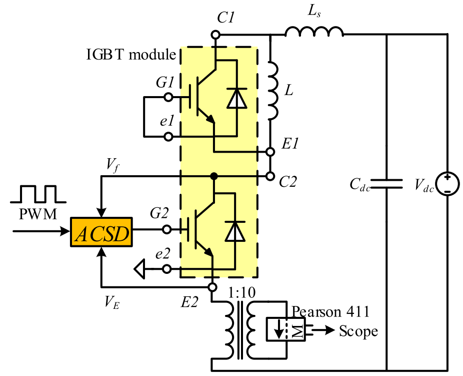

Fig. 6. Setup of the double pulse test.

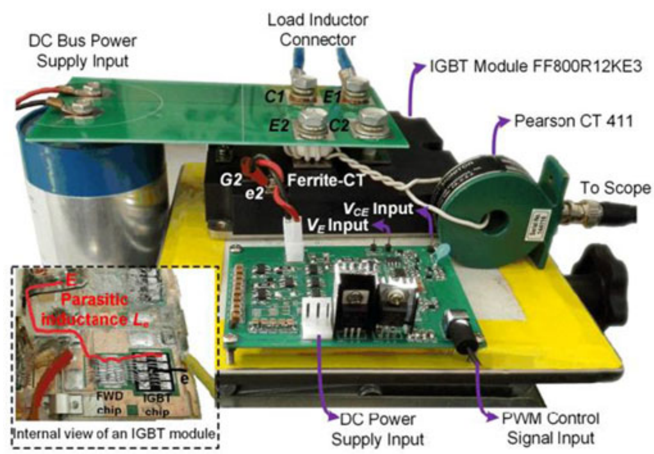

Fig. 7. Photograph of the test platform and measurement setup.

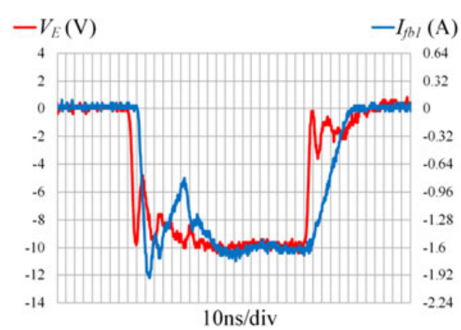

Fig. 8. Response time of the feedback circuit at turn-on.

measurement equipment and ICs used in the proposed gate drive shown in Figs. 3 and 4 are listed in Table I.

A. Response Speed

The response speed of the VCCS in the proposed ACSD method is very important to effectively control the current and voltage overshoot. Fig. 8 shows the response time of the feedback circuit VCCS1 at turn-on, where V_E is -10 V as the feedback voltage and I_{fb1} is the output feedback current extracting from the gate terminal. The delay time is around 10 ns between these two signals, which is quite small compared to the collector current rising time in a few hundred nanoseconds. The response time of the feedback circuit VCCS2 at turn-off is around 20 ns

TABLE I
DATA OF DOMINANT ICS AND MEASUREMENT EQUIPMENT

IGBT module	Infineon FF800R12KE3, 1200V/800A
V_{CE} measurement	Tektronix P5100A
I_C measurement	Pearson current monitor 411
T1 & T2 (T5 & T6)	Diode/Zetex ZDT6790
T3 & T4 (T7 & T8)	Diode/Zetex ZDT1049, dual NPN
T9 & T10	Diode/Zetex ZXT12P40DX, dual PNP
OPAMP	Texas Instruments THS3062

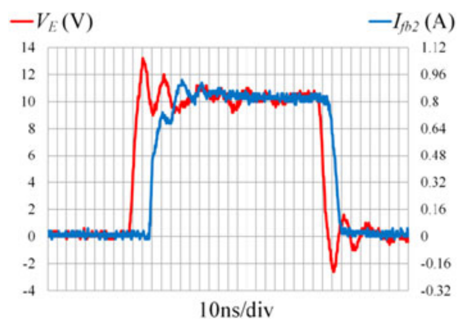

Fig. 9. Response time of the feedback circuit at turn-off.

TABLE II
PARAMETERS SETUP AT TURN-ON

V_{Zon} (V)	R_{Son} (Ω)	R_1 (Ω)	R_2 (Ω)
5.1	1	2k	1k

as shown in Fig. 9, where V_E is 10 V as the feedback voltage and $I_{\mathrm{fb}2}$ is the output feedback current injecting to the gate terminal. This response time is slightly higher than that at turn-on because of the more complex feedback circuit at turn-off. It is still quite small compared with the collector–emitter voltage rising time and the collector current falling time, which are around several hundred nanoseconds.

B. Turn-ON Performance

The feedback current is adjusted by changing the VCCS1 resistance R_{fon}, and the amplifier gain K_{i1} is set as -0.5. The experimental parameters at turn-on are shown in Table II.

Fig. 10 shows IGBT switching performance at turn-on with the proposed ACSD method compared with the CGD method. As shown in Fig. 10(a), for the IGBT with CGD, the larger the gate resistance is, the slower the turn-on speed is and the lower the current overshoot is. However, large gate resistance leads to high turn-on delay and Miller plateau time, which results in high power losses. For comparison, the tested waveforms with the proposed ACSD method are shown in Fig. 10(b). When the feedback resistance R_{fon} is changed, the current overshoot can be controlled effectively. Unlike the CGD method, the turn-on delay time and Miller plateau time nearly unaffected with different R_{fon}. This is preferred for dead time design and switching losses reduction in practical applications.

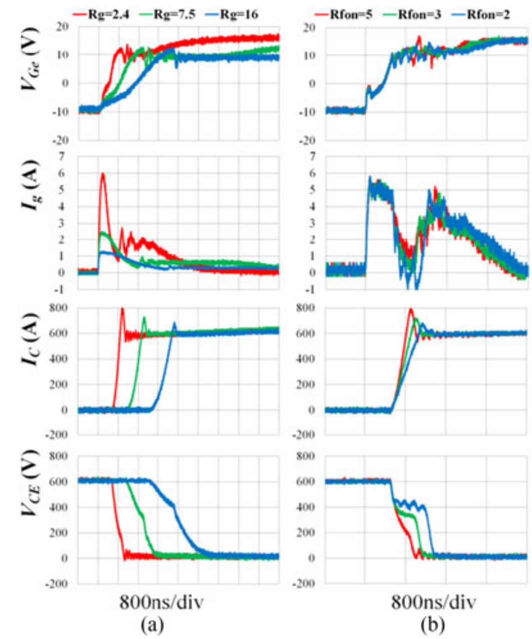

Fig. 10. Waveforms at turn-on for (a) CGD and (b) ACSD.

TABLE III
TURN-ON DELAY TIME AND MILLER PLATEAU TIME WITH ACSD

R_{fon} (Ω)	I_{rr} (A)	$t_{d(\mathrm{on})}$ (ns)	$t_{M(\mathrm{on})}$ (ns)
w/o FB	230	580	860
6	192	580	860
4	148	580	880
3	112	580	880
2	80	580	890

TABLE IV
TURN-ON DELAY TIME AND MILLER PLATEAU TIME WITH CGD

R_g (Ω)	I_{rr} (A)	$t_{d(\mathrm{on})}$ (ns)	$t_{M(\mathrm{on})}$ (ns)
1	230	470	880
2.4	192	640	1210
4.7	148	920	2020
7.5	112	1310	3280
16	80	2320	5580

The turn-on delay time $t_{d(\mathrm{on})}$ and Miller plateau time $t_{M(\mathrm{on})}$ with ACSD and CGD are given in Tables III and IV, respectively. When the current overshoot is controlled from 230 to 80 A, $t_{d(\mathrm{on})}$ with ACSD remains 580 ns, while that with CGD increases from 470 to 2320 ns. A 75% turn-on delay time reduction is achieved by ACSD compared with CGD at the same limited current overshoot, 80 A. Similarly, $t_{M(\mathrm{on})}$ with ACSD slightly changes from 860 to 890 ns, while that with CGD increases significantly from 880 to 5580 ns. An 84% Miller plateau time reduction is achieved by using ACSD at the same limited current overshoot, 80 A.

As described in Section II, the turn-on losses are determined by the power losses during current rising (stage II), voltage falling (stage III) and tail voltage stages (stage IV), that is, E_{ri},

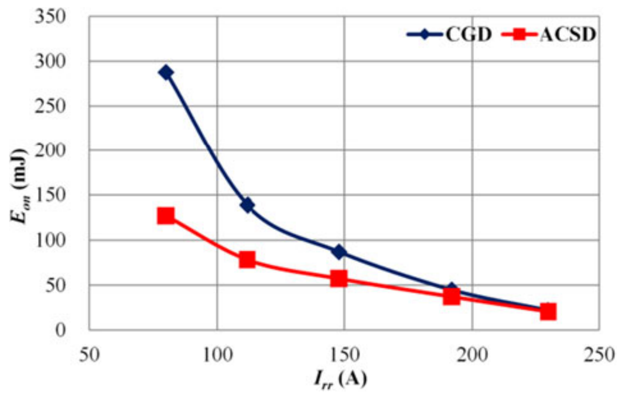

Fig. 11. Total switching losses at turn-on of ACSD and CGD.

E_{fv} and E_{vtail}

$$E_{\mathrm{on}} = E_{\mathrm{ri}} + E_{\mathrm{fv}} + E_{\mathrm{vtail}}. \quad (13)$$

The total turn-on losses utilizing the proposed ACSD method compared with the CGD method are shown in Fig. 11. The gate resistance R_g of CGD and the feedback resistance R_{fon} of ACSD are changed to achieve various current overshoots. From Fig. 11, it is clear that the power losses with ACSD are always lower than those with CGD, where the smaller the current overshoot is, the larger the turn-on losses reduction is. When the current overshoot is 80 A, up to 56% power losses reduction is achieved by ACSD.

For further understanding the power losses reduction with the ACSD method, the turn-on losses break-down for different stages is shown in Fig. 12. Large gate resistance leads to an overall deterioration in switching speed. Therefore, the switching losses and switching time with CGD are both high. However, the proposed ACSD method controls the di/dt during the current rising stage, but advantageously the other stages are not affected. When I_C begins to rise, V_{CE} with large gate resistance drops slowly while the V_{CE} dropping curve tracks with ACSD almost coincide, as shown in Fig. 10. Thus the proposed ACSD method achieves a slightly lower E_{ri} than CGD, as shown in Fig. 12(a). In the voltage falling stage, as shown in Fig. 12(b), E_{fv} with CGD increase much faster than that with ACSD. With CGD, the gate drive current reduces as V_{Ge} increases, thus V_{CE} drops slowly and the power losses are large. For ACSD, however, the gate drive current is near constant and is not affected by V_{Ge}. In the tail voltage stage, E_{vtail} shown in Fig. 12(c) is related to collector–emitter voltage falling speed, so E_{vtail} with ACSD is much smaller than that with CGD.

Based on the turn-on experimental results presented, the proposed ACSD method effectively controls the current overshoot, and achieves lower turn-on losses, delay time, and Miller plateau time than the CGD method.

C. Turn-Off Performance

To evaluate the turn-off performance of the proposed ACSD method, the feedback resistance R_{foff} is changed to control the collector–emitter voltage overshoot. The amplifier gain K_{i2} and K_v are both set as 0.25. The experimental parameters at turn-off are shown in Table V.

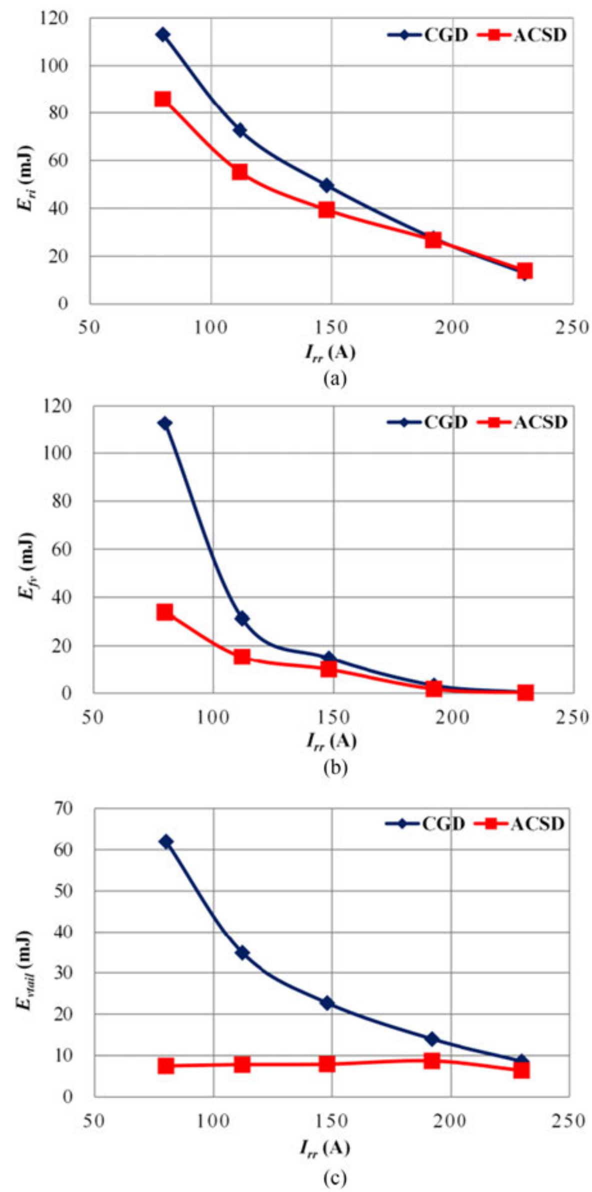

Fig. 12. Comparison of power losses in different turn-on stages: (a) E_{ri}; (b) E_{fv}; and (c) E_{vtail}.

TABLE V
PARAMETERS SETUP AT TURN-OFF

V_{Zoff} (V)	R_{Soff} (Ω)	R_3 (Ω)	R_4 (Ω)	R_5 (Ω)	R_6 (Ω)	R_7 (Ω)	R_f (Ω)	C_f (pF)
5.1	2	7k	1k	7k	1k	1k	300	47

Fig. 13 shows the turn-off switching waveforms with the proposed ACSD method and the CGD method. In Fig. 13(a), large gate resistance reduces the voltage overshoot, but the turn-off switching time increases significantly. A large turn-off delay complicates the dead time design and distorts the output waveform in inverter applications. These problems can be solved

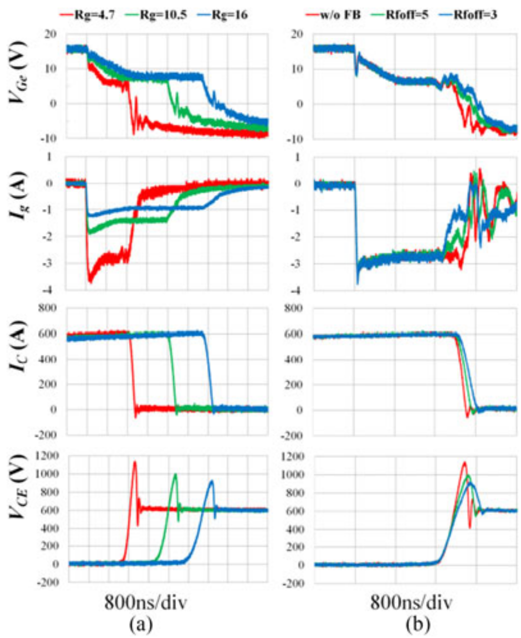

Fig. 13. Waveforms at turn-off for (a) CGD and (b) ACSD.

TABLE VI
TURN-OFF DELAY TIME AND MILLER PLATEAU TIME WITH ACSD

$R_{\rm foff}$ (Ohm)	$V_{\rm OS}$ (V)	$t_{\rm d(off)}$ (ns)	$t_{\rm M(off)}$ (ns)
w/o FB	520	2020	1260
5	384	2060	1290
4	348	2080	1300
3	308	2110	1330
2	244	2170	1380

TABLE VII
TURN-OFF DELAY TIME AND MILLER PLATEAU TIME WITH CGD

$R_{\rm g}$ (Ohm)	$V_{\rm OS}$ (V)	$t_{\rm d(off)}$ (ns)	$t_{\rm M(off)}$ (ns)
4.7	520	1720	1160
10.5	384	3280	2290
13.5	348	4000	2880
16	308	4680	3530
24	244	6630	4820

by the proposed ACSD method as shown in Fig. 13(b). With ASCD, the turn-off switching time is shorter and is minimally affected by the VCCS2 feedback resistance $R_{\rm foff}$.

The measured turn-off delay time $t_{d(\rm off)}$ and Miller plateau time $t_{M(\rm off)}$ with ACSD and CGD are given in Tables VI and VII, respectively. When the voltage overshoot $V_{\rm OS}$ is controlled from 520 to 244 V, $t_{d(\rm off)}$ and $t_{M(\rm off)}$ with ACSD increase from 2020 to 2170 ns and from 1260 to 1380 ns, respectively. But for the IGBT using CGD, $t_{d(\rm off)}$ and $t_{M(\rm off)}$ increase from 1720 to 6630 ns and from 1160 to 4820 ns, respectively. With the proposed ACSD method, a 68% turn-off delay time reduction and a 69% Miller plateau time reduction are achieved, when $V_{\rm OS}$ is limited to 244 V.

The total turn-off losses can be divided into three parts as described in Section II: the power losses during voltage rising, current falling, and tail current stages, that is, $E_{\rm rv}$, $E_{\rm fi}$, and $E_{\rm itail}$

$$E_{\rm off} = E_{\rm rv} + E_{\rm fi} + E_{\rm itail}. \tag{14}$$

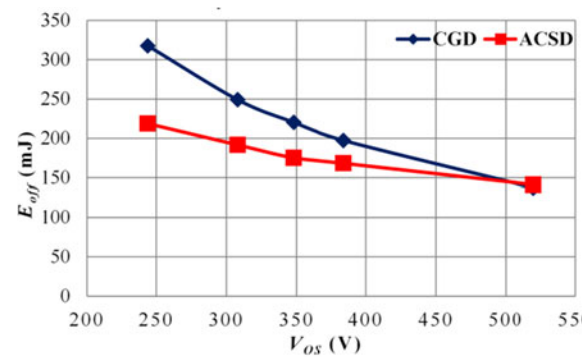

Fig. 14. Turn-off losses $E_{\rm off}$ versus $V_{\rm os}$.

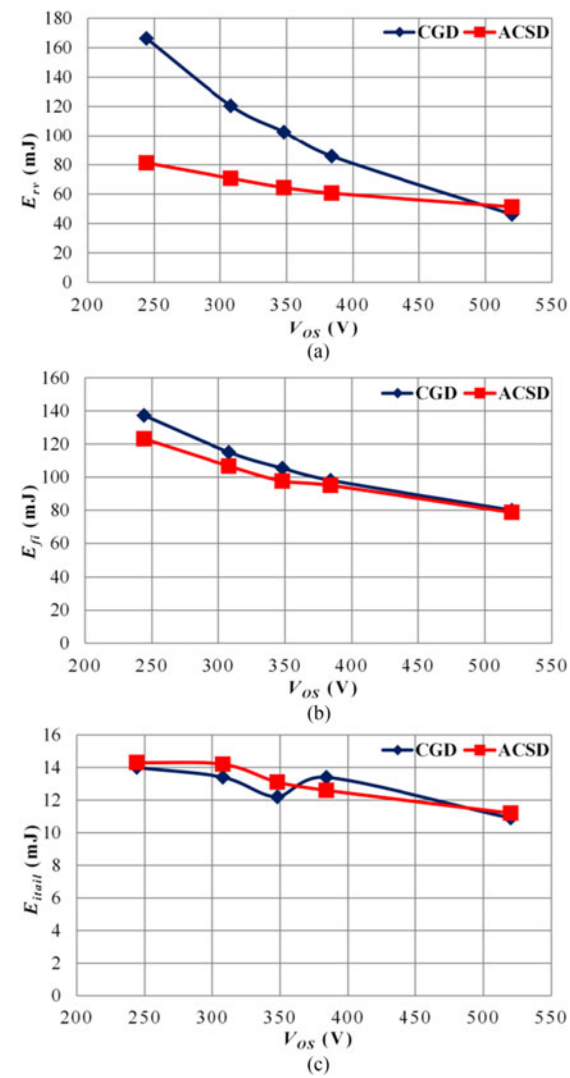

Fig. 15. Comparison of power losses in different turn-off stages: (a) $E_{\rm rv}$; (b) $E_{\rm fi}$; and (c) $E_{\rm itail}$.

The IGBT turn-off losses for different voltage overshoots ($V_{\rm OS}$) are given in Fig. 14, for both gate drive methods. $V_{\rm OS}$ is controlled to different values, and with both gate drivers, the

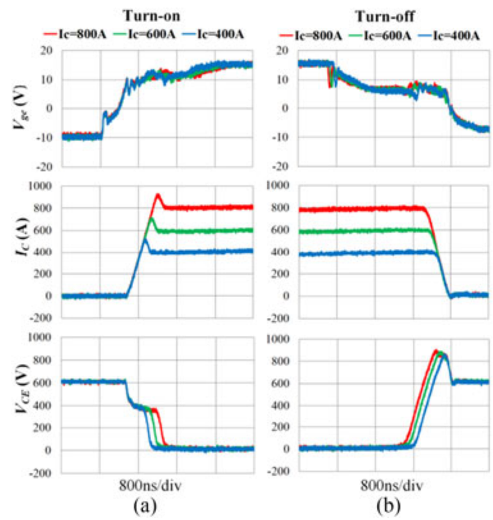

Fig. 16. Switching waveforms at various switching currents: (a) turn-on and (b) turn-off.

power losses increase as V_{OS} decreases. When V_{OS} is high, 520 V, the turn-off losses of the IGBTs with both methods are similar due to similar switching speed. While V_{OS} is controlled to a low voltage, for instance 244 V, the ACSD turn-off losses are only 69% of that with CGD.

Fig. 15 shows turn-off losses components with various voltage overshoots. During the voltage rising stage, I_C is near constant and E_{rv} is mainly determined by V_{CE} rising speed. Large gate resistance results in small gate drive current, significantly slowing down the V_{CE} rising speed. Therefore, E_{rv} increases quickly with CGD when V_{OS} is controlled small as shown in Fig. 15(a). With the proposed ACSD method, however, the $\mathrm{d}v/\mathrm{d}t$ is only minimally affected by the feedback resistance as shown in Fig. 13, resulting in lower power losses. In Fig. 15(b), the power losses during current falling stage are similar because the $\mathrm{d}i/\mathrm{d}t$ is controlled similarly to achieve the same voltage overshoot for both gate drive methods. In the tail current stage, E_{itail} is mainly determined by the device minority carrier and near unaffected by the gate, as shown in Fig. 15(c). The slight variation is mainly caused by the measurement noise.

Based on the experimental results, the proposed ACSD method effectively controls the voltage overshoot during turn-off transient, shortens the turn-off delay, and decreases the turn-off losses, compared with the CGD method.

D. Performance at Various Switching Currents

The experimental waveforms at various switching currents both at turn-on and turn-off with the proposed ACSD method are shown in Fig. 16. Both of the VCCS feedback resistances R_{fon} and R_{foff} are 2.5 Ω. In Fig. 16(a), the turn-on delay time and Miller plateau time are unchanged at different switching currents, with about 100-A current overshoot. This verifies the effectiveness of the proposed method. The turn-off results in Fig. 16(b) show that the turn-off time and the voltage overshoots are similar when the switching currents are 400, 600, and 800 A. In summary, the ACSD method is adaptive to various switching currents, a feature desirable for high-power applications.

IV. Conclusion

An ACSD method based on $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$ feedback control strategy is proposed in this paper. A constant current source is utilized to drive the gate and a VCCS is adopted to control the current and voltage overshoots during turn-on and turn-off transients, respectively. By simply sensing the $\mathrm{d}i/\mathrm{d}t$ or $\mathrm{d}v/\mathrm{d}t$ signal, the VCCS can generate a feedback current to regulate the net gate drive current to control the $\mathrm{d}i/\mathrm{d}t$ or $\mathrm{d}v/\mathrm{d}t$ during the switching transients, and then the current/voltage overshoot can be controlled. Compared with the common voltage source gate drive, the proposed ACSD method put forward a new strategy for direct control of the gate drive current rather than the gate drive voltage. And this method features low power losses, simple circuit, high dynamic response speed, low switching delay time, and small Miller plateau time, which is quite attractive for high efficiency and high reliability power converter applications. Experimental results verify the effectiveness of the proposed ACSD method. The circuit model for stability analysis and the optimal regulation of the feedback control strategy will be discussed in future works.

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