A Dual Series-Resonant DC–DC Converter

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***Abstract*—A dual series-resonant dc–dc converter with zero-voltage switching and zero-current switching features is proposed in this paper. The topology consists of two switches and a clamping capacitor on the primary side of an isolating transformer. The two switches are operated in a complementary mode under a pulse width modulation (PWM) scheme. The secondary side of the transformer is connected to the load through two series-resonant circuits and a half-bridge diode rectifying stage, in which the rise and fall slopes of the diode currents are limited by the slope of the currents in the resonant circuits, resulting in reduced switching losses in the diodes. The two series-resonant circuits provide power transfer to the output load without interruption throughout the positive and negative cycles of operation. It is shown that the output voltage of the proposed converter can be regulated using either PWM control or frequency modulation control. Both step-down and step-up voltage conversions can be achieved using the proposed topology. Programmable system-on-chip is used as the controller platform to implement a 40 W laboratory prototype. A complete steady-state analysis is presented and the experimental results of the prototype of the proposed converter are discussed.**

***Index Terms*—DC–DC converter, extended describing function, series-resonant circuit, zero-current switching (ZCS), zero-voltage switching (ZVS).**

NOMENCLATURE

$Q1$, $Q2$	Semiconductor switches.
$L_{r1} = L_{r2}$	Resonant inductors.
$C_{r1} = \mathrm{C_{r2}}$	Resonant capacitors.
$D1$, $D2$	Output rectifying diodes.
N_p	Primary winding turns.
N_s	Secondary winding turns.
N	Turns ratio of the transformer ($N_\mathrm{s}/N_\mathrm{p}$).
L_m	Magnetizing inductance of the transformer.
C_c	Clamping capacitor.
R_o	Output load.
C_o	Output capacitor.
D_{Q1}	Antiparallel diode of $Q1$.
D_{Q2}	Antiparallel diode of $Q2$.
C_{Q1}	Drain-to-source capacitor of $Q1$.
C_{Q2}	Drain-to-source capacitor of $Q2$.
J_1 & J_2	Shunt jumpers.
ω_r	Angular resonant frequency of L_r and C_r.
ω_m	Angular resonant frequency of L_m and C_c.
ω_s	Angular switching frequency.
f_r	Resonant frequency.
f_sw	Switching frequency.
T_s	Time period ($T_s = 1/f_\mathrm{sw}$).
Z_o	Characteristic impedance ($Z_o = \sqrt{L_r/C_r}$).
i_{Lm}	Magnetizing inductor current of L_m.
i_{Lr1}	Resonant inductor current of L_{r1}.
i_{Lr2}	Resonant inductor current of L_{r2}.
i_{NLr}	Normalized resonant inductor current.
v_{Cr1}	Resonant capacitor voltage of C_{r1}.
v_{Cr2}	Resonant capacitor voltage of C_{r2}.
v_{NCr}	Normalized resonant capacitor voltage.
v_d	Input dc voltage.
v_o	Output dc voltage.
v_{Cc}	Clamping capacitor voltage.
v_{Lm}	Magnetizing inductor voltage.
d	Duty ratio of $Q2$.
F	Normalized switching frequency (f_sw/f_r).
θ	Phase angle between $sgn(i_{Lr1} + i_{Lr2})$ and v_{Lm} waveforms.
i_{nFCLr}	The nth cosine coefficient of the Fourier expansion of the resonant inductor current.
i_{nFSLr}	The nth sine coefficient of the Fourier expansion of the resonant inductor current.
v_{nFCCr}	The nth cosine coefficient of the Fourier expansion of the resonant capacitor voltage.
v_{nFSCr}	The nth sine coefficient of the Fourier expansion of the resonant capacitor voltage.
a_n	The nth cosine coefficient of the Fourier expansion of the magnetizing inductor voltage.
b_n	The nth sine coefficient of the Fourier expansion of the magnetizing inductor voltage.
A_n	The nth cosine coefficient of the Fourier expansion of the $sgn(i_{Lr1} + i_{Lr2})$.
B_n	The nth sine coefficient of the Fourier expansion of the $sgn(i_{Lr1} + i_{Lr2})$.

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I. INTRODUCTION

DC–DC power converters play a significant role in several applications including dc electric power distribution systems, renewable energy generation technologies, and dc-switched-mode power supplies. As a result, the development of new topologies and control schemes are always an ongoing challenge for researchers. The main objectives of this challenge are improvement in efficiency, increased power density, reduced complexity of the control scheme, and reduction in total manufacturing cost of the converter. Significant progress in soft-switching methods, including zero-voltage switching (ZVS) and

zero-current switching (ZCS) techniques, have enabled dc–dc converters to be operated at high switching frequencies with reduced switching losses. As a result, several classes of miniaturized, high-efficient dc–dc converters are available commercially.

Among the several topologies for soft-switching dc–dc converters proposed to meet new requirements and industry standards, isolated converters are preferred due to the galvanic isolation, reliability, safety, and protection requirements in accordance with IEEE Standards 519 and 1547 [1]. Multiresonant converters such as isolated *LLC* dc–dc converters have brought about significant improvement in the overall efficiency of the converter [2], [3]. However, in a number of these converters, the regulation of the output voltage is achieved by controlling the switching frequency, resulting in complex implementation of the control scheme and poor efficiency when the switching frequency is far away from the resonant frequency [4]–[6].

Another category of isolated, soft-switching converters is the forward converters, which are popular because of their low cost, simple structure, and ZVS operational characteristics [7]–[9]. However, forward converters suffer from limited range of output voltage variation and transformer resetting problem [10]. Attempts to resolve these challenges have resulted in some improvements but at the cost of violating the soft-switching feature of the converter, resulting in reduced converter efficiency [11], [12]. Active-clamped resonant converters which incorporate a clamped capacitor to overcome the problem of transformer resetting have been proposed for low-power applications due to their simplicity and low cost [13]–[15]. In these converters, the switches can be operated at high switching frequency under ZVS and ZCS conditions. Consequently, the size of the passive components can be further reduced. However, the existing topologies, which consist of a single transformer with a single resonant circuit, do not provide continuous output power transfer during the complete cycle of operation. As a result, these converters suffer from high current ripple at the output, reduction in efficiency, and deterioration in power density [16].

Several attempts have been made to improve the power density of clamped resonant converters [17]–[19]. An interleaving technique is one of the well-known proposed methods to increase the power transferred to the load and reduce the input and output current ripples in power factor correction circuits [20], [21] and dc–dc converters [22]–[24]. In this technique, identical units of the converter are paralleled and operated at the same switching frequency but with phase-shifted switching signals. Despite the improvement in the transferred power to the load, this approach results in increased number of switching and passive components, increased sophistication in the switching scheme, as well as increased manufacturing costs [25]. For example, Hsia *et al.* [24] proposed a two-stage interleaved active-clamping resonant converter, which provides continuous power transfer to the output load during the complete cycle of operation. However, the doubling of the active and passive components does not significantly improve the power density of the converter.

In this paper, an alternative topology of the active-clamping resonant dc–dc converter is proposed. By implementing two series-resonant circuits, the power transfer to the output load is not interrupted, resulting in improved power transfer capability.

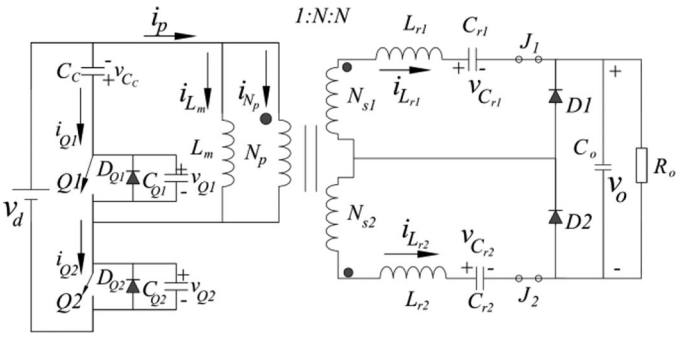

Fig. 1. Proposed dual series-resonant dc–dc converter [28].

The proposed converter, referred to as the dual series-resonant dc–dc converter, features ZVS and ZCS conditions over a wide range of switching frequency operation and output voltage variations. Using the extended describing function method [26], a complete analytical model of the converter is developed. It is shown in this paper that the power density of the converter is increased without using the interleaved technique. PLECS standalone software [27] is used to perform the simulation tasks and MATLAB is used to verify the modeling analysis. A 40 W prototype of the proposed topology is also implemented and tested over a wide range of switching frequency between 160 and 640 kHz. The experimental results of the prototype are compared with the simulation and modeling results to validate the operation and behavior of the proposed converter.

The rest of this paper is organized as follows: the proposed topology and its principle of operation are presented in Section II.In Section III, the steady-state analysis of the converter is presented. The development of the extended describing function approach for the proposed converter is detailed in this section. The simulation and experimental results demonstrating the steady-state behavior of the converter are presented in Section IV, and the conclusions of the work are summarized in Section V.

II. Topology and Principle of Operation

The proposed topology of the dual series-resonant dc–dc converter is shown in Fig 1. The primary side of the isolation transformer consists of a winding of turns N_p and magnetizing inductance L_m. The circuit configuration at the input of the transformer consists of two active switches, $Q1$ and $Q2$, and a clamp capacitor C_c in series with $Q1$. The antiparallel diodes and internal capacitors of the switches (D_{Q1}, C_{Q1}, D_{Q2}, and C_{Q2}) are shown in Fig. 1. The secondary side of the transformer has two windings (N_{s1} and N_{s2}), each connected to separate but identical series-resonant circuit with identical parameters (i.e., L_{r1} and C_{r1} to N_{s1}, L_{r2} and C_{r2} to N_{s2}, with $L_{r1} = L_{r2}$, $C_{r1} = C_{r2}$, and $N_{s1} = N_{s2} = N_s$). Two shunt jumpers (J_1 and J_2) are included in the circuit. By removing one of the jumpers, the topology can be changed to a single series-resonant circuit to allow comparison of results between the single series-resonant topology and the dual series-resonant topology. A diode rectifying stage ($D1$ and $D2$) connects the output load and output capacitor to the series-resonant circuits.

Fig. 2. Operating modes of the dual series-resonant dc–dc converter: (a) Mode I, (b) Mode II, (c) Mode III, (d) Mode IV, (e) Mode V, and (f) Mode VI.

The positive polarity of all voltage and current variables is shown in Fig. 1 with $\pm$ sign and solid arrow, respectively.

The operating modes of the converter as well as the subsequent analysis are based on the following assumptions: the parasitic resistances of the electrical connections and the turn-on resistances of the switches and diodes are assumed to be zero; the angular resonant frequency of L_r and C_r (ω_r) is much higher than the angular resonant frequency of L_m and C_c (ω_m); the continuous conduction mode (CCM) of operation of the converter is considered. For $F = f_{\rm sw}/f_r \geq 2$, CCM operation of the converter is guaranteed.

The operation of the proposed converter can be described in six modes. Fig. 2 shows the equivalent circuits of the converter in each mode, where the current paths are illustrated with dashed arrows. The corresponding key ideal waveforms of the converter during steady-state operation are depicted in Fig. 3. The principle of operation of the proposed converter is detailed as follows:

Prior to *Mode I* ($t = T_0^-$): $Q2$ is OFF; $Q1$ is ON and conducts the current $i_{Q1} = -i_p$ at the primary side of the transformer; i_{Lm} is positive and is decreasing; i_{Lr1} and i_{Lr2} are negative (therefore, i_{Np} is negative), and $D1$ conducts i_{Lr1} and i_{Lr2}. While i_{Lr1} circulates in the series-resonant circuit through N_{s1}, i_{Lr2} supplies the load current. During this mode, $D2$ is OFF.

Mode I ($T_0 < t < T_1$): At $t = T_0$, $Q1$ is triggered OFF, the parasitic capacitor C_{Q1} starts to charge by i_{Q1}, and the parasitic capacitor C_{Q2} starts to discharge. Therefore, the voltage drop across $Q1$ increases from zero to $V_d + V_{Cc}$. Meanwhile, the voltage drop across $Q2$ decreases from $V_d + V_{Cc}$ to zero. As soon as the voltage drop across $Q2$ equals zero, D_{Q2} starts to conduct the current. Due to the small value of parasitic capacitor of the semiconductor switches, this time interval is very small and can be neglected. During this mode, the primary current of the transformer (i_p) can be assumed constant. Following the same argument, the variables on the secondary side of the

transformer can be assumed unchanged. Fig. 2(a) shows the current paths during this mode.

Mode II ($T_1 < t < T_2$): During this mode, $Q1$ is OFF; $Q2$ is ON and the voltage at the primary side of the transformer is equal to V_d. On the primary side, D_{Q2} conducts the negative current of i_p; therefore, $Q2$ can be triggered on at ZVS condition. Since the voltage at the primary side of the transformer is positive, both i_{Np} and i_{Lm} start to increase. On the secondary side, the resonant inductor currents (i_{Lr1} and i_{Lr2}) are both still negative values but start to increase, and the resonant capacitor voltages (v_{Cr1} and v_{Cr2}) keep decreasing. Fig. 2(b) shows the paths of the currents during this mode. This mode ends when $i_{Lr1} + i_{Lr2}$ becomes zero. In other words, at the end of this mode, $D1$ turns off naturally and $D2$ turns on at ZCS condition and conducts the resonant and load currents. The slopes of the turn-off current of $D1$ and the turn-on current of $D2$ are limited by the slope of the current in the series-resonant circuits, which in turn reduce the switching losses in the diodes.

Mode III ($T_2 < t < T_3$): At $t = T_2^+$, $i_{Lr1} + i_{Lr2}$ is a positive value; therefore, $D1$ is OFF and $D2$ carries the resonant currents. During this mode, i_{Lr2} circulates in the series-resonant circuit through N_{s2} and i_{Lr1} supplies the load current in the positive cycle of operation. On the primary side, i_{Np} becomes positive which makes i_p positive; therefore, $Q2$ starts to carry the positive current i_p at the primary side of the transformer. The resonant currents and resonant voltages increase during this mode. Fig. 2(c) shows the paths of the currents during this mode. The operation continues until $Q2$ is triggered OFF at $t = T_3$. Since the switching frequency is more than twice the resonant frequency, i_{Lr1} and i_{Lr2} remain positive at the end of this mode.

Mode IV ($T_3 < t < T_4$): When $Q2$ is triggered OFF, i_{Lr1} and i_{Lr2} are still positive, and v_{Cr1} and v_{Cr2} keep charging. On the primary side, i_p is positive; therefore, C_{Q2} conducts i_p, v_{CQ2} increases from zero to $V_d + V_{Cc}$, and C_{Q1} starts to discharge to zero. Therefore, v_{CQ1}, which was $V_d + V_{Cc}$, reaches zero and D_{Q1} conducts the current at the end of this mode. This mode is the dual of *Mode I*. Fig. 2(d) shows the converter current paths in this mode. The time interval of this mode is negligibly small and the current i_p can be assumed constant.

Mode V ($T_4 < t < T_5$): During this mode, the voltage at the primary side of the transformer is $-V_{Cc}$. On the primary side, i_p is still positive so that D_{Q1} conducts and i_{Lm} and i_p start to decrease. At this time, $Q1$ can be triggered ON at ZVS condition. On the other hand, i_{Lr1} and i_{Lr2} are still positive on the secondary side of the transformer and v_{Cr1} and v_{Cr2} keep increasing. However, due to the negative voltage across the secondary side of the transformer, the resonant currents start to decrease to zero. Fig. 2(e) shows the converter during this mode. This mode ends when $i_{Lr1} + i_{Lr2}$ reaches zero.

Mode VI ($T_5 < t < T_6$): This mode is the dual of Mode III. At $t = T_5^+$, and on the secondary side of the transformer, $i_{Lr1} + i_{Lr2}$ is a negative value and v_{Cr1} and v_{Cr2} start to decrease. $D2$ is OFF and $D1$ conducts the resonant and load currents. This makes i_{Np} and subsequently i_p negative and $Q1$ conducts the current at the primary side of the transformer. Due to the negative voltage on the primary side, i_{Lm} keeps decreasing. Fig. 2(f) shows the paths of the currents during this mode. These variations continue

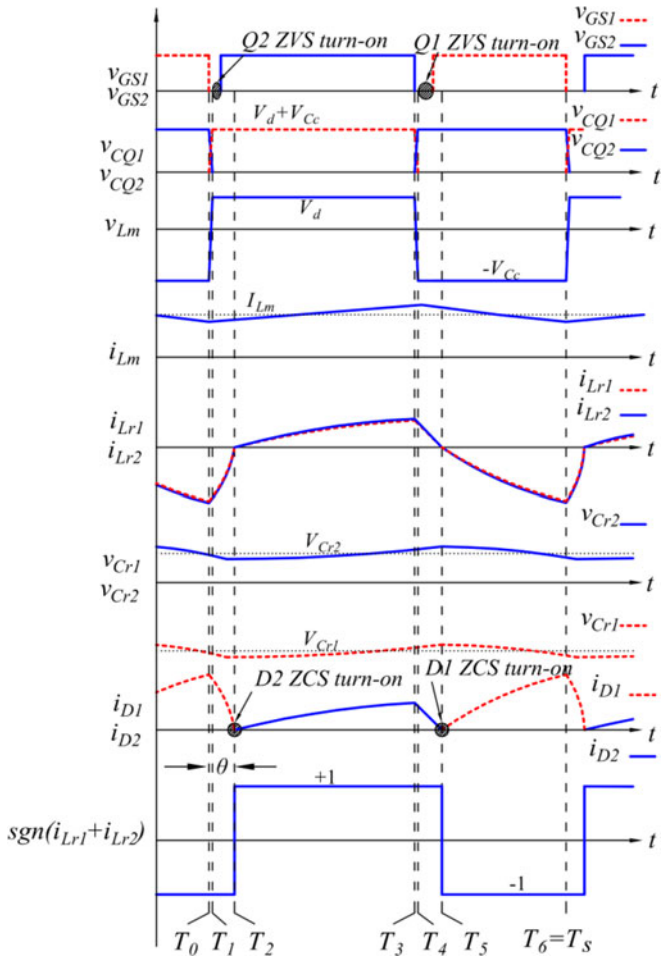

Fig. 3. Key ideal waveforms during steady-state condition of the dual series-resonant dc–dc converter: Mode I ($T_0 < t < T_1$), Mode II ($T_1 < t < T_2$), Mode III ($T_2 < t < T_3$), Mode IV ($T_3 < t < T_4$), Mode V ($T_4 < t < T_5$), and Mode VI ($T_5 < t < T_6$).

until $Q1$ is triggered OFF. At this stage, the converter returns to *Mode I* and repeats the cycle. At the end of this mode, the resonant currents remain negative as the switching frequency is more than twice the resonant frequency.

It can be seen that current is supplied to the output load without interruption through the entire operation of the converter. Unlike the case of the interleaved technique, the power transfer capability in the proposed converter is improved without doubling the number of active components. Therefore, a smaller footprint of the dual series-resonant topology would be capable of delivering the same level of power as the interleaved topology. This fact increases the power density of the proposed dc–dc converter. From Fig. 3, it can be visually confirmed that the resonant inductor currents and, consequently, the ac components in the resonant capacitor voltages are equal.

Fig. 4 shows the state-plane trajectory of the normalized resonant inductor current (i_{NLr}) with V_d/Z_o and normalized resonant capacitor voltages (v_{NCr}) with V_d under three different loading conditions obtained from PLECS simulation results. The trajectories of the L_{r1} and C_{r1} are shown with solid lines and the trajectories of L_{r2} and C_{r2} are shown with dashed lines. As the load increases, the resonant inductor currents increase;

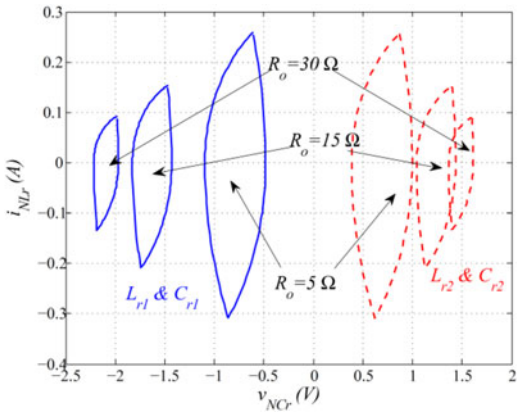

Fig. 4. State-plane trajectories for two different loading conditions (R_o = 30 Ω, R_o = 15 Ω, and R_o = 5 Ω).

however, the resonant capacitor voltages decrease. It is observed that the shape of the trajectories of L_{r1} and C_{r1}, and L_{r2} and C_{r2} are identical. This fact signifies that the ac components in i_{Lr1} and i_{Lr2} as well as the ac components in the v_{Cr1} and v_{Cr2} are equal. However, the dc components in the v_{Cr1} and v_{Cr2} are not equal.

III. Steady-State Analysis

On the primary side of the transformer, $Q1$ and $Q2$ are operated in a complementary mode under a pulse width modulation (PWM) switching scheme. However, in order to model the converter, the traditional state-space averaging method [29] cannot be used. The reason is that the assumption of small ripple condition during the averaging interval, which is necessary for state-space averaging method, is not valid in the resonant converter.

A sampled-data method is a modeling tool that has been used to model resonant dc–dc converters [30]–[32]. This method does not give an in-depth understanding to design the converter. Besides, this method is difficult to use in converters with multiple switching components [33]. Instead, this paper uses the extended describing function method to model the proposed converter [26]. This method is based on decomposing the state-space variables into dc and ac terms. Furthermore, ac components are decomposed in a Cartesian form into sin(·) and cos(·) terms. Then, each of the decomposed signals is expressed as the summation of large-signal and small-signal components. Steady-state analysis can be completed by separately equating the large-signal components in the state-space equation.

The proposed converter consists of seven passive components, i.e., two resonant circuits (L_{r1}, C_{r1}, L_{r2}, and C_{r2}), a magnetizing inductor (L_m), clamping capacitor (C_c), and output capacitor (C_o). The state variables can be expressed in the Fourier expansion form as follows:

$$i_{Lr1}(t) = \sum_{n=1,2,\ldots} (i_{nFSLr1}(t)\sin(nF\omega_r t) + i_{nFCLr1}(t)\cos(nF\omega_r t)) \quad (1.1)$$

$$i_{Lr2}(t) = \sum_{n=1,2,\ldots} (i_{nFSLr2}(t)\sin(nF\omega_r t) + i_{nFCLr2}(t)\cos(nF\omega_r t)) \quad (1.2)$$

$$v_{Cr1}(t) = v_{Cr1} + \sum_{n=1,2,..} (v_{nFSCr1}(t)\sin(nF\omega_r t) + v_{nFCCr1}(t)\cos(nF\omega_r t)) \quad (1.3)$$

$$v_{Cr2}(t) = v_{Cr2} + \sum_{n=1,2,\ldots} (v_{nFSCr2}(t)\sin(nF\omega_r t) + v_{nFCCr2}(t)\cos(nF\omega_r t)) \quad (1.4)$$

$$i_{Lm}(t) = i_{Lm} \quad (1.5)$$

$$v_{Cc}(t) = v_{Cc} \quad (1.6)$$

$$v_o(t) = v_o. \quad (1.7)$$

As listed in (1.1)–(1.7), each ac component is decomposed into its Fourier harmonic components. It is helpful to represent the voltage on the primary side of the transformer (v_{Lm}) and the sign function of $i_{Lr1} + i_{Lr2}$ (i.e., $sgn(i_{Lr1} + i_{Lr2})$) shown in Fig. 3, as Fourier expansion according to

$$v_{Lm}(t) = a_0 + (v_d + v_{Cc}) \sum_{n=1,2,\ldots} (a_n\cos(nF\omega_r t) + b_n\sin(nF\omega_r t)) \quad (2.1)$$

$$\mathrm{sgn}(i_{Lr1}(t) + i_{Lr2}(t)) = A_0 + \sum_{n=1,2,\ldots} (A_n\cos(nF\omega_r t) + B_n\sin(nF\omega_r t)) \quad (2.2)$$

where

$$a_0 = dv_d - (1-d)v_{Cc}(t) \quad (3.1)$$

$$a_n = \frac{\sin(2\pi nD)}{n\pi} \quad (3.2)$$

$$b_n = \frac{1-\cos(2\pi nD)}{n\pi} \quad (3.3)$$

$$A_0 = \frac{2T_5 - 2T_2 - T_s}{T_s} \quad (3.4)$$

$$A_n = \frac{2}{n\pi}\left(\sin\left(\frac{2n\pi(T_5 - T_0)}{T_s}\right) - \sin\left(\frac{2n\pi(T_2 - T_0)}{T_s}\right)\right) \quad (3.5)$$

$$B_n = \frac{2}{n\pi}\left(-\cos\left(\frac{2n\pi(T_5 - T_0)}{T_s}\right) + \cos\left(\frac{2n\pi(T_2 - T_0)}{T_s}\right)\right). \quad (3.6)$$

The state-space equations that describe the operation of the converter are obtained in general form as follows:

$$L_{r1}\frac{di_{Lr1}(t)}{dt} = -v_{Cr1}(t) - \frac{v_o(t)}{2}\left(1 + \mathrm{sgn}(i_{Lr1}(t) + i_{Lr2}(t))\right) + Nv_{Lm}(t) \quad (4.1)$$

$$L_{r2}\frac{di_{Lr2}(t)}{dt} = -v_{Cr2}(t) + \frac{v_o(t)}{2}\left(1 - \mathrm{sgn}(i_{Lr1}(t) + i_{Lr2}(t))\right) + Nv_{Lm}(t) \quad (4.2)$$

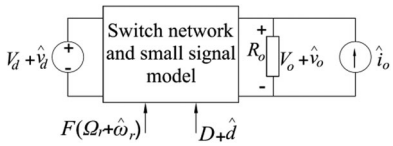

Fig. 5. General representation of the converter.

$$C_{r1}\frac{dv_{Cr1}(t)}{dt} = i_{Lr1}(t) \tag{4.3}$$

$$C_{r2}\frac{dv_{Cr2}(t)}{dt} = i_{Lr2}(t) \tag{4.4}$$

$$L_m\frac{di_{Lm}(t)}{dt} = v_{Lm}(t) \tag{4.5}$$

$$C_c\frac{dv_{Cc}(t)}{dt} = u\left(\frac{d}{dt}\left(-i_{Lr1}(t) - i_{Lr2}(t)\right)\right) \times \left(i_{Lm} + N\left(i_{Lr1}(t) + i_{Lr2}(t)\right)\right) \tag{4.6}$$

$$C_o\frac{dv_o(t)}{dt} = \frac{1}{2}(i_{Lr1}(t) - i_{Lr2}(t)) + \frac{1}{2}(i_{Lr1}(t) + i_{Lr2}(t))\mathrm{sgn}(i_{Lr1}(t)+i_{Lr2}(t)) - \frac{v_o}{R_o} + i_o(t) \tag{4.7}$$

where *sgn*(·) and *u*(·) are the sign and unit step functions, respectively, and $i_o(t)$ represents small perturbations of the load current.

By representing the small-signal perturbations with "ˆ", and large-signal parts with capital letters, each of the variables defined in (1.1)–(1.7) can be expressed in the form of the summation of a constant large signal and a small signal as $x_{nFS\bullet}(t) = X_{nFS\bullet} + \hat{x}_{nFS\bullet}$ (for sine coefficients), and $x_{nFC\bullet}(t) = X_{nFC\bullet} + \hat{x}_{nFC\bullet}$ (for cosine coefficients) for ac signals, and $x = X + \hat{x}$, for dc signals. In these representations, "*x*" is either the capacitor voltage or the inductor current and "•" is the corresponding inductor (L_{r1} or L_{r2}) or capacitor (C_{r1} or C_{r2}) in the state-space equations. The variables of (1.1)–(1.7) can be inserted into the state-space equations (4.1)–(4.7). A general procedure for extracting the steady-state equations involves equating the large signals of sin(·), cos(·), and dc terms on both sides of the resulting equations. If the converter is represented as a general block diagram (see Fig. 5), the inputs of the system can be expressed in the form of a constant large signal and a small signal according to

$$v_d = V_d + \hat{v}_d \tag{5.1}$$

$$d = D + \hat{d} \tag{5.2}$$

$$\omega_s = \Omega_s + \hat{\omega}_s = F\omega_r = F(\Omega_r + \hat{\omega}_r) \tag{5.3}$$

$$i_o = \hat{i}_o. \tag{5.4}$$

The steady-state solutions can be obtained by equating the derivative parts in (4.1)–(4.7) to zero and considering only the large-signal components. For a given operating point $\{V_d, D, \Omega_s = F\Omega_r, R_o\}$, the following steady-state variables can be derived:

$$V_{Cr1} = -\frac{V_o}{2}(1 + A_0) \tag{6.1}$$

$$V_{Cr2} = +\frac{V_o}{2}(1 - A_0) \tag{6.2}$$

$$V_{nFSCr2} = \frac{I_{nFCLr2}}{nF\Omega_r C_r} \tag{6.3}$$

$$V_{nFSCr1} = \frac{I_{nFCLr1}}{nF\Omega_r C_r} \tag{6.4}$$

$$V_{nFCCr2} = -\frac{I_{nFSLr2}}{nF\Omega_r C_r} \tag{6.5}$$

$$V_{nFCCr1} = -\frac{I_{nFSLr1}}{nF\Omega_r C_r} \tag{6.6}$$

$$I_{nFSLr1} = I_{nFSLr2} = \frac{-V_{nFCCr} - \frac{V_o}{2}A_n + N\left(\frac{V_d + V_{Cc}}{n\pi}\right)(\sin(2n\pi D))}{L_{r1}nF\Omega_r} \tag{6.7}$$

$$I_{nFCLr1} = I_{nFCLr2} = \frac{-V_{nFSCr} - \frac{V_o}{2}B_n + N\left(\frac{V_d + V_{Cc}}{n\pi}\right)(1 - \cos(2n\pi D))}{-L_{r1}nF\Omega_r} \tag{6.8}$$

$$V_{Cc} = \frac{D}{1-D}V_d \tag{6.9}$$

$$I_{Lm} = \frac{N}{(1-D)}\sum_{n=1,2,\ldots}\left[I_{nFCLr1}a_n + I_{nFSLr1}b_n\right] \tag{6.10}$$

$$V_o = \frac{R_o}{2}\sum_{n=1,2,\ldots}\left[I_{nFCLr1}A_n + I_{nFSLr1}B_n\right]. \tag{6.11}$$

After realizing the steady-state values of the variables in the converter, the time duration of each mode can be determined as follows:

$$T_0 = T_1 \approx 0 \tag{7.1}$$

$$\Omega_r T_2 = \arctan\left(\frac{\left(\frac{-DNV_d}{1-D} - V_{Cr1}\right)}{V_{Cr1} - NV_d}\sin\left(\Omega_r(T_s - T_5)\right)\right) \tag{7.2}$$

$$T_3 = T_4 \tag{7.3}$$

$$T_4 = DT_s \tag{7.4}$$

$$\Omega_r T_5 = \Omega_r DT_s + \arctan\left(\frac{(NV_d - V_{Cr1} - V_o)}{\frac{DNV_d}{1-D} + V_{Cr1} + V_o}\sin\left(\Omega_r(DT_s - T_2)\right)\right) \tag{7.5}$$

$$T_6 = T_s. \tag{7.6}$$

It is observed from (6.11) that the output voltage (V_o) is in terms of the Fourier components of *sgn*($i_{Lr1} + i_{Lr2}$) and the resonant inductor currents, which in turn are dependent on V_d, D, Ω_s, and R_o. An equation for the output voltage can be developed by assuming that the pulse width of *sgn*($i_{Lr1} + i_{Lr2}$) and $v_{Lm}(t)$ are equal, but with a phase difference between the two

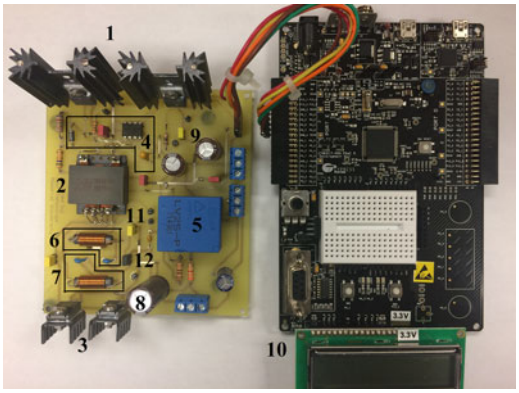

Fig. 6. Experimental prototype of the dual series-resonant dc–dc converter.

TABLE I
EXPERIMENTAL PROTOTYPE PARAMETERS

No.	Parameter	Part no./value
1	MOSFET switches	IPP320N20N3
2	Transformer	Wurth Electronics Midcom 750341142 ($L_m = 70\ \mu$H, $N = 1$)
3	Output diodes	RF2001T4S
4	Driver and bootstrap circuit	IRS2011
5	Voltage transducer	LV 25-P
6	Series-resonant circuit ($L_{r1} - C_{r1}$)	$L_{r1} = 4\ \mu$H $- C_{r1} = 1\ \mu$F
7	Series-resonant circuit ($L_{r2} - C_{r2}$)	$L_{r2} = 4\ \mu$H $- C_{r2} = 1\ \mu$F
8	Output capacitor	100 μF
9	Clamping capacitor (C_c)	10 μF
10	Gate signal generator	PSoC 5LP
11	Shunt jumper *J*1	–
12	Shunt Jumper *J*2	–

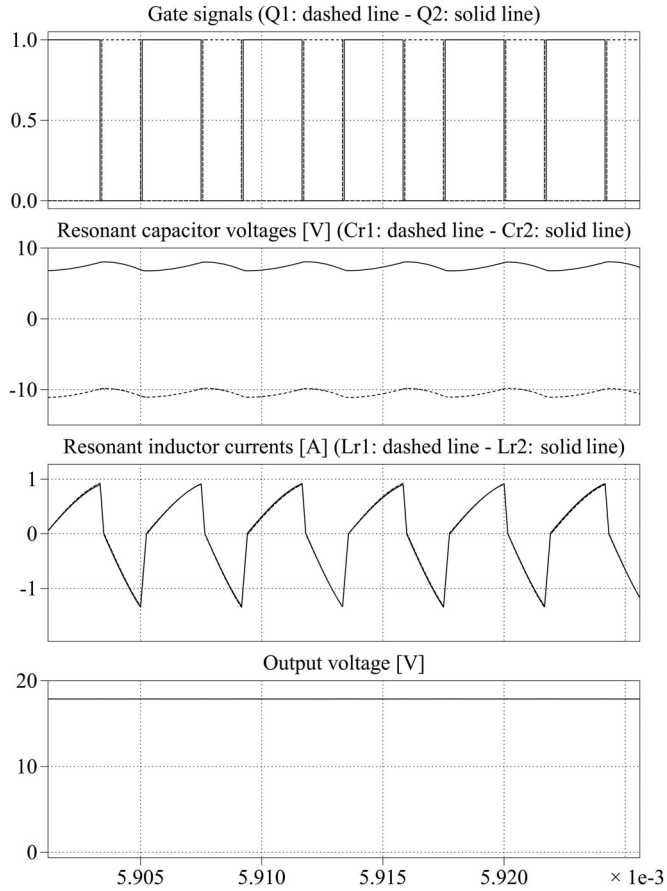

Fig. 7. PLECS simulation results for a case study ($V_d = 10$ V, $D = 0.6$, $f_{\rm sw} = 240$ kHz, $R_o = 30\ \Omega$, and $V_o = 18$ V).

signals. This assumption can be visually realized in Fig. 3. In this figure, this phase difference is marked as θ and can be expressed as $\theta = 2\pi.T_2/T_s$. By comparing the simulation results and the modeling results, it is observed that these approximations are acceptable.

Applying the previous approximation to calculate the Fourier coefficients of $sgn(i_{Lr1} + i_{Lr2})$, (3.4), (3.5), and (3.6) can be simplified to the following equations:

$$A_0 \approx A_0' = 2D - 1 \tag{8.1}$$

$$A_n \approx A_n' = \frac{2}{n\pi}\left(\sin(2\pi nD + n\theta) - \sin(n\theta)\right) \tag{8.2}$$

$$B_n \approx B_n' = \frac{2}{n\pi}\left(-\cos(2\pi nD + n\theta) + \cos(n\theta)\right). \tag{8.3}$$

Substituting the steady-state solutions of the resonant currents given in (6.7) and (6.8) into (6.11), and considering the first two components of (6.11), the output voltage is expressed in (9). This equation shows that the dc output voltage can be regulated by the duty ratio (D) and switching frequency ($\Omega_{\rm s}$)

$$V_o = 2R_o\left(\frac{\left|V_o\angle\theta - \frac{NV_d}{1-D}\right|}{\pi^2\left(\Omega_s L_r + 1/\Omega_s C_r\right)}\left(1 - \cos(2\pi D)\right) + \frac{\left|V_o\angle 2\theta - \frac{NV_d}{1-D}\right|}{(2\pi)^2\left(2\Omega_s L_r + 1/2\Omega_s C_r\right)}\left(1 - \cos(4\pi D)\right)\right). \tag{9}$$

IV. SIMULATION AND EXPERIMENTAL RESULTS

An experimental 40 W prototype of the proposed topology was implemented, as shown in Fig. 6. The parameter values of the prototype are listed in Table I. The gate signals are generated using the programmable system-on-chip (PSoC 5LP) from Cypress Semiconductor with a 32-bit ARM Cortex-M3 CPU [34]. PSoC includes programmable digital and programmable analog components, programmable routing and interconnects, and a graphical interface that facilitates the configuration and programming tasks of the embedded ICs [34]–[36]. Besides, the size and volume of this platform are smaller compared to other field-programmable gate arrays and digital signal processors [37]. A voltage transducer is used in the prototype for voltage control purpose in a closed-loop configuration. Fig. 7 shows the PLECS simulation results of the proposed converter for the parameters indicated. As it is expected from the results of steady-state analysis in (6.1)–(6.6), the dc components of the resonant capacitor voltages are different; however, the ac components of v_{Cr1} and v_{Cr2} are equal. In addition, the resonant inductor currents are equal, as stated in (6.7) and (6.8). Fig. 8 shows the corresponding experimental results of the proposed converter. It can be seen that the experimental results agree with the simulation results. The experimental results of Fig. 7 show that small mismatches between the components of the two series-resonant circuits result in slight differences between the

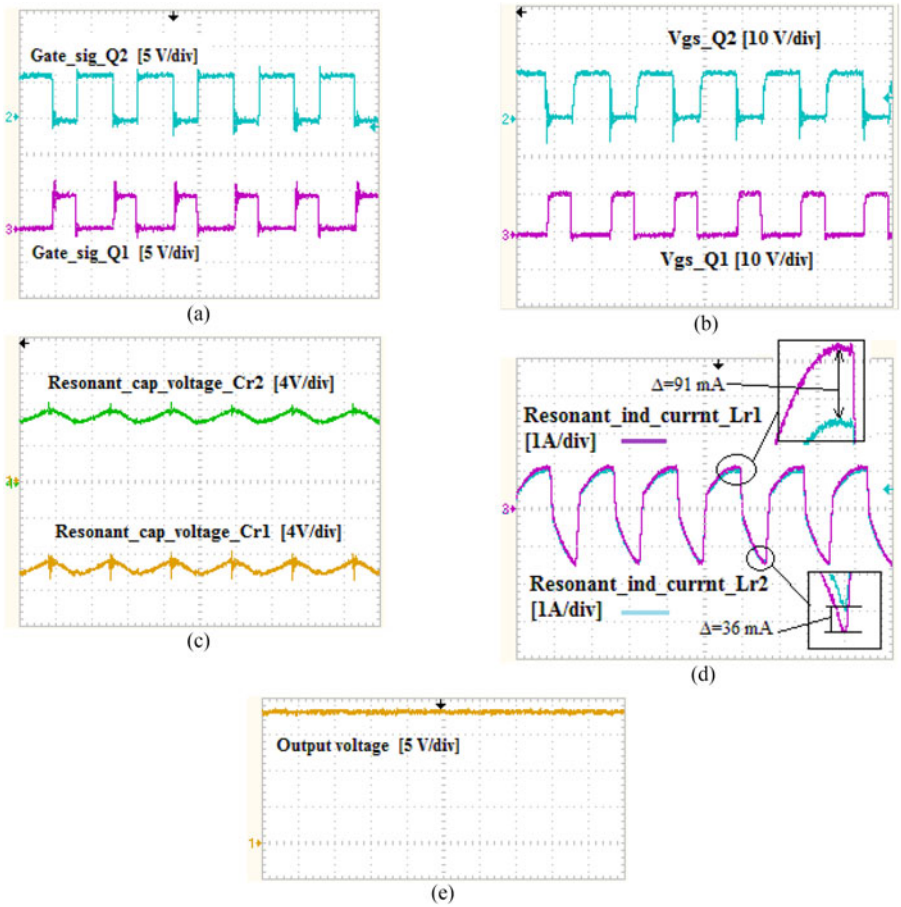

Fig. 8. Experimental results for the same case study ($V_d = 10$ V, $D = 0.6$, $f_{\rm sw} = 240$ kHz, $R_o = 30\ \Omega$, and $V_o = 18$ V). (a) Gate signals generated by PSoC 5LP, (b) gate-source voltage of MOSFETs, (c) resonant capacitor voltages, (d) resonant inductor currents, and (e) output voltage.

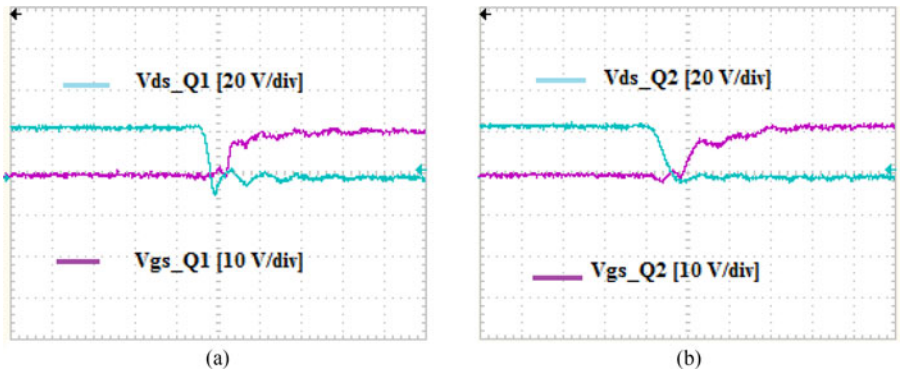

Fig. 9. ZVS operation for the MOSFETs ($V_d = 10$ V, $D = 0.6$, and dead time $= 80$ ns). (a) ZVS in $Q1$. (b) ZVS in $Q2$.

measured resonant inductor currents. However, the mismatches do not affect the performance of the converter.

The drain-to-source and gate-to-source voltages of the switches are shown in Fig. 9. The figure shows that for each switch, the drain-to-source voltage across the switch reaches zero before the gate-to-source voltage of the switch is applied, confirming the ZVS operation for $Q1$ and $Q2$ during switching transitions. The simulation and modeling results of the voltage conversion ratio of the proposed converter for wide range of duty ratio and different switching frequencies are shown in Fig. 10. These results were obtained by simulating the proposed topology in PLECS software and implementing the output voltage equation in (9) from the extended describing function modeling in the MATLAB environment. The differences between the simulation results in PLECS and the modeling results in MATLAB are negligible for $D < 0.7$. The slight deviations in the results for $D > 0.7$ are due to the assumed approximation in Section III (i.e., $v_{Lm}(\mathrm{t})$ and $sgn(i_{Lr1} + i_{Lr2})$ have the same

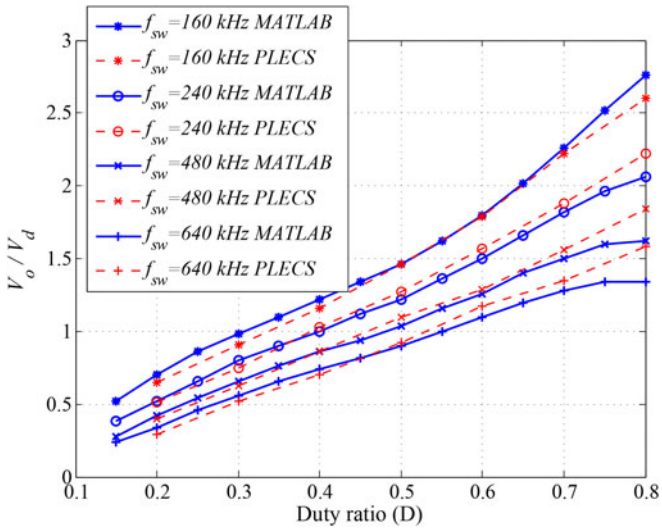

Fig. 10. Simulation and modeling results of voltage transfer ratio versus duty ratio for different switching frequencies ($V_d = 10$ V and $R_o = 30\ \Omega$).

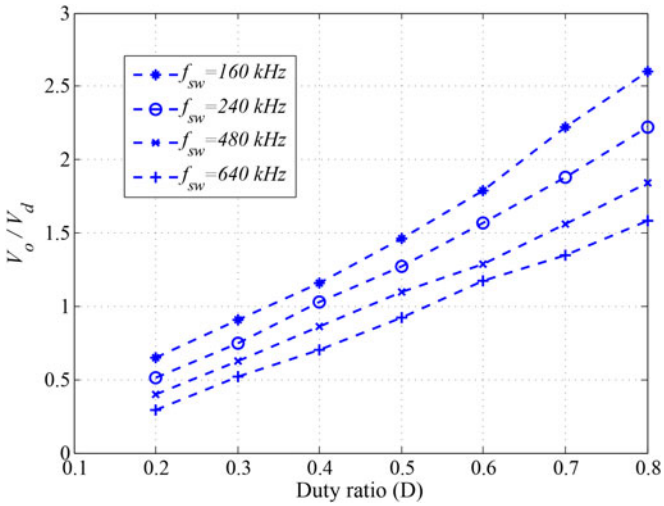

Fig. 11. Experimental results of voltage transfer ratio versus duty ratio for different switching frequencies ($V_d = 10$ V and $R_o = 30\ \Omega$).

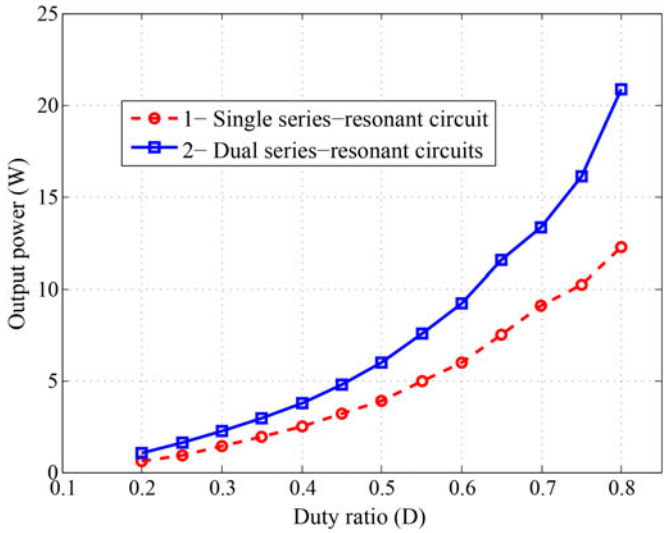

Fig. 12. Experimental comparison between the transferred power to the output load ($V_d = 10$ V, $f_{\rm sw} = 240$ kHz, and $R_o = 30\ \Omega$).

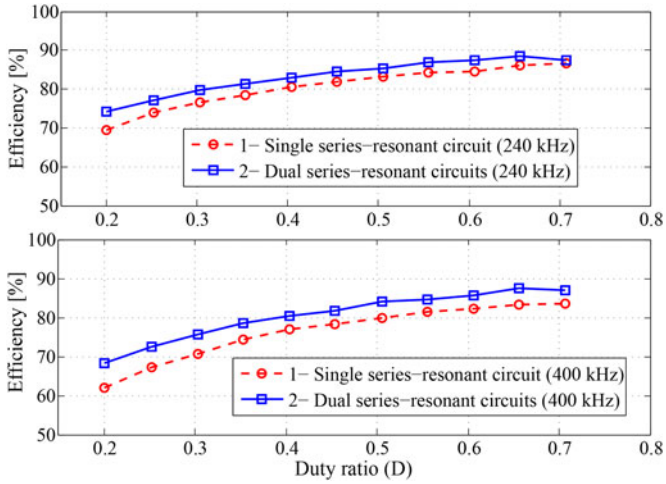

Fig. 13. Experimental comparison between efficiencies ($V_d = 10$ V and $R_o = 30\ \Omega$).

pulse width). The deviation between the pulse widths of $v_{Lm}(\mathrm{t})$ and $sgn(i_{Lr1} + i_{Lr2})$ increases for $D > 0.7$. Both the simulation and modeling results agree with the experimental results, which are shown in Fig. 11. It is observed that the proposed converter can be operated in the step-down and step-up modes depending on the duty ratio and switching frequency.

The experimental results of the proposed converter for the power transferred to the output load as a function of the duty ratio is shown in Fig. 12. The results are compared with the case of the single series-resonant circuit. The single series-resonant circuit converter is realized by removing the shunt jumper J_2 in Fig. 1 in order to disconnect the second series-resonant circuit (L_{r2} and C_{r2}) from the converter. It is worth mentioning that because of the balance operation of each series-resonant circuit in the proposed dual series-resonant circuit, removing either J_1 or J_2, yields the same results. Fig. 12 demonstrates that the proposed dual series-resonant dc–dc converter achieves improved power transfer ratio as D increases. For example, for $D = 0.6$, a 54% improvement in power transfer over the single series-resonant converter topology can be obtained. The experimental comparison of the efficiencies of conversion between the proposed dual series-resonant circuit topology and the single series-resonant circuit topology is shown in Fig. 13. The experimental conversion efficiency plots are obtained at two different switching frequencies (i.e., $f_{\rm sw} = 240$ kHz and $f_{\rm sw} = 400$ kHz). This figure shows the improvement in the conversion efficiency in a wide range of duty ratio for the proposed dual series-resonant dc–dc converter. It is also observed that the difference between the efficiencies of the single series-resonant topology and the dual series-resonant topology does not remain constant as the duty ratio increases. This is due to the nonlinear relationship between the duty ratio and output voltage for the same level of resonant inductor current.

V. Conclusion

An alternative topology of the active-clamping resonant dc–dc converter that uses a dual series-resonant topology was proposed. The two identical series-resonant circuits on the secondary side of the converter provide complementary paths to supply the load current without interruption during the complete operational modes of the converter, resulting in improved output power transfer capability of the converter. It features zero voltage turn-on for the switches and zero current turn-on for the output diodes, where the rise and fall slope of the diode current is limited by the slope of the current of the resonant circuit. Results from an experimental prototype of the proposed topology showed good agreement with simulation and modeling results. The experimental results confirmed the feature of the proposed topology that allows the output voltage to be regulated through either duty ratio of the PWM switching signal or switching frequency. In addition, the converter was able to operate in both step-down and step-up regimes. It was experimentally demonstrated that the proposed topology improves the power transfer capability and conversion efficiency of the converter. The proposed topology can be used as an alternative approach to the interleaving method, since it uses fewer numbers of active and passive components, resulting in reduced size and manufacturing cost of the converter for a given power rating of the dc–dc converter.

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