Online High-Power p-i-n Diode Junction Temperature Extraction With Reverse Recovery Fall Storage Charge

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***Abstract*—This paper proposes a method to extract the junction temperature of high-voltage and high-power p-i-n diodes. It is investigated that the swept-out charge during reverse recovery current fall time is affected by junction temperature variation, which makes the swept-out charge a possible thermo-sensitive electrical parameter (TSEP). Thanks to the specific package of high-power IGBT modules with p-i-n diodes, the swept-out charge of a p-i-n diode can be measured by the induced voltage v_{eE} on the parasitic inductor L_{eE} between Kelvin and power emitter terminals. In typical inductive half-bridge circuit, the comprehensive analysis of commutation between the upper p-i-n diode and lower enabled IGBT discloses the monotonic relationship among the reverse recovery charge, reverse current fall time, and junction temperature. A double pulse chopper circuit is used to validate the theoretical analysis. The experimental results show that the dependence between diode junction temperature and charge during the reverse recovery current fall time is approximately linear. A three-dimensional lookup table is calibrated and can be used to estimate the p-i-n diode junction operating temperature. Finally, an experimental comparison of four TSEPs for p-i-n diode is presented to verify the feasibility of the implementation of proposed TSEP.**

***Index Terms*—High-power p-i-n diodes, junction temperature extraction, reverse recovery charge, thermo-sensitive electrical parameter.**

I. Introduction

HIGH-POWER voltage source converters (VSCs) play an important role in renewable generation, high-voltage direct current (HVdc) transmission, adjustable-speed motor drives, electric locomotive, etc. [1]–[3]. High-power and high-voltage insulated gate bipolar transistor (IGBT) devices are core components in the employed high-power VSCs. With the development of semiconductor technology and advanced manufacturing, the switching power and frequency product of silicon-based power semiconductors are approaching the silicon material limits [4]. Taking Infineon as an example, so far, the maximum power capacities of compact IGBT modules $(140 \times 190\ \text{mm}^2)$ are up to $1.7\ \text{kV} \times 3.6\ \text{kA}, 3.3\ \text{kV} \times 1.5\ \text{kA}, 4.5\ \text{kV} \times 1.2\ \text{kA}$, and $6.5\ \text{kV} \times 0.75\ \text{kA}$ [5]. However, the IGBT capacity development still lags the power demand of high-power applications. For example, at the point of interconnection of France–Spain dc systems, a 401-level HVdc system with dc cables and filters can transmit the power of over 1000 megawatts (MW) [6]. An 8 MW wind turbines was reported in 2012, and the wind turbines up to 10 MW are being developed [7]. In order to achieve higher output power in high-voltage applications, many high-power multichip IGBT modules are connected in series and parallel. Furthermore, the service working conditions permit a very close approach to the limiting output capacity of IGBT modules. Hence, the resultant high-power IGBT reliability issues have drawn academic and industrial interest for decades [8]. In the practical operation, high-power IGBT failure mechanisms vary with external operational conditions, robustness of power devices, topologies, and related control methods. Hence, increasing studies are concerned with physics-of-failure mechanisms, which involve field data and statistics [9]–[11]. According to the related industrial statistics, one critical failure in power electronic systems is due to temperature-induced stresses, which accounts for about 55% of the total failure distribution [12]. Thus, the implementation of junction temperature (T_j) monitoring is more important than case temperature measurement. The key temperature indices are average T_j, swing amplitude of T_j, and peak T_j. Therefore, the online T_j measurement is the basis for the lifetime modeling, thermal stress calculation, and over temperature protection [13], [14].

Normally, the high accuracy T_j measurement is addressed by the physical contact methods, optical methods, and temperature sensitive electrical parameter (TSEP) methods [15]. Thermocouple and built-in thermistor are prone to measurement error due to their slow response. An optical infrared (IR) camera has the advantages of global temperature mapping. However, these optical methods require IGBT module modification like unpackaging and grease gel removal. Moreover, the bus bar located on the top of modules should be removed for T_j mapping in IR-based methods. Recently, some IGBT modules have emerged with an on-chip temperature sensor [16]. Though this temperature measurement approach can provide accurate T_j information, it only monitors a specific region instead of the average temperature of the multichip module. Therefore, a TSEP-based temperature extraction method is the most likely to yield an online monitoring approach without module modification, at microsecond response level [15]. Many TSEP candidates have been investigated and reviewed in

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[15], [17], and [18]. It is concluded that the sensitivity, linearity, accuracy, generalization, and calibration are the most important considerations for evaluating TSEP candidate performance.

However, most TSEP candidates are orientated around IGBT modules, rather than the corresponding antiparallel p-i-n diodes. Voltage drop at low current source injection [19], short-circuit current [20], turn-off time [21], and threshold voltage v_{th} [22] based TSEPs have been applied for the online estimation of IGBT T_j. Since the device manufacturer trades off the IGBT area to that devoted to diode area, the antiparallel p-i-n diodes can be more thermally stressed than IGBTs in some severe working conditions [23], [24]. In the case of wind turbine system with partial-scale power converter, the antiparallel p-i-n diodes in rotor-side converter would withstand the maximum thermal stress at super-synchronous mode [24]. In [25], the forward voltage drop at low current is used as a TSEP for p-i-n diodes. However, an auxiliary current source injection circuit is required for T_j extraction procedure. The injection current is controlled at a fixed milliampere level to avoid self-heating effects, but the auxiliary circuit should be designed to withstand high voltages.

To solve these problems, a dynamic TSEP method without a current injection circuit, based on the maximum recovery current di_d/dt is proposed in [26]. The temperature-dependent reverse recovery di_d/dt can be extracted from the induced voltage v_{eE} across the parasitic inductor L_{eE} between the Kelvin emitter and power emitter. In this paper, a new TSEP method based on reverse recovery stored charge is proposed. The monotonic relationship among the diode stored charge, forward current, and junction temperature is built. Besides, the swept-out charge can also be extracted from the induced voltage v_{eE}. Thus, the swept-out charge can be employed as a measurable TSEP for p-i-n diodes. Compared with the dynamic maximum recovery current di_d/dt-based TSEP [26], the proposed TSEP is more capable of large current and high T_j range.

This paper is organized as follows: In Section II, the basic idea of the online temperature measurement method for the high-power p-i-n diode is introduced. In Section III, the proposed temperature-dependent TSEP and the extraction method are analyzed. The relationship between reverse recovery stored charge and diode temperature is also discussed. In Section IV, the substantiating experimental results and comparisons are presented, while the findings form the final Section V.

II. Reveres Recovery Charge Extraction

In this section, the relationship between the carrier profile in the on-state and T_j is introduced. On the basis of a two-level VSC, the charge in p-i-n diode in the on-state can be extracted during a commutation transition. The extraction procedure is then discussed for nonideal p-i-n diode characteristics.

A. Concept and Feasibility of Online Diode Stored Charge

For the voltage ratings of at least 1.7 kV, the high-voltage p-i-n diode usually consists of a sandwiched $p^+n^-n^+$ structure [27]. The n^- drift region is lightly doped to support high voltages when reverse blocking. In the case of on-state high-level injection, the carrier distribution in the base region of a p-i-n diode is plotted in Fig. 1. Charge neutrality makes the holes and electron concentrations in the n^- drift region approximately equal as the n^- doping concentration can be ignored.

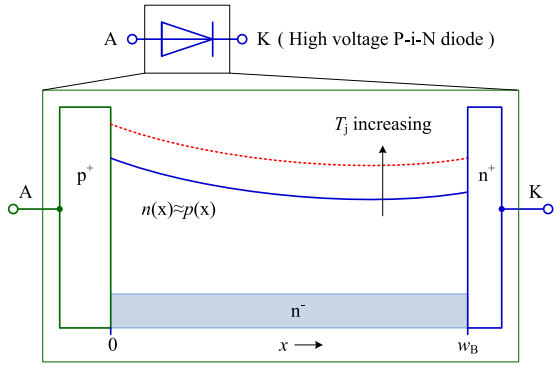


Fig. 1. Distribution of carries in high-voltage p-i-n diode.

The mean carrier concentrations $\overline{n}$ and $\overline{p}$ in the base region are given by

$$\overline{n} = \overline{p} = \frac{1}{w_B}\int_{-1/2wB}^{1/2wB} pdx = \frac{j\tau_{HL}}{qw_B} \tag{1}$$

where w_B is the length of base region, j is current concentration, τ_{HL} is the high-level carrier lifetime, and q is per unit charge. The base region stored charge Q_F under forward current is

$$Q_F = qAw_B\overline{p} \tag{2}$$

where A is the active chip area of the p-i-n diode. Inserting (1) into (2), the stored charge can be obtained as

$$Q_F = I_F\tau_{HL}. \tag{3}$$

Q_F is proportional to forward current carrier lifetime. The relationship between τ_{HL} and T_j is

$$\tau_{HL} = \tau_0\left(\frac{T_j}{300}\right)^k \Rightarrow Q_F = I_F\tau_0\left(\frac{T_j}{300}\right)^k \tag{4}$$

where the exponent k is greater than 1 [18]. As a result, the stored charge in the base region increases with T_j. During the turn-off reverse recovery process, the stored charge is swept out of the base region. For an assembled converter with fixed gate driver and bus bar, the amount of swept-out charge is related to bus voltage V_{dc}, load current, I_L, and T_j variations. Once the relationship between diode T_j and related parameters is determined and calibrated, the real-time diode T_j can be extracted by the temperature-dependent stored charge.

B. Reverse Recovery Current Measurement Method

Fig. 2 shows a compact IGBT module rated at 3.3 kV/800 A with associated antiparallel p-i-n diodes and its equivalent circuit. The high output current from a single IGBT module is achieved through power devices parallel operation, where two separate IGBT devices with associated p-i-n diodes in parallel, share a common gate driver. In order to reduce the induced affects due to the impedance of the drive loop section in the principal current path, two emitter terminals are provided in high-power compact IGBT modules. One is the auxiliary

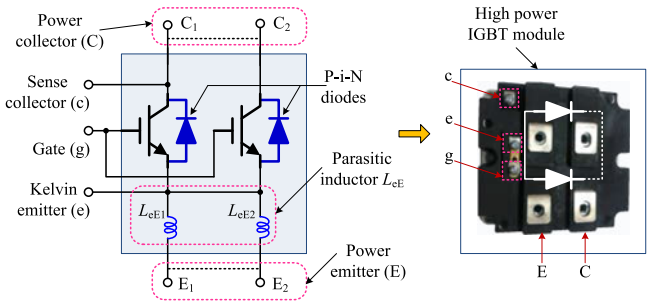


Fig. 2. High-power IGBT module and its equivalent circuit.

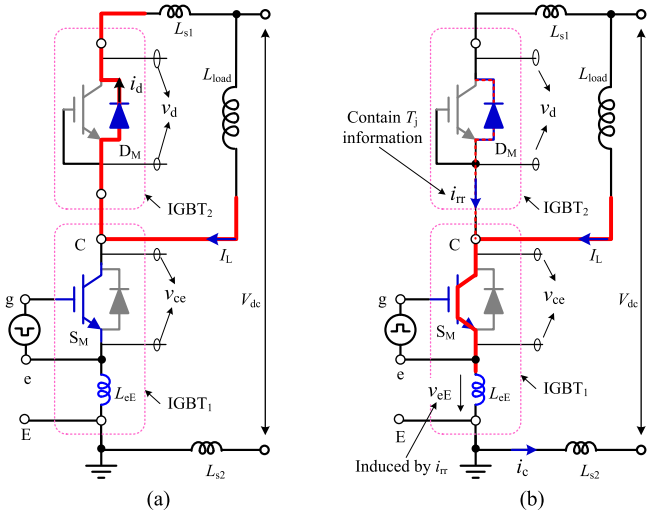


Fig. 3. Commutation between upper diode and lower IGBT (a) diode freewheeling stage and (b) diode reverse recovery stage.

Kelvin emitter e for gate driver, and the other is the power emitter E for power flow delivery. While the power emitter terminals E_1 and E_2 are internally interconnected, there is no electrical connection within the module between the power collector terminals C_1 and C_2. The internal connection inductors L_{eE1} and L_{eE2} are equivalent to a single parasitic inductor L_{eE}.

A two-level half-bridge topology is shown in Fig. 3, where the parasitic inductors L_{s1}, L_{s2}, and L_{eE} are considered in the equivalent circuit. The parasitic inductor L_{s1} is the combination of series parasitic inductors in the positive bus bar and diode under test D_M, and L_{s2} is the series parasitic inductors of negative bus bar and lower IGBT module, except for L_{eE}. The parasitic inductors L_{eE} between Kelvin and power emitters are the intermediary for evaluating the reverse recovery current of D_M. Because of a highly inductive load L_{load}, the load current I_L can be considered constant during the relatively short commutation period, with a fixed bus voltage V_{dc}.

The commutation occurs between upper p-i-n diode D_M and lower switching device S_M. When I_L begins to commutate from diode D_M to enabled IGBT S_M, the reverse recovery current i_{rr} of D_M, which is T_j dependent, induces a measureable voltage v_{eE} across the parasitic inductor L_{eE}. Since v_{eE} caused by the reverse recovery current i_{rr} contains D_M temperature

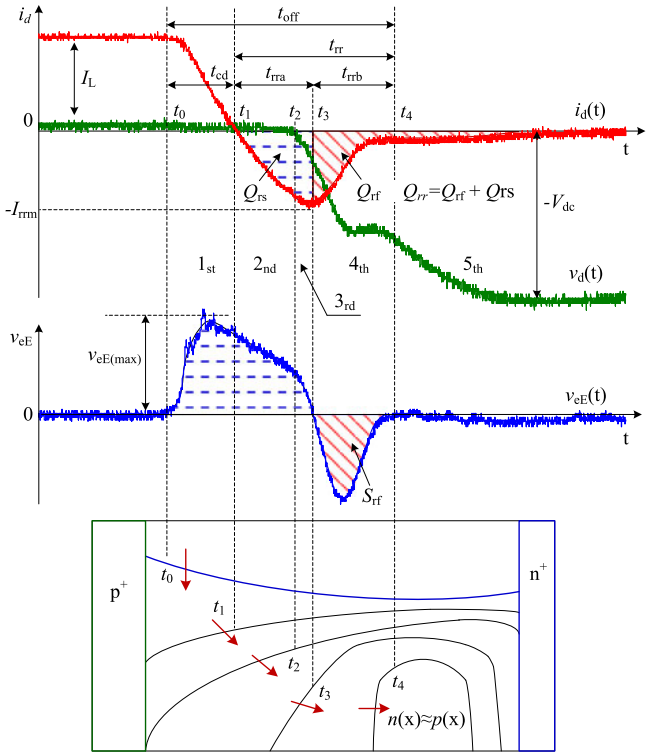


Fig. 4. Turn-off waveforms and changes of carrier profile of high power p-i-n diode with induced inductor voltage v_{eE}.

information, T_j of inspected D_M can be extracted by sampling v_{eE} during the commutation.

C. Analysis of Nonideal Diode Reverses Recovery Process Based on v_{eE}

The behavior of inspected diode during the turn-off process depends on the switching characteristics of S_M and the semiconductor properties of p-i-n diodes. The modeling and physics mechanisms of p-i-n turn-off transition are disclosed in [28] and [29]. The aim of this section is to introduce the relationship between p-i-n diode turn-off transition and the induced v_{eE} during commutation.

In Fig. 4, the key turn-off waveforms and corresponding p-i-n diode carrier profile changes are depicted. The nonideal high-voltage p-i-n diode turn-off process can be presented in five sequential phases. Before time t_0, the lower S_M is turned OFF and the load current I_L flows through the antiparallel diode. Since no collector current flows to S_M, v_{eE} is zero before the commutation.

Stage 1 $[t_0, t_1]$: At t_0, once the gate–emitter voltage v_{ge} exceeds the threshold gate voltage v_{th}, the diode current i_d, which initially equals I_L, begins to decline with a nearly linear slope. This linear slope is reflected by the induced v_{eE}. The maximum fall slope of collector current i_c occurs in this stage, by investigation of the maximum $v_{eE(\max)}$

$$v_{eE(\max)} = -L_{eE}\frac{di_c}{dt}\bigg|_{(\max)}. \tag{5}$$

During this stage, the inspected D_M retains a low forward voltage. The induced v_{eE} is mainly affected by the switching speed of S_M and is unrelated to the diode characteristics.

Stage 2 $[t_1, t_2]$*:* At t_1, the forward current though D_M is decreased to zero and the reverse recovery process begins. Because a reverse bias depletion region in n^- region cannot yet form, the diode remains forward biased with reduced forward voltage v_d. The reverse recovery current i_{rr} at this stage is calculated by subtracting i_L from the total collector current $i_c, i_{rr} = i_c - I_L$. At t_2, it can be argued that the carrier concentration at the left p^+-n^- junction falls to zero, so the diode can start to support reverse voltage [30]. The measured v_{eE} has a linear decline, which means the absolute di_c/dt decreases.

Stage3 $[t_2, t_3]$*:* As the depletion region widens after t_2, diode D_M begins to withstand the reverse blocking voltage v_d. In the analysis of [30], the small reverse blocking voltage v_d can be omitted when compared with the bus voltage V_{dc} during this stage. At t_3, the induced v_{eE} falls to zero because the reverse recovery current rate di_d/dt of D_M equals zero.

Stage 4 $[t_3, t_4]$*:* The measured v_{eE} goes negative and the diode reverse current begins to fall to zero from negative peak $-I_{rrm}$. The diode current $di_d(t)/dt$ is defined as the recovery *di/dt* during this stage [31]. Unlike conventional low-voltage diode technology, the high-power p-i-n diode is designed as soft recovery diode. This characteristic means that the overshoot of v_d is lower than V_{dc} to decrease the likelihood of overvoltage failure. As a result, there is a lower overshoot voltage and no oscillatory recovery, as with fast low-voltage switching diodes [32].

Stage 5 $[t_4, t_5]$*:* The diode current now shows a soft recovery performance, and is defined as diode tail current. Since the current rate change is slow, the measured induced v_{eE} is near zero, compared with the earlier stages. Undesirable power losses occur, and the charge associated with the tail current are not adequately reflected by the near zero v_{eE}.

D. Relationship Between v_{eE} and the Proposed TSEP

Assuming the excess carriers in the n^- base region are swept out at a linear rate, p-i-n diode reverse recovery current can be simplified to a triangle [30], [33]. The simplified p-i-n diode turn-off waveform and Q_{rf} calculation are plotted in Fig. 5. The reverse recovery charge can be subdivided into the charge Q_{rs} occurring during storage time t_{rra} and the charge Q_{rf} occurring during reverse current fall time t_{rrb}. Hence, Q_{rr} is the sum of Q_{rs} and Q_{rf}, viz.

$$Q_{rr}(T_j) = Q_{rs} + Q_{rf}. \tag{6}$$

The zero crossing point of v_{eE} at t_3 forms the boundary between the two charge parts. During the *Stage 4*, the measured v_{eE} is induced by the variation of i_d shown as

$$v_{eE}(t) = L_{eE}\frac{di_c(t)}{dt} = L_{eE}\frac{di_d(t)}{dt}. \tag{7}$$

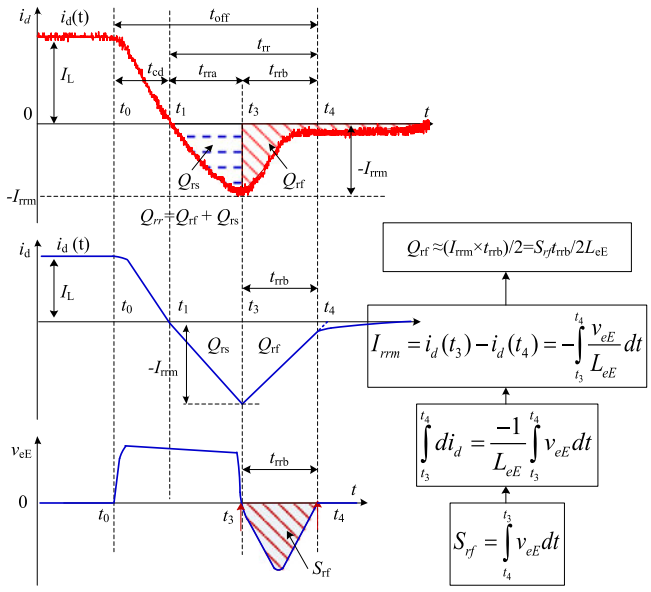


Fig. 5. Simplified turn-off waveforms and calculation process of Q_{rf}.

By integrating the induced voltage v_{eE} in (2), the reverse recovery current i_d during *Stage 4* can be estimated as

$$i_d(t) = -I_{rrm} + \int \frac{v_{eE}(t)}{L_{eE}}dt. \tag{8}$$

The peak reverse recovery current I_{rrm} can be evaluated by the definite integration over *Stage 4*

$$I_{rrm} = \frac{1}{L_{eE}}\int_{t_3}^{t_4} -v_{eE}\,dt = \frac{1}{L_{eE}}\int_{t_4}^{t_3} v_{eE}\,dt = \frac{S_{rf}}{L_{eE}} \tag{9}$$

where S_{rf} is the area enclosed by negative v_{eE}. On the basis of estimated reverse recovery current during *Stage 4*, the charge Q_{rf} during this stage can be obtained from (4)

$$Q_{rf} \approx 1/2 I_{rrm} t_{rrb} = 1/2 \frac{t_{rrb} S_{rf}}{L_{eE}}. \tag{10}$$

In (5), L_{eE} can be considered a proportionality constant for a particular module, which is unrelated to T_j. The values of t_{rrb} and S_{rf} can be extracted from the negative part of the induced v_{eE} at a time. In terms of the positive part of v_{eE} before t_3, the area surrounded by positive v_{eE} contains both forward load current and reverse recovery current information. It is difficult to determine the location of t_1 by only using v_{eE}, so that the impacts of collector current i_c at *Stage 1* cannot be excluded from reverse recovery current.

In Fig. 6, the calculation of Q_{rf} flowchart using the measured v_{eE} is demonstrated. The measurable v_{eE} can be captured during the p-i-n diodes turn-off transition. Then, the negative part of the induced v_{eE} will be extracted for subsequent processing. The length of reverse current fall time t_{rrb} can be extracted by a time counter because the voltage zero-crossing points are the start and end points of the reverse current fall time. The measured $v_{eE}(t_3 \sim t_4)$ during *Stage 4* is integrated from t_3 to t_4 and the negative v_{eE} area can be extracted by an analog

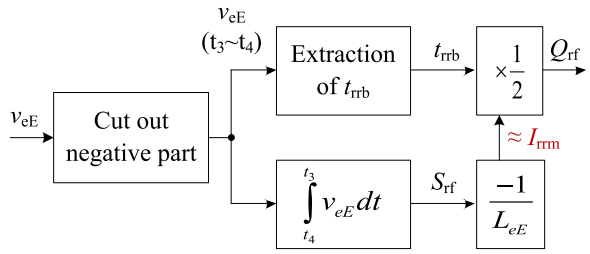


Fig. 6. Calculation flowchart of Q_{rf} by using measured v_{eE}.

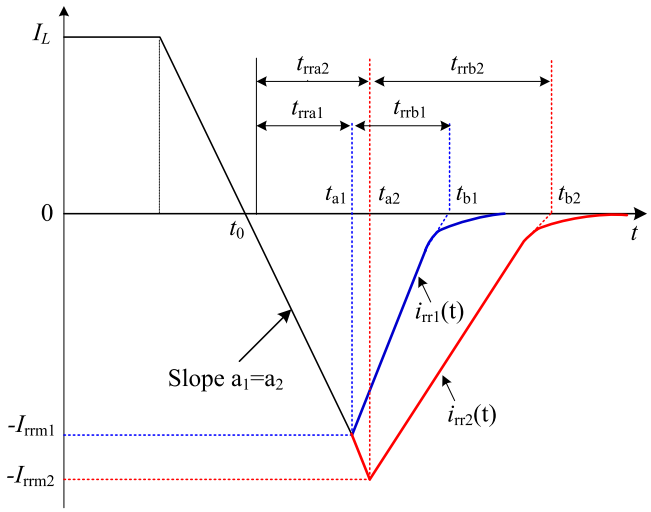


Fig. 7. Simplified p-i-n diodes reverse recovery current under different diode T_j.

integrator [34]. Then, the temperature-dependent charge Q_{rf} can be calculated, for a constant L_{eE}.

The charge Q_{rf} during the reverse current fall time t_{rrb} can be selected as a suitable TSEP for p-i-n diode T_j extraction. Accordingly, the negative part of induced v_{eE} can be used for assessing the charge Q_{rf} extraction during p-i-n diode turn-off transition.

III. Relationship Between Charge Q_{rf} and Junction Temperature T_j

The relationship among the negative part of v_{eE}, charge Q_{rf}, and T_j changes is determined in this section. When the diode voltage v_d at *Stage 3* is insignificant compared with V_{dc}, the collector current from *Stage1* to *Stage 3* are the regions when the p-i-n diode is forward biased. During this period, the di_d/dt current slope is determined by the external circuit parameters and the switching speed of enabled IGBT. Since the value of v_d after the peak $-I_{rrm}$ is sufficiently high, the diode current slope di_d/dt is affected by v_d. As a result, the current slope is constant before the peak $-I_{rrm}$ independent of diode T_j. The simplified diode reverse recovery current diagrams at different diode T_j with a fixed IGBT temperature are plotted in Fig. 7. Moreover, the p-i-n diode T_j is defined as T_D and two junction temperatures T_{D1} and T_{D2} are shown, where T_{D2} is higher than T_{D1}. The definitions plotted in Fig. 7 are listed in Table I.

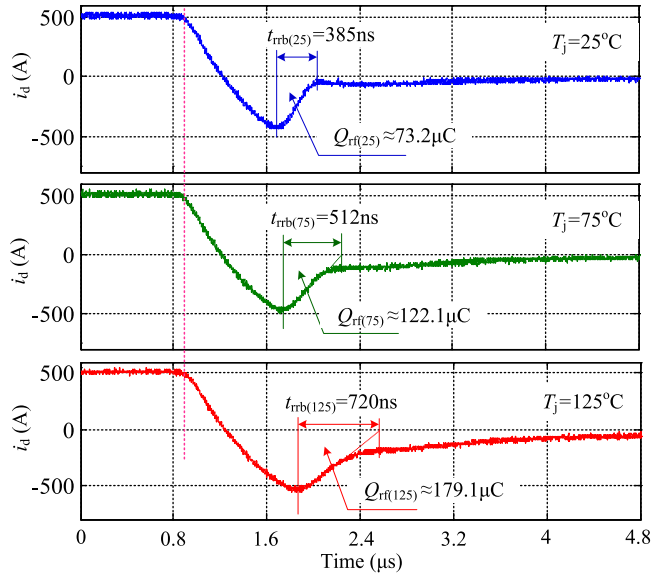


Fig. 8. Turn-off waveforms of p-i-n diode current i_d at three different diode T_j (V_{dc} = 1600 V, I_L = 500 A and T_{Ij} = 25°C).

TABLE I
Electrical Definitions for Different Diode Temperatures

Notation	T_{D1}	T_{D2}
Reverse recovery current	i_{rr1}	i_{rr2}
Current slope before reverse peak current	$a1$	$a2$
Reverse peak current	I_{rrm1}	I_{rrm2}
Reverse peak current time point	t_{a1}	t_{a2}
Cut-off time of reverse recovery current	t_{b1}	t_{b2}
Recovery time	t_{rrb1}	t_{rrb2}
Storage time	t_{rra1}	t_{rra2}
Diode softness factor	$SF1$	$SF2$
Charge occurring during reverse current fall time	Q_{rf1}	Q_{rf2}

The ratio of recovery time t_{rrb} to storage time t_{rra} is defined as the diode softness factor SF, viz.

$$SF = \frac{t_{rrb}}{t_{rra}}. \tag{11}$$

Since the current slopes before peak I_{rrm} for different T_j are equal, as plotted in Fig. 7

$$\frac{I_{rrm1}}{t_{rra1}} = \frac{I_{rrm2}}{t_{rra2}} \Rightarrow \frac{I_{rrm2}}{I_{rrm1}} = \frac{t_{rra2}}{t_{rra1}}. \tag{12}$$

For a fixed load current, the softness factor SF increases with T_j increasing [31]. That is

$$\frac{t_{rrb1}}{t_{rra1}} < \frac{t_{rrb2}}{t_{rra2}} \Rightarrow \frac{t_{rra2}}{t_{rra1}} < \frac{t_{rrb2}}{t_{rrb1}}. \tag{13}$$

The peak I_{rrm} increases with diode T_j, thus (12) can be substituted into (13)

$$1 < \frac{I_{rrm2}}{I_{rrm1}} = \frac{t_{rra2}}{t_{rra1}} \Rightarrow 1 < \frac{I_{rrm2}}{I_{rrm1}} < \frac{t_{rrb2}}{t_{rrb1}}. \tag{14}$$

In (14), certain generalizations can be derived since $I_{rrm1} < I_{rrm2}$ and $t_{rrb1} < t_{rrb2}$. With increasing T_j, not only SF but also t_{rrb2}/t_{rrb1} increases. Therefore, the charge during

TABLE II
PROTOTYPE SPECIFICATIONS

Parameters	Value	Parameters	Value
IGBT module (Fuji)	1MBI800UG-330	Gate driver Voltage (v_{ge})	+15 V on/–10 V off
Bus voltage (V_{dc})	1400–1800 V	Turn-on/off gate resistance (R_{on}/R_{off})	2.4 Ω/3.75 Ω
Bus capacitor (C_{dc})	1000 μF	p-i-n diode T_j	25–125 °C
Load current (I_L)	200–600 A	L_{eE} inductance	≈6 nH
Load inductor (L_{load})	400 μH	Commutation parasitic inductor (L_{loop})	≈265 nH

the reverse current fall time Q_{rf} for different diode T_j is given by

$$I_{rrm1}t_{rrb1} < I_{rrm2}t_{rrb2} \Rightarrow Q_{rf1} < Q_{rf2}. \quad (15)$$

Equation (15) implies that Q_{rf} increases with higher diode T_j under fixed external operation parameters and the relationship between T_j and Q_{rf} is monotonic at *Stage 4*. As a result, the reverse current fall time Q_{rf} during can be employed as an effective TSEP, which reflects T_j variation of p-i-n diode.

IV. EXPERIMENTAL INVESTIGATION

A. Experimental Verification

In order to verify the effectiveness of the proposed TSEP method, a double pulse test platform shown in Fig. 3 has been used to assess two 3.3 kV/800 A high-power high-voltage IGBT modules. The specifications of test parameters are shown in Table II, where the bus voltage is 1400–1800 V and the load current is 200–600 A. A 1000-μF bus capacitor bank maintains V_{dc}. Since the inductance of air coil load is 400 μH, I_L can be considered constant during switching period. The total commutation parasitic inductance is about 265 nH, which can be obtained by the maximum current change rate and its corresponding turn-off peak collector voltage. In order to eliminate the temperature impacts of the enabled IGBT, the junction temperatures of upper module and lower module are maintained by two separated heat plates. The junction temperature of upper p-i-n is controlled and varied between 25 and 125 °C, while the temperature of lower enabled IGBT T_{Ij} is fixed to 25 °C. The data postprocessing uses MATLAB software.

In fact, during the IGBT turn-on process, the effect of gate current i_{ge} would also induce an additional voltage variation on L_{eE} [35]. The induced v_{eE} caused by di_{ge}/dt occurs when the gate voltage v_{ge} is lower than the threshold voltage v_{th}. At that stage, the enabled IGBT has not been turned ON successfully. Subsequently, the second v_{eE} variation induced by the turn-on collector current containing the reverse recovery current is the focus of this study. This paper mainly focuses on the temperature dependence between the reverse recovery current and the corresponding v_{eE} when I_L begins to commutate from diode to IGBT. Hence, the previous voltage variation induced by di_{ge}/dt would not be discussed in the following experimental results.

Fig. 8 shows the turn-off diode current i_d waveforms at three different diode junction temperatures, for the same working

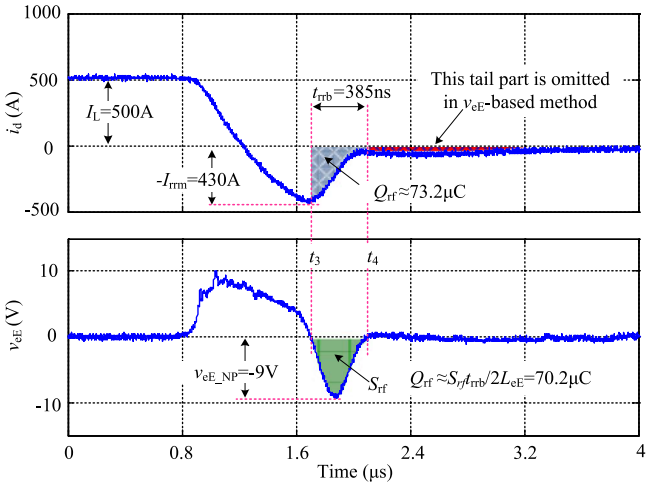


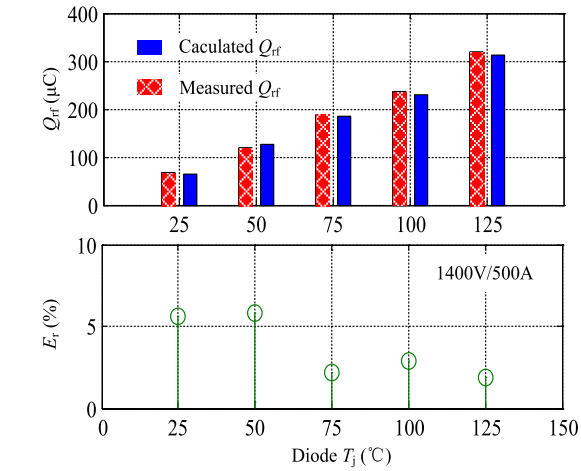
Fig. 9. Waveforms of diode current i_d and induced v_{eE} (V_{dc} = 1600 V, I_L = 500 A and $T_j = T_{Ij}$ = 25°C).

conditions of V_{dc} = 1600 V, I_L = 500 A, and commutation IGBT junction temperature T_{Ij} = 25°C. At T_j = 25°C, the reverse current fall time $t_{rrb(25)}$ is about 385 ns, and the related $Q_{rf(25)}$ is 73.2μC. The fall time increases to 512 ns with the related $Q_{rf(75)}$ increasing to 122.1 μC at 75 °C. When the diode T_j increases to 125 °C, $t_{rrb(125)}$ is 720 ns and $Q_{rf(125)}$ is 179.1 μC. For the fixed V_{dc} and I_L, the reverse current fall time increases and the related Q_{rf} also increases as T_j increases. These measured results correspond to the analysis in the previous section.

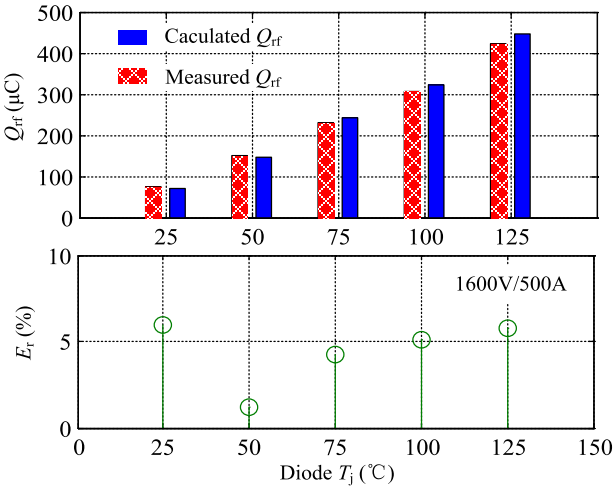
The turn-off current i_d and the related induced voltage v_{eE} at V_{dc} = 1600 V, I_L = 500 A and $T_j = T_{Ij}$ = 25°C are plotted in Fig. 9. The peak reverse recovery current is 430 A, and the related negative peak voltage v_{eE_NP} is about –9 V. It is worth noting that there would be a tail current due to the soft behaviors at the high diode T_j operation after t_4. The reverse recovery current change rate di_d/dt becomes very small but is not zero. In terms of the high-temperature reverse recovery process, when the reverse recovery current reduced to a value less than 10% of I_{rrm}, the whole reverse recovery process can be considered completed in theory. Therefore, the tail current part cannot be counted in the calculation of reverse recovery charge. As a result, the most of reverse recovery storage charge i_{rf} can be extracted by the v_{eE}-based method.

A relatively fixed L_{eE} is the prerequisite for calculating the Q_{rf} when using the induced v_{eE}. For the inspected module, the parasitic inductance L_{eE} is approximately 6 nH. The recovery time t_{rrb} can be extracted by setting a –0.5 V threshold voltage in the data postprocessing of MATLAB. Compared with the extracted measured charge Q_{rf} 73.2 μC, the calculated Q_{rf} by (10) is 70.2 μC. Therefore, the extracted Q_{rf} can be predicted by using the negative v_{eE} area, S_{rf}, and the related t_{rrb} at a given L_{eE}. Both S_{rf} and t_{rrb} can be extracted concurrently from the induced v_{eE}. The accuracy of the proposed calculation method can be evaluated by using the error rate E_r

$$E_r = \frac{\left|Q_{rf(irr)} - Q_{rf(veE)}\right|}{\left|Q_{rf(irr)}\right|} 100(\%) \quad (16)$$



(a)



(b)

Fig. 10. Error rate E_r between measured value and calculated Q_{rf}, at different T_j and working conditions: (a) $V_{dc} = 1400$ V and $I_L = 500$A, (b) $V_{dc} = 1600$ V and $I_L = 500$ A.

where $Q_{rf(irr)}$ is the measured charge, from the reverse recovery current during the fall time from $-I_{rrm}$ to 10% of $-I_{rrm}$, and $Q_{rf(veE)}$ is the calculation charge using (10). In the condition of $T_j = T_{Ij} = 25°$C, the error E_r between the measured value from the reverse recovery current and calculated value from v_{eE} is plotted in Fig. 10.

The maximum E_r is 5.8% at $V_{dc} = 1400$ V and $I_L = 500$ A in Fig. 10(a), while the maximum error rate E_r at $V_{dc} = 1600$ V and $I_L = 500$ A is 5.1%. The practical measured Q_{rf} can be precisely calculated and predicted by using the induced v_{eE}. Since the temperature dependent Q_{rf} during the reverse recovery process can be calculated from v_{eE},Q_{rf} is an effective TSEP for diode T_j extraction. The sensitivity ratio of calculated Q_{rf} at 1400 and 1600 V under $I_L = 500$ A is about 2.5 and 3.8 μC/°C. Hence, the sensitivity ratio of calculated Q_{rf} increases with rising of V_{dc}.

A three-dimensional (3-D) plot of Q_{rf} calculated from the induced v_{eE} as a function of the load current and diode T_j at $V_{dc} = 1400$ V is shown in Fig. 11. For fixed

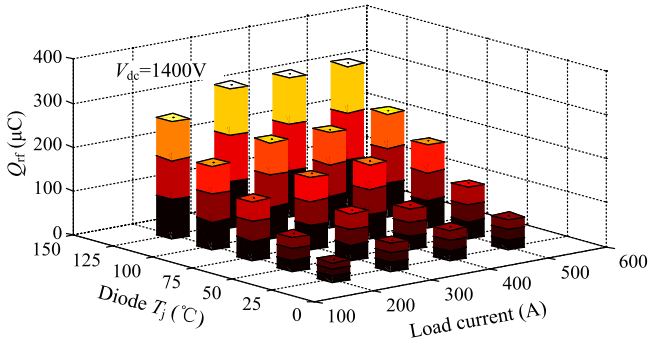


Fig. 11. Three-dimensional database of Q_{rf} with varied p-i-n junction temperature and load current, at $V_{dc} = 1400$ V and $T_{Ij} = 25°$C.

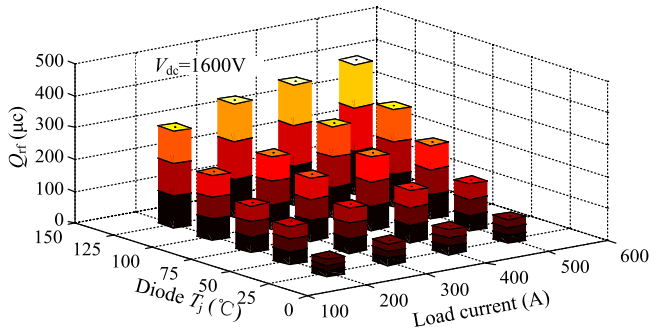


Fig. 12. Three-dimensional database of Q_{rf} with varied p-i-n junction temperature and load current at $V_{dc} = 1600$ V and $T_{Ij} = 25°$C.

$V_{dc} = 1400$ V and $T_{Ij} = 25°$C, the calculated Q_{rf} monotonically increases with the increasing of diode T_j. The swept out Q_{rf} is proportional to the load current with constant T_j and V_{dc}. The maximum Q_{rf} in Fig. 11 is about 318.2 μC at a test condition of $V_{dc} = 1400$ V, $T_j = 125°$C, and $I_L = 500$ A. When the test condition is $V_{dc} = 1400$ V, $T_j = 25°$C, and $I_L = 200$ A, the calculated Q_{rf} decreases from a maximum to a minimum value 69.1 μC.

In Fig. 12, the created 3-D database reflects the relationship between diode T_j and I_L at $V_{dc} = 1600$ V. With increase in bus voltage, Q_{rf} for the same I_L and T_j is higher than that with $V_{dc} = 1400$ V. The maximum Q_{rf} in Fig. 12 is about 409 μC at the test condition of $V_{dc} = 1600$ V, $T_j = 125°$C, and $I_L = 500$ A. This is about 90.5 μC more than at $V_{dc} = 1400$ V. Under the test condition of $V_{dc} = 1600$ V, $T_j = 25°$C and $I_L = 500$ A, minimum Q_{rf} is reached, viz., 73.2 μC. Based on the 3-D database illustrated in Figs. 11 and 12, the variations of Q_{rf} with p-i-n diode T_j at different V_{dc} and I_L are revealed. As V_{dc} increases from 1400 to 1600 V, the measured swept out Q_{rf} increases at the same diode T_j, commutation IGBT T_{Ij} and I_L. Since the swept-out speed increases as V_{dc} increases, more stored charge is swept out and less time for the recombination.

However, the diode current slope after the peak $-I_{rrm}$ is affected by the junction temperature of enabled IGBT. Therefore, there is also a dependence of Q_{rf} on the commutation IGBT junction temperature. For a given power module, a

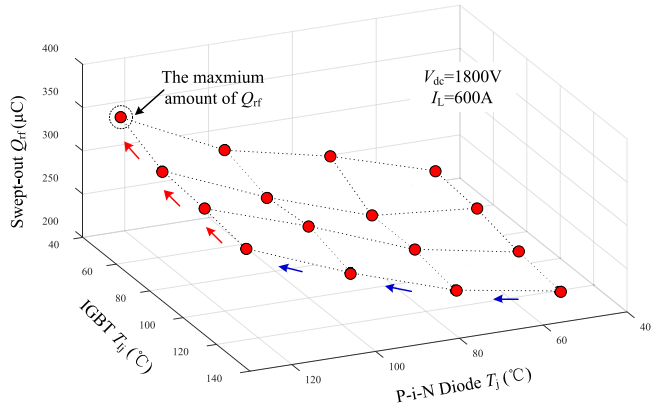


Fig. 13. Three-dimensional database of Q_{rf} with variety of IGBT T_j and p-i-n diode T_j at bus voltage $V_{dc} = 1800$ V, $I_L = 600$ A.

3-D database of Q_{rf} at different IGBT T_j and p-i-n diode T_j with $V_{dc} = 1800$ V, $I_L = 600$ A is depicted in Fig. 13. As the carrier lifetime increases with diode T_j decreasing, more stored charge should be swept out in the condition of higher T_j. Moreover, the switching speed of the commutated IGBT increases as T_{Ij} decreases; the excess carriers in the diode can be fast swept out, thereby avoiding the carrier recombination. As a result, the maximum amount of Q_{rf} can be measured at IGBT $T_{Ij} = 25°$C and diode $T_j = 125°$C.

Once the relationship among the swept-out Q_{rf}, bus voltage V_{dc}, load current I_L, commutation IGBT T_{Ij}, and p-i-n diode T_j are practically calibrated in advanced, the real-time operational diode T_j can be determined by means of the proposed Q_{rf}, which is precisely calculated by the measured v_{eE}. The demonstrated multidimensional database can be used as a lookup table to extract p-i-n diode T_j under operational conditions. Since the commutation loop of each power module is different for the particular layout design, the multidimensional database should be built for each alternate power module.

B. Comparisons of State-of-the-Art TSEPs and Proposed TSEP

In previous studies, the state-of-the-art TSEPs for high power diodes can be summarized as the voltage at low current injection V_{sat} [25], voltage at high current injection V_f [36] and the negative peak voltage of $v_{eE}(v_{eE\_NP})$ induced by the maximum turn-off di_d/dt [26]. For the inspected antiparallel diode of 1MBI800UG-330, the experimental comparisons of three published state-of-the-art TSEPs and the proposed TSEP in this study are presented in Fig. 14.

In terms of the static characteristics, the dependences of diode T_j on V_{sat} and V_F are extracted by a semiconductor parameter analyzer HP4155B from Hewlett-Packard and datasheet, as shown in Fig. 14(a) and (b). For inspected p-i-n diodes, V_{sat} shows a negative correlation and has good linearity with diode T_j under 10 and 20 mA current injection. Nevertheless, the current source injection circuit and sampling circuit are designed to withstand high voltages for the implementation of online diode T_j extraction. Moreover, in order to separate the inspected

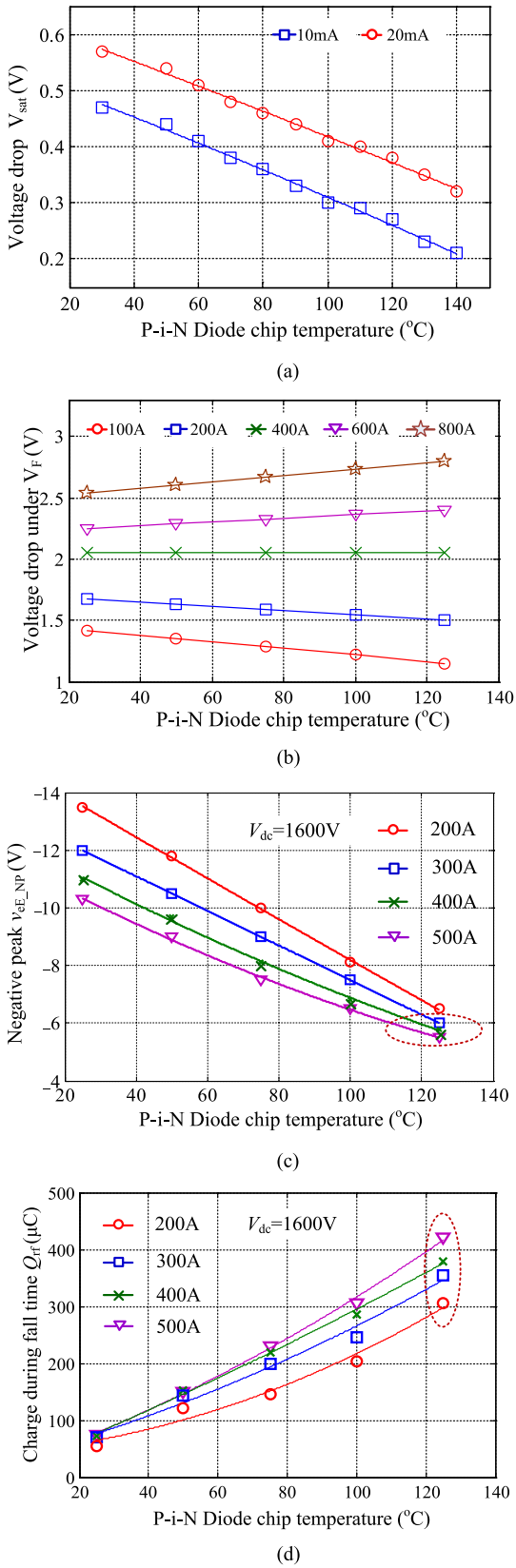


Fig. 14. Experimental comparisons of four state-of-the-art TSEPs: (a) voltage at low current injection V_{sat}, (b) voltage at high current injection VF, (c) negative peak voltage v_{eE_NP} induced by reverse recovery current, and (d) charge during fall time Q_{rf}.

p-i-n diodes from the converter for small current injection, some auxiliary circuits are required and the control strategy should be interrupted for the implementation procedure. To address these issues, the voltage at high current injection V_F is applied for diode T_j. Since the inspected high power p-i-n diode is a bipolar device, V_F is independent of diode T_j around 400 A load current level as plotted in Fig. 14(b). It can be seen the closer to 400 A load current, the lower the V_F sensitivity ratio.

The experimental results of the dependence between v_{eE_NP} induced by the maximum turn-off di_d/dt and diode T_j at $V_{dc} = 1600$ V are plotted in Fig. 14(c). Unlike the static V_{sat}-based TSEP, the extraction of the maximum turn-off di_d/dt do not need the sophisticated current source injection circuit. The relationship between the maximum turn-off di_d/dt and diode T_j is monotonic compared with V_F. However, the sensitivity ratio decreases with increasing load current. Furthermore, for the high-temperature region around 125 °C, the difference of v_{eE_NP} per 100 A is very small as shown in the dashed circle. In Fig. 14(c), as long as the sampled v_{eE_NP} is around –5.7 V, it is difficult to estimate the actual diode T_j at a rough sampled load current. Fortunately, an opposite tendency is plotted in Fig. 14(d). This means that the diode T_j can be easily estimated in dashed circle by means of numerical interpolation method at different load current in the range of 500 A. The proposed TSEP is characterized by the monotonicity for diode T_j and no current injection circuit. Compared with the maximum turn-off di_d/dt-based dynamic TSEP, the proposed TSEP is more applicable to large load current and high-temperature conditions.

In general, benefitting from the transferring effect of the parasitic inductor L_{eE} of high-power IGBT module, the dynamic TSEPs can be extracted effectively and feasibly for the online implementation compared with static TSEPs. In terms of the proposed TSEP, it is difficult to accurately extract the diode T_j information during low-temperature stage (e.g., from 25 to 50 °C). However, the experimental results indicate that Q_{rf}-based TSEP has more advantages than v_{eE_NP}-based TSEP under large current and high diode T_j range.

V. Conclusion

This paper has presented an indirect junction temperature extraction method for high power p-i-n diode, which uses the module parasitic inductor L_{eE} between the Kelvin emitter and power emitter. The reverse recovery charge during the reverse current fall time Q_{rf} has been extracted and calculated by the induced voltage v_{eE} across L_{eE}. The relationship among the junction temperature, induced v_{eE}, and Q_{rf} has been theoretically deduced. It is deduced that Q_{rf} increases with p-i-n diode junction temperature increases, and the extracted Q_{rf} has be calculated from the induced v_{eE}. Therefore, Q_{rf} can be applied as a TSEP for p-i-n diode junction temperature extraction.

An experimental platform based on the chopper circuit has been used to verify the theoretical analysis. Due to the package feature of high-voltage and high-power IGBT modules, their internal parasitic inductor L_{eE} can be used to measure the induced v_{eE} during p-i-n diode reverse recovery current. This provides a flexible mechanism for measuring Q_{rf}. The experimental results showed an approximately linear dependence between the p-i-n diode junction temperature and Q_{rf}. The multidimensional database of calculated Q_{rf} with varying temperature and other relevant factors is invaluable for online p-i-n diodes junction temperature prediction.

By comparison the state-of-the-art TSEPs for p-i-n diodes, the proposed TSEP has the features of monotonicity with temperature and high sensitivity under large I_L. These features make the proposed TSEP have more advantages in high diode T_j and large current conditions.

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