Multiloop Minimum Switching Cycle Control Based on Nonaveraged Current Discrete-Time Model for Buck Converter

Run Min, Qiao Zhang, *Member, IEEE*, Qiaoling Tong, *Member, IEEE*, Xuecheng Zou, Xiaofei Chen, and Zhenglin Liu

***Abstract*—Exploring high-performance controller for buck converter is challenging since it can be easily affected by converter model accuracy. In this paper, a novel nonaveraged current discrete-time (NCD) model is proposed, in which inductor current is expressed as time-varying equations during switch-on and switch-off states. It achieves higher accuracy than the conventional averaged model at high-frequency range, thus can be used to optimize high-speed controller design. Based on the NCD model, a multiloop minimum switching cycle (MMSC) control strategy, composed of output feedback (OF), line feed forward (LFF), and reference feed forward (RFF) loops, is proposed and tuned for buck converter operating in continuous conduction mode. Mutual influences among three loops are considered and eliminated by specifically designed LFF and RFF compensations, which adapt the OF compensation. With consideration of sampling and calculation delays, relationship between transient switching cycles and geometric center of controller poles is discovered from a calculated output voltage error series. Furthermore, theoretical minimum switching cycles are calculated by moving the center inside the unit cycle of complex plane, which ensures system stability. Moreover, load/line transient response and reference tracking time are simultaneously optimized to the minimum switching cycles. Effectiveness of the controller is proved by converter closed-loop pole/zero plots, transient response simulations, and experiments.**

***Index Terms*—Buck, continuous conduction mode, dc–dc, minimum switching cycle, multiloop, nonaveraged current discrete-time (NCD) model, reference tracking, transient response.**

I. Introduction

In recent years, control strategies for buck converters are extensively studied to improve the control performance with respect to load/line transient response and reference tracking. They are implemented by analog circuits or digital signal processors. Analog ripple based or V^2 controllers are simple and practical to achieve a fast load transient response [1]–[4]. They have various modulation methods, such as constant frequency peak voltage mode, constant on-time (COT) and constant off-time modulations, in which COT is the most popular method owing to its high efficiency at light-load condition [5]–[8]. Furthermore, V^2 control is improved by additional current sensing and current control, resulting in faster reference tracking speed [9]. These controllers are widely used in industrial applications, and can achieve a high control loop bandwidth. In comparison with analog controllers, digital controllers have advantages of low sensitivity to noise and parameter variations, ease of integration with other digital systems, programmability, and possibilities to improve performance using more advanced control strategies [10]–[13].

For digital controlled pulse width modulation (PWM) converters, the control scheme, and converter modeling accuracy are both important with respect to load/line transient response and reference tracking. With respect to control scheme, conventional voltage mode controllers employ a single compensator that feeds the output voltage error to the duty cycle. Only one specific kind of dynamic performance can be optimized through compensation, since the closed-loop transfer functions are different for load/line transient responses and reference tracking [14], [15]. For current mode controllers, digital dead-beat current mode and predictive current programmed controllers are proposed to maximize the current loop bandwidth [16]–[21]. Through simple and robust control for inductor current, line disturbance can be effectively suppressed, as indicated in the line-to-output transfer function [22]. However, aforementioned control schemes do not have the ability to simultaneously optimize load/line transient response and reference tracking, which have different closed-loop transfer functions.

The other issue that influences the performance is the converter model, which affects the controller design. Based on continuous s-domain models, the frequency compensator can be easily designed and mapped to discrete z-domain by the conventional analog-to-digital redesign technique, which relies on approximation methods such as Euler, bilinear or pole/zero matching, etc., [15], [23], [24]. However, the mapping process suffers from frequency warping, while zero-order hold and calculation delays are disregarded [25], [26]. An alternative way is to directly design digital controllers by using discrete-time transfer functions, of which the modeling accuracy determines the control performance [27], [28]. Therefore, the growing interests in high-performance digital controller design prompts study in discrete-time modeling. In [29], exact small-signal discrete-time models are proposed with consideration of sampling, modulator

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effects, and delays. However, they are too complex to use for practical applications because of matrix exponentials and integrals involved in the modeling process. A simplified approach for discrete-time modeling is the state-space average technique [30]–[32]. However, this method was reported in [33] that fails to predict fast-scale instabilities.

For converter modeling, discrete-time transfer functions can be derived from the well-known averaging method, where inductor current is taken as constant in each switching cycle. However, this method leads to model error at high-frequency range, and it constrains the high-performance controller design. This paper solves the issue by a novel nonaveraged current discrete-time (NCD) model, where inductor current is expressed as time-varying equations during switch-on and switch-off states. Furthermore, the model is used to tune the multiloop minimum switching cycle (MMSC) controller, which is carried out by a multiloop control scheme that contains an output feedback (OF) loop, a line feed forward (LFF) loop, and a reference feed forward (RFF) loop. Mutual influences of the loops are eliminated by specifically designed LFF and RFF compensations, which adapt the OF compensation, since all closed-loop transfer functions are affected by the OF compensation. With consideration of sampling and calculation delays, relationship between the transient switching cycles and geometric center of controller poles is discovered from a calculated output voltage error series. Furthermore, theoretical minimum switching cycles are calculated by moving the center inside the unit cycle of complex plane, which ensures system stability. Moreover, load/line transient response and reference tracking time are simultaneously optimized to the theoretical minimum switching cycles.

The paper is organized as follows. Section II presents the converter NCD model, where the variation of inductor current within one switching cycle is taken into consideration. In Section III, the MMSC control strategy is given that simultaneously reduce load/line transient and reference tracking times to minimal switching cycles. Section IV proves the MMSC control strategy and NCD model through spectrum analyses, pole/zero plots, and step response simulations. Experimental results are presented in Section V to verify effectiveness of the controller. Finally, a brief conclusion is given in Section VI.

II. NCD Model

For the conventional averaged model, inductor current is taken as constant in each switching cycle. In comparison, the NCD model describes the inductor current $i(t)$ as time-varying equations during switch-on and switch-off states. Furthermore, output voltage variation in one switching cycle is given, and converter transfer functions $G_{vl}(z)$, $G_{vd}(z)$, and $G_{vg}(z)$ are derived.

As shown in Fig. 1, the output voltage $v(t)$ is determined by current on the output capacitor $i(t) - v(t)/R$, it falls when $i(t) < v(t)/R$ and rises when $i(t) > v(t)/R$. Since voltage ripple is very small, $i(t) - v(t)/R$ approximates $i(t) - v(0)/R$ in the k th switching cycle. Therefore, the output voltage variation

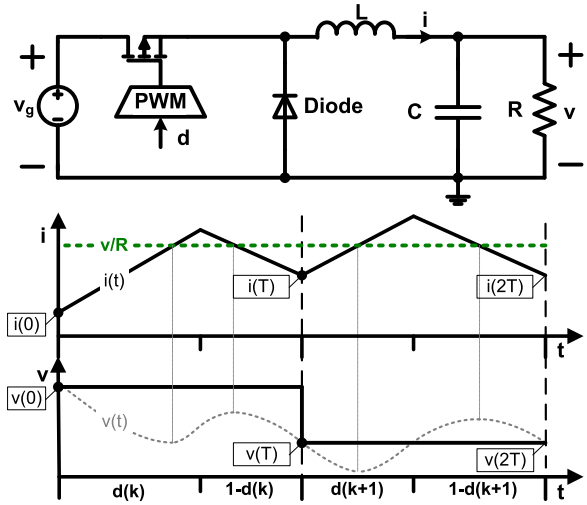

Fig. 1. Buck converter and its inductor current and output voltage.

in one switching cycle is given by

$$\begin{aligned} v(T) - v(0) &= \frac{1}{C}\int_0^T \left(i(t) - \frac{v(t)}{R}\right) dt \\ &\approx \frac{1}{C}\int_0^T \left(i(t) - \frac{v(0)}{R}\right) dt \\ &= \frac{1}{C}\int_0^{dT} i_d(t)dt + \frac{1}{C}\int_{dT}^T i_{1-d}(t)dt \\ &\quad -\frac{1}{C}\int_0^T \frac{v(0)}{R}dt \end{aligned} \tag{1}$$

where $i_d(t)$ and $i_{1-d}(t)$ are inductor currents during switch-on and switch-off states, shown as follows:

$$\begin{cases} i_d(t) = i(0) + \dfrac{v_g(0) - v(0)}{L}t \\ i_{1-d}(t) = i(0) + \dfrac{v_g(0) - v(0)}{L}dT - \dfrac{v(0)(t - dT)}{L} \end{cases}. \tag{2}$$

The inductor current is described as time-varying equations, whereas is taken as constant in the conventional averaged model. Furthermore, (3) is given by substituting (2) into (1), which is the variation of output voltage in one switching cycle

$$v(T) - v(0) = \frac{i(0)T}{C} + \frac{v_g(0)dT^2(2-d)}{2LC} - \frac{v(0)T^2}{2LC} - \frac{v(0)T}{RC}. \tag{3}$$

Besides, variation of the inductor current is determined by $v_g(0)$ and $v(0)$, shown as follows:

$$i(T) - i(0) = \frac{T}{L}[dv_g(0) - v(0)]. \tag{4}$$

Furthermore, universalized forms of (3) and (4) are given by

$$\begin{cases} v(k+1)-v(k)=\dfrac{i(k)T}{C}+\dfrac{v_g(k)dT^2(2-d)}{2LC}-\dfrac{v(k)T^2}{2LC} \\ \qquad\qquad -\dfrac{v(k)T}{RC} \\ i(k+1)-i(k)=\dfrac{T}{L}[dv_g(k)-v(k)] \end{cases}. \tag{5}$$

Based on z-transform, discrete-time function of (5) is given by

$$\begin{cases} v(z-1)=\dfrac{iT}{C}+\dfrac{v_gdT^2(2-d)}{2LC}-\dfrac{vT^2}{2LC}-\dfrac{vT}{RC} \\ i(z-1)=\dfrac{T}{L}(dv_g-v) \end{cases}. \tag{6}$$

Furthermore, it gives

$$v(z-1)=\frac{T^2}{LC}\frac{dv_g-v}{z-1}+\frac{T^2}{LC}\left[\frac{2d-d^2}{2}v_g-\frac{1}{2}v\right]-\frac{vT}{RC}. \tag{7}$$

Through (7), total differential function of v is derived by derivatives of $d,\ v_g$, and R, shown as

$$\hat{v}=G_{vd}(z)\hat{d}+G_{vg}(z)\hat{v}_g+G_{vl}(z)\hat{R} \tag{8}$$

where transfer functions from $\hat{d}$, $\hat{v}_g$, and $\hat{R}$ to $\hat{v}$ are at shown as (9) bottom of the page.

These closed-loop transfer functions are derived from the NCD model, which considers nonaveraged inductor current within one switching cycle. The NCD model acquires higher accuracy than the conventional averaged model at high-frequency range. This will be proved by simulations in Section IV.

III. MMSC Control Strategy

Construction of buck converter with MMSC controller is shown in Fig. 2(a). The controller operates in voltage mode, and current sampling is not required, while $v,\ v_{\rm ref}$, and v_g are sampled and fed to calculate d. Based on superposition principle, the controller is carried out through the OF, LFF, and RFF compensations, of which the outputs are summed as duty cycle.

The control process is given in Fig. 2(b), where the output voltage error is caused by load, line, and reference disturbances, and shall be eliminated by the MMSC controller. Reference and line disturbances can be directly sampled and regulated through RFF and LFF, whereas a load disturbance can only be detected from the output voltage error and then controlled through OF. Therefore, the OF compensator is designed to reject load disturbance. LFF and RFF compensators are designed to adapt the OF compensator, while reject line and reference disturbances.

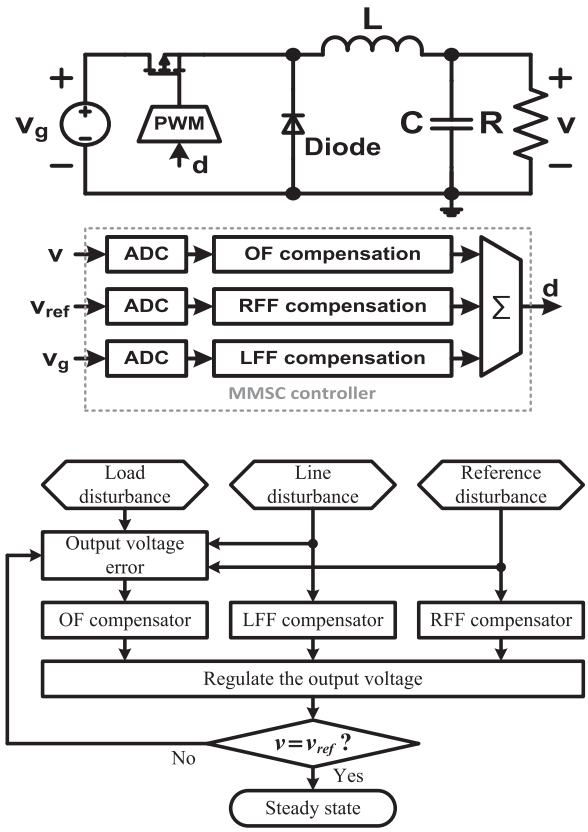

Fig. 2. MMSC control (a) structure and (b) process.

The MMSC controller is tuned to simultaneously reject load/line and reference disturbances in minimal switching cycles. With consideration of sampling and calculation delays, relationship between the transient switching cycles and geometric center of controller poles is discovered from a calculated output voltage error series. The center is moved inside unit cycle of the complex plane. With this constrain, the minimal switching cycles to ensure system stability can be derived.

A. System Closed-Loop Small-Signal Model

With MMSC control, system closed-loop small-signal model is given in Fig. 3, where $F_{vl}(z),\ F_{vr}(z)$, and $F_{vg}(z)$ are closed-loop transfer functions from $R,\ v_{\rm ref}$ and v_g to v, respectively. $G_{vl}(z),\ G_{vd}(z)$, and $G_{vg}(z)$ are converter transfer functions from $R,\ d$ and v_g to v. $H_{dv}(z)$, $H_{dg}(z)$, and $H_{dr}(z)$ are transfer functions of OF, LFF, and RFF compensations, respectively.

$$\begin{cases} G_{vd}(z)=\dfrac{2v_gT^2R^2[(1-d)z+d]}{2R^2LCz^2+(T^2R^2-4R^2LC+2LTR)z+2R^2LC+T^2R^2-2LTR} \\ G_{vg}(z)=\dfrac{dT^2R^2[(2-d)z+d]}{2R^2LCz^2+(T^2R^2-4R^2LC+2LTR)z+2R^2LC+T^2R^2-2LTR} \\ G_{vl}(z)=\dfrac{2vLT(z-1)}{2R^2LCz^2+(T^2R^2-4R^2LC+2LTR)z+2R^2LC+T^2R^2-2LTR} \end{cases} \tag{9}$$

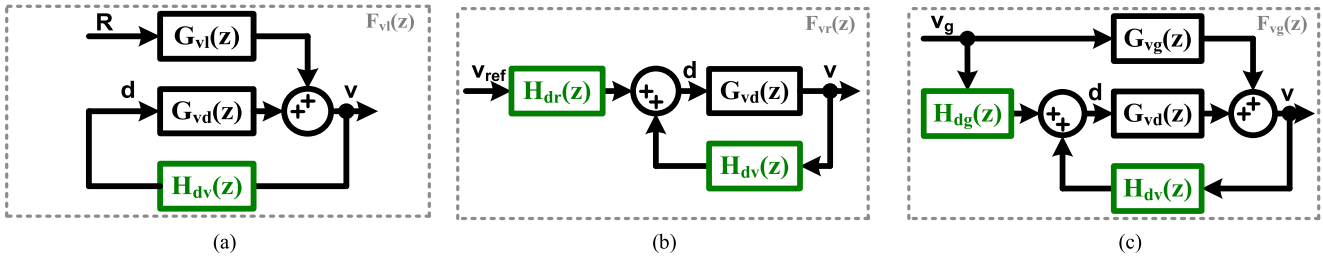

Fig. 3. Closed-loop small-signal models for (a) load-output, (b) reference-output and (c) line-output loops.

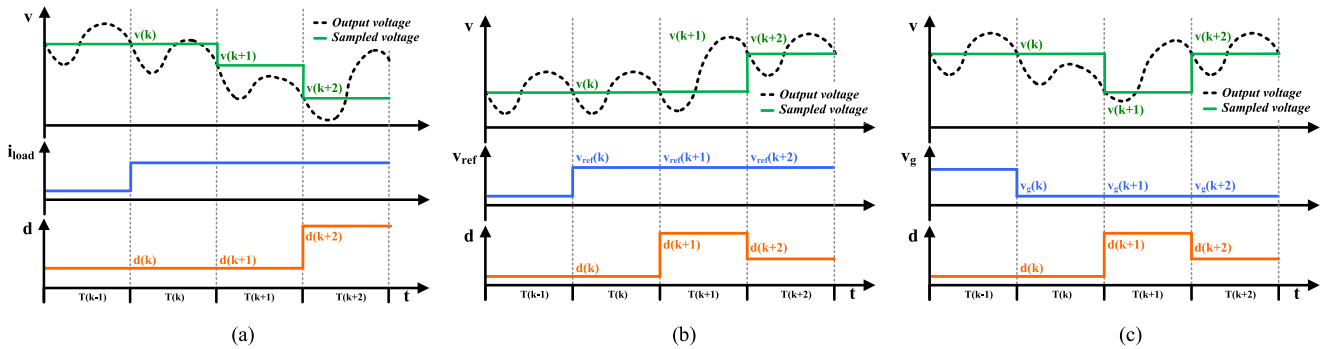

Fig. 4. (a) Load transient response, (b) reference tracking, and (c) line transient response with consideration of sampling and calculation delays.

Based on the models, converter closed-loop transfer functions are given by

$$\begin{cases} F_{\rm vl}(z) = \dfrac{G_{\rm vl}(z)}{1 - G_{\rm vd}(z)H_{\rm dv}(z)} \\ F_{\rm vr}(z) = H_{\rm dr}(z)\dfrac{G_{\rm vd}(z)}{1 - G_{\rm vd}(z)H_{\rm dv}(z)} \\ F_{\rm vg}(z) = \dfrac{G_{\rm vg}(z) + G_{\rm vd}(z)H_{\rm dg}(z)}{1 - G_{\rm vd}(z)H_{\rm dv}(z)} \end{cases}. \tag{10}$$

These functions indicate closed-loop responses to load/line and reference disturbances, and should be tuned to optimize the load/line transient responses and reference tracking time. All closed-loop transfer functions are controlled by $H_{dv}(z)$, whereas $F_{vr}(z)$ and $F_{vg}(z)$ are also controlled by $H_{dr}(z)$ and $H_{dg}(z)$, respectively. In the following, the OF, RFF, and LFF compensations will be designed to optimize load/line transient response and reference tracking time to minimal switching cycles.

B. Compensations to Achieve Minimum Switching Cycles

The OF, RFF, and LFF compensators aim at optimizing load/line transient and reference tracking times to minimal switching cycles. As shown in Fig. 4, supposing load current $i_{\rm load}$, reference voltage $v_{\rm ref}$ or line voltage v_g steps in the k th switching cycle and influences the output voltage without sampling $i_{\rm load}$, the OF compensator can detect the disturbance in the $k+1$ th switching cycle from the sampled output voltage $v(k+1)$. Furthermore, the duty cycle is adjusted to reject the disturbance, which is carried out after the $k+2$ th switching cycle owing to the calculation delay. The RFF and LFF compensators directly detect $v_{\rm ref}$ and v_g step changes and adjust the duty cycle to control the output voltage, which are carried out after the $k+1$ th switching cycle owing to the calculation delay.

1) OF Compensation: To derive the OF compensation strategy, relationship between load step transient time and geometric center of the compensator poles is obtained from a calculated output voltage error series. As shown in Fig. 4(a), owing to sampling and calculation delays, $d(k)$ and $d(k+1)$ hold the value after the disturbance, and OF compensator is unable to control $v(k+1)$ and $v(k+2)$. Therefore, with respect to small-signal analysis, the output voltage errors in the $k+1$ th and $k+2$ th switching cycles are only determined by $G_{vl}(z)$, shown as follows:

$$\begin{cases} G_{vl}(z)\frac{z}{z-1} = e_{vl}(1)z^{-1} + e_{vl}(2)z^{-2} + \cdots \\ e_{vl}(1) = \frac{vT}{R^2C} \\ e_{vl}(2) = \frac{vT}{R^2C}\frac{4LRC - 2LT - RT^2}{2LRC} \end{cases} \tag{11}$$

where $e_{vl}(1)$ and $e_{vl}(2)$ are voltage errors during $k+1$ th and $k+2$ th switching cycles. Supposing the objective error series under closed-loop control is

$$E_{vl}(z) = F_{vl}(z)\frac{z}{z-1} = e_{vl}(1)z^{-1} + e_{vl}(2)z^{-2} + P_l(z) \tag{12}$$

where $P_l(z)$ is determined by the OF law. Substituting $F_{vl}(z)$ into (12) gives

$$\frac{G_{vl}(z)}{1 - G_{vd}(z)H_{dv}(z)}\frac{z}{z-1} = E_{vl}(z). \tag{13}$$

Furthermore, $H_{dv}(z)$ is given by (14), shown at the bottom of the page where $a = 2RLC + T^2R - 2LT$ and $b = T^2R - 4RLC + 2LT$. The denominator order exceeds the

nominator order by one, which indicates that one switching cycle is reserved for digital calculations as bottom of the page.

Supposing the transient lasts for n switching cycles, then n poles are generated by $E_{vl}(z) = e_{vl}(1)z^{-1} + e_{vl}(2)z^{-2} + P_l(z)$. One of the poles must be located at (1,0) to acquire integrative characteristic, which ensures zero steady-state error in output voltage. Therefore, $E_{vl}(z)$ is given by

$$\begin{aligned} E_{vl}(z) &= e_{vl}(1)z^{-1} + e_{vl}(2)z^{-2} + P_l(z) \\ &= e_{vl}(1)z^{-1}(1 - z^{-1})(1 - z_2 z^{-1}) \\ &\quad \times (1 - z_3 z^{-1}) \cdots (1 - z_n z^{-1}). \end{aligned} \tag{15}$$

Factors of z^{-2} are $e_{vl}(2)$ and $e_{vl}(1)(-1 - z_2 - z_3 - \cdots - z_n)$ for left- and right-hand sides of (15), respectively. Since they are equal, it gives

$$-1 - z_2 - z_3 - \cdots - z_n = e_{vl}(2)/e_{vl}(1). \tag{16}$$

Furthermore, (16) is written as

$$\frac{z_2 + z_3 + \cdots + z_n}{n-1} = \frac{-1 - e_{vl}(2)/e_{vl}(1)}{n-1}. \tag{17}$$

Equation (17) indicates that the geometric center of $\{z_2, z_3, \ldots, z_n\}$ locates at $([-1 - e_{vl}(2)/e_{vl}(1)]/(n-1), 0)$. Therefore, an essential condition to ensure system stability is given by

$$\frac{-1 - e_{vl}(2)/e_{vl}(1)}{n-1} \geq -1. \tag{18}$$

As a result, the minimum switching cycles for load transient response must satisfy

$$n \geq e_{vl}(2)/e_{vl}(1) + 2. \tag{19}$$

However, additional switching cycles must be reserved to ensure system stability. Take $e_{vl}(2)/e_{vl}(1) = 3$, for example, the minimum switching cycles are $n = 5$ according to (19). For comparison, poles under $n = 5$ and $n = 7$ are plotted in Fig. 5. For $n = 5$, the geometric center of the poles is $(-1, 0)$, thus some of the poles must be outside the unit cycle. For $n = 7$, geometric center of the poles is $(-0.67, 0)$, which ensures system stability.

To increase the system stability, the minimum switching cycles for the transient response are given by

$$n = e_{vl}(2)/e_{vl}(1) + 2 + S_M \tag{20}$$

where S_M is a switching cycle margin. Furthermore, $\{z_2, z_3, \ldots, z_n\}$ are set as multiple poles z_c to prevent them from splitting and moving outside the unit cycle, shown as follows:

$$z_c = \frac{-1 - e_{vl}(2)/e_{vl}(1)}{n-1}. \tag{21}$$

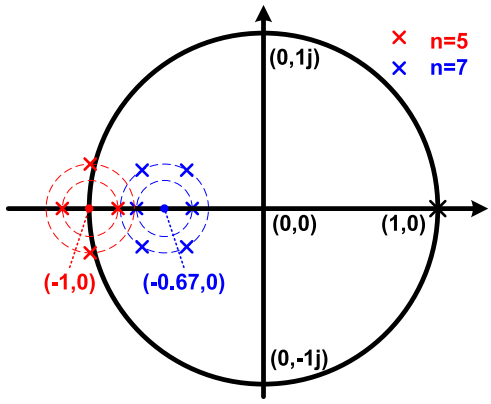

Fig. 5. Poles of $H_{dv}(z)$ for $e_{vl}(2)/e_{vl}(1) = 3$, when $n = 5$ and $n = 7$.

Taking (21) into (15) gives the output voltage error series, shown as follows:

$$\begin{aligned} E_{vl}(z) &= e_{vl}(1)z^{-1}(1 - z^{-1})(1 - z_2 z^{-1}) \\ &\quad (1 - z_3 z^{-1}) \ldots (1 - z_n z^{-1}) \\ &= e_{vl}(1)z^{-1}(1 - z^{-1})(1 - z_c z^{-1})^{n-1}. \end{aligned} \tag{22}$$

Furthermore, taking (22) into (14) gives the OF strategy, shown as

$$H_{dv}(z) = \frac{[ae_{vl}(1) + be_{vl}(2)]z^{-1} + ae_{vl}(2)z^{-2} + P_l(z)(2RLCz^2 + bz + a)}{2v_g T^2 R[(1-d)z + d]e_{vl}(1)(1 - z^{-1})(1 - z_c z^{-1})^{n-1} z^{-1}} \tag{23}$$

An integral factor $z - 1$ exists in the denominator, which acquires integrative characteristic for the loop and eliminates steady-state error in output voltage. Furthermore, one switching cycle is reserved for calculation since the denominator order exceeds the nominator order by one.

Taking (23) into (10) gives the closed-loop transfer function, shown as follows:

$$F_{vl}(z) = \frac{e_{vl}(1)(z-1)^2(z - z_c)^{n-1}}{z^{n+2}}. \tag{24}$$

$F_{vl}(z)$ has $n + 2$ poles at $(0,\ 0)$, $n - 1$ zeros at $(z_c, 0)$ and 2 zeros at $(1,\ 0)$. Therefore, the transient response to a load step lasts for $n + 2$ switching cycles.

2) RFF Compensation: The RFF compensator is able to regulate the output voltage to the reference in the $k + 2$ th switching cycle. To devise the control strategy, the closed-loop transfer function is assumed to be a delay of two switching cycles, shown

$$\begin{aligned} H_{dv}(z) &= [1 - \frac{G_{vl}(z)}{E_{vl}(z)(z-1)/z}]/G_{vd}(z) \\ &= \frac{[ae_{vl}(1) + be_{vl}(2)]z^{-1} + ae_{vl}(2)z^{-2} + P_l(z)(2RLCz^2 + bz + a)}{2v_g T^2 R[(1-d)z + d]E_{vl}(z)} \end{aligned} \tag{14}$$

as follows:

$$F_{vr}(z) = H_{dr}(z)\frac{G_{vd}(z)}{1 - G_{vd}(z)H_{dv}(z)} = \frac{1}{z^2}. \quad (25)$$

Based on (25), the RFF compensator transfer function is given by

$$\begin{aligned} H_{dr}(z) &= \frac{G_{vl}(z)}{G_{vd}(z)}\frac{1}{E_{vl}(z)(z^2 - z)} \\ &= \frac{LC}{v_g T^2[(1-d)z + d]}\frac{1}{(1 - z^{-1})(1 - z_c z^{-1})^{n-1}}. \end{aligned} \quad (26)$$

Since the denominator order exceeds the nominator order by one, one switching cycle is reserved for calculation. The control law tunes $F_{vr}(z)$ as $1/z^2$, thus makes the output voltage track the reference in theoretical minimum switching cycles. System stability is ensured since z_c is inside the unit cycle.

3) LFF Compensation: As shown in Fig. 4(c), owing to the calculation delays, $d(k)$ holds its value after the disturbance, and the LFF compensator is unable to affect $v(k+1)$. Therefore, with respect to small-signal analysis, the output voltage error in the $k+1$ th switching cycle is only determined by $G_{vg}(z)$, shown as follows:

$$\begin{cases} G_{vg}(z)\frac{z}{z-1} = e_{vg}(1)z^{-1} + \cdots \\ e_{vg}(1) = \frac{dT^2}{LC}\frac{2-d}{2} \end{cases} \quad (27)$$

where $e_{vg}(1)$ is the voltage error during $k+1$ th switching cycles. Supposing the objective error series with LFF compensator is

$$\begin{aligned} E_{vg}(z) &= F_{vg}(z)\frac{z}{z-1} \\ &= \frac{G_{vg}(z) + G_{vd}(z)H_{dg}(z)}{1 - G_{vd}(z)H_{dv}(z)}\frac{z}{z-1} \\ &= e_{vg}(1)z^{-1} + P_g(z) \end{aligned} \quad (28)$$

where $P_g(z)$ is determined by LFF law. For $P_g(z) = 0$, the LFF compensator transfer function is given by are (29) as shown bottom of the page.

TABLE I
SPECIFICATIONS OF THE CONVERTER

Parameter	Value
v_g	15 V
v	5 V
L	25 μH
C	15 μF
R	1.5 Ω
f	100 kHz

System stability is ensured since z_c is inside the unit cycle. Furthermore, the closed-loop transfer function is given by

$$F_{vg}(z) = e_{vg}(1)\frac{z-1}{z^2}. \quad (30)$$

$F_{vg}(z)$ has 2 poles at $(0,\ 0)$ and 1 zero at $(1,\ 0)$. Since $E_{vg}(z)$ is tuned as $e_{vg}(1)z^{-1}$, v_g induced output voltage disturbance is rejected in theoretical minimum switching cycles.

Through OF, RFF and LFF compensations, load/line transient response and reference tracking time are simultaneously optimized to theoretical minimum switching cycles. Effective of the strategy will be proved by simulations and experiments.

IV. SIMULATIONS

In order to verify the proposed control strategy, a buck converter is constructed in MATLAB-Simulink, where the main specifications are listed in Table I. According to (11), $e_{vl}(1)$ and $e_{vl}(2)$ are set as 0.6 and 1.0, respectively. Therefore, the minimum switching cycles are chosen by $n = 6$ where a switching cycle margin of $S_M = 2$ is reserved to increase system stability. According to (21), geometric center of the poles locates at $(-0.48, 0)$.

According to (23), (26), and (29), the OF, RFF, and LFF compensators are tuned as (31) shown at the bottom of the page.

To verify accuracy of the proposed model, spectrum analyses are given for the NCD, averaged, and circuit models. Furthermore, closed-loop pole/zero plots are given to prove stability of the converter. Finally, step responses are given to verify the transient response.

$$\begin{aligned} H_{dg}(z) &= \frac{E_{vg}(z)[1 - G_{vd}(z)H_{dv}(z)](z-1) - G_{vg}(z)z}{G_{vd}(z)z} \\ &= \frac{[2e_{vl}(1) + (2-d)e_{vl}(2)]z^{-1} + de_{vl}(2)z^{-2} + P_l(z)[(2-d)z + d]}{-2v_g[(1-d)z + d]e_{vl}(1)(1 - z^{-1})(1 - z_c z^{-1})^{n-1}z^{-1}/d} \end{aligned} \quad (29)$$

$$\begin{cases} H_{dv}(z) = \dfrac{-5.22z^6 - 0.46z^5 + 2.99z^4 + 0.53z^3 - 0.99z^2 - 0.49z - 0.07}{9.88z^7 + 18.98z^6 + 6.28z^5 - 12.32z^4 - 14.48z^3 - 6.71z^2 - 1.49z - 0.13} \\ H_{dr}(z) = \dfrac{3.70z^6}{9.88z^7 + 18.98z^6 + 6.28z^5 - 12.32z^4 - 14.48z^3 - 6.71z^2 - 1.49z - 0.13} \\ H_{dg}(z) = \dfrac{-0.719z^6 - 0.057z^5 + 0.336z^4 + 0.303z^3 + 0.116z^2 + 0.021z + 0.001}{9.88z^7 + 18.98z^6 + 6.28z^5 - 12.32z^4 - 14.48z^3 - 6.71z^2 - 1.49z - 0.13} \end{cases} \quad (31)$$

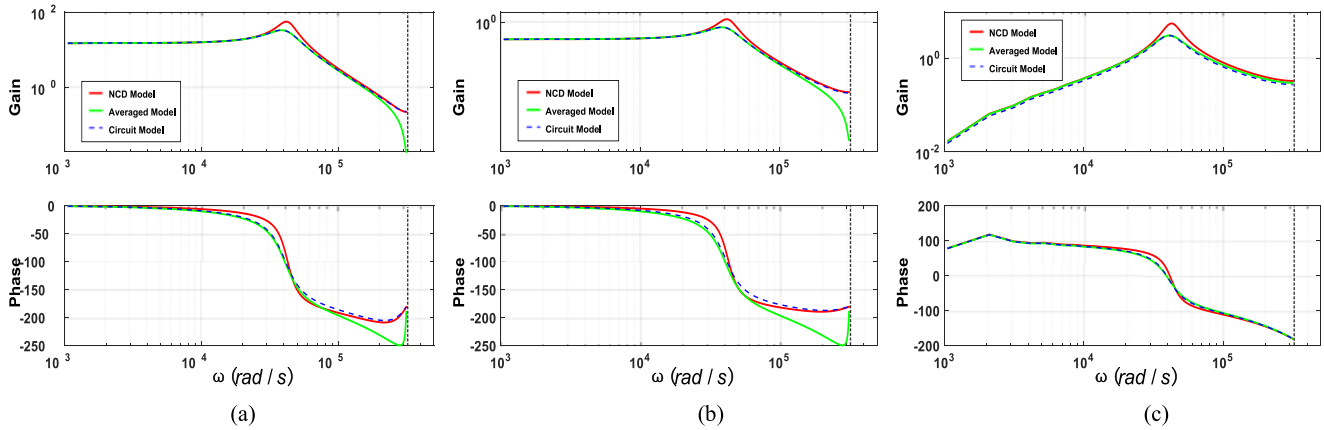

Fig. 6. Spectrum analyses for (a) $d-v$, (b) v_g-v, and (c) $R-v$ transient responses.

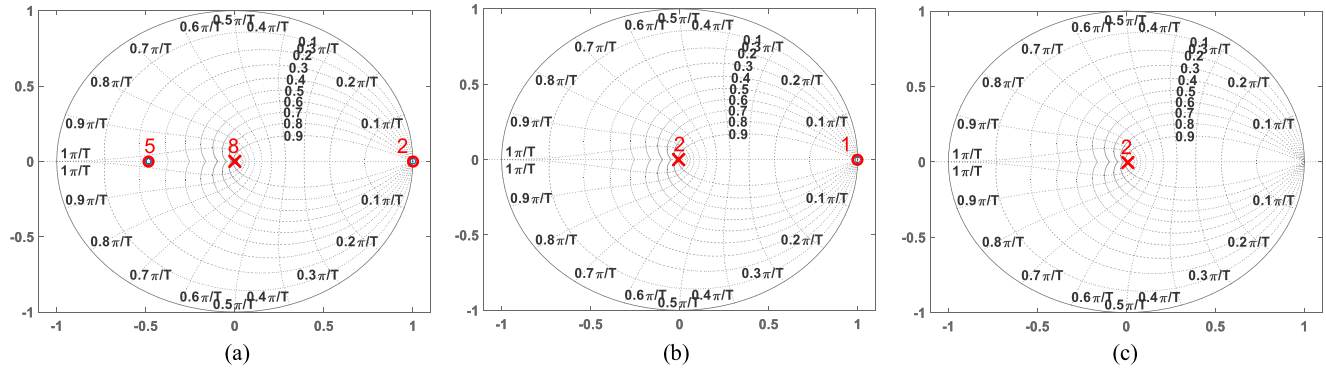

Fig. 7. Pole/zeros of (a) $F_{vl}(z)$, (b) $F_{vr}(z)$, and (c) $F_{vg}(z)$.

A. *Comparison of Different Models*

In order to verify the modeling accuracy, spectrum analyses are carried out for the NCD, averaged and circuit models. The averaged s-domain model is expressed as

$$\begin{cases} G_{vd}(s) = \frac{v_g R}{s^2RLC+sL+R} \\ G_{vg}(s) = \frac{dR}{s^2RLC+sL+R} \\ G_{vl}(s) = \frac{sLv}{R}\frac{1}{s^2RLC+sL+R} \end{cases}. \tag{32}$$

The circuit model is constructed through circuit elements, thus achieves the highest accuracy and is used as a reference to simulate the actual converter. As shown in Fig. 6, the NCD model achieves higher accuracy than the averaged model at high-frequency range, since its frequency response is closer to that of circuit model.

For $d-v$ response, all models have the same gain and phase when $\omega < 10k$ rad/s, which proves that both NCD and averaged models are accurate at low-frequency range. For $10k < \omega < 100k$ rad/s, spectrum of the averaged model is closer to that of circuit model, thus is more accurate than NCD model. For $100k < \omega < 314k$ rad/s, the NCD model has accurate spectrum characteristic, whereas the averaged model has deviated gain and phase. The error leads to inaccurate estimation for system stability at high-frequency range, thus constrains the design for high-performance controllers.

Frequency spectrums for $v_g - v$ responses are similar to that of $d-v$ response, where both NCD and averaged models are accurate at low-frequency range. For $10k < \omega < 70k$ rad/s, the averaged model is more accurate than NCD model. For $70k < \omega < 314k$ rad/s, NCD model achieves higher accuracy than the averaged model. With respect to $R-v$ response, both NCD and averaged models are accurate when $\omega < 20k$ rad/s and $100k < \omega < 314k$ rad/s. For $20k < \omega < 100k$ rad/s, the averaged model achieves higher accuracy than NCD model.

The NCD model is less accurate than the averaged s-domain model around the LC resonant frequency, which is caused by using discrete-time operator to describe the resonant poles [26], [34].

B. *Closed-Loop Analysis*

System stability is verified through closed-loop pole/zero plots of $F_{vl}(z)$, $F_{vg}(z)$ and $F_{vr}(z)$. All plots prove system stable since poles are inside the unit cycle, shown as Fig. 7, where $F_{vl}(z)$ has 8 poles at $(0,0)$, 5 zeros at $(-0.48,0)$ and 2 zeros at $(1,0)$. Therefore, the transient response to a load step lasts for eight switching cycles. $F_{vr}(z)$ has 2 poles at $(0,0)$ and is a delay of two switching cycles, which is the transient time that output voltage follows the reference. $F_{vg}(z)$ has 2 poles at $(0,0)$ and a zero at $(1,0)$. The function contains a differential

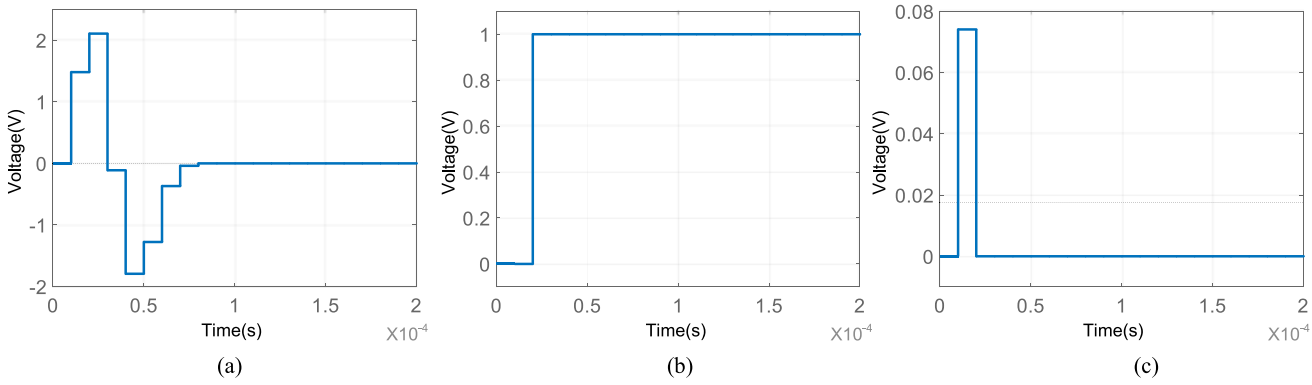

Fig. 8. Step response of (a) $F_{vl}(z)$, (b) $F_{vr}(z)$, and (c) $F_{vg}(z)$.

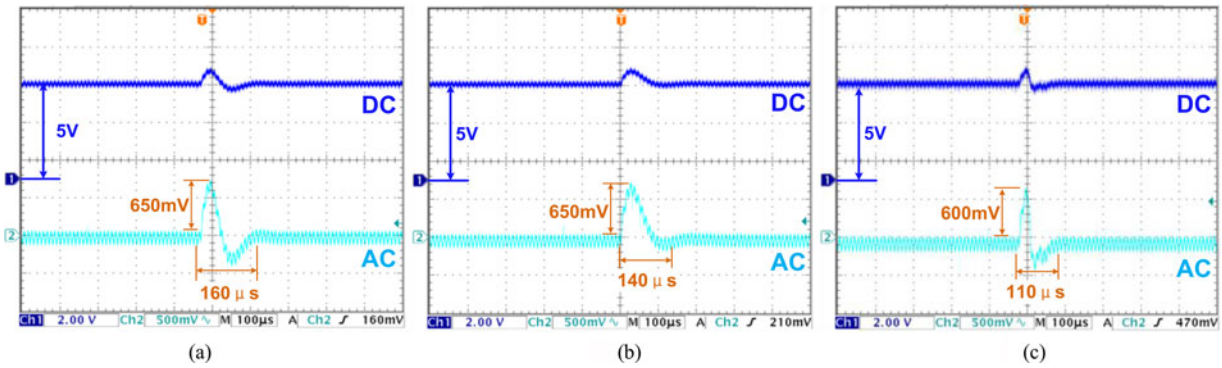

Fig. 9. Transient responses with (a) PID controller, (b) SCM controller and (c) MMSC controller —when load resistance steps up from 1.5 to 2 Ω.

factor and a delay of two switching cycles. Therefore, the output voltage deviates for one switching cycle when line voltage steps.

C. Closed-Loop Step Responses

The transient performances are proved by step responses of $F_{vl}(z)$, $F_{vr}(z)$ and $F_{vg}(z)$. As shown in Fig. 8, all results prove the analysis and stability of the converter. For load transient, step response of $F_{vl}(z)$ lasts for eight switching cycles. The maximum deviation is 210% of the step magnitude. For reference transient, step response of $F_{vr}(z)$ shows that output voltage follows the reference after two switching cycles. For line transient, step response of $F_{vg}(z)$ lasts for two switching cycles. The maximum deviation is less than 7.5% of the step magnitude.

V. Experiments

In order to verify the proposed control strategy, experiments are carried out with buck converter. The designed specifications are the same with that of simulations in Section IV (see Table I). The minimum switching cycles are $n = 6$ where a switching cycle margin of $S_M = 2$ is reserved.

The transient performance of MMSC controller is compared to that of a PID controller and a sensorless current mode (SCM) controller. The PID controller has a cross-over frequency of $0.2/T$ rad/s and a phase margin of 90°. The SCM controller is carried out by a current observer, a PI compensator and a current controller. All of the controllers are designed with consideration of sampling effect and calculation delay.

A. Transient Responses to Load Step

As shown in Fig. 9, when load resistance steps up from 1.5 to 2 Ω, the output voltage deviates by $\{650,\ 650,\ 600\ \mathrm{m}V\}$, respectively. The transient responses last for $\{160,\ 140,\ 110\ \mu\mathrm{s}\}$, respectively. For MMSC controller, the actual transient time is 11 switching cycles, which is three cycles longer than that of analysis in Section III. The output voltage deviation is 120% of the step magnitude.

B. Transient Responses to Reference Voltage Step

As shown in Fig. 10, when v_{ref} steps up from 5 to 5.5 V, the output voltage tracks the reference in $\{130,\ 110\ ,\ 70\ \mu\mathrm{s}\}$, respectively. All of the controllers carry out the tracking without inducing steady-state error. For MMSC controller, the actual transient response lasts for seven switching cycles, whereas is two switching cycles according to analysis in Section III. However, the transient response is much faster than that of PID and SCM controllers.

C. Transient Responses to Line Voltage Step

As shown in Fig. 11, when v_g steps down from 15 to 12 V, the output voltage deviates by $\{1\ V,\ 320\ \mathrm{m}V,\ 300\ \mathrm{m}V\}$,

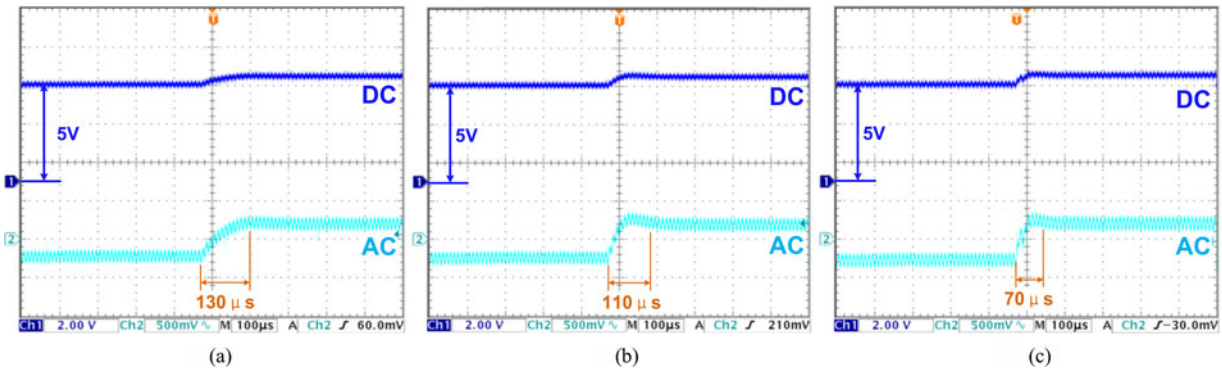

Fig. 10. Transient responses with (a) PID controller, (b) SCM controller, and (c) MMSC controller—when $v_{\rm ref}$ steps up from 5 to $5.5\ V$.

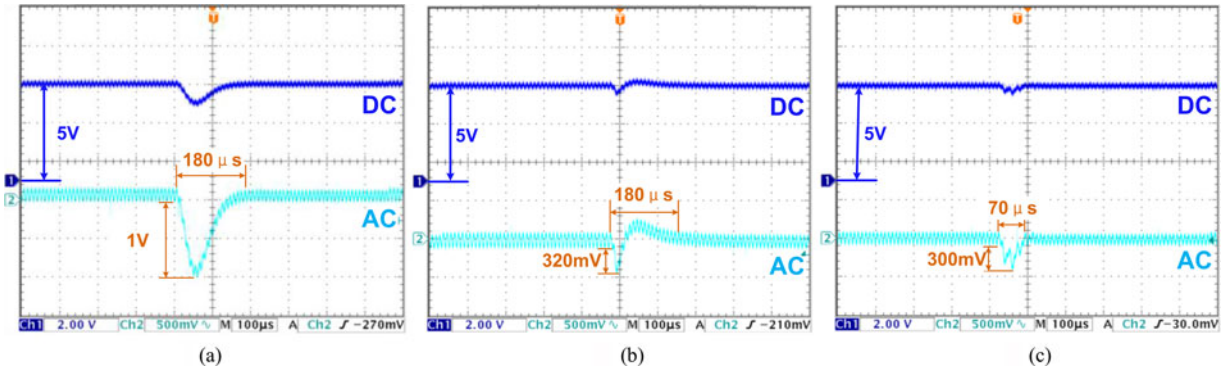

Fig. 11. Transient responses with (a) PID controller, (b) SCM controller, and (c) MMSC controller—when v_g steps down from 15 to $12\ V$.

respectively. The transient responses last for $\{180,\ 180,\ 70\ \mu s\}$, respectively. For MMSC controller, the transient time is two switching cycle according to analysis in Section III, while the experimental result is seven switching cycles. The output voltage deviation is 10% of the step magnitude, which is larger than that of simulation result in Section IV. Despite of the deviations, the transient performance is much better than that of PID and SCM controllers.

VI. Conclusion

This paper proposes a MMSC controller for buck converter operating in continuous conduction mode. In order to optimize the transient response, a NCD model is proposed to improve the accuracy of converter discrete-time transfer functions at high frequency. Compared to the conventional averaged model, the proposed model is more accurate at high-frequency range, thus optimizes the design for high-performance controllers. Based on the NCD model, the MMSC controller is carried out, which simultaneously rejects load/line and reference disturbances in minimum switching cycles.

Accuracy of the NCD model is proved by simulations, which is compared with the conventional averaged model and circuit model. Stability of the MMSC controller is proved by simulations of closed-loop pole/zero plots and step responses. Finally, experiments are carried out with MMSC, PID, and SCM controllers, and prove effectiveness of the proposed controller.

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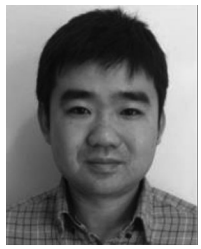

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