Modulation Method of a Full-Bridge Three-Level *LLC* Resonant Converter for Battery Charger of Electrical Vehicles

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***Abstract*—This paper proposes a modulation method for a full-bridge three-level *LLC* resonant converter. The target converter is known to enable fixed frequency operation, small resonant inductance ratio, and zero-current switching operation of rectifier diodes under wide output-voltage variation. Therefore, it is suitable for an application such as in battery chargers. A new parameter named "master duty," which determines each voltage-level duty, is introduced to this modulation method. It simplifies the modulation method; therefore, a modification of the modulation is easy. It also makes possible seamless handling of two-level, three-level, and mixed modes. The modulation method is represented by the relationship between the master duty and each gate-pulse edge position. This representation can clearly depict a complex modulation such as a combination of pulse-width and phase-shift modulations. The voltage gain of the converter is analyzed using the first-harmonic approximation technique. The result of the analysis is verified by the circuit simulation. The voltage gain is also analyzed using lossy components, which is verified by the experimental result. A 385-V input 225- to 378-V/6.6-kW output prototype converter is fabricated for this verification. It shows 98.14% peak efficiency, and its power density is 1036 W/L.**

***Index Terms*—First-harmonic approximation (FHA), *LLC*, modulation, resonant converter, three level.**

Nomenclature

$C_{\mathrm{IN1}}, C_{\mathrm{IN2}}$	Input capacitors.
C_R	Resonant capacitor and its capacitance.
D_1–D_6	Body diode of Q_1–Q_6.
$D_{\mathrm{C1}}, D_{\mathrm{C2}}$	Clamp diodes.
Q_1–Q_4	Three-level leg switch.
Q_5, Q_6	Two-level leg switch.
L_{R1}	Primary resonant inductor and its inductance.
L_{R2}	Secondary resonant inductor and its inductance.
L_M	Magnetizing inductance.
n	Transformer turns ratio: Primary turns/secondary turns.
$V_{\mathrm{IN}}, E_{\mathrm{IN}}$	Input voltage, fundamental component of V_{IN}.
$V_{\mathrm{OUT}}, E_{\mathrm{OUT}}$	Output voltage, fundamental component of V_{OUT}.
M	Normalized output voltage: $nV_{\mathrm{OUT}}/V_{\mathrm{IN}}$.
I_{OUT}	Output current.
J	Normalized output current: $I_{\mathrm{OUT}}/(nV_{\mathrm{IN}}/Z_O)$.
R_{OUT}	Load resistance.
I_{CR}	Current of C_R.
I_{TSEC}	Current of transformer secondary winding.
V_{AB}	Output voltage of the full bridge circuit.
V_{CR}	Voltage of C_R.
f_R	Resonant frequency: $1/(2\pi\sqrt{C_R(L_{R1}+n^2L_{R2})})$.
f_{SW}	Switching frequency.
f_N	Normalized switching frequency: f_{SW}/f_R.
λ_1	Primary inductance ratio: L_{R1}/L_M.
λ_2	Secondary inductance ratio: n^2L_{R2}/L_M.
Z_O	Characteristic impedance: $\sqrt{(L_{R1}+n^2L_{R2})/C_R}$.
Q	Quality factor: Z_O/R_{AC}.
R_{AC}	Reflected R_{OUT} : $8n^2/\pi^2 * R_{\mathrm{OUT}}$.
R_P, ρ_P	Primary loss component resistance, normalized R_P.

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I. Introduction

In recent years, electric vehicles (EVs) have been commercialized to meet the market demand of reducing fossil-fuel consumption and greenhouse gas emissions. These EVs, such as plug-in hybrid EVs and pure EVs, install a rechargeable battery pack and an on-board charger. Therefore, car drivers can charge the battery pack through an ac power outlet. The main challenge of an on-board charger is to attain a high power density; thus, a high-efficiency power conversion is necessary to achieve it.

The power architecture of an on-board charger in a 3- to 6-kW power range usually includes an ac–dc converter with power factor correction (PFC) followed by an isolated dc–dc converter. The PFC converter improves the quality of the input current and regulates its output voltage. The dc–dc converter charges the battery pack with the required charging current and provides isolation between the utility mains and the battery pack.

The power conversion efficiency of both converters should be improved to maintain high total efficiency of the on-board charger. The considered major feature is to improve the dc–dc converter efficiency because improvement of a nonisolated PFC converter is comparatively easy.

Among the various dc–dc converter topologies, the *LLC* converter is widely used owing to its advantages, such as zero-voltage switching capability of each main switch from zero to

full load without an auxiliary circuit, zero-current switching (ZCS) capability for rectifier diodes, and integration of two inductors into a single transformer. However, when output-voltage range is too wide, the rectifier diodes cannot achieve ZCS operation, and the voltage spike occurs. In addition, a too wide frequency range makes the optimization of the converter to be difficult. A design methodology is researched to avoid such disadvantage [1], [2]. As a result of this design method, a large resonant inductance ratio is selected. This large ratio causes a large magnetizing current; therefore, a large conduction loss occurs at the MOSFETs and transformer.

In the field of high-voltage power conversion, a multilevel converter that can reduce the voltage stress of the switching devices is proposed [3]–[8]. A combination of the *LLC* converter and a three-level conversion technique is also proposed [9]–[12]. The hybrid full-bridge three-level *LLC* resonant converter [13]–[15] can solve the above-described problem of the *LLC* converter. This converter integrates the advantages of the *LLC* converter and the three-level conversion technique. The conduction loss of the converter can be reduced by the three-level conversion circuit because low-voltage-rating power semiconductors can be used. In addition to such advantages, it can control the output power at a fixed frequency despite the *LLC* converter, and its rectifier diodes have a ZCS capability under wide output-voltage variation.

The control strategy of [13] uses a variable duty, and it can operate at a fixed frequency. However, using the graph of the voltage gain to design the converter parameters is difficult because it lacks versatility and the analysis uses a numerical method. The result of the analysis in the two- and a three-level modes is separately provided, which also makes the result difficult to use.

A fixed duty is used by the control strategy in [14], and it selects a two- or a three-level mode depending on the output voltage. Therefore, it cannot operate in a fixed frequency. It uses frequency modulation in combination with mode selection.

Wei *et al.* [15] does not operate in a state in which a full-bridge circuit outputs half of the input voltage to control the output power. It uses frequency modulation only. Therefore, it is the same as the conventional two-level converter from the perspective of control strategy.

This paper proposes a modulation method for a full-bridge three-level *LLC* resonant converter. It uses a variable duty and can operate at a fixed frequency. A parameter named "master duty" is introduced, which can seamlessly handle two-level, three-level, and mixed modes. The voltage gain can be calculated from the master duty and other normalized parameters unlike conventional numerical method. Because it is analyzed using the first-harmonic approximation (FHA) technique to design the converter parameters. The proposed modulation method is represented by the relationship between the master duty and each gate-pulse edge position. This representation clearly depicts a complex modulation such as a combination of pulse-width and phase-shift modulations. Moreover, configuring this modulation method is possible by changing this relationship. Therefore, the modulation method is expandable. The configured modulation method, which is suitable for the drive circuit using a bootstrap circuit, is also presented in this paper.

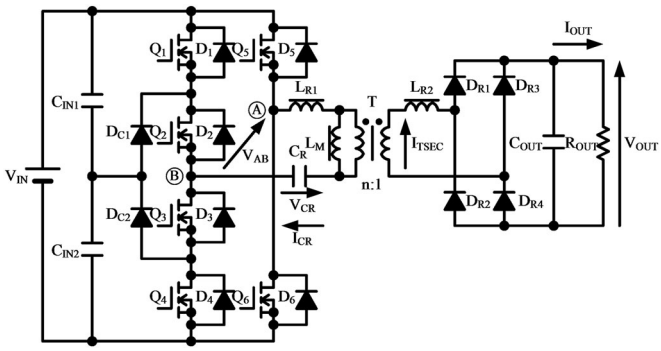

Fig. 1. Full-bridge three-level *LLC* resonant converter.

The circuit configuration and modulation method are described in Section II. In Section III, the voltage gain of the converter is analyzed by the FHA technique using this modulation method for the designer convenience. To confirm the validity of the analysis, a 6.6-kW prototype converter is fabricated, and the experimental results are shown in Section IV. The specification of the prototype converter is defined to ensure that it can be used in an on-board charger. The input voltage of the converter is 385 V, which is assumed as a minimum point of the output voltage of the PFC converter with a voltage ripple. The output-voltage range of the converter is from 225 to 378 V, which is assumed as a lithium-ion battery pack voltage with 90 cells in series and has a 4.2-V/cell charge cutoff voltage and a 2.5-V/cell discharge cutoff voltage. The rated output power of the converter is 6.6 kW, and the rated output current is 22 A.

II. Operating Principle

A. Relationship Between the Full-Bridge Output Voltage and Each Gate Pulse

Fig. 1 shows the target converter of the proposed modulation method. The voltage between points A and B in Fig. 1 is the output voltage of the full-bridge circuit. This voltage (V_{AB}) is the input voltage of the *LLC* resonant tank, and higher V_{AB} generates more energy through the *LLC* resonant tank; lower V_{AB} obtains less energy through the *LLC* resonant tank. Therefore, V_{AB} needs to be controlled to regulate the output power.

The absolute value of V_{AB} can be selected from zero, $V_{\mathrm{IN}}/2$, and V_{IN}. Fig. 2 shows the relationship between the V_{AB} and each gate pulse. We assume that the voltages of C_{IN1} and C_{IN2} are regulated to be $V_{\mathrm{IN}}/2$. The duty of the $V_{\mathrm{IN}}/2$ voltage level should be varied to balance the voltages of C_{IN1} and C_{IN2} because current flows to C_{IN1} or C_{IN2} when V_{AB} is equal to $\pm V_{\mathrm{IN}}/2$.

In a light or low-voltage load case, the absolute value of V_{AB} is selected from zero or $V_{\mathrm{IN}}/2$, as shown in Fig. 2(a), which is a two-level mode. In heavy and high-voltage loads, the absolute value of V_{AB} is selected from $V_{\mathrm{IN}}/2$ or V_{IN}, as shown in Fig. 2(b), which is a three-level mode. The mixed mode shown in Fig. 2(c) can be used if necessary. The output power can be regulated by the modulation of each duty of zero, $V_{\mathrm{IN}}/2$, and V_{IN}. Fig. 2 shows the edge position of the gate pulses that must be varied to control V_{AB}.

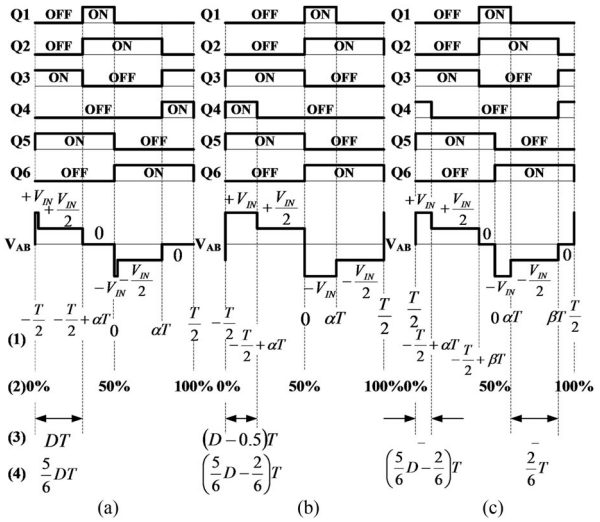

Fig. 2. Relationship between the full-bridge output voltage V_{AB} and each gate pulse. (1) Time, (2) edge position, (3) proposed modulation, and (4) modified modulation. (a) Two-level mode. (b) Three-level mode. (c) Mixed mode.

B. Modulation Method

The conventional modulation method described in [13] uses pulse width modulation for Q_1 and Q_4 in the three-level mode applied in heavy and high-voltage loads. It uses phase-shift modulation for Q_2, Q_3, Q_5, and Q_6 in the two-level mode applied in light or low-voltage load. In the three-level mode, the shifted phase is fixed, and in the two-level mode, the pulse width of Q_1 and Q_4 is zero. Fig. 3(a) shows the transitions of the leading and trailing edges of each gate pulse. In this figure, the dead time of each gate pulse and the small fixed-shift phase are omitted to facilitate understanding of the modulation method. The values of the edge position are 0% at the start of the switching period and 100% at the end of the switching period. They are shown in Fig. 2.

A problem arises in the fact that the conventional modulation method cannot handle the two- and three-level modes in the same manner, which makes the analysis of the three-level *LLC* resonant converter difficult. Therefore, this paper proposes a modulation method that introduces the parameter "master duty." The master duty determines each voltage-level duty, and the modulation method is defined by the relationship between the master duty and the position of the leading and trailing edges of each gate pulse, as shown in Fig. 3(b). Each edge position is calculated using the simple equations listed in Table I, and can be calculated in the same manner even under different modes, as shown in Fig. 2. The difference in the form between the conventional and the proposed modulation methods is only the leading edge of the Q_1 and Q_4 gate pulses. When V_{AB} is zero, resonant current flows through D_1 or D_4 if conventional modulation is used, and it flows through Q_1 or Q_4 if the proposed modulation is used except a short transition time. This operation is the same with the synchronous rectification. Therefore, the circuit operation of the proposed modulation is the same as that of the conventional modulation.

A problem in the proposed modulation arises if the Q_3 drive circuit uses the bootstrap power-supply technique because the on-duty of the Q_4 gate pulse is zero when the master duty is 50%. This problem can be solved by modifying of the proposed modulation, as shown in Fig. 3(c). The minimum on-duty of the Q_4 gate pulse is 16.7% in the modulation method, as shown in Fig. 3(c), and no problem arises if the bootstrap power-supply technique is used. The mixed mode occurs when the master duty is greater than 40% and less than 60%.

III. Characteristics of the Three-level *LLC* Converter Using the Proposed Modulation Method

The FHA technique is often used to analyze the characteristics of a resonant converter [16], [17], [19]. The FHA is based on the assumption that power transfer from the input to the output is essentially due to the fundamental Fourier series components of the currents and voltages. The normalized parameters are used in the analysis in consideration of general versatility. They are defined in the nomenclature section.

A. Analysis by FHA

The equivalent circuit shown in Fig. 1 by the FHA is shown in Fig. 4. From Fig. 4, nE_{OUT} is calculated using $C_R, L_{R1}, L_{R2}, L_M, R_{\mathrm{AC}}$, and E_{IN}. The transfer function is analyzed in [18], and the result is expressed as

$$\frac{nE_{\mathrm{OUT}}}{E_{\mathrm{IN}}} = \frac{1}{\sqrt{\left(1+\lambda_1-\frac{\lambda_1+\lambda_2}{f_N^2}\right)^2+Q^2\left(\left(1+\frac{\lambda_1\lambda_2}{\lambda_1+\lambda_2}\right)f_N-\frac{1+\lambda_2}{f_N}\right)^2}}. \tag{1}$$

E_{OUT} is the voltage fundamental component of a square waveform whose amplitude is V_{OUT}. Therefore, E_{OUT} is equal to $4V_{\mathrm{OUT}}/\pi$.E_{IN} is the voltage fundamental component of waveform V_{AB} shown in Fig. 2. Therefore, the value of E_{IN} is calculated by (2) in the three-level mode using the proposed modulation, and it is calculated by (3) in the two-level mode using the proposed modulation, where "*D*" in (2) and (3) represents the "master duty." Equations (4)–(6) show the value of E_{IN} in the three-level, mixed, and two-level mode, respectively, using the proposed modified modulation method. The procedure to derive (2)–(6) is described in the Appendix. We assumed that the short-term V_{IN} voltage level can be neglected in two-level mode

$$E_{\mathrm{IN}} = \frac{V_{\mathrm{IN}}}{\pi}\sqrt{10+6\cos 2\pi D} \tag{2}$$

$$E_{\mathrm{IN}} = \frac{V_{\mathrm{IN}}}{\pi}\sqrt{2-2\cos 2\pi D} \tag{3}$$

$$E_{\mathrm{IN}} = \frac{V_{\mathrm{IN}}}{\pi}\sqrt{10+3\cos\frac{5}{3}\pi D-3\sqrt{3}\sin\frac{5}{3}\pi D} \tag{4}$$

$$E_{\mathrm{IN}} = \frac{V_{\mathrm{IN}}}{\pi}\sqrt{5-2\cos\frac{5}{3}\pi D-2\sqrt{3}\sin\frac{5}{3}\pi D} \tag{5}$$

$$E_{\mathrm{IN}} = \frac{V_{\mathrm{IN}}}{\pi}\sqrt{2-2\cos\frac{5}{3}\pi D}. \tag{6}$$

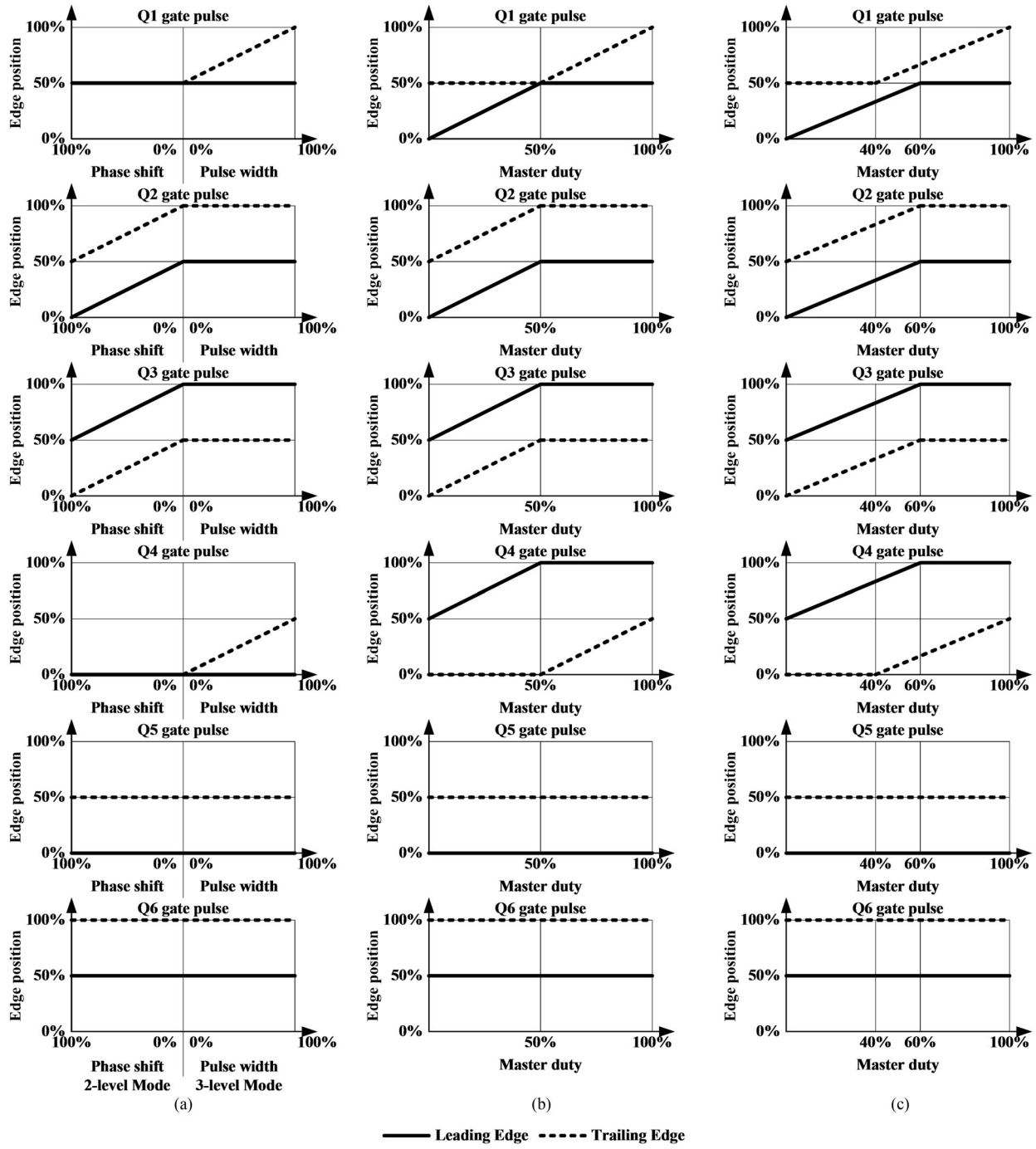

Fig. 3. Modulation methods expressed by the gate-pulse edge position. (a) Conventional modulation. (b) Proposed modulation. (c) Modified modulation.

The voltage gain M of the proposed modulation is obtained from (1)–(3)

$$M = \frac{M_1}{\sqrt{\left(1+\lambda_1-\frac{\lambda_1+\lambda_2}{f_N^2}\right)^2 + Q^2\left(\left(1+\frac{\lambda_1\lambda_2}{\lambda_1+\lambda_2}\right)f_N-\frac{1+\lambda_2}{f_N}\right)^2}}$$

$$M_1 = \begin{cases} \sqrt{\dfrac{1-\cos 2\pi D}{8}}, & 0 < D \le 0.5 \\ \sqrt{\dfrac{5+3\cos 2\pi D}{8}}, & 0.5 < D < 1 \end{cases}. \quad (7)$$

The voltage gain M of the modified modulation is obtained from (1) and (4)–(6)

$$M = \frac{M_1}{\sqrt{\left(1+\lambda_1-\frac{\lambda_1+\lambda_2}{f_N^2}\right)^2 + Q^2\left(\left(1+\frac{\lambda_1\lambda_2}{\lambda_1+\lambda_2}\right)f_N-\frac{1+\lambda_2}{f_N}\right)^2}}$$

$$M_1 = \begin{cases} \sqrt{\dfrac{1-\cos\frac{5}{3}\pi D}{8}}, & 0 < D \le 0.4 \\ \sqrt{\dfrac{5-2\cos\frac{5}{3}\pi D-2\sqrt{3}\sin\frac{5}{3}\pi D}{16}}, & 0.4 < D < 0.6 \\ \sqrt{\dfrac{10+3\cos\frac{5}{3}\pi D-3\sqrt{3}\sin\frac{5}{3}\pi D}{16}}, & 0.6 \le D < 1 \end{cases}. \quad (8)$$

TABLE I
EQUATIONS OF THE GATE PULSE EDGE POSITION

Switch	Edge selection	Edge position	
		Proposed modulation	Modified modulation
Q_1	Leading Edge	min(0.5, D)	min(0.5, 5/6 × D)
	Trailing Edge	max(0.5, D)	max(0, 5/6 × D + 1/6)
Q_2	Leading Edge	min(0.5, D)	min(0.5, 5/6 × D)
	Trailing Edge	min(1, D + 0.5)	min(1, 5/6 × D + 0.5)
Q_3	Leading Edge	min(1, D + 0.5)	min(1, 5/6 × D + 0.5)
	Trailing Edge	min(0.5, D)	min(0.5, 5/6 × D)
Q_4	Leading Edge	min(1, D + 0.5)	min(1, 5/6 × D + 0.5)
	Trailing Edge	max(0, D - 0.5)	max(0, 5/6 × D - 2/6)
Q_5	Leading Edge	0	0
	Trailing Edge	0.5	0.5
Q_6	Leading Edge	0.5	0.5
	Trailing Edge	1	1

D: Master duty.

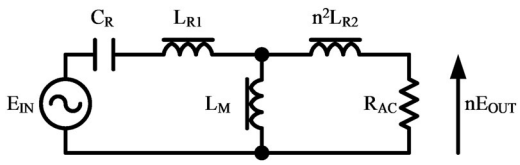

Fig. 4. AC equivalent circuit of the proposed converter.

When the converter operates at a fixed frequency, the controller can change only M_1. The relationship between M_1 and the master duty is shown in Fig. 5, which shows that M changes from zero to the value determined by the denominator of M. Therefore, the proposed converter is suitable for a wide output-voltage range application. Fig. 5 shows that the modified modulation method has better linearity than the proposed modulation method.

In the conventional *LLC* converter case, (1) only expresses M because both the input and output voltages in Fig. 4 have a square waveform

$$M = \frac{1}{\sqrt{\left(1+\lambda_1-\frac{\lambda_1+\lambda_2}{f_N^2}\right)^2+Q^2\left(\left(1+\frac{\lambda_1\lambda_2}{\lambda_1+\lambda_2}\right)f_N-\frac{1+\lambda_2}{f_N}\right)^2}}. \tag{9}$$

This equation reveals that decreasing M is difficult when the inductance ratio is small. Therefore, the conventional *LLC* converter is not suitable for a wide output-voltage range application.

Fig. 6 shows the comparison result of the voltage gain calculated by (7) and (8) and that calculated by the circuit simulator by using parameters listed in Table II. FHA analysis corresponds to that of the circuit simulator.

Fig. 7 shows the output characteristics curves calculated by (7) by using parameters listed in Table II. The quality factor Q is changed from 0.01 to 1000 to draw these curves.

The normalized switching frequency f_N is 1.1 in Table II. That means switching frequency is higher than resonant frequency. In this case, secondary diodes cannot run at the ZCS condition in two-level *LLC* converter; however, they can run

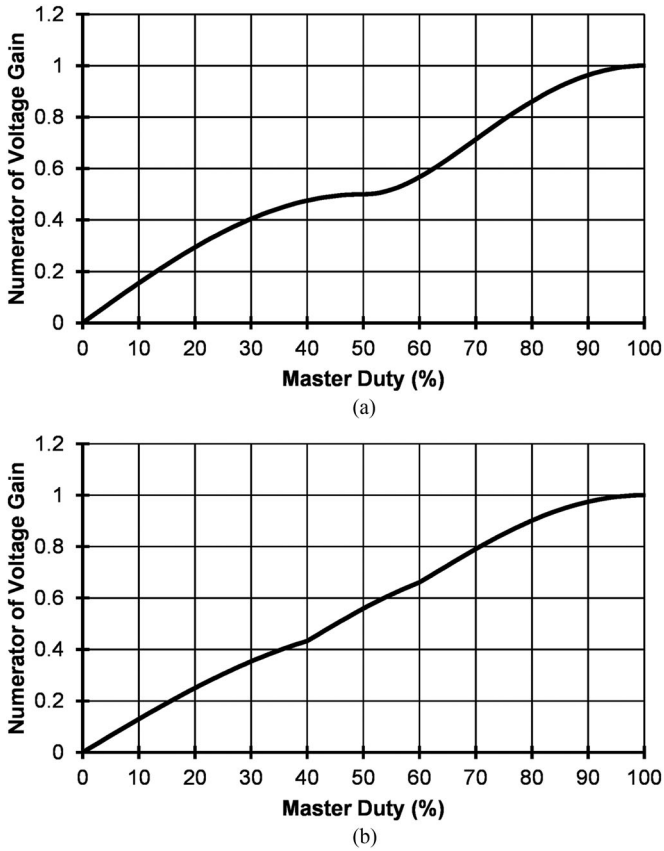

Fig. 5. Numerator of the voltage gain versus master duty. (a) Proposed modulation. (b) Modified modulation.

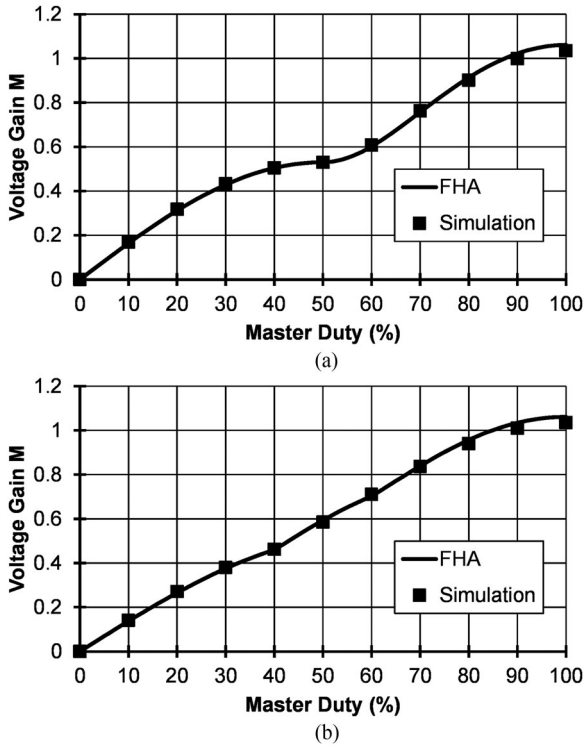

Fig. 6. Voltage-gain comparison between the FHA and simulated value. (a) Proposed modulation. (b) Modified modulation.

TABLE II
NORMALIZED PARAMETERS SHOWN IN FIG. 6

λ_1	λ_2	f_N	Z_O	n	Q
0.1	0.1	1.1	10	1	0.57

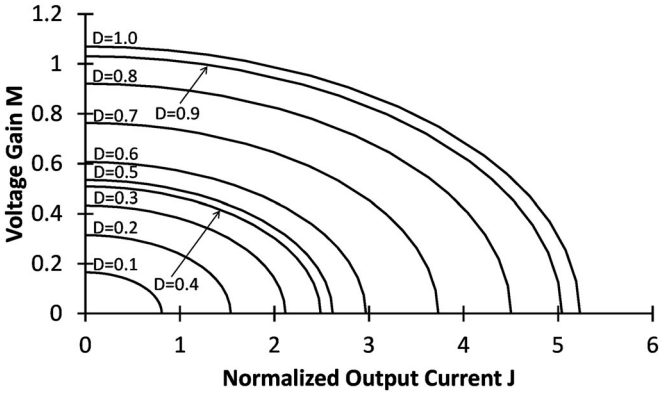

Fig. 7. Output characteristics curves.

TABLE III
PARAMETERS OF THE PROTOTYPE CONVERTER

V_{IN} 385 V	V_{OUT} 378 V	R_{OUT} 21.65 Ω	C_{IN1} C_{IN2} 3,760 μF	C_{OUT} 10 μF	f_{SW} 90 kHz	n 1
C_R 0.297 μF	L_{R1} L_{R2} 7 μH	L_M 190 μH	λ_1 λ_2 0.0368	f_N 1.153	Z_O 6.866 Ω	Q 0.391
Q_1–Q_4 IPB200N25N3 G 250 V 64 A 20 mΩ Infinion/2 parallel		Q_5, Q_6 Custom chip 500 V 42 A 120 mΩ Shindengen/4 parallel			Transformer PC40 EC90 × 90 × 30 Pri 11 turns Sec 11 turns Litz wire 100/0.08ϕ 12 layers	
D_{C1}, D_{C2} DF20LC30 300 V 20 A Shindengen/2 parallel		D_{R1}–D_{R4} S20LC40UV 400 V 20 A Shindengen/2 parallel				

at the ZCS condition in three-level *LLC* converter, because the current of the resonant tank decreases more quickly when $V_{\rm AB}$ is equal to $V_{\rm IN}/2$. Fig. 8 shows the difference of both converters. The parameters used in this simulation are shown in Table III except $V_{\rm IN}$, $V_{\rm OUT}$, and $R_{\rm OUT}$.

B. Analysis With Lossy Components

In the above analysis, we assume that all components have no loss. However, real converters have lossy components. Therefore, analysis considering the lossy components is required. To simplify the analysis, primary resistor $R_{\rm P}$ is added, which represents all losses in the converter. An extended equivalent circuit is shown in Fig. 9.

Primary resistor R_P is normalized to ρ_P by $R_{\rm AC}$

$$\rho_P = \frac{R_P}{R_{\rm AC}}. \tag{10}$$

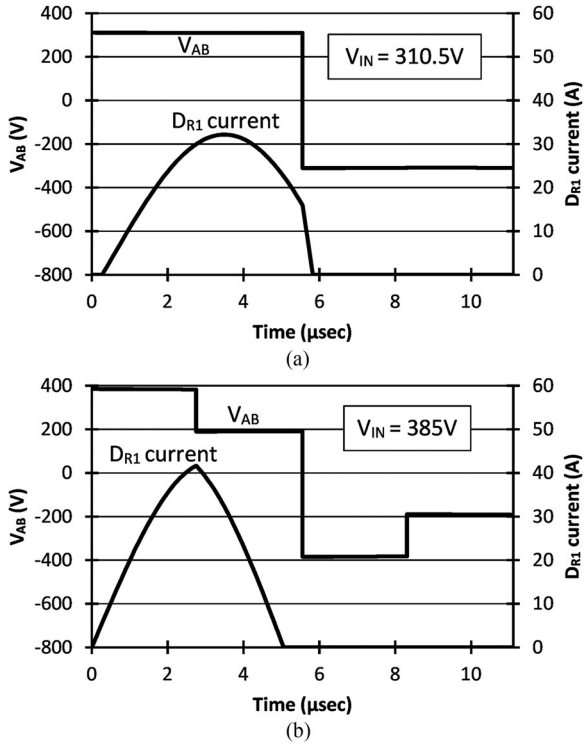

Fig. 8. D_{R1} current comparison between the two-level and three-level *LLC* converter. (a) Two-level *LLC* converter at $V_{\rm OUT} = 300\,{\rm V}$ and $R_{\rm OUT} = 13.64\,\Omega$. (b) Three-level *LLC* converter at $V_{\rm OUT} = 300\,{\rm V}$ and $R_{\rm OUT} = 13.64\,\Omega$.

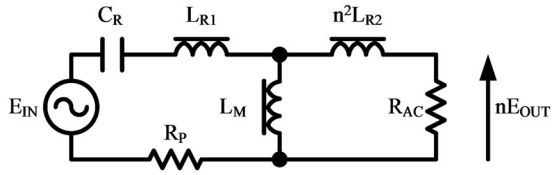

Fig. 9. AC equivalent circuit of the proposed converter.

Equation (7) is reexpressed as (11) by ρ_P

$$\begin{aligned} M &= \frac{M_1}{\sqrt{M_2^2 + M_3^2}} \\ M_1 &= \begin{cases} \sqrt{\frac{1-\cos 2\pi D}{8}}, & 0 < D \le 0.5 \\ \sqrt{\frac{5+3\cos 2\pi D}{8}}, & 0.5 < D < 1 \end{cases} \\ M_2 &= 1 + \lambda_1 + \rho_P\,(1+\lambda_2) - \frac{\lambda_1+\lambda_2}{f_N^2} \\ M_3 &= \left(1 + \frac{\lambda_1\lambda_2}{\lambda_1+\lambda_2}\right) Q f_N - \frac{Q^2\,(1+\lambda_2) + \rho_P\,(\lambda_1+\lambda_2)}{Q f_N} \end{aligned} \tag{11}$$

The estimated $R_{\rm P}$ value is 349 mΩ ($V_{\rm OUT}$: 378 V; $I_{\rm OUT}$: 17.46 A). It consists of the following: transformer winding resistance: 104 mΩ (52 mΩ for the primary and secondary windings), core loss: 69 mΩ (21 W/17.46 A^2), Q_1–Q_4 on-resistance: 20 mΩ

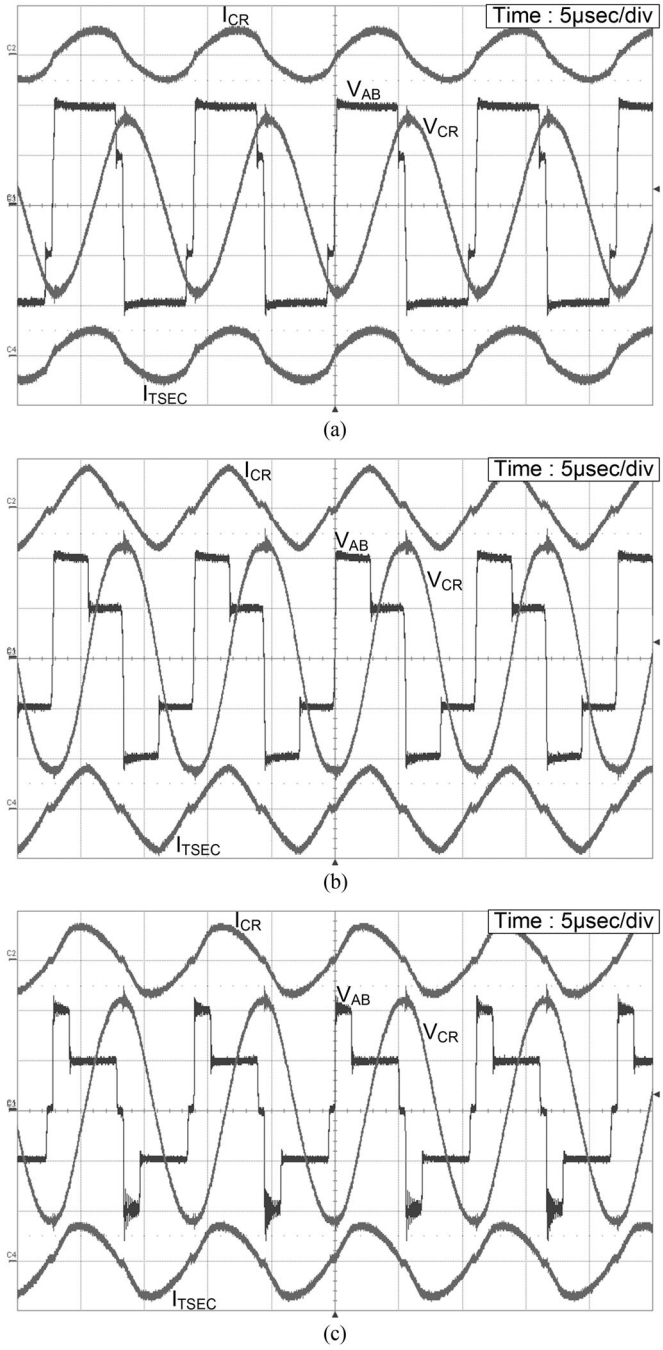

Fig. 10. Experimental waveforms. (a) $I_{\mathrm{CR}}\,[20\,\mathrm{A/div}], V_{\mathrm{CR}}\,[200\,\mathrm{V/div}], V_{\mathrm{AB}}\,[200\,\mathrm{V/div}]$, and $I_{\mathrm{TSEC}}\,[20\,\mathrm{A/div}]$ at $V_{\mathrm{OUT}} = 378\,\mathrm{V}$ and $W_{\mathrm{OUT}} = 6.6\,\mathrm{kW}$. (b) $I_{\mathrm{CR}}\,[20\,\mathrm{A/div}], V_{\mathrm{CR}}\,[200\,\mathrm{V/div}], V_{\mathrm{AB}}\,[200\,\mathrm{V/div}]$, and $I_{\mathrm{TSEC}}\,[20\,\mathrm{A/div}]$ at $V_{\mathrm{OUT}} = 300\,\mathrm{V}$ and $W_{\mathrm{OUT}} = 6.6\,\mathrm{kW}$. (c) $I_{\mathrm{CR}}\,[20\,\mathrm{A/div}], V_{\mathrm{CR}}\,[200\,\mathrm{V/div}], V_{\mathrm{AB}}\,[200\,\mathrm{V/div}]$, and $I_{\mathrm{TSEC}}\,[20\,\mathrm{A/div}]$ at $V_{\mathrm{OUT}} = 225\,\mathrm{V}$ and $I_{\mathrm{OUT}} = 22\,\mathrm{A}$.

(20 mΩ; two parallel and two series connections), Q_5 and Q_6 on-resistance: 30 mΩ (120 mΩ; four parallel connections), and $D_{\mathrm{R}1}$–$D_{\mathrm{R}4}$: 126 mΩ (1.1 V/17.46 A; two series connections).

IV. Experimental Results

Table III shows the parameters of the prototype converter, which are calculated to have a 94.56% master duty at 378-V output voltage and 6.6-kW output power using lossy analysis. The converter is controlled by digital signal processor TMS320F28034. The switching frequency is selected to be greater than resonant frequency. However, secondary diodes can run at the ZCS condition because the current of the resonant tank decreases more quickly when V_{AB} is equal to $V_{\mathrm{IN}}/2$.

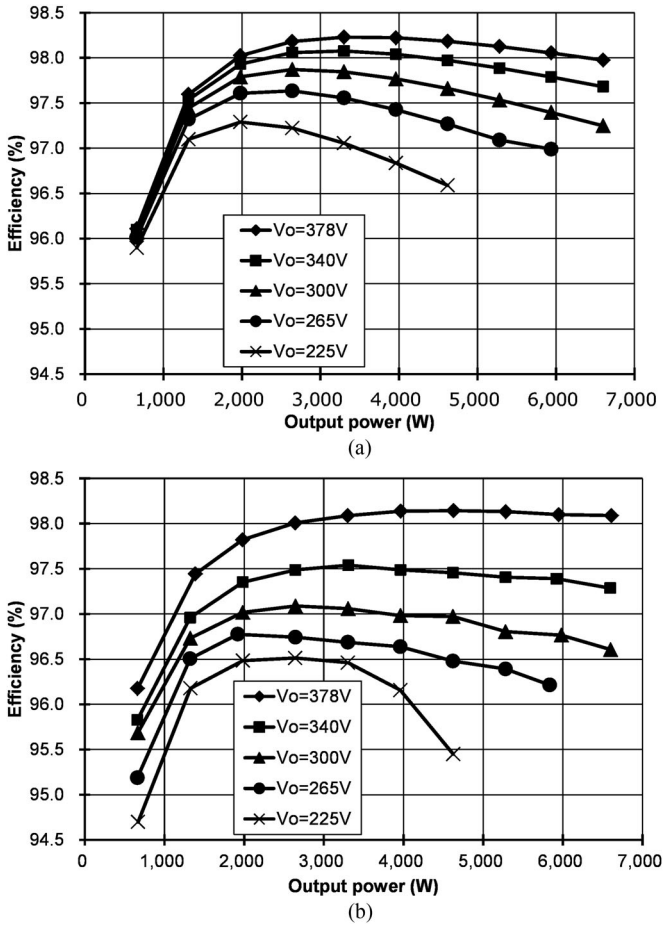

Fig. 11. Efficiency at different output power under 225-, 265-, 300-, 340-, and 378-V output voltage. (a) Simulated result. (b) Experimental result.

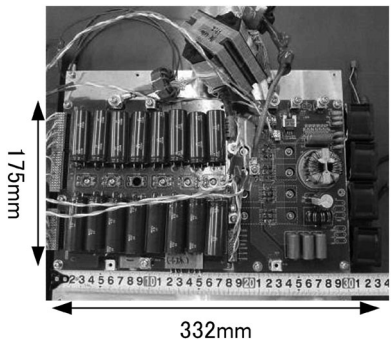

Fig. 12. Photograph of the prototype converter.

A. ZCS of Rectifier Diodes

Fig. 10(a)–(c) shows the experimental waveforms of $I_{\mathrm{CR}}, V_{\mathrm{CR}}, V_{\mathrm{AB}}$, and I_{TSEC} at the output voltage–power–current

TABLE IV
FOURIER SERIES COMPONENTS OF WAVEFORM V_{AB}

Two-level mode	$-\frac{V_{\mathrm{IN}}}{\pi}\sum_{n=1,3,5\ldots}\frac{\sin 2\pi n\alpha\cos n\omega t+(1-\cos 2\pi n\alpha)\sin n\omega t}{n}$
Three-level mode	$-\frac{V_{\mathrm{IN}}}{\pi}\sum_{n=1,3,5\ldots}\frac{\sin 2\pi n\alpha\cos n\omega t+(3-\cos 2\pi n\alpha)\sin n\omega t}{n}$
Mixed mode	$-\frac{V_{\mathrm{IN}}}{\pi}\sum_{n=1,3,5\ldots}\frac{(\sin 2\pi n\alpha+\sin 2\pi n\beta)\cos n\omega t+(2-\cos 2\pi n\alpha-\cos 2\pi n\beta)\sin n\omega t}{n}$

values of 378 V–6.6 kW–17.5 A, 300 V–6.6 kW–22 A, and 225 V–4.95 kW–22 A, respectively. These waveforms illustrate how the ZCS operation of the rectifier diodes is achieved in a wide output-voltage range. No snubber circuit is required for the rectifier diodes in the prototype converter. No waveform for the no-load operation is presented. The voltage-balancing control for C_{IN1} and C_{IN2} cannot correctly work because sufficient magnetizing current is not obtained at no-load. Therefore, the PFC converter should perform the voltage-balancing control.

B. Efficiency Characteristic

Fig. 11 shows the simulated and measured efficiency of the prototype converter as a function of the output power, where the output voltage changes from 225 to 378 V. The simulated efficiency at full load and 378-V output voltage is 97.98%, and the measured efficiency is 98.09%. The maximum efficiency of the converter, which occurs around 4600 W, is 98.14%. The measured "$V_{\mathrm{O}} = 378$ V" curve is similar to the simulated one.

C. Power Density

Fig. 12 shows a photograph of the prototype converter. It has PFC and dc–dc converters. Its size without the transformer and PFC inductors is $332 \times 175 \times 95\,\mathrm{mm}$. The actual volume of the prototype converter after considering the transformer and inductors is 6.05 L. Therefore, the power density of the prototype converter is 1091 W/L.

D. Validation of the Analysis

The prototype converter uses the proposed modulation method. The measured master duty at full load and 378-V output voltage is 94.2%, and the master duty calculated by (11) is 94.56%.

Calculating R_{P} using the efficiency is possible. The efficiency at full load and 378-V output voltage is 98.09%; therefore, the input dc current is 6600 W/(98.09% × 385 V) = 17.48 A. Then, the primary resonant current is $17.48\,\mathrm{A} \times \pi/2\sqrt{2} = 19.41\,\mathrm{A}$ because the average of the primary resonant current is equal to the input dc current. The total loss is $6600\,\mathrm{W} \times (1/0.9809 - 1) = 128.5\,\mathrm{W}$. Therefore, $R_P = 128.5\,\mathrm{W}/(19.41\,\mathrm{A} \times 19.41\,\mathrm{A}) = 0.341\,\mathrm{W}$. The estimated R_P is 0.349 Ω. The estimated value approximately corresponds to the value calculated from the efficiency.

V. CONCLUSION

A modulation method for a full-bridge three-level *LLC* converter has been proposed. This method enables the converter to operate at a fixed frequency. Each gate-pulse edge position can be easily calculated from the master duty, and determining the operating mode, i.e., two-level, three-level, or mixed mode, is not necessary. The modulation method can be modified by changing the relationship between the master duty and the edge of each gate pulse. A sample modification is presented, which is useful when the bootstrap power-supply technique is used in the drive circuit.

The equation for the voltage gain in this paper is derived by the FHA technique using the proposed and modified modulation methods with lossy circuits. This equation is versatile, unlike that in the numerical method. This equation allows the designer to possibly calculate the proper transformer turns ratio. A prototype converter is fabricated for validation. The turn's ratio of the prototype converter is designed to have a 94.56% maximum master duty, and the experimental result is 94.2%. Therefore, we have validated that the equation for the voltage gain is useful in the design of the full-bridge three-level *LLC* converter.

Our next research target is to introduce a multilevel conversion technique to the PFC converter to solve the capacitor-balancing problem.

APPENDIX

The waveforms of V_{AB} shown in Fig. 2 can be expressed by the equations listed in Table IV using the Fourier series components. By substituting 1 for *n*, the fundamental components of V_{AB} are obtained, and they are listed in Table V. To derive the formula, the following relationship is used:

$$\alpha\,\sin x + b\cos\,x = \sqrt{a^2+b^2}\sin(\mathrm{x}+\varphi)$$
$$\varphi\begin{cases}\sin^{-1}\dfrac{b}{\sqrt{a^2+b^2}}, & a \geq 0\\ \pi-\sin^{-1}\dfrac{b}{\sqrt{a^2+b^2}}, & a<0\end{cases}. \tag{12}$$

The peak value of the fundamental component is obtained from Table V, and they are listed in Table VI. The edge position of the V_{AB} is also listed in this table. Each edge position can be obtained from Table I. For example, α in the mixed mode of the modified modulation can be obtained from the trailing edge of Q_4.

TABLE V
FUNDAMENTAL COMPONENT OF WAVEFORM V_{AB}

Two-level mode	$-\frac{V_{\mathrm{IN}}}{\pi}\cdot\sqrt{2-2\cos 2\pi\alpha}\sin\left(\omega t+\sin^{-1}\frac{\sin 2\pi\alpha}{\sqrt{2-2\cos 2\pi\alpha}}\right)$
Three-level mode	$-\frac{V_{\mathrm{IN}}}{\pi}\cdot\sqrt{10-6\cos 2\pi\alpha}\sin\left(\omega t+\sin^{-1}\frac{\sin 2\pi\alpha}{\sqrt{10-6\cos 2\pi\alpha}}\right)$
Mixed mode	$-\frac{V_{\mathrm{IN}}}{\pi}\cdot\sqrt{6+2\cos 2\pi\left(\beta-\alpha\right)-4\left(\cos 2\pi\alpha+\cos 2\pi\beta\right)}\sin\left(\omega t+\sin^{-1}\frac{\sin 2\pi\alpha+\sin 2\pi\beta}{\sqrt{6+2\cos 2\pi\left(\beta-\alpha\right)-4\left(\cos 2\pi\alpha+\cos 2\pi\beta\right)}}\right)$

TABLE VI
PEAK VALUES OF THE FUNDAMENTAL COMPONENTS AND EACH EDGE POSITION

		Two-level mode	Three-level mode	Mixed mode
Peak value of the fundamental component		$\frac{Vin}{\pi}\cdot\sqrt{2-2\cos 2\pi\alpha}$	$\frac{Vin}{\pi}\cdot\sqrt{10-6\cos 2\pi\alpha}$	$\frac{Vin}{\pi}\cdot\sqrt{6+2\cos 2\pi(\beta-\alpha)-4(\cos 2\pi\alpha+\cos 2\pi\beta)}$
Proposed modulation	**α**	D	$D-\frac{1}{2}$	
Modified modulation	**α**	$\frac{5}{6}D$	$\frac{5}{6}D-\frac{2}{6}$	$\frac{5}{6}D-\frac{2}{6}$
	β			$\frac{5}{6}D$

TABLE VII
PEAK VALUES OF THE FUNDAMENTAL COMPONENTS EXPRESSED BY MASTER DUTY

	Two-level mode	Three-level mode	Mixed mode
Proposed modulation	$\frac{V_{IN}}{\pi}\sqrt{2-2\cos 2\pi D}$	$\frac{V_{IN}}{\pi}\sqrt{10+6\cos 2\pi D}$	
Modified modulation	$\frac{V_{IN}}{\pi}\sqrt{2-2\cos\frac{5}{3}\pi D}$	$\frac{V_{IN}}{\pi}\sqrt{10+3\cos\frac{5}{3}\pi D-3\sqrt{3}\sin\frac{5}{3}\pi D}$	$\frac{V_{IN}}{\pi}\sqrt{5-2\cos\frac{5}{3}\pi D-2\sqrt{3}\sin\frac{5}{3}\pi D}$

From the information listed in Table VI, the peak value of the fundamental components can be expressed by the master duty. They are listed in Table VII.

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