Modeling Inductive Switching Characteristics of High-Speed Buffer Layer IGBT

Peng Xue, Guicui Fu, and Dong Zhang

***Abstract*—In this study, a physics-based compact model for high-speed buffer layer insulated gate bipolar transistor (IGBT) is proposed. The model utilizes the 1-D Fourier-based solution of ambipolar diffusion equation (ADE) implemented in MATLAB and Simulink. Based on the improved understanding on the inductive switching behavior of a high-speed buffer layer IGBT, the ADE is solved for all injection levels instead of high-level injection only as usually done. Assuming high-level injection condition in the buffer layer, the excess carrier transport, redistribution and recombination in the buffer layer are redescribed. Moreover, some physical characteristics such as the low conductivity of N-base at turn-on transient and free holes appeared in the depletion layer during turn-off process are also considered in the model. Finally, the double-pulse switching tests for a commercial field stop IGBT and a light punch-through carrier-stored trench bipolar transistor are used to validate the proposed model. The simulation results are compared with experiment results and good agreement is obtained.**

***Index Terms*—Field stop (FS) IGBT, insulated gate bipolar transistor (IGBT), light punch-through (LPT), carrier-stored trench bipolar transistor (CSTBT), physics-based IGBT model, power semiconductor modeling.**

I. Introduction

In recent years, the improvements of the insulated gate bipolar transistor (IGBT) technology are mainly to reduce switching losses while maintaining a low forward voltage drop [1]–[4]. In order to achieve this technical goal, many similar concepts like "field stop (FS)" [1], "soft punch-through (PT)" [2], "light punch-through (LPT)" [3] and "thin wafer PT" [4] are introduced. In these design concepts, an optimized N^+ buffer layer is introduced. With the buffer layer, the new kinds of IGBTs can provide better tradeoff relationship between the forward voltage drop and switching losses compared to the conventional PT IGBT and non-punch-through (NPT) IGBT [1], [3]. Since these design concepts have been widely used in the high-speed IGBT nowadays, it is necessary to develop a unified IGBT compact model with these concepts taken into account.

Review the previous literature on compact IGBT modeling [5]–[23], most of the works focus on modeling the NPT IGBT [8]–[18] or PT IGBT [5]–[7]. The high-speed buffer layer IGBT, so far, has received relatively scare attention and only a few compact models are available to date [19]–[23]. Among these works, the models proposed in [19]–[21] focus on characterizing the IGBT turn-off transient while the works [22], [23] are presented for IGBT turn-on modeling. In [19] and [20], the PT IGBT model proposed in [6] is directly used to characterize the inductive turn-off behavior of FS IGBT and LPT carrier stored trench bipolar transistor (CSTBT). This fails to consider the fabrication characteristics of FS layer and LPT buffer layer. Compared to the conventional PT buffer layer, the new kinds of buffer layers are optimized to be lighter and thinner [1], [24]. The low-level injection assumption for PT buffer layer is not valid any more. Therefore, the carrier transport, redistribution, and recombination in the buffer layer should be reconsidered. In [21], the high-level injection assumption is adopted for the FS layer to model the unclamped inductive turn-off behavior of FS IGBT. However, the model has few main disadvantages. First, since the unclamped inductive switching is not utilized in the industrial converter applications, this model may be incapable to be used in the converter simulation. Second, the model utilizes the analytical solution of ambipolar diffusion equation (ADE) proposed by Hefner [5], [12], which can only approximately describe the excess carrier dynamics in N-base. Finally, the relatively high doping concentration in the FS layer is not considered in the buffer layer modeling. For the turn-on modeling, the models proposed in [22] and [23] assume the high-level injection condition in the N-base at turn-on transient. Since the low-level injection in the N-base is not included, these models may be incapable to accurately model the conductivity modulation process during turn-on process.

In the industrial applications, the IGBTs usually operate under clamped inductive switching conditions. Nowadays, with the introduction of the optimized N^+ buffer layer, the turn-off losses is significantly reduced. On the other hand, duo to the freewheel diode reverse recovery, the IGBT turn-on losses are also considerable, and may be comparable to the turn-off losses [23]. Therefore, the inductive turn-on behavior should also be considered in the buffer layer IGBT modeling method. In this study, based on the improved understanding on the inductive switching behavior of fast buffer layer IGBT, a compact IGBT model is presented to model both of the inductive turn-on and turn-off behaviors. The Fourier-based method [13], [20], which can provide fast and accurate simulation, is utilized to solve the ADE. Unlike the previous attempts, the solution includes both the high-level and low-level injection conditions. Moreover, based on the design concept of buffer layer in the high-speed IGBT, the excess carrier transport, redistribution, and recombination in the buffer layer are redescribed. The low conductivity of N-base at turn-on transient and free holes

Manuscript received November 5, 2015; revised February 8, 2016 and March 29, 2016; accepted May 11, 2016. Date of publication May 19, 2016; date of current version January 20, 2017. This work was supported by the Academic Excellence Foundation of BUAA for Ph.D. students. Recommended for publication by Associate Editor A. Mertens.

The authors are with the School of Reliability and System Engineering, Beihang University, Beijing 100191, China (e-mail: demosupen@buaa.edu.cn; fuguicui@buaa.edu.cn; zhangdong@buaa.edu.cn).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2570838

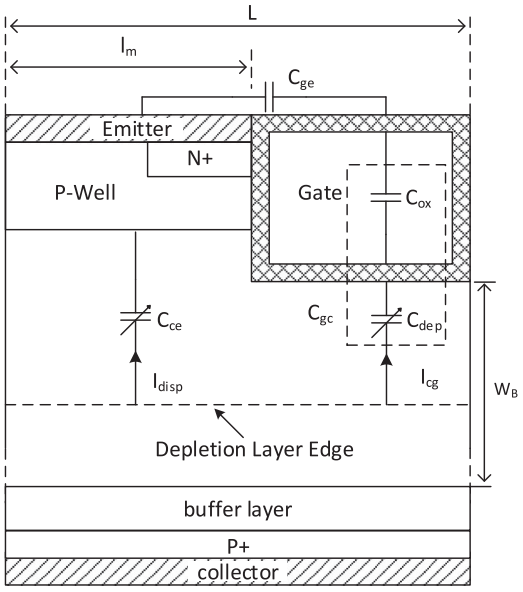

Fig. 1. Buffer layer IGBT structure with geometry definition and capacitance distribution.

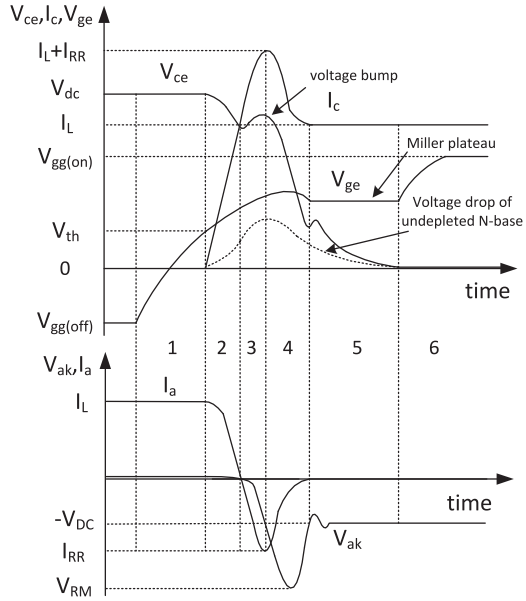

Fig. 2. Waveforms of buffer layer IGBT inductive turn-on and diode reverse recovery behaviors.

presented in the depletion layer during turn-off process are also considered in the model.

The paper is organized as follows. In Section II, the characteristics of buffer layer IGBT and their influences on the inductive switching behaviors are discussed. In Section III, the physics-based model for the high-speed buffer layer IGBT is presented. In Section IV, the implementation of the proposed model using MATLAB and Simulink is given in details. In Section V, the results of double-pulse tests on a commercial FS IGBT and an LPT CSTBT are presented. The proposed model is then validated by the comparison between the experiment and simulation results.

II. Inductive Switching Behavior of High-Speed Buffer Layer IGBT

The description of the switching transient of the NPT and PT IGBTs have already been reported in [25], [26], and [23]. In this section, the various design concepts of the buffer layer in high-speed IGBTs are briefly reviewed at first. Based on the buffer layer design concepts, the inductive turn-on and turn-off processes are extensively discussed. The aim is to find out the physical characteristics of the buffer layer IGBT that influence the inductive switching behavior, which is presented in the end of this section.

During switching transient, the stray capacitances in the IGBT play an important role in determining the inductive switching behavior. The capacitance distribution of buffer layer IGBT is shown in Fig. 1. In the switching transient, the variation of depletion layer width results in two branches of displacement current, the collector–gate displacement current $I_{\rm cg}$, and the collector–emitter displacement current $I_{\rm disp}$. The $I_{\rm disp}$ flows through the capacitance $C_{\rm ce}$. The $I_{\rm cg}$ flows through the gate-side Miller capacitance $C_{\rm gc}$, which is the series combination of gate-oxide capacitance $C_{\rm ox}$ and the depletion capacitance $C_{\rm dep}$. Another gate-side stray capacitance is the gate–emitter capacitance $C_{\rm ge}$, which is in parallel with the Miller capacitance $C_{\rm gc}$.

A. Concepts of Buffer Layer in High-Speed IGBTs

In a high-speed IGBT, the buffer layer design concepts like "FS," "soft PT," "LPT," and "thin wafer PT" share a same technical goal, which is to provide the best tradeoff relationship between the forward voltage drop and switching losses [1], [2], [4], [24]. In order to achieve this goal, the buffer layer in high-speed IGBT is optimized to be thin and lightly doped. Typically, the doping concentration of the buffer layer is approximately $10^{15} - 10^{16}\text{cm}^{-3}$ [1], [27].

The buffer layer excess carrier injection conditions in these high-speed IGBTs are different from that of the conventional PT IGBT. In static condition, the excess carrier concentration in buffer layer can exceed 10^{16}cm^{-3} [3], [27]. During turn-off transient, the excess carrier concentration in buffer layer is further increased since all the excess holes in N-base are swept into the buffer layer [21]. The injected excess carrier concentration approaches or exceeds the doping concentration of buffer layer at all time. Therefore, the conventional low-level injection assumption for PT buffer layer is not validated anymore, it is necessary to adopt the high-level injection assumption in the new kinds of buffer layers.

B. Inductive Turn-On Behavior

In the inductive turn-on switching, there is a strong interaction between IGBT that is turning ON and the freewheel diode that is undertaking reverse recovery [23]. The typical waveforms of buffer layer IGBT inductive turn-on and diode reverse recovery

are given in Fig. 2. The turn-on process can be divided into six phases, which are as follows.

Phase 1). In phase 1, the IGBT is OFF and gate–emitter voltage V_{ge} is below the threshold voltage V_{th}. Since the depletion layer is very wide, the depletion capacitance C_{dep} is very small. The Miller capacitance C_{gc} is thereby much smaller than the capacitance C_{ge}. During this phase, only the capacitance C_{ge} is charging, which results in the increasing of V_{ge}.

Phase 2). Once V_{ge} exceeds V_{th}, the phase 2 starts. In this phase, the metal-oxide semiconductor (MOS) channel begins to form, the electrons are allowed to inject into the N-base. The carrier levels start to build up, but the undepleted N-base is still under low-level injection condition. At this period, the output current I_L begins to transfer from the freewheel diode to the IGBT, and the IGBT collector current I_c starts to increase accordingly. Meanwhile, due to the increasing of collector current I_c, a voltage drop appears across the stray inductance L_s. This results in the decreasing of collector–emitter voltage V_{ce}. The current increases in a constant rate set by [23]

$$\frac{dI_c}{dt} = \frac{V_{dc} - V_{ce}}{L_s} \tag{1}$$

where V_{dc} is the source supply voltage. At this period, since the freewheel diode is still in forward conduction, the voltage across the diode remains at its forward conduction level.

Phase 3). When IGBT collector current I_c reaches to the output current I_L, the phase 3 starts. At this time, the freewheel diode current I_a reaches to zero, the diode then starts to reverse recover. After that, the diode current I_a decreases from zero to the peak reverse current I_{RR}. Meanwhile, the collector current I_c increases toward the peak value $I_L + I_{RR}$.

In this phase, the diode needs time to reverse recover and cannot support large reverse voltage immediately. Therefore, the diode voltage decreases slowly toward $-V_{dc}$. Since the undepleted N-base has low conductivity due to the low-level injection condition at this time, the great rising of I_c causes a significant overshoot of voltage drop across the N-base [26]. A voltage bump of V_{ce} is thereby formed, as shown in Fig. 2.

Phase 4). Once I_c reaches to the maximum value of $I_L + I_{RR}$, the phase 4 starts. At this period, the quick rising in diode reverse voltage results in a rapid fall of V_{ce}. Meanwhile, the diode current returns back to zero, the collector current I_c decreases accordingly. Since I_c is very large, the carrier levels in undepleted N-base are quickly built up, which results in a significant reduction of voltage drop across the undepleted N-base. However, during this period, the N-base is still under low-level injection, and the conductivity modulation is not achieved yet.

Phase 5). When the depletion layer adjacent to the MOS channel comes out of depletion, the depletion capacitance C_{dep} greatly increases. The Miller capacitance C_{gc} becomes much larger and starts to be charged. A plateau zone of the gate–emitter voltage V_{ge} is then generated by the well-known Miller effect [26].

In the beginning of the phase, most of the N-base is conductivity modulated except the region closed to the MOS-end. As the region is under high-level injection at the end of this phase, the N-base is fully conductivity modulated and the V_{ce} drops to its steady-state value. In this phase, some voltage and current oscillations may develop due to the stray elements of the test circuit [25].

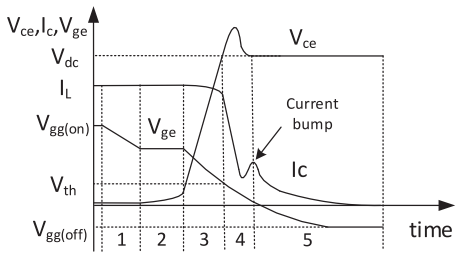

Fig. 3. Waveforms of buffer layer IGBT inductive turn-off process.

Phase 6). In phase 6, the depletion capacitance C_{dep} becomes very large. The Miller capacitance C_{gc} can be considered equal to C_{ox}. Therefore, the gate drive current charges the capacitance C_{ox} and C_{ge}, and V_{ge} rises to the gate drive voltage $V_{gg(on)}$. In this phase, the V_{ce} and I_c approximately remain constant at their steady-state values.

C. Inductive Turn-Off Behavior

Unlike the inductive turn-on behavior, the inductive turn-off behavior of buffer layer IGBT is determined by its internal characteristics. The inductive turn-off waveforms of buffer layer IGBT are shown in Fig. 3. The turn-off process can be divided into five phases, which are as follows.

Phase 1). In this phase, the V_{ge} starts to decrease, discharging the capacitances C_{ox} and C_{ge}. Meanwhile, the V_{ce} and I_c remain at their steady-state values.

Phase 2). When the V_{ge} reduces to a value that is just sufficient to support the collector current I_c, the phase 2 starts. During this phase, the depletion layer starts to undertake a slightly extension, which results in a slow rising of V_{ce}. The depletion capacitance C_{dep} is charging and the charging current serves as a feedback current flowing through C_{gc}. Due to the feedback action, the V_{ge} stays nearly constant at this stage [25]. On the other hand, since the freewheel diode is still reverse biased, the output current I_L cannot transfer into the diode and I_c still remains unchanged during this period.

Phase 3). As the collector–emitter voltage V_{ce} increases few volts, the phase 3 starts. Since the excess charge under the accumulation layer has been removed, the depletion capacitance C_{dep} greatly decreases, which significantly reduces the feedback current. The V_{ge} then decreases toward the gate off voltage $V_{gg(off)}$ while the V_{ce} increases rapidly toward V_{dc}.

During this period, the depletion capacitances C_{ce} is charged. The charging current greatly compensates the collector current reduction due to the shrinking of the MOS electron current. The collector current I_c then undertakes a slow decreasing.

Phase 4). Once V_{ce} reaches V_{dc}, the phase 4 starts. At this time, the freewheel diode begins to forward recover, the output current then starts to transfer into the diode. Since V_{ge} is under the threshold voltage V_{th}, the MOS electron current and the hole drift current associated with it are removed. This results

in an initial rapid fall of collector current I_c. Since the N-base depletion width greatly increases, a large amount of excess holes are swept into the buffer layer. The excess carriers in the buffer layer and undepleted N-base then have to spend a short period of time to redistribute [12], a current bump of I_c may form accordingly at the end of this phase, as shown in Fig. 3.

Phase 5). When the $V_{\rm ce}$ falls back to $V_{\rm dc}$, the phase 5 starts. In this period, the $V_{\rm ce}$ approximately remains constant, while the collector current I_c undertakes a slow decaying mainly due to the remaining excess carrier recombination in the undepleted N-base and buffer layer. However, thanks to the low lifetime in the buffer layer due to its relatively high doping level, the decay of collector current is much faster than the conventional NPT IGBT.

D. Influences of the Device Physical Characteristics

From the previous section, the physical characteristics of the buffer layer IGBT that critically influence the inductive switching behavior can be summarized. For the turn-on process, the physical characteristics are as follows.

1). The excess carrier dynamics in the low-level injected N-base: At turn-on transient, the N-base is always under the low-level injection condition except for the end of the phase 5. Therefore, in order to model the turn-on process, it is essential to characterize the N-base carrier dynamics under low-level injection condition. The low-level injection condition should be included in the solution of ADE.
2). The low conductivity of N-base: During turn-on process, the N-base is not fully conductive modulated until the end of phase 5. The low conductivity due to the low-level injection condition should be considered in the calculation of N-base voltage drop.
3). Freewheel diode reverse recovery: Since the IGBT collector current strongly depends on the diode reverse recovery current, the characterization of reverse recovery behavior of freewheel diode is very important. In the high-speed IGBT module, the fast p-i-n diode is often utilized as the freewheel diode. Some new design concepts like local lifetime control [28], emitter control [29], and deep FS [29] are adopted to perform a fast and soft reverse recovery. In order to accurately model the reverse recovery behavior of the fast p-i-n diode, a physics-based model is developed. The details of the model are presented in [30].

For the turn-off process, the device physical characteristics are as follows.

1) The excess carrier dynamics in the high-level injected buffer layer: During the first three phases of the turn-off transient, the excess carrier concentration in buffer layer approaches or exceeds the doping concentration. During phases 4 and 5, the buffer layer excess carrier density is further increased since all the excess holes in N-base are swept into the buffer layer. Therefore, the buffer layer is under high-level injection at all time during the turn-off transient. The high-level injection condition should be included to describe the excess carrier dynamics in the buffer layer. Moreover, since the buffer layer doping concentration is still comparable to the excess carrier concentration during the turn-off transient, the relatively high buffer layer doping concentration should also be considered in the modeling method.
2). Free holes in the depletion layer: During phases 3 and 4 of the turn-off transient, the MOS electron current shrinks and most of the collector current is carried by holes. Due to the collector current flowing through the device, a large amount of free holes are presented in the depletion layer. When the device conducts high current, the concentration of the free holes will be very closed to the N-base doping concentration [31]. This must be taken into account in the model.

Including all the physical characteristics presented above, a physics-based IGBT model is built. All the details of the model will be presented in the next section.

III. IGBT Model

A. N-Base Modeling

In the N-base region, the dynamics of the excess carrier distribution is governed by ADE

$$D\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau_{\rm SRH}} + \frac{p(x,t)}{t} \tag{2}$$

where D is the ambipolar diffusion coefficient. $\tau_{\rm SRH}$ is the excess carrier lifetime in the N-base. $p(x,t)$ is the N-base excess carrier concentration. Assuming M coefficients are required, the Fourier series solution of $p(x,t)$ can be written as

$$p(x,t) = p_0(t) + \sum_{k=1}^{M-1} p_k(t)\cos\left[\frac{k\pi(x-x_1)}{x_2-x_1}\right] \tag{3}$$

where

$$p_0(t) = \frac{1}{(x_2-x_1)}\int_{x_1}^{x_2} p(x,t)dx \tag{4}$$

$$p_k(t) = \frac{2}{(x_2-x_1)}\int_{x_1}^{x_2} p(x,t)\cos\left[\frac{k\pi(x-x_1)}{x_2-x_1}\right]dx \tag{5}$$

x_1 at $x=0$ and x_2 at $x=W_L$ are the left and right boundaries of the N-base, as shown in Fig. 4. The undepleted N-base region width W_L is given by

$$W_L = W_B - W_d \tag{6}$$

where W_B is the N-base width. W_d is the depletion region width.

In order to describe both the high-level and low-level injection condition in N-base, the carrier lifetime $\tau_{\rm SRH}$ is written on the basis of Shockley–Read–Hall model [26]

$$\tau_{\rm SRH} = \frac{p\tau_H + N_B\tau_L}{p+N_B} \tag{7}$$

where τ_H and τ_L are high-level and low-level carrier lifetimes in N-base, respectively. N_B is the N-base doping concentration.

The ambipolar diffusion coefficient D is

$$D = D_n\frac{2p+N_B}{(1+b)p+bN_B} \tag{8}$$

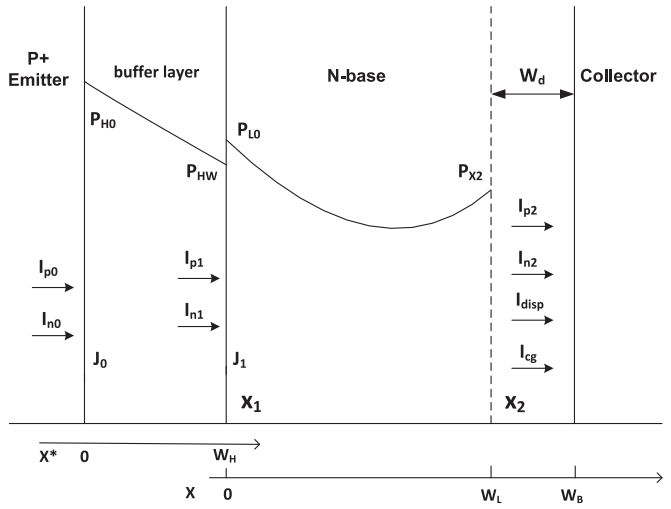

Fig. 4. Coordinate diagram of buffer layer IGBT with boundary condition definition.

where $b = \mu_n/\mu_p = D_n/D_p$ is the mobility ratio. μ_n and μ_p are the electron and hole mobility, D_p and D_n are the hole and electron diffusion coefficients, respectively.

In order to get the solution of ADE with varied injection conditions, the lifetime τ_{SRH} and ambipolar diffusion coefficient D are expressed as

$$\frac{1}{\tau_{\text{SRH}}(x,t)} = R(x,t) = \sum_{n=0}^{M-1} R_n(t)\cos\left[\frac{n\pi(x-x_1)}{x_2-x_1}\right] \quad (9)$$

$$D(x,t) = \sum_{n=0}^{M-1} D_n(t)\cos\left[\frac{n\pi(x-x_1)}{x_2-x_1}\right] \quad (10)$$

where $R_n(t)$ and $D_n(t)$ are the Fourier coefficients which only vary in time.

Including (9) and (10) in the ADE (2), integrate the two side of the ADE, substitute (4) into the equation, then the solution of ADE for $k = 0$ case is given by

For $k = 0$

$$\sum_{n=0}^{M-1} D_n\left[(-1)^n\frac{\partial p}{\partial x}\bigg|_{x2} - \frac{\partial p}{\partial x}\bigg|_{x1}\right] = (x_2-x_1)\frac{dp_0}{dt}$$
$$+\frac{x_2-x_1}{2}\left\{2R_0p_0 + \sum_{n=1}^{M-1} p_n\left[R_n + D_n\left(\frac{n\pi}{x_2-x_1}\right)^2\right]\right\}$$
$$-\sum_{n=1}^{M-1} p_n\left[(-1)^n\frac{dx_2}{dt}\right]. \quad (11)$$

For $k > 0$ case, including (9) and (10) in the ADE (2), integrate the two sides of the ADE multiplied by the $\cos[\frac{k\pi(x-x_1)}{x_2-x_1}]$. Substitute (4) and (5) into the equation, then the solution of ADE is given by

For $0 < k < M-1$

$$\sum_{n=0}^{M-1} D_n\left[(-1)^{n+k}\frac{\partial p}{\partial x}\bigg|_{x2} - \frac{\partial p}{\partial x}\bigg|_{x1}\right] = \frac{x_2-x_1}{2}\frac{dp_k}{dt}$$
$$+\frac{x_2-x_1}{2}\left\{\sum_{n=0}^{M-1} p_{I(n+k)}\left[\frac{D_n}{2}\left(\frac{\pi I(n+k)}{x_2-x_1}\right)^2 + \frac{R_n}{2}\right]\right\}$$
$$+\frac{x_2-x_1}{2}$$
$$\times\left\{\sum_{\substack{n=0\\n\neq k}}^{M-1} p_{I(n-k)}\left[\frac{D_n}{2}\left(\frac{\pi I(n-k)}{x_2-x_1}\right)^2 + \frac{R_n}{2}\right] + R_kp_0\right\}$$
$$-\frac{dx_2}{dt}\left[\frac{p_k}{4} + \sum_{\substack{n=1\\n\neq k}}^{M-1}(-1)^{n+k}p_n\frac{n^2}{n^2-k^2}\right]. \quad (12)$$

For $k = M-1$:

$$\sum_{n=0}^{M-1} D_n\left[(-1)^{n+k}\frac{\partial p}{\partial x}\bigg|_{x2} - \frac{\partial p}{\partial x}\bigg|_{x1}\right] = \frac{x_2-x_1}{2}\frac{dp_k}{dt}$$
$$+\frac{x_2-x_1}{2}$$
$$\times\left\{\sum_{n=0}^{M-2} p_{I(n+k)}\left[\frac{D_n}{2}\left(\frac{\pi I(n+k)}{x_2-x_1}\right)^2 + \frac{R_n}{2}\right] + R_kp_0\right\}$$
$$+\frac{x_2-x_1}{2}$$
$$\times\left\{\sum_{n=0}^{M-2} p_{I(n-k)}\left[\frac{D_n}{2}\left(\frac{\pi I(n-k)}{x_2-x_1}\right)^2 + \frac{R_n}{2}\right] + R_kp_0\right\}$$
$$-\frac{dx_2}{dt}\left[\frac{p_k}{4} + \sum_{\substack{n=1\\n\neq k}}^{M-1}(-1)^{n+k}p_n\frac{n^2}{n^2-k^2}\right] \quad (13)$$

with $x \in [-(M-1), 2M-2]$, $I(x)$ is defined as

$$I(x) = \begin{cases} 2(M-1)-x & x > M-1 \\ x & 0 \le x \le M-1 \\ -x & x < 0. \end{cases} \quad (14)$$

In (9) and (10), the cosine Fourier series are used. Since the coefficients of the cosine Fourier series are even, any value of the indices $n-k$ or $n+k$ that less than zero or greater than $M-1$ should be obtained by reflecting the coefficients about the end indices 0 and $M-1$, as shown in (14).

The coefficients $R_n(t)$ and $D_n(t)$ in (11), (12), and (13) are obtained by calculating the inverse transform of (9) and (10)

$$\begin{bmatrix} R_0(t) \\ R_1(t) \\ R_2(t) \\ \vdots \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & \cdots \\ 1 & \cos\left(\frac{\pi}{M-1}\right) & \cos\left(\frac{2\pi}{M-1}\right) & \cdots \\ 1 & \cos\left(\frac{2\pi}{M-1}\right) & \cos\left(\frac{4\pi}{M-1}\right) & \cdots \\ \vdots & \vdots & \vdots & \ddots \end{bmatrix}^{-1}$$

$$\times \begin{bmatrix} R(x_1,t) \\ R(x_1+\Delta x,t) \\ R(x_1+2\Delta x,t) \\ \vdots \end{bmatrix} \tag{15}$$

$$\begin{bmatrix} D_0(t) \\ D_1(t) \\ D_2(t) \\ \vdots \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & \cdots \\ 1 & \cos(\frac{\pi}{M-1}) & \cos(\frac{2\pi}{M-1}) & \cdots \\ 1 & \cos(\frac{2\pi}{M-1}) & \cos(\frac{4\pi}{M-1}) & \cdots \\ \vdots & \vdots & \vdots & \ddots \end{bmatrix}^{-1} \times \begin{bmatrix} D(x_1,t) \\ D(x_1+\Delta x,t) \\ D(x_1+2\Delta x,t) \\ \vdots \end{bmatrix}. \tag{16}$$

The boundary conditions needed to solve the ADE are the gradients of the carrier concentration at x_1 and x_2, which are given by

$$\left.\frac{\partial p}{\partial x}\right|_{x_1} = \frac{1}{2qA}\left(\frac{I_{n1}}{D_n} - \frac{I_{p1}}{D_p}\right) \tag{17}$$

$$\left.\frac{\partial p}{\partial x}\right|_{x_2} = \frac{1}{2qA}\left(\frac{I_{n2}}{D_n} - \frac{I_{p2}}{D_p}\right) \tag{18}$$

where A is the device active area. I_{n1} and I_{p1} are electron and hole currents at x_1. I_{n2} and I_{p2} are electron and hole currents at x_2.

The current continuity requires

$$I_c = I_{p1} + I_{n1} = I_{p2} + I_{n2} + I_{\rm disp} + I_{\rm cg}. \tag{19}$$

In this paper, to achieve the best tradeoff between the simulation speed and accuracy, $M = 7$. Combining (17), (18), and (19), the solutions on the left-hand side of (11), (12), and (13) are obtained. For even and odd numbers of k, the solutions are given by

$$L_{\rm even} = \begin{bmatrix} I_0 & I_1 & I_0 & I_1 & I_0 & I_1 & I_0 \end{bmatrix} \times \begin{bmatrix} D_0 \\ D_1 \\ \vdots \end{bmatrix} \tag{20}$$

$$L_{\rm odd} = \begin{bmatrix} I_1 & I_0 & I_1 & I_0 & I_1 & I_0 & I_1 \end{bmatrix} \times \begin{bmatrix} D_0 \\ D_1 \\ \vdots \end{bmatrix} \tag{21}$$

with

$$I_0 = \frac{1}{2qAD}\begin{bmatrix} -2 & 2 & 0 & \frac{D}{D_p} & \frac{D}{D_p} \end{bmatrix} \times \begin{bmatrix} I_{n1} \\ I_{n2} \\ I_c \\ I_{\rm disp} \\ I_{\rm cg} \end{bmatrix} \tag{22}$$

$$I_1 = \frac{1}{2qAD}\begin{bmatrix} -2 & -2 & \frac{2D}{D_p} & -\frac{D}{D_p} & -\frac{D}{D_p} \end{bmatrix} \times \begin{bmatrix} I_{n1} \\ I_{n2} \\ I_c \\ I_{\rm disp} \\ I_{\rm cg} \end{bmatrix}. \tag{23}$$

Assuming quasi-neutrality ($n = p + N_B$) valid in the N-base, the expression of electric field can be written as [32]

$$E(x) = \frac{J_D/q - (D_n - D_p)(dp/dx)}{(\mu_p + \mu_n)p + \mu_n N_B}. \tag{24}$$

Then, the voltage drop across the undepleted N-base is obtained by

$$V_b = \int_{x_1}^{x_2} E(x) = \frac{I_c}{qA(\mu_p+\mu_n)}\frac{x_2 - x_1}{M-1} \times \sum_{k=0}^{M-1}\left[\frac{1}{p_{T_k} - p_{T_{k-1}}}\ln\left(\frac{p_{T_k}}{p_{T_{k-1}}}\right)\right] + V_T\left(\frac{b-1}{b+1}\right)\ln\left(\frac{p_{T_0}}{p_{T_{M-1}}}\right) \tag{25}$$

where the carrier concentration p_{T_k} is

$$p_{T_k} = p\left(x_1 + \frac{k(x_2 - x_1)}{M-1}, t\right) + \frac{N_B}{1+b}. \tag{26}$$

The N-base voltage V_b is comprised of two components, the first term on the right of (25) is resistive voltage drop component due to the resistivity of the lightly doped N-base, whereas the second term corresponds to the Dember voltage drop associates with the asymmetrical carrier gradient produced by the difference in the mobility of electrons and holes. Since the N-base is under low-level injection condition during turn-on transient, the N-base doping concentration is considered, as shown in (26).

B. Buffer Layer Modeling

In buffer layer, the time-dependent ADE is given by

$$\frac{\partial^2 \delta p}{\partial x^2} = \frac{\delta p}{L_H^2} + \frac{1}{D_a}\frac{\partial \delta p}{\partial t} \tag{27}$$

where $L_H = \sqrt{D_a \tau_{\rm BF}}$ is the ambipolar diffusion length. $D_a = \frac{2D_n D_p}{D_n + D_p}$ is the ambipolar diffusion coefficient. $\tau_{\rm BF}$ is the excess carrier lifetime in the buffer layer.

Solving ADE (27) with the boundary conditions of $p(0,t) = P_{H0}$ and $p(W_H,t) = P_{\rm HW}$, the excess carrier concentration in steady state is [5]

$$\delta p(x^*) = \frac{P_{H0}\sinh\left(\frac{W_H - x^*}{L_H}\right) - P_{\rm HW}\sinh\left(\frac{x^*}{L_H}\right)}{\sinh\left(\frac{W_H}{L_H}\right)} \tag{28}$$

where P_{H0}, $P_{\rm HW}$ are excess hole concentrations at $x^* = 0$ and $x^* = W_H$, respectively, as shown in Fig. 4. W_H is the buffer layer width.

In high-speed IGBT, the buffer layer is optimized to be very light and thin [24], $L_H > W_H$ can thereby be assumed. Notice

$\sinh(x) \approx x$ when $x < 1$, (28) is thereby modified as

$$\delta p(x^*) = P_{H0} - \frac{P_{H0} - P_{\rm HW}}{W_H} x^*. \tag{29}$$

Equation (29) can only describe the steady-state excess carrier distribution. In transient condition, the equation is not accurate enough, since the excess carrier recombination and redistribution are not taken into account. Substitute (29) into ADE, (27) and (30) can be obtained

$$\frac{\partial^2 \delta p}{\partial x^2} = \frac{\delta p}{L_H^2} + \frac{1}{D}\left[\frac{(W_H - x^*)}{W_H}\frac{dP_{H0}}{dt} + \frac{x^*}{W_H}\frac{dP_{\rm HW}}{dt}\right]. \tag{30}$$

Integrating (30) twice with the boundary conditions of $p(0,t) = P_{H0}$ and $p(W_H, t) = P_{\rm HW}$, the excess hole distribution at transient state in buffer layer is obtained as follows:

$$\begin{aligned}\delta p(x^*,t) \;=\; & \left[P_{H0} - \frac{P_{H0} - P_{\rm HW}}{W_H}x^*\right] + \frac{1}{L_H^2}\left[\frac{P_{H0}}{2}x^{*2}\right. \\ & \left. - \frac{(P_{H0} - P_{\rm HW})}{W_H}\frac{x^{*3}}{6} - \frac{(2P_{H0}W_H + P_{\rm HW}W_H)}{6}x^*\right] \\ & + \frac{1}{D}\left[\frac{dP_{H0}}{dt}\frac{x^{*2}}{2} - \left(\frac{dP_{H0}}{dt} - \frac{dP_{\rm HW}}{dt}\right)\frac{x^{*3}}{6W_H}\right. \\ & \left. - \left(\frac{dP_{H0}}{dt}\frac{W_H}{3} + \frac{dP_{\rm HW}}{dt}\frac{W_H}{6}\right)x^*\right]\end{aligned} \tag{31}$$

where the first term is the linear charge control component, the second term corresponds to the carrier recombination and the third term denotes the carrier redistribution. In the PT IGBT model proposed in [6] and [20], the second term is always neglected without the buffer layer carrier recombination taken into account.

In general, the electron and hole current are given by

$$I_n = q\mu_n AnE + qAD_n\frac{dn}{dx} \tag{32}$$

$$I_p = q\mu_p ApE - qAD_p\frac{dp}{dx}. \tag{33}$$

Assuming quasi-neutrality ($n = p + N_H$) valid in the buffer layer, combine (32) and (33), the hole current transmission equation in the buffer layer is obtained to be

$$I_p = \frac{pI_c}{p(1+b) + bN_H} - qAD_p\frac{(2p + N_H)b}{p(1+b) + bN_H}\frac{dp}{dx} \tag{34}$$

where N_H is the buffer layer doping concentration. Since N_H is comparable to the buffer layer excess carrier concentration, it is included in (34).

Substituting (31) into (34) with $x^* = 0$ and $x^* = W_H$, the hole currents I_{p0} at $x^* = 0$ and I_{p1} at $x^* = W_H$ are obtained, as shown in

$$\begin{aligned}I_{p0} = \; & qAD_p\frac{(2P_{H0} + N_H)b}{P_{H0}(1+b) + bN_H}\left[\frac{P_{H0} - P_{\rm HW}}{W_H}\right. \\ & + \frac{W_H}{6D\tau_H}(2P_{H0} + P_{\rm HW}) \\ & \left. + \frac{W_H}{D}\left(\frac{1}{3}\frac{dP_{H0}}{dt} + \frac{1}{6}\frac{dP_{\rm HW}}{dt}\right)\right] \\ & + \frac{I_c P_{H0}}{P_{H0}(1+b) + bN_H}\end{aligned} \tag{35}$$

$$\begin{aligned}I_{p1} = \; & qAD_p\frac{(2P_{\rm HW} + N_H)b}{P_{\rm HW}(1+b) + bN_H}\left[\frac{P_{H0} - P_{\rm HW}}{W_H}\right. \\ & - \frac{W_H}{6D\tau_H}(P_{H0} + 2P_{\rm HW}) \\ & \left. - \frac{W_H}{D}\left(\frac{1}{6}\frac{dP_{H0}}{dt} + \frac{1}{3}\frac{dP_{\rm HW}}{dt}\right)\right] \\ & + \frac{I_c P_{\rm HW}}{P_{\rm HW}(1+b) + bN_H}.\end{aligned} \tag{36}$$

The terms contain $dP_{\rm HW}/dt$ and dP_{H0}/dt in (35) and (36) are the capacitive current due to the carrier redistribution in the buffer layer. In the PT IGBT model in [6] and [20], the capacitive current is assumed to only contribute the hole current I_{p1}. In (35) and (36), based on the carrier redistribution component represented in (31), the capacitive currents in I_{p0} and I_{p1} are redescribed.

Using the quasi-equilibrium simplification at the J_1 junction

$$P_{\rm HW}(P_{\rm HW} + N_H) = P_{L0}(P_{L0} + N_B). \tag{37}$$

Since $P_{\rm HW}$ can approaches or exceeds N_H in buffer layer, $P_{\rm HW}$ is included in (37) instead of neglected as usually done in [6] and [20].

The electron current I_{n0} at the J_0 junction is [13]

$$I_{\rm no} = qAh_p N_H P_{H0} \tag{38}$$

where h_p is hole recombination coefficient in emitter.

The voltage across J_0 junction is [26]

$$V_{j0} = V_T \ln\left(\frac{P_{H0}N_H}{n_i^2}\right) \tag{39}$$

and the voltage across J_1 junction is [26]

$$V_{j1} = V_T \ln\left(1 + \frac{P_{L0}}{N_B}\right). \tag{40}$$

C. MOS-Side Modeling

The MOS structure supplies the MOS-side electron current I_{n2}, therefore

$$I_{n2} = I_{\rm MOS}. \tag{41}$$

$I_{\rm MOS}$ is the MOS current, which can be obtained by Shockley equations [6].

In the linear region ($V_{\rm ge} \geq V_{\rm th}, V_{\rm ge} - V_{\rm th} \geq V_d$), $I_{\rm MOS}$ is given by

$$I_{\rm MOS} = K_p\left[V_d(V_{\rm ge} - V_{\rm th}) - \frac{V_d^2}{2}\right]. \tag{42}$$

In the saturated region ($V_{\rm ge} \geq V_{\rm th}, V_{\rm ge} - V_{\rm th} < V_d$), the MOS current is

$$I_{\rm MOS} = \frac{K_p}{2}(V_{\rm ge} - V_{\rm th})^2(1 + \lambda V_d) \tag{43}$$

where K_p is the MOS transconductance. V_{th} is the MOS threshold voltage. V_{ge} is the gate–emitter voltage. λ is the MOS short-channel coefficient. V_d is the MOS voltage.

The MOS-side displacement current I_{disp} corresponds to the depletion capacitance C_{ce}, as shown in Fig. 1. I_{disp} is given by

$$I_{\text{disp}} = \frac{\epsilon_{\text{si}} A(1-a_i)}{W_d} \frac{dV_d}{dt} \tag{44}$$

where a_i is intercell area ratio. V_d is the MOS voltage. W_d is the depletion region width. With the cell width L and intercell width l_m defined in Fig. 1, a_i is expressed as

$$a_i = \frac{(L - l_m)}{L}. \tag{45}$$

W_d is given by [33]

$$W_d = \sqrt{\frac{2\epsilon_{\text{si}} V_d}{q\left(N_B + \frac{|I_{p1}|}{q v_{\text{sat}} A}\right)}} \tag{46}$$

where v_{sat} is the saturated drift velocity. In (46), the free holes at depletion region due to the hole current I_{p1} are included, since the free hole concentration is comparable to N_B during the turn-off transient.

V_d can be calculated by a feedback from the boundary carrier density p_{x2}

$$V_d = \begin{cases} 0, & \text{for } p_{x2} > 0 \\ -K \cdot p_{x2}, & \text{for } p_{x2} < 0 \end{cases} \tag{47}$$

where K is a large gain. p_{x2} is the excess carrier concentration at x_2, as shown in Fig. 4.

The depletion capacitance C_{dep} under the gate is

$$C_{\text{dep}} = \frac{\epsilon_{\text{si}} A a_i}{W_d}. \tag{48}$$

The Miller capacitance C_{gc} is given by the series combination of gate-oxide capacitance C_{ox} and the depletion capacitance C_{dep}

$$C_{\text{gc}} = \frac{C_{\text{ox}} A a_i}{1 + \frac{C_{\text{ox}}}{\epsilon_{\text{si}}} W_d}. \tag{49}$$

The collector–gate displacement current due to the variation of Miller capacitance is [33]

$$I_{\text{cg}} = C_{gac}\left(\frac{dV_d}{dt} - \frac{dV_{\text{ge}}}{dt}\right) \tag{50}$$

with

$$\frac{dV_{\text{ge}}}{dt} = \frac{1}{C_{\text{gc}} + C_{\text{ge}}}\left(I_g + C_{\text{gc}} \frac{dV_d}{dt}\right) \tag{51}$$

where I_g is the gate current.

IV. Model Realization in Simulink

The proposed model is implemented using MATLAB and Simulink, as shown in Fig. 5. It has two inputs, collector current I_c and gate current I_g, and two outputs, collector–emitter voltage V_{ce} and gate–emitter voltage V_{ge}. The model contains

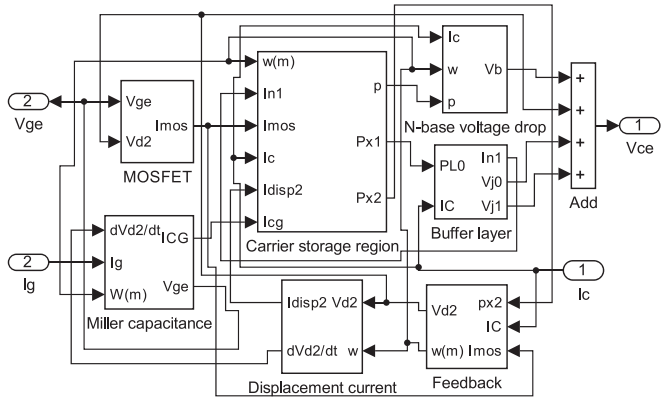

Fig. 5. Block diagram of buffer layer IGBT model in Simulink.

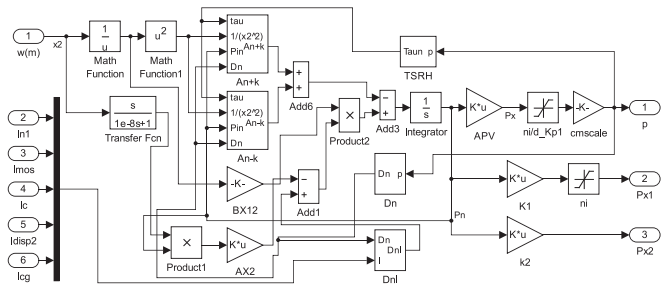

Fig. 6. Carrier storage region subsystem of the model.

the following subsystems: MOSFET, buffer layer, carrier storage region, feedback, N-base voltage drop, Miller capacitance, displacement current, and a sum of the total voltage drop V_{ce}.

The MOSFET subsystem uses (42) and (43) to calculate the MOS current I_{MOS}. The buffer layer subsystem uses (35), (36), (37), (38), and (19) to calculate I_{n1}. The subsystem also utilizes (39) and (40) to calculate V_{j0} and V_{j1}, respectively. The feedback subsystem uses (47) to calculate V_d, and uses (46) to calculate W_d. In displacement current subsystem, (44) is utilized to obtain I_{disp}. The Miller capacitance subsystem implements (49), (50), and (51) to calculate I_{cg} and V_{ge}. The N-base voltage drop subsystem uses (25) and (26) to calculate V_b. Finally, the total voltage V_{ce} is obtained by summing all the voltage component

$$V_{\text{ce}} = V_{j0} + V_{j1} + V_b + V_d. \tag{52}$$

The carrier storage region subsystem is the most important and complicated subsystem in the model. The subsystem uses (11), (12), (13), (14) to provide the solution of the ADE (2) under all injection levels, as shown in Fig. 6. In the subsystem, to avoid the poor convergence results from the direct calculation of the dx_2/dt, the transfer function G(s) given by

$$G(s) = \frac{1}{10^{-8}s + 1} \tag{53}$$

is used to calculate dx_2/dt. The calculated dx_2/dt is multiplied by Fourier coefficient p_k and matrix Ax2 to obtain the last terms on the right side of (11), (12), and (13). The matrixes Apv, K1, and K2 obtained from (3) are also multiplied by Fourier

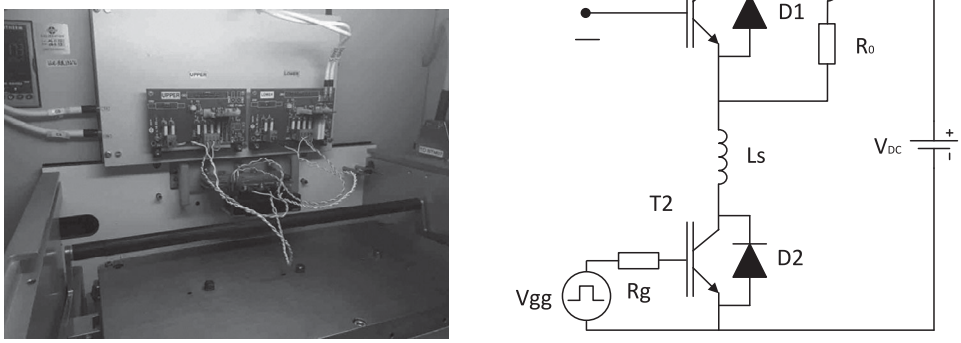

Fig. 7. Experiment platform circuit and equivalent circuit for the double-pulse test (a) Experiment platform (b) Equivalent circuit.

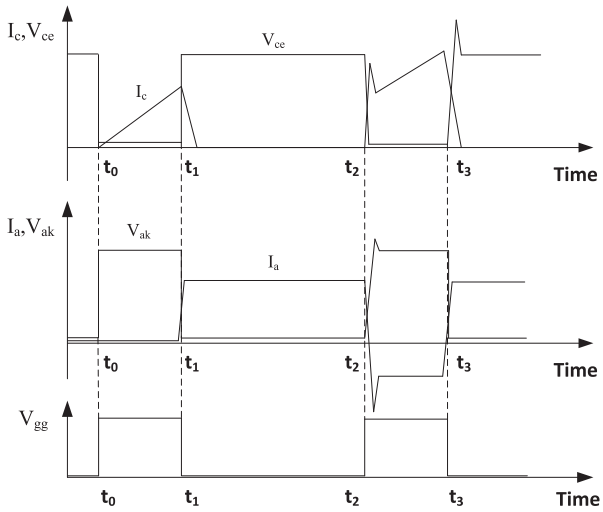

Fig. 8. Transistor and diode current and voltage characteristics during the double-pulse test.

coefficient p_k to calculate the carrier density profile in the N-base and the boundary carrier densities P_{x1} and P_{x2}, respectively.

Three subsystems are also included in the carrier storage region subsystem. The subsystem Dn uses (8) and (16) to calculate the Fourier series coefficient D_n. The subsystem TSRH uses (7) and (15) to calculate the Fourier series coefficients R_n. The DnI subsystem implements (20), (21), (22), and (23) to calculate the terms on the left side of (11), (12), and (13). The An+k subsystem obtains the second terms on the right side of (11), (12), and (13), while An-k subsystem obtains the third terms on the right side of (12) and (13).

V. Model Validation

With an Infineon 600V/200A FS IGBT module and Mitsubishi 600V/150A CSTBT module utilized, the double-pulse tests are performed to obtain the inductive switching characteristics. The experimental waveforms are directly compared with the simulation results for validation. All the experiment results are measured at 300 K.

TABLE I
Parameter Estimation and Optimization

Parameters	Initial Extraction method; **Waveforms fitting (bold)**
A	Open the package and measure. **Turn-off voltage and current**
$V_{\rm th}$, K_p, λ	From the *I–V* characteristic curve [34]. **Gate waveforms**
a_i, $C_{\rm ge}$, $C_{\rm ox}$	From the input capacitance $C_{\rm ies}$ and reverse transfer capacitance $C_{\rm res}$ given in datasheet [34]. **Gate waveforms, Miller plateau**
h_p, h_n	The empirical range of h_n and h_p is $10^{14}-10^{11}\,{\rm cm}^{-3}$ [34]. h_n **: Turn-off dV/dt,** h_p **: tail current**
W_B, N_B	From breakdown voltage [34]. **Turn-off dV/dt**
N_H, W_H	W_H is about $4-10\mu$ s, N_H is about $10^{15}-10^{16}$ cm^{-3} for high speed buffer layer IGBT [1], [27]. **Tail current**
τ_H, $\tau_{\rm BF}$	From decay rate of tail current [35]. **Tail current**
τ_L	$\tau_L = \tau_H$ in the initial estimation. **Turn-on voltage bunp**
L_s	From dI_c/dt during turn-off transient[34]. **Turn-off voltage overshoot**

A. Test Step

The experiment platform and the equivalent test circuit of the double-pulse test are shown in Figs. 7 a and 7 b, respectively. In the circuit, a large inductor L_0 is used to maintain a nearly constant current throughout the switching cycle. L_0 has an equivalent series resistance R_0. R_g is the gate resistance. L_s is the stray inductance of the test circuit.

In the double-pulse test, the transistor T2 is turned ON and OFF twice, as shown in Fig. 8. The second turn-on at t_2 is used to measure the turn-on characteristics, while the second turn-off at t_3 is used to measure the turn-off characteristics.

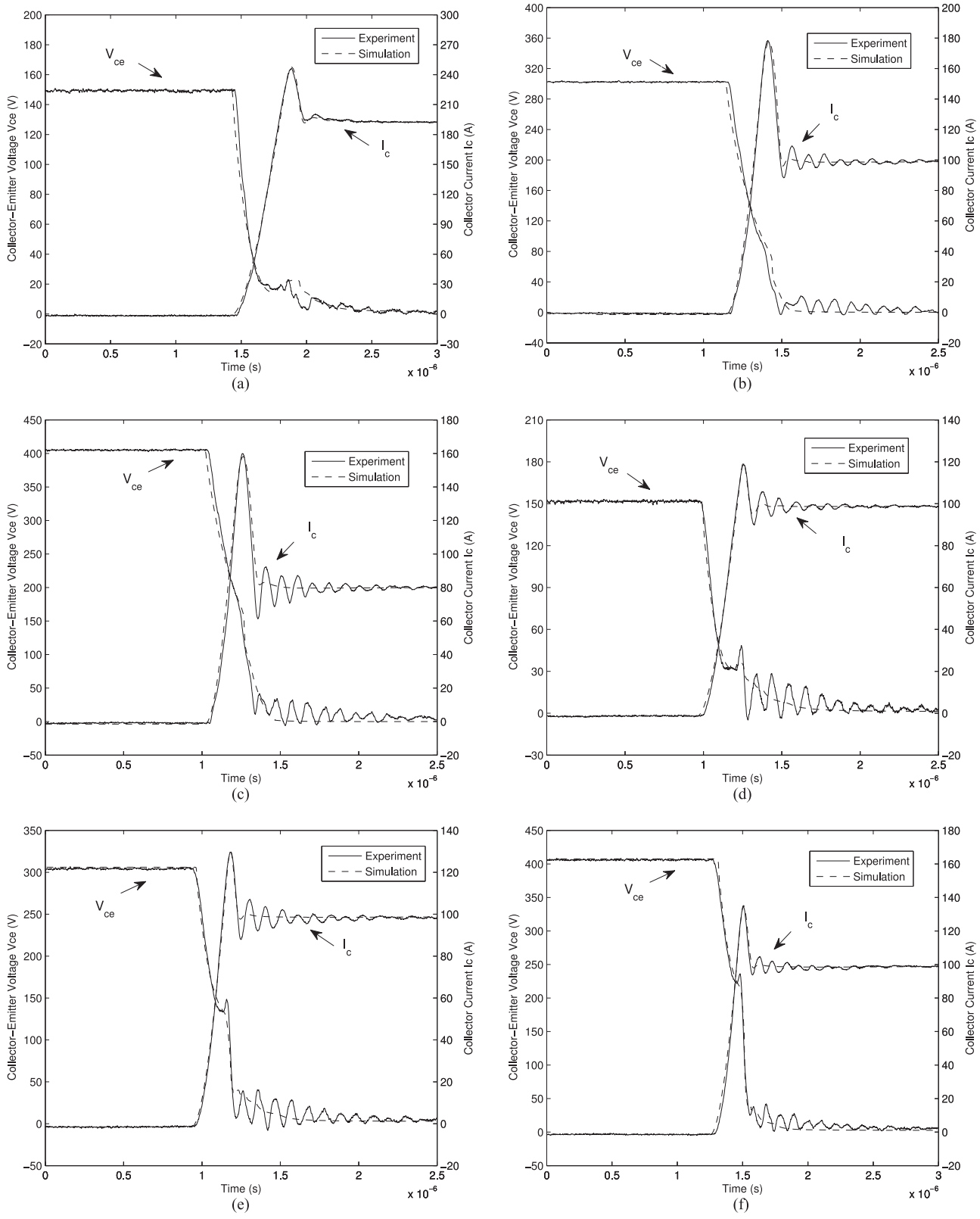

Fig. 9. Comparison between experiment and simulation turn-on waveforms of FS IGBT and CSTBT. (a) FS IGBT using $R_g = 10\,\Omega$ and $L_0 = 500\,\mu H$, at 150 V/200 A. (b) FS IGBT using $R_g = 10\,\Omega$ and $L_0 = 1$ mH, at 300 V/100 A. (c) FS IGBT using $R_g = 10\,\Omega$ and $L_0 = 1$ mH, at 400 V/80 A. (d) CSTBT using $R_g = 10\,\Omega$ and $L_0 = 1$ mH, at 150 V/100 A. (e) CSTBT using $R_g = 10\,\Omega$ and $L_0 = 1$ mH, at 300 V/100 A. (f) CSTBT using $R_g = 10\,\Omega$ and $L_0 = 1$ mH, at 400 V/100 A.

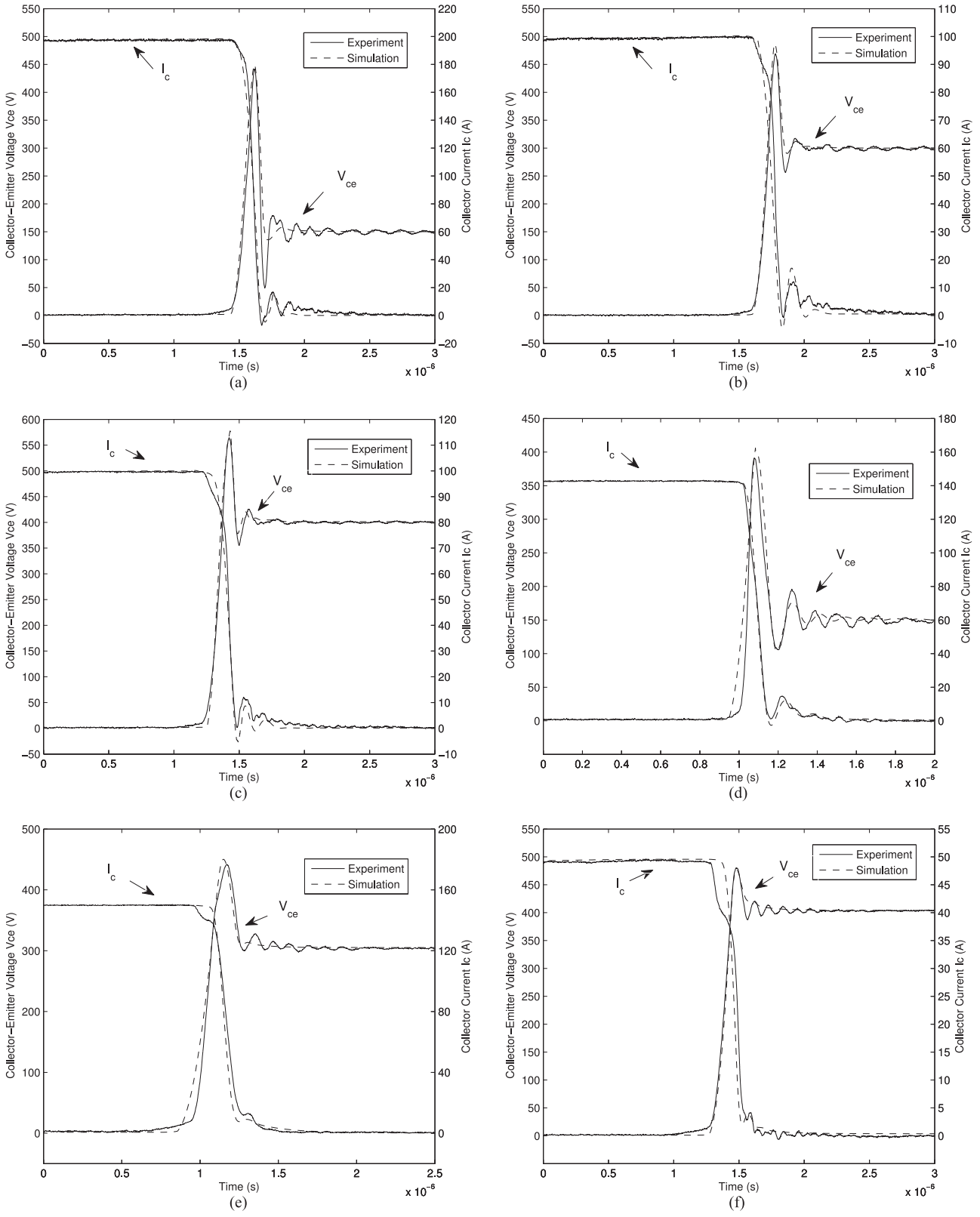

Fig. 10. Comparison between experiment and simulation turn-off waveforms of FS IGBT and CSTBT. (a) FS IGBT using $R_g = 10\,\Omega$ and $L_0 = 500\,\mu$H, at 150 V/200 A. (b) FS IGBT using $R_g = 10\,\Omega$ and $L_0 = 500\,\mu$H, at 300 V/100 A. (c) FS IGBT using $R_g = 10\,\Omega$ and $L_0 = 1$ mH, at 400 V/100 A. (d) CSTBT using $R_g = 10\,\Omega$ and $L_0 = 500\,\mu$H, at 150 V/150 A. (e) CSTBT using $R_g = 20\,\Omega$ and $L_0 = 1$ mH, at 300 V/150 A. (f) CSTBT using $R_g = 20\,\Omega$ and $L_0 = 2$ mH, at 400 V/50 A.

B. Model Parameters

Table I summarizes the initial extraction methods. The die area A is obtained by direct measurement. The parameters a_i $V_{\rm th}$, K_p, λ, h_p, h_n, $C_{\rm ge}$, W_B, N_B, $C_{\rm ox}$, and L_s are extracted based on the method proposed in [34]. The lifetime parameters τ_H and $\tau_{\rm BF}$ are extracted by tail current decay rate following the procedure presented in [35]. Based on the design concept of buffer layer in high-speed IGBT, N_H and W_H are estimated by their empirical value ranges. The low-level lifetime τ_L is initially assumed to have the same value with τ_H. After the initial extraction, a parameter optimization procedure described in [23] and [34] is performed to fit the experimental and simulation waveforms by varying model parameters. The waveforms utilized in the fitting procedure are given in bold in Table I.

C. Inductive Turn-On Characteristics

The turn-on experiments are performed at 150 V/200 A, 300 V/100 A, 400 V/80 A for FS IGBT, and 150 V/100 A, 300 V/100 A, 400 V/100 A for CSTBT. The experimental turn-on waveforms are given in Fig. 9.

D. Inductive Turn-Off Characteristics

The turn-off experiments are performed at 150 V/200 A, 300 V/100 A, 400 V/100 A for FS IGBT, and 150 V/150 A, 300 V/150 A, 400 V/50 A for CSTBT. The experimental turn-off waveforms are given in Fig. 10.

VI. Discussion

The experimental and simulation results in Figs. 9 and 10 show excellent agreement. This demonstrates that both of the inductive turn-on and turn-off processes can be well described by the proposed model.

It should be noticed that significant oscillations appear in the measured waveforms of $V_{\rm ce}$ and I_c. The oscillations may be the *LC* oscillation induced by the interaction between the device junction capacitances and external parasitic inductances [36]. In the proposed model, in order to improve the convergence of the model, the transfer function (53) is used to calculate dx_2/dt. Therefore, some of the high-frequency oscillations cannot be captured in the model.

VII. Conclusion

In this paper, a physics-based model implemented in MATLAB and Simulink has been presented for buffer layer high-speed IGBT. The model utilizes the Fourier-series solution of ADE under all injection levels to characterize the excess carrier transport in the N-base. This enables the model to provide more accurate prediction on the IGBT turn-on behavior. Moreover, the high-level injection assumption in the buffer layer is also adopted. Based on the assumption, the ambipolar transport form of hole current transition equation and quasi-equilibrium simplification are used to characterize the excess carrier transport in the buffer layer. The carrier recombination and redistribution in the buffer layer are taken into account. The capacitive currents due to the carrier redistribution are redescribed. In the end, The accuracy of the model has been experimentally verified by the good agreement of the experiment and simulation results.

References

[1] T. Laska, M. Munzer, F. Pfirsch, C. Schaeffer, and T. Schmidt, "The field stop IGBT (FS IGBT). A new power device concept with a great improvement potential," in *Proc. 12th Int. Symp. Power Semicond. Devices ICs*, 2000, pp. 355–358.

[2] S. Dewar, S. Linder, C. von Arx, A. Mukhitinov, and G. Debled, "Soft punch through (SPT)—Setting new standards in 1200V IGBT," in *Proc. PCIM Eur.*, 2000, pp. 593–600.

[3] H. Takahashi, E. Haruguchi, H. Hagino, and T. Yamada, "Carrier stored trench-gate bipolar transistor (CSTBT) - A novel power device for high voltage application," in *Proc. IEEE 8th Int. Symp. Power Semicond. Devices ICs*, 1996, pp. 349–352.

[4] T. Matsudai and A. Nakagawa, "Ultra high switching speed 600 V thin wafer PT-IGBT based on new turn-off mechanism," in *Proc. 14th IEEE Int. Symp. Power Semicond. Devices ICs*, 2002, pp. 285–288.

[5] A. R. Hefner Jr, "Modeling buffer layer IGBT's for circuit simulation," *IEEE Trans. Power Electron.*, vol. 10, no. 2, pp. 111–123, Mar. 1995.

[6] X. Kang, "Characterization and modeling of trench gate punch through IGBTs," *Ph.D. dissertation*, Dept. Elect. Eng., Univ. of South Carolina, Columbia, SC, USA, 2002.

[7] R. Chibante, A. Araujo, and A. Carvalho, "Modeling buffer layer IGBTs with an efficient parameter extraction method," in *Proc. IEEE 36th Power Electron. Specialists Conf.*, Jun. 2005, pp. 2194–2200.

[8] M. Cotorogea, "Physics-based spice-model for IGBTs with transparent emitter," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2821–2832, Dec. 2009.

[9] P. Igic, "Exponential ADE solution based compact model of planar injection enhanced IGBT dedicated to robust power converter design," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1914–1924, Apr. 2015.

[10] S. Ji, Z. Zhao, T. Lu, L. Yuan, and H. Yu, "HVIGBT physical model analysis during transient," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2616–2624, May 2013.

[11] S. Ryu *et al.*, "A transient model for insulated gate bipolar transistors (IGBTs)," *Int. J. Electron.*, vol. 95, no. 4, pp. 399–409, 2008.

[12] A. R. Hefner and D. L. Blackburn, "An analytical model for the steady-state and transient characteristics of the power insulated-gate bipolar transistor," *Solid-State Electron.*, vol. 31, no. 10, pp. 1513–1532, 1988.

[13] P. R. Palmer *et al.*, "Circuit simulator models for the diode and IGBT with full temperature dependent features," *IEEE Trans. Power Electron.*, vol. 18, no. 5, pp. 1220–1229, Sep. 2003.

[14] A. T. Bryant, P. R. Palmer, E. Santi, and J. L. Hudgins, "Simulation and optimization of diode and insulated gate bipolar transistor interaction in a chopper cell using MATLAB and Simulink," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 874–883, Jul./Aug. 2007.

[15] L. Lu *et al.*, "Modeling of MOS-side carrier injection in trench-gate IGBTs," *IEEE Trans. Ind. Appl.*, vol. 46, no. 2, pp. 875–883, May 2010.

[16] L. Lu, A. Bryant, J. L. Hudgins, P. R. Palmer, and E. Santi, "Physics-based model of planar-gate IGBT including MOS side two-dimensional effects," *IEEE Trans. Ind. Appl.*, vol. 46, no. 6, pp. 2556–2567, Nov./Dec. 2010.

[17] X. Yang, M. Otsuki, and P. R. Palmer, "Physics-based insulated-gate bipolar transistor model with input capacitance correction," *IET Power Electron.*, vol. 8, no. 3, pp. 417–427, 2015.

[18] L. Lu, "Physical modeling of variable-lifetime p-i-n diodes and of two-dimensional effects in insulated gate bipolar transistors (IGBTs)," *Ph.D. dissertation*, Dept. Elect. Eng., Univ. of South Carolina, Columbia, SC, USA, 2006.

[19] X. Kang *et al.*, "Characterization and modeling of the LPT CSTBT—The 5th generation IGBT," in *Proc. 38th IAS Annu. Meeting*, 2003, vol. 2, pp. 982–987.

[20] X. Kang, A. Caiafa, E. Santi, J. L. Hudgins, and P. R. Palmer, "Characterization and modeling of high-voltage field-stop IGBTs," *IEEE Trans. Ind. Appl.*, vol. 39, no. 4, pp. 922–928, Jul./Aug. 2003.

[21] Y. Tang, B. Wang, M. Chen, and B. Liu, "Simulation model and parameter extraction of field-stop (FS) IGBT," *Microelectron. Rel.*, vol. 52, no. 12, pp. 2920–2931, 2012.

[22] X. Kang *et al.*, "Physical modeling of IGBT turn on behavior," in *Proc. 38th IAS Annu. Meeting*, 2003, vol. 2, pp. 988–994.

[23] A. Bryant, L. Lu, E. Santi, J. Hudgins, and P. Palmer, "Modeling of IGBT resistive and inductive turn-on behavior," *IEEE Trans. Ind. Appl.*, vol. 44, no. 3, pp. 904–914, May 2008.
[24] K. Nakamura, D. Oya, S. Saito, H. Okabe, and K. Hatade, "Impact of an LPT(II) concept with thin wafer process technology for IGBT's vertical structure," in *Proc. 21st Int. Symp. Power Semicond. Devices IC's*, 2009, pp. 295–298.
[25] R. S. Chokhawala, J. Catt, and B. R. Pelly, "Gate drive considerations for IGBT modules," *IEEE Trans. Ind. Appl.*, vol. 31, no. 3, pp. 603–611, May/Jun. 1995.
[26] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York, NY, USA: Springer, 2010.
[27] J. G. Bauer *et al.*, "6.5 kV-modules using IGBTs with field stop technology," in *Proc. 13th Int. Symp. Power Semicond. Devices ICs*, 2001, pp. 121–124.
[28] E. Napoli, A. Strollo, and P. Spirito, "Numerical analysis of local lifetime control for high-speed low-loss p-i-n diode design," *IEEE Trans. Power Electron.*, vol. 14, no. 4, pp. 615–621, Jul. 1999.
[29] F. Hille *et al.*, "1200v Emcon4 freewheeling diode—A soft alternative," in *Proc. 19th Int. Symp. Power Semicond. Devices IC's*, 2007, pp. 109–112.
[30] P. Xue, G. Fu, and D. Zhang, "Comprehensive physics-based compact model for fast pin diode using MATLAB and Simulink," *Solid-State Electron.*, vol. 121, pp. 1–11, 2016.
[31] J. Lutz and R. Baburske, "Dynamic avalanche in bipolar power devices," *Microelectron. Reliab.*, vol. 52, no. 3, pp. 475–481, 2012.
[32] S. Bellone, F. Della Corte, L. Albanese, and F. Pezzimenti, "An analytical model of the forward I-V characteristics of 4H-SiC p-i-n diodes valid for a wide range of temperature and current," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2835–2843, Oct. 2011.
[33] T. K. Gachovska, J. L. Hudgins, E. Santi, A. Bryant, and P. R. Palmer, *Modeling Bipolar Power Semiconductor Devices (Synthesis Lectures on Power Electronics)*, vol. 4. San Rafael, CA, USA: Morgan & Claypool Publishers, 2013.
[34] A. T. Bryant, X. Kang, E. Santi, P. R. Palmer, and J. L. Hudgins, "Two-step parameter extraction procedure with formal optimization for physics-based circuit simulator IGBT and p-i-n diode models," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 295–309, Mar. 2006.
[35] G. Fu and P. Xue, "An excess carrier lifetime extraction method for physics-based IGBT models," *J. Power Electron.*, vol. 16, no. 2, pp. 778–785, 2016.
[36] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor Power Devices: Physics, Characteristics, Reliability*. New York, NY, USA: Springer, 2011.

Peng Xue received the M.cs. degree in industrial engineering from the Beihang University, Beijing, China, in 2013, where he is currently working toward the Ph.D. degree in the School of Reliability and Systems Engineering.

His major research interests include the modeling, failure analysis and reliability improvement of the power devices.

Guicui Fu received her M.S. degree in aircraft manufacturing engineering from Northwestern Ploytechnical University, Xian, China in 1993, and the Ph.D. degree in system engineering from Beihang University, Beijing, China, in 2005.

Since 1993, She has been with the Beihang University, Beijing, China, where she is currently a Professor with the school of reliability and system engineering. Her research interests include thermal design and optimization, reliability engineering, and failure analysis on electron devices.

Dong Zhang received the M.S degree in system engineering from Beihang University, Beijing, China, in 2006.

He has been appointed as a Lecturer in Beihang University since 2007. His research interest includes failure analysis on electron devices.