Low-Frequency Power Decoupling in Single-Phase Applications: A Comprehensive Overview

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***Abstract*—This paper presents a literature overview of all techniques proposed until the submission of this paper in terms of mitigating power oscillation in single-phase applications. This pulsating energy is the major factor for increasing the size of passive components and power losses in the converter and can be responsible for losses or malfunctioning of the dc sources. Reduction of power ripple at twice the fundamental frequency is one of the key elements to increase power converter density without lack of dc stiffness. Pulsation reduction is achieved by incorporating control techniques or auxiliary circuitries with energy storage capability in reactive elements to avoid this oscillating power to propagate through the converter, creating what is called as single-phase power decoupling. The topologies are divided as: rectifiers, inverters, and bidirectional. Among them, it is possible to classify as isolated and nonisolated converters. The energy storage method may be classify as: capacitive and inductive. For the power decoupling technique, it is convenient to divide as control and topology. The power decoupling technique may be implemented as series or parallel with respect to the ac, dc or link side. This paper represents the best reference on this topic.**

***Index Terms*—Low-frequency oscillation, power decoupling, single-phase.**

I. Introduction

SINGLE-PHASE converters are mainly used to connect systems that work with relatively low-power range (<10 kW). Such kind of converters have been used specialty to connect renewable energy source to the utility in a distributed power generation context applied to small consumers. Thus, a wide class of single-phase equipment can be achieved by using such converters, i.e., power factor correction (PFC), microinverters, line voltage regulators, universal active power filters (APFs), standby power supplies, uninterruptible power supplies, etc. These converters provide sinusoidal input/output currents with a unitary input power factor, and they are effective to protect the load against line disturbances. Consequently, using stable ac voltage is recommended to feed critical loads such as computers, telecommunication systems, and biomedical instrumentation.

Manuscript received January 14, 2016; revised April 27, 2016; accepted June 6, 2016. Date of publication June 10, 2016; date of current version January 20, 2017. This work was supported in part by the National Council for Scientific and Technological Development, and by the Coordination of Improvement of Higher Education Personnel. Recommended for publication by Associate Editor C. K. Tse.

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Digital Object Identifier 10.1109/TPEL.2016.2579740

The second-order harmonic power oscillation is the most common issue in single-phase applications including both dc–ac or ac–dc. Nowadays, higher power density converter design is very critical in many applications such as more electric aircraft, data center (Google just launched the little box challenge last year), etc. Therefore, it is quite valuable to have a thorough overview which especially focuses on the single-phase converter with active energy storage and power decoupling.

A. Single-Phase Power

In order to evaluate the single-phase power, let us assume that, under operation, voltage and current in the ac side of single-phase converters are given by

$$v_{\rm ac}(t) = V_{\rm ac}\sin(\omega t), \tag{1}$$

$$i_{\rm ac}(t) = I_{\rm ac}\sin(\omega t - \phi), \tag{2}$$

where ω is the electrical frequency in rad/s, $v_{\rm ac}(t)$ is the "instantaneous average" output voltage, $i_{\rm ac}(t)$ is the output current, $V_{\rm ac}$ is the peak of the "instantaneous average" output voltage $v_{\rm ac}$, $I_{\rm ac}$ is the peak of the average output current $i_{\rm ac}$, and ϕ corresponds to the phase displacement between $v_{\rm ac}$ and $i_{\rm ac}$ in radian.

The instantaneous power at the converter input/output can be computed by $p_{\rm ac} = v_{\rm ac} i_{\rm ac}$. Using (1) and (2), it has

$$\begin{aligned} p_{\rm ac} &= P_{\rm dc} + p_{\rm osc}, \\ &= \frac{V_{\rm ac} I_{\rm ac}}{2}\cos(\phi) - \frac{V_{\rm ac} I_{\rm ac}}{2}\cos(2\omega t - \phi). \end{aligned} \tag{3}$$

From (3) it is possible to see that $p_{\rm ac}$ has a continuous ($P_{\rm dc}$) and an alternate ($p_{\rm osc}$) component at twice the load/grid frequency. The behavior of these waveforms can be depicted in Fig. 1.

B. Problems due to the Single-Phase Power Oscillation

Single-phase ac power has a typical frequency that corresponds to twice the electrical grid frequency. Processing of such power made by converters means low-frequency oscillation of current or voltage along the dc link in them. In order to avoid interference of such oscillations along the power processing, it is necessary to use a large capacitor or inductor as a part of the ac converter. These oscillations degenerates the quality of power processing and are present in both operation mode: rectifier and inverter. Side effects can be seen in several applications [1]–[11]. In [1] and [2], it is shown that oscillations in the dc link can result in torque oscillation in a three-phase induction motor. Moon *et al.* [3]–[5] show that fuel cells that supply a

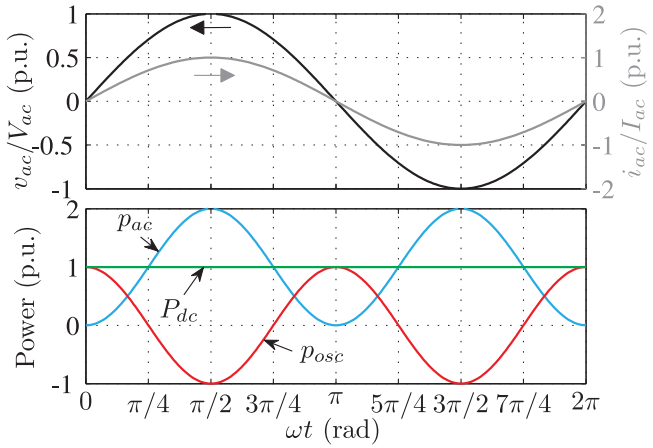

Fig. 1. Waveforms of the ac signals processed in single-phase converters: (top) ac voltage and current; and (bottom) power overlap.

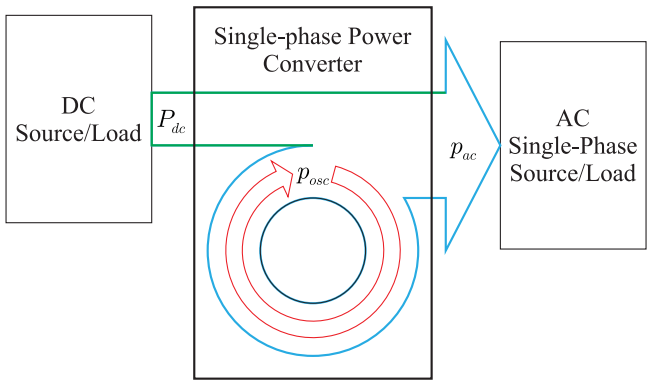

Fig. 2. Power flow in a single-phase converter with power decoupling.

single-phase inverter have their performance, life time, and control stability widely influenced by power flow oscillation. In [6], it is shown that the battery internal temperature increases when it operates under oscillating current profile. In [7] and [8], it is shown that the low-frequency current through the bus capacitor reduces its life time because of the equivalent series resistance of the bus capacitor. When a photovoltaic (PV) array is used to supply energy to a single-phase load, the oscillating power profile causes loss of efficiency to operate at the maximum power point [9]–[14]. As it can be seen, there are many situations that it are desirable to avoid power oscillation at the dc side.

To avoid the single-phase power to propagate through the converter, it has to be able to process the oscillating power $p_{\rm osc}$ and prevent the application from inappropriate signal quality. To process the oscillating power, the converter needs to have the feature of storage or buffering such power during its operation. This capability may be illustrated in Fig. 2, where it is possible to observe that the dc side is providing only $P_{\rm dc}$.

If a dc-load side do not have tight requirements for the ripple, the energy buffer component size will be greatly reduced. This may be true in certain applications. However, in many other applications like aviation, data center, health care, etc., the dc-link requirement is quite strict. Therefore, the power density can

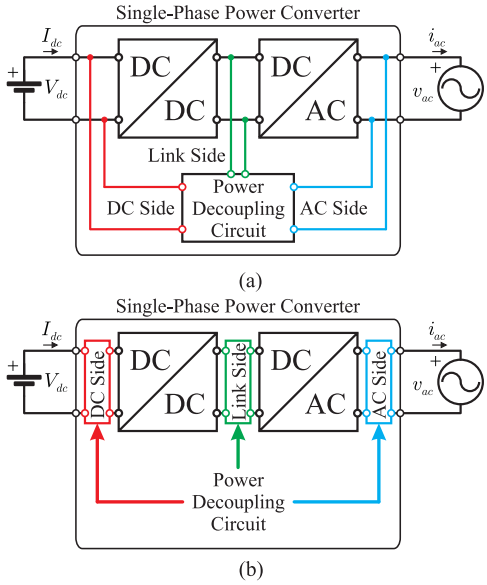

Fig. 3. Single-phase power decoupling hardware methods: (a) parallel and (b) series.

be greatly improved if it uses the proper energy buffer solution. The load-side sensitivity to the ripple energy will greatly impact the energy buffer component size or volume.

C. Topologies and Classification

In this paper, the evaluated topologies are divided as: rectifiers, inverters, and bidirectional. Among them, it is possible to classify as isolated and nonisolated converters. The energy storage method may be classified as: capacitive and inductive. For power decoupling technic, it is convenient to divide it as control and topology, which means that the converter has only a modified control strategy keeping its original structure or it has additional components that modified its original structure, respectively. The power decoupling technic may be implemented as series or parallel with respect to the ac, dc or link side of the converter, as shown in Fig. 3. It is worth noting that the converters may be composed by one or two stages, i.e., a directly dc–ac (or ac–ac) conversion or a dc–dc then dc–ac conversion, respectively. The authors' suggested application is also presented. As it will be seen through this paper, some authors name their topologies as rectifier or inverter; however, these topologies may be able to work as bidirectional operation.

II. Rectifiers

A. Nonisolated Rectifiers

Most power decoupling technics use auxiliary circuit for this purpose; however, [15], [16] simplifies it proposing to use conventional PFC to inject the appropriate required third harmonic into the input current to reduce the electrolytic boost capacitor, as shown in Fig. 4. A solution for a noncontrolled rectifier was proposed by Ohnuma and Itoh [17], [18], where it is based on an indirect matrix converter with an active buffer to decouple

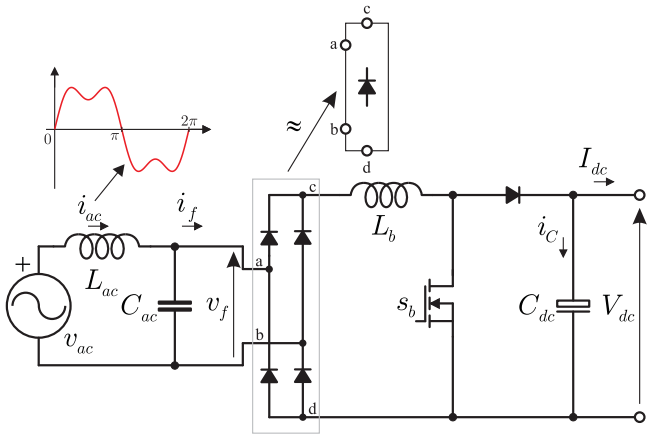

Fig. 4. Third harmonic injection proposed in [15] and [16].

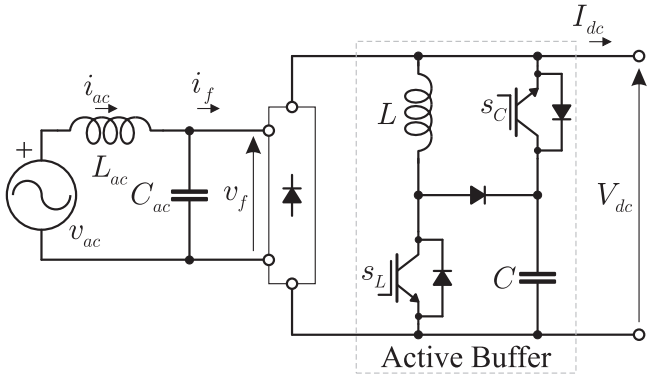

Fig. 5. Proposed in [17] and [18].

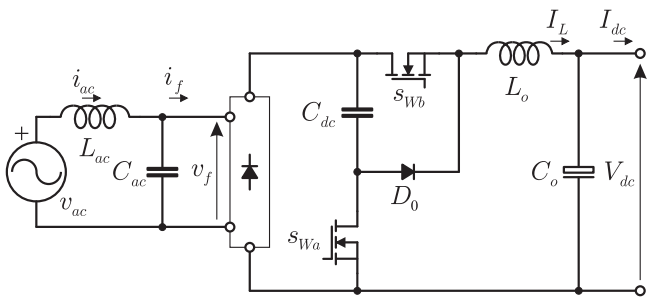

Fig. 6. Proposed in [19].

the power ripple, see Fig. 5. The buffer circuit is located in the dc link of a back-to-back single- to three-phase converter.

A single-phase buck ac–dc converter (see Fig. 6) with a power pulsation decoupling function and a control method with PFC are proposed in [19]. The proposed converter uses an active buffer, which is composed of two switching devices (s_{Wa} and s_{Wb}), a diode, and a small capacitor ($C_{\rm dc}$) which is responsible to absorb the power pulsation generated with twice the power supply frequency. The decoupling function is achieved controlling the current flowing through the capacitor $C_{\rm dc}$. The value of the active buffer capacitance is reduced by controlling the

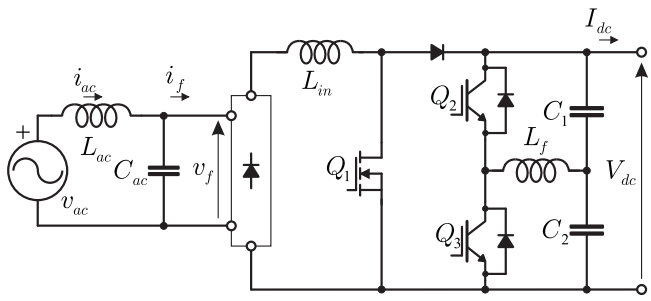

Fig. 7. Proposed in [21].

capacitor voltage variation, allowing the use of small capacitors such as film capacitors or laminated ceramic capacitors.

In [20], an active filter applied in the dc link is proposed by using a scheme based on a thyristor converter and a paralleled IGBT dc active filter. This work was focused in reducing the low-frequency ripple current and avoids using the large electrolytic capacitors. This method applies the dc chopper to inject the ripple current to avoid a power ripple. The proposed topology uses extra switching devices, resulting in a large total volume device.

A symmetrical half-bridge circuit to decouple the fluctuating power in single-phase ac–dc systems is proposed in [21]. As can be seen in Fig. 7, two identical film capacitors (C_1 and C_2) are employed and connected in series in the dc link, whose midpoint is then connected to another phase leg (formed by the switches Q_2 and Q_3) through a small filtering inductor L_f. In order to provide the double-line-frequency ripple power, the capacitor voltages are then controlled to be sinusoidal with an offset value equals to half the dc-link voltage $V_{\rm dc}/2$. The added symmetrical half-bridge circuit is also easy to control because the voltages of the two film capacitors are both sinusoidal.

In [22], a grid-input-current-shaping method that is applied to the motor drive without electrolytic capacitor is proposed. The system considered consists of a single-phase diode rectifier, a three-phase inverter, and a small dc-link capacitor. The work was focused on controlling the output power of the inverter, but the proposed method is composed by a current reference generation, the direct output power control by modification of the output voltage reference, and the overmodulation method that maintains the output power of the inverter after the output voltage limitation. With the proposed method, the harmonic components of the grid input current are suppressed under the limits in regulation, and then the decoupling power is achieved without the PFC circuit or the input filter.

For a current source rectifier (CSR), Sun *et al.* [23] proposes a decoupling solution without requiring additional active switches, as seen in Fig. 8. The proposed topology requires two additional identical capacitors to buffer the ripple power (C_1 and C_2) and two more diodes (D_3 and D_4) to guarantee the safety operation of the converter during start up and stop processes. A closed-control strategy is presented, in which the decoupling control is responsible for regulating the dc-link current and maintaining the dc component of the decoupling capacitor voltages (u_1 and u_2) at a given level.

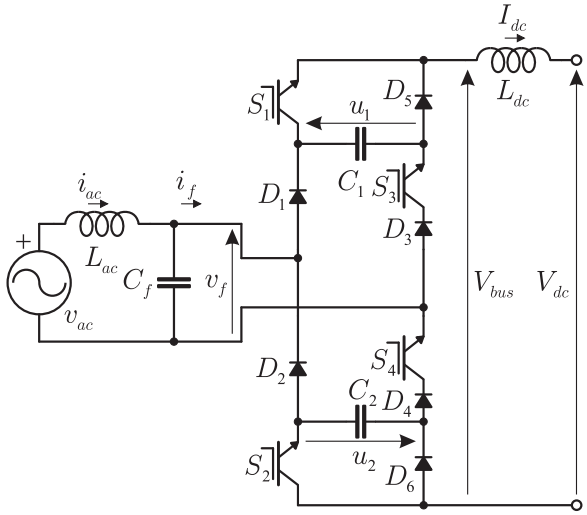

Fig. 8. Proposed in [23].

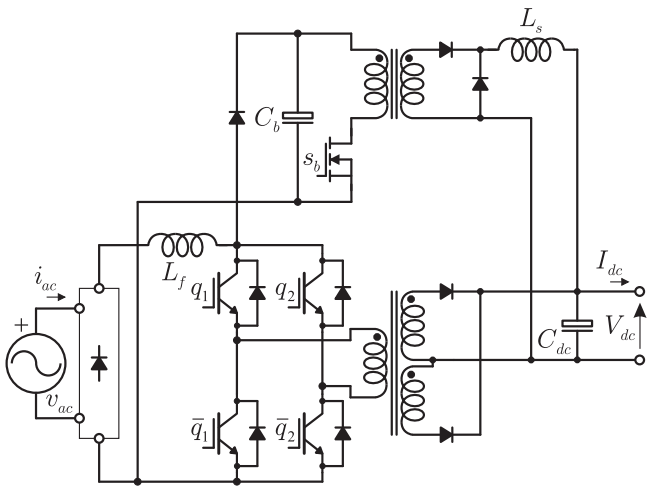

Fig. 9. PPFC concept proposed in [24].

B. Isolated Rectifiers

In [24], a concept is proposed to implement the PFC circuit in parallel with the main power flow path and is only rated for 30% of the total power. The circuit shown in Fig. 9 implements the above parallel power factor correction (PPFC) concept. The main power stage is an isolated full-bridge boost converter. The auxiliary stage here is a typical forward converter. The flyback PPFC converters would also be attractive for low-power applications requiring tight output regulation. In [25], the flyback PPFC converter, as shown in Fig. 10(a), is obtained by adding the auxiliary network composed of s_2, s_3, and C_B to the normal flyback converter. This auxiliary network controls the power flow to achieve the output regulation. A variation of the above flyback PPFC converter can be obtained by replacing the switch s_2 with the diode d_1 and putting switch s_4 in series with the rectifier diode d_2, as shown in Fig. 10(a). A big advantage here is that the flyback transformer leakage problem is eliminated, since the diode d_1 clamps the maximum switch voltage to the bulk capacitor voltage.

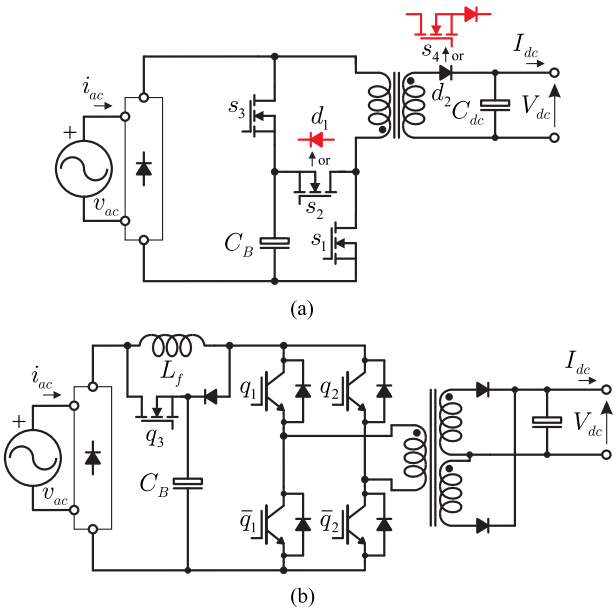

Fig. 10. Proposed in [25]. (a) Flyback PPFC converter. (b) Single-stage boost PPFC converter.

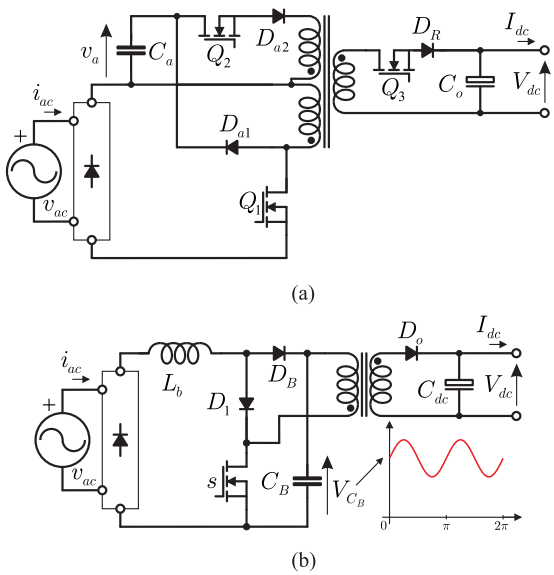

Fig. 11. Flyback PFC topologies: proposed in (a) [26] and in (b) [27].

For power higher than several hundred watts, flyback is not suitable for the difficulty of designing the flyback transformer, and the boost converter would be the choice. Also, in [25], the single-stage boost PPFC converter is proposed and shown in Fig. 11(b). The full-bridge boost converter provides input current and the isolation. According to the authors, the total efficiency of 93% has been achieved with the proposed boost PPFC converter.

In [26] and [27], (Fig. 11(a) and (b), respectively) two more topologies for PFC using flyback as an ac–dc converter with power decoupling in the link are proposed. In [26], a full power decoupling is possible due to the freedom generated by the

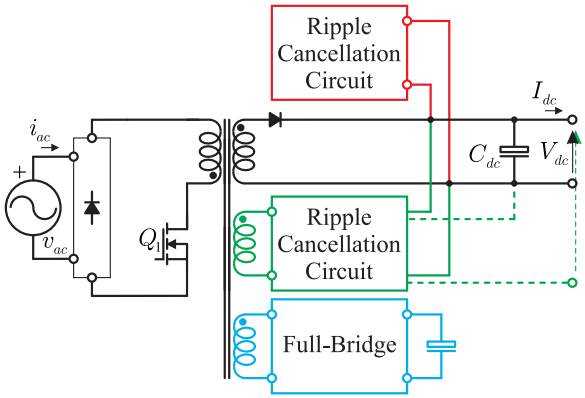

Fig. 12. Proposed in [28], [29] (red), [30], [31] (green), and [32] (blue) for PFC LED driver applications.

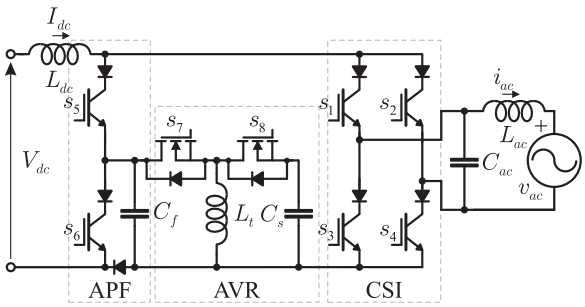

Fig. 13. Proposed in [33].

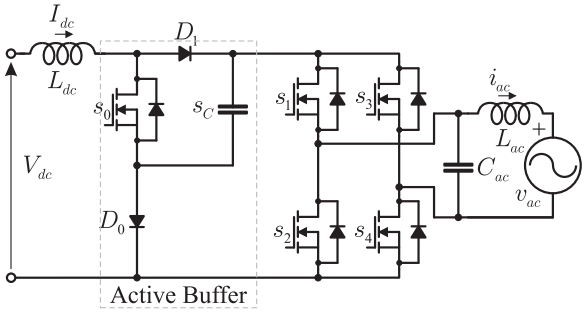

Fig. 14. Proposed in [34].

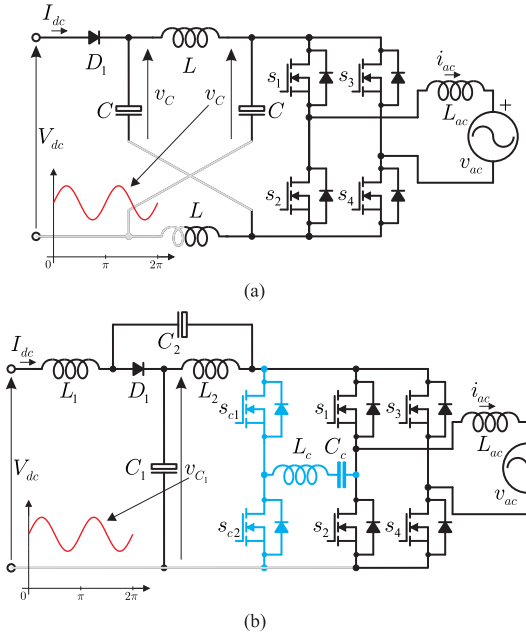

Fig. 15. Impedance source inverters: (a) conventional ZSI [35]; and (b) qZSI [36]–[39] and [40] (blue).

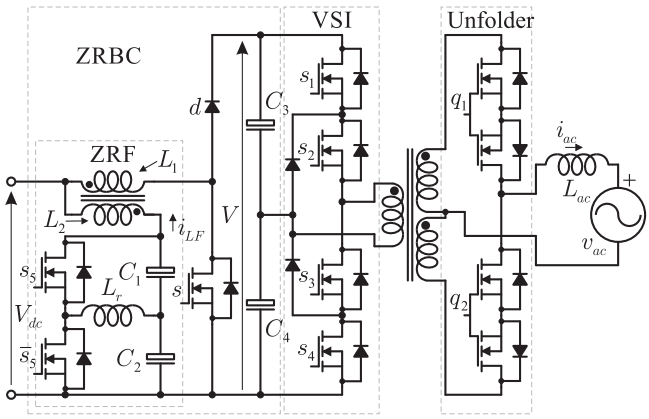

Fig. 16. Proposed in [41].

auxiliary circuit made main by C_a, Q_2, and D_{a1}. The topology proposed in [27] uses only one switch for controlling the converter, which means that the pulsating power is transferred to a small capacitor with large voltage ripple.

Topologies used in ac–dc light-emitting diode (LED) driver applications without electrolytic capacitor can be generalized in Fig. 12. In [28] and [29], a bidirectional auxiliary converter is utilized, which serves to absorb the ac component of the pulsating current of the flyback PFC path, leaving only a dc component to drive the LEDs, illustrated by Fig. 12 (red). The current compensator circuits shown in Figs. 31 and 35 are used for [28] and [29], respectively. The idea proposed by Valipour *et al.* [30] uses a buck converter supplied by a third winding of the transformer to generate the necessary single-phase ripple cancellation demanded by the dc side, as shown in Fig. 12 (solid green). Similar idea of using a third winding is used in [31]; however, the ripple cancellation circuit is a full-bridge converter whose output is connected in series with the dc side, as illustrated in Fig. 12 (dashed green). Another topology for the PFC LED driver is proposed in [32] where an auxiliary winding in the transformer and an additional full-bridge circuit are used for power compensation [see Fig. 12 (blue)].

III. Inverters

A. Nonisolated Inverters

Fig. 13 shows the topology proposed by Roman and Silva [33]. It is an auxiliary circuit composed of an APF and an active voltage regulator (AVR) in addition to a typical H-bridge current source inverter (CSI). The APF is composed of one phase leg connected to the CSI input through a diode, and an

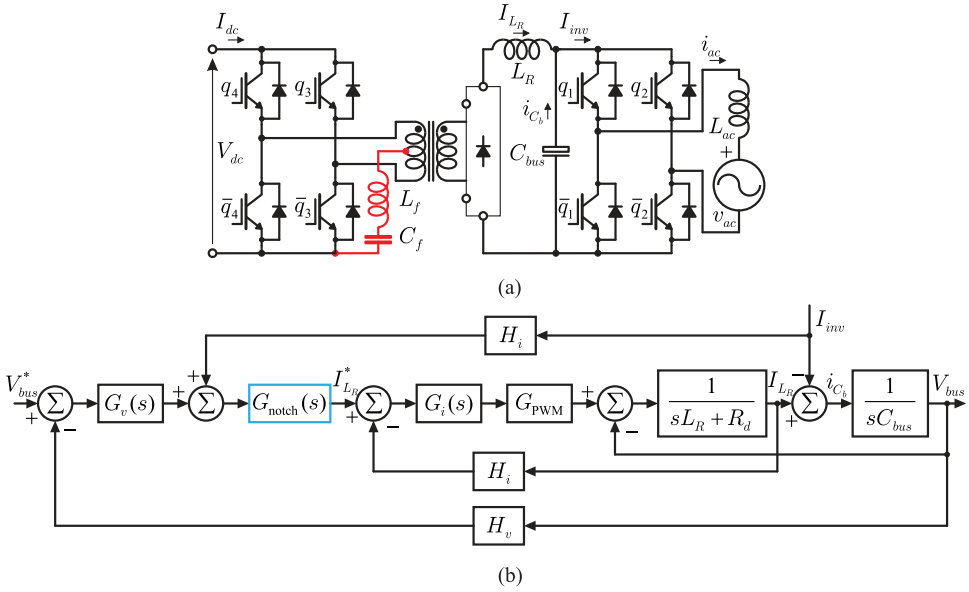

Fig. 17. Isolated two-stage VSI: (a) proposed in [42] and [43] and [44] (add red); and (b) control block diagram proposed in [42].

auxiliary capacitor C_f that works as a dc voltage source. The APF operates as a voltage source inverter (VSI) in series with the PV array, providing the required voltage to compensate dc voltage oscillations. The AVR, composed of one phase leg, an energy transfer inductor L_t, and an energy storage capacitor C_s, is a bidirectional buck–boost and it regulates the voltage of C_f storing the excess amount of energy in C_s and delivering it when necessary. Because inductors are not good energy storage components, the AVR works in discontinuous current mode. As the power decoupling is achieved, no electrolytic capacitors are needed, improving the longer life time and dc link ripple minimization.

Topology and control method are proposed in [34], as shown in Fig. 14, which is constructed based on a CSI with an active buffer in which its circuit consists of one switch, two diodes, and one small capacitor. This active buffer allows the PV to operates without low-frequency fluctuations, improving, thus, the solar power extraction.

Impedance source inverters (ZSI) are being widely studied, which is shown in Fig. 15(a). The control strategy proposed in [35] allows the power oscillation to be transferred to capacitors C without changing the topology structure. A quasi-Z-source inverter (qZSI) system is shown in Fig. 15(b). In order to balance the power mismatch between the dc side and ac side, the low-frequency ripple power needs to be buffered by the passive components, mainly the qZSI capacitor C_1 which has higher voltage rating than C_2. In [36]–[39], control strategies are proposed for single-phase qZSI to mitigate the input oscillating power without using large capacitance. This power is transferred to capacitor C_1. An active filter integrated single-phase qZSI is proposed in [40] [see Fig. 15(b) (blue)]. This topology has one more half-bridge leg (s_{c1} and s_{c2}), paralleled to the half-bridge legs of traditional single-phase qZSI. Meanwhile, a small inductor L_c is in series with the capacitor C_c to smooth the high-frequency current ripple.

B. Isolated Inverters

In the topology proposed by Mazumder *et al.* [41], a zero-ripple boost converter (ZRBC) that comprises a zero-ripple filter (ZRF) is used to reduce the input low- and high-frequency current ripples. A half-bridge neutral-point-clamped multilevel VSI is used as a dc–ac converter. A half-bridge APF is incorporated in ZRF for mitigating the low-frequency ripple. The APF is composed by the capacitors C_1, C_2, the switches s_5 and $\bar{s}_5$, and the inductor L_2 (see Fig. 16). The coupled inductors L_1 and L_2 in combination with the capacitors C_1 and C_2 minimizes the high-frequency ripple current, and the APF minimizes the low-frequency ripple current. The current in the inductor L_2 (i_{LF}) is controlled in such a way that the low-frequency ripple current mitigation is achieved.

In [42], control strategies that can not only reduce the second harmonic current (SHC) in the front-end dc–dc converter [see Fig. 17(a)], but also remarkably improve the system dynamic performance are proposed. Based on the current mode control, which can effectively suppress the SHC in the front-end dc–dc converter, a notch-filter inserted load current feed-forward scheme that improves the dynamic performance during load transient while keeping the advantage of reducing the SHC in the front-end dc–dc stage is proposed. Furthermore, one more notch-filter is introduced into the voltage regulator to eliminate the SHC in the front-end dc–dc stage. Then, these two notch-filters are further combined into one that is inserted into the inner current loop reference branch, represented as $G_{\text{notch}}(s)$ shown in Fig. 17(b). In order to reduce the current ripple in the fuel cell, Liu and Lai [43] use high-speed current control to eliminate the the ripple current propagation path and its linearized ac model is derived. The equivalent circuit model and ripple current reduction is reached by using passive energy storage component and an advanced active control technique is proposed to incorporate a current control loop in the dc–dc converter for ripple

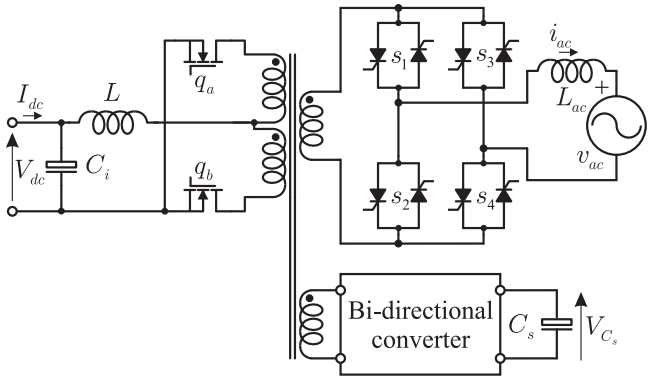

Fig. 18. Proposed in [45] and [46].

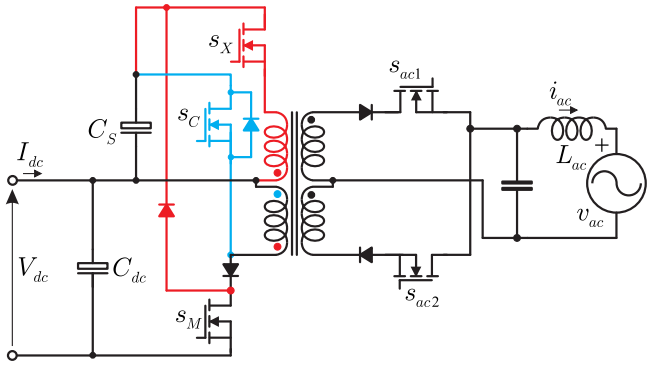

Fig. 19. Proposed in [47], [48] (blue), and in [49] (red).

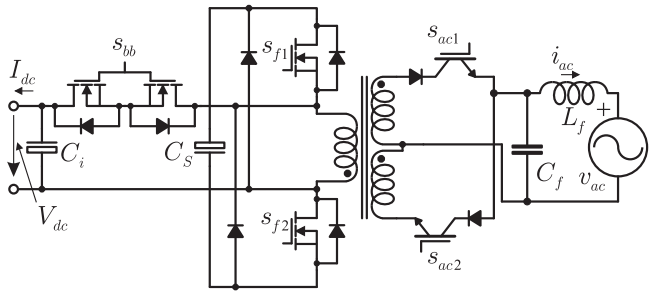

Fig. 20. Proposed in [50].

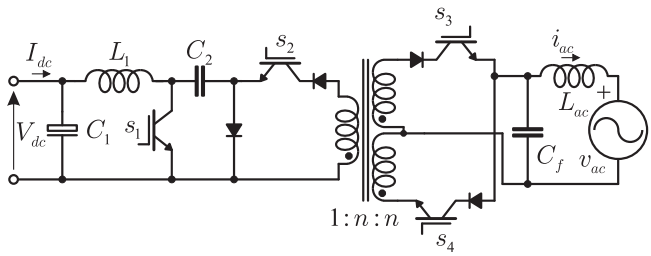

Fig. 21. Proposed in [51].

reduction. In [44], a single-phase isolated converter was proposed for grid interconnection applications. The proposed circuit consists of an isolated dc–dc converter, an active filter, and the interconnection inverter, as shown in Fig. 17(a) (red). The main idea is to control the center tap potential to divert the ripple power to the capacitor C_f, which is connected to the center tap of a medium-frequency transformer. The leakage inductance of the transformer is used to suppress the switching current in addition to the inductor L_f. The benefit of the proposed topology is the realization of the dc active filter function without increasing the number of switching devices, And also, if the leakage inductance is large enough, then the inductor L_f is not required.

An active filter configuration, shown in Fig. 18, composed by a voltage-sourced push–pull interface on the dc side, a Thyristor bridge on the ac side, and a bidirectional converter (BC) to power decoupling is proposed in [45] and [46]. In this topology, the BC controls the voltage on the capacitor C_s such that the power flow cancels the double frequency. The small inductor on the BC is used only to smooth out switching frequency. According to the authors, the peak capacitor voltage V_{C_s} can be chosen by design, and the capacitor value can be made arbitrarily small.

Fig. 19 (blue) shows the circuit topology proposed by Shimizu *et al.* [47], [48]. It is a flyback inverter with a power decoupling circuit formed by the switch S_C and capacitor C_S. This circuit behaves as a bidirectional buck–boost chopper, which supplies the pulsating power, and the flyback inverter circuit can operate satisfactory without using a bulky dc-link capacitor. The basic idea of this circuit is that the power pulsation on the dc link is converted into the voltage pulsation on the capacitor C_S. In [49], the topology shown in Fig. 19 (red) is proposed. The paper analysis two modulation methods discussing their characteristics and the conversion efficiency.

Fig. 20 shows the dual-transistor flyback converter proposed by Kjaer and Blaabjerg [50]. The work was focused in to derive the stress and power losses, and hereby developing a tool for optimizing the inverter in terms of efficiency and ratings, But the topology permits that the bulky electrolytic decoupling capacitor (C_S) may be replaced with a smaller film capacitor.

In [51], a single-phase flyback inverter is proposed (see Fig. 21), which has the main purpose of obtaining the soft-switching operation for all of the active switches. But in addition, this proposed circuit converts the low-frequency power pulsation into the voltage pulsation on capacitor C_2 such that the voltage of the dc input capacitor C_1 is kept constant and its capacitance can be reduced to a very small value. Compared with a buck–boost inverter and other flyback inverter topologies, no extra active switches are used in the proposed inverter to enhance the power decoupling, so only four active switches are required.

A type of three-port flyback inverter using additional decoupling circuit (composed by the switches s_c, s_d, the capacitor C_x, and the inductor L_2) which covers surplus energy and behaves as a charging or discharging decoupling capacitor is proposed in [52] and [53], as shown in Fig. 22. This circuit is configured to have a small value of the inductance L_2 to attenuate switching frequency and prevent drastic current flow to the capacitor C_x. The main idea to cancel the double-line-frequency ripple power is defined by comparing the dc input power and instantaneous output power. When the input power is larger than the output

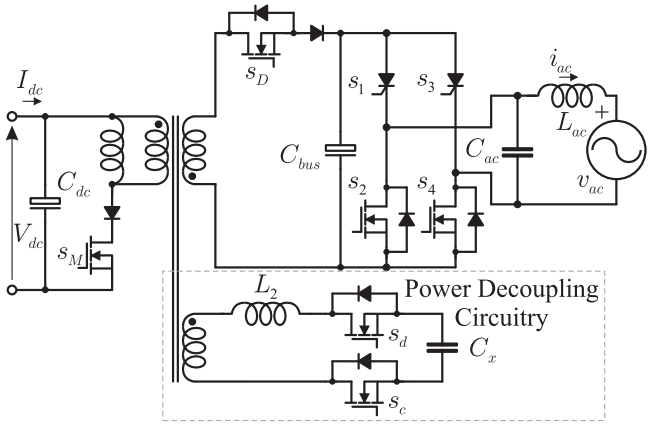

Fig. 22. Proposed in [52] and [53], similar to [54] which uses H-bridge at power decoupling circuitry.

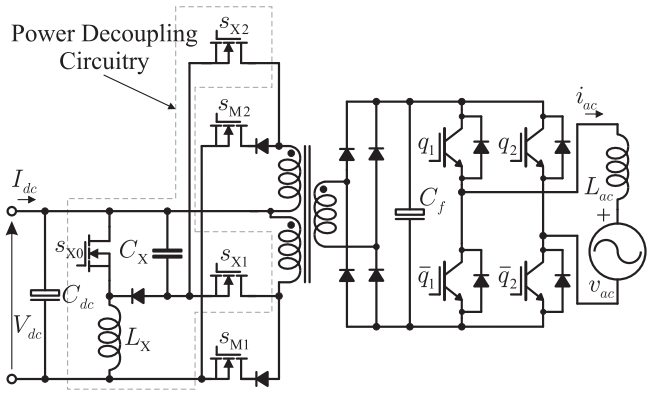

Fig. 23. Proposed in [55]. The same power decoupling circuit is further used in [56].

power, surplus energy has to be charged in decoupling capacitor. Also, when the input power is smaller than the output power, then insufficient input power is supplied by the already charged decoupling capacitor. In this topology, only two switches are used for charging and discharging the decoupling capacitor, which is a simplified structure compared with the topology proposed by Chen and Liao [54], which is similar to the decoupling circuit proposed using H-bridge at power decoupling circuitry.

The topology shown in Fig. 23 is proposed in [55]. The power decoupling circuit (composed of switches $S_{\rm X0}$–$S_{\rm X2}$, the capacitor $C_{\rm X}$, and the inductor $L_{\rm X}$) is also the same circuit used in [56] for a parallel flyback (except for switch $S_{\rm X2}$). This circuit carries on boost/buck mode to storage/release energy. In addition, to reduce the value of the decoupling capacitor to achieve a small film capacitor instead of the electrolytic capacitor, this circuit reduces the peak power, core volume of the transformer, and grid frequency ripple current. It also improves the power density and the conversion efficiency.

Fig. 24 shows the topology studied in [57], which the decoupling circuit consists of only one switch S_2 and two diodes D_1 and D_2 in addition to the decoupling capacitor C_D. The operation of this topology is divided into two main modes: charging mode; and discharging mode. The decoupling capacitor will

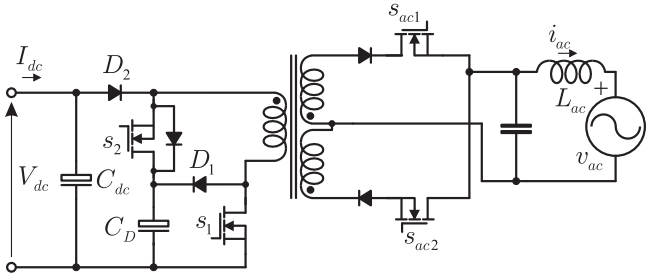

Fig. 24. Proposed in [57].

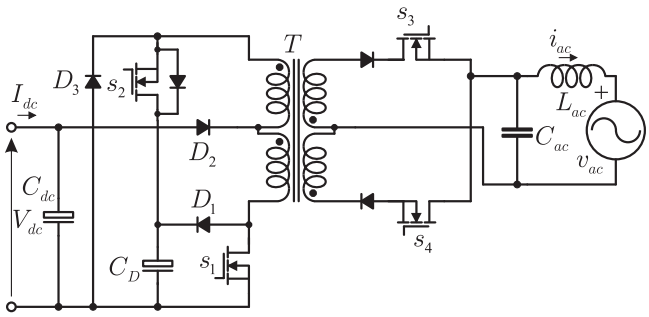

Fig. 25. Proposed in [58].

act as a secondary port. It will work as a load in the charging mode and as a source in the discharging mode. The operation depends on the value of the output power; the circuit will operate comparing the output power P_o with the constant input power $P_{\rm in}$. When $P_o(t) < P_{\rm in}$, the extra energy will be stored in the decoupling capacitor. When $P_o(t) > P_{\rm in}$, the decoupling capacitor will support the PV panel by discharging energy into the transformer and transferring the required power to the output. It can be noticed that no double power conversion is used, and the transformer leakage energy is stored in the decoupling capacitor through D_1. This means that there is no need for extra dissipative clamp circuits. This will reduce the power losses.

A microinverter topology proposed by Hu *et al.* [58] is shown in Fig. 25. The proposed topology employs a different power decoupling technique, which is basically derived from a conventional flyback by adding additional switch s_2, and another transformer winding at primary side to implement power decoupling function. The power decoupling capacitor C_D behaves as both an energy storage element and a snubber capacitor to recycle the transformer leakage energy. A diode D_2 prevents the reverse current from power decoupling capacitor C_D to PV source. The diode D_3 offers a leakage energy discharge path, which consists of D_3, T, D_1, and C_D in the loop. Using the comparison between the output power and input power, the decoupling power is achieved and a long lifetime film capacitor can be used.

The topology proposed in [59] is a power converter architecture, which incorporates a multilevel energy buffer and voltage modulator (MEB) to achieve compression of the high-frequency inverter operating range, thereby improving the efficiency of the high-frequency-link dc–ac converter stage. The MEB also partially replaces the original bulk input capacitor and provides

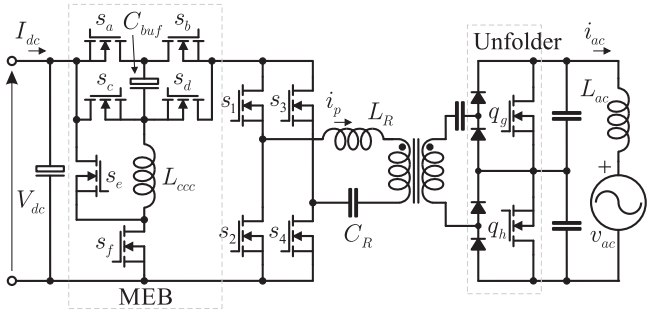

Fig. 26. Proposed in [59].

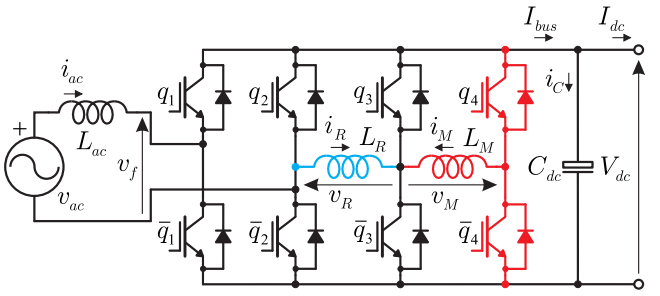

Fig. 28. Proposed in [61] for three legs (blue), and further in [62] for four legs (red).

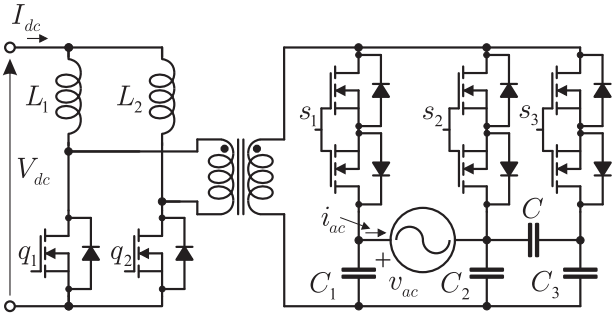

Fig. 27. Proposed in [60].

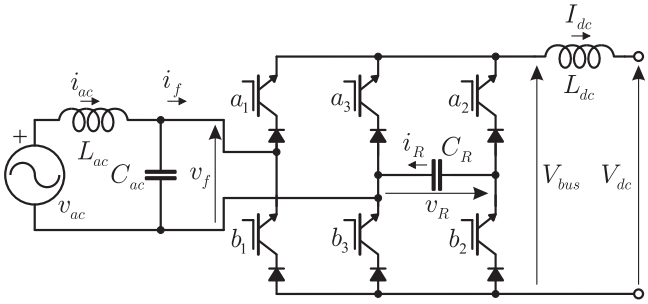

Fig. 29. Proposed in [63] and [64].

the twice-line-frequency energy buffering between dc and ac. The architecture of the proposed MEB microinverter is shown in Fig. 26. The MEB is connected in cascade between the input capacitor and a dc–ac converter block. The MEB comprises a switched-capacitor energy buffer (SCEB) composed by the switches s_a–s_d and the capacitor $C_{\rm buf}$ and an optional charge control circuit (CCC) composed by the switches s_e–s_f and the inductor $L_{\rm ccc}$. The SCEB works as an active energy buffer and helps to reduce the total energy storage requirement for the twice-line-frequency energy buffering by separating the energy buffer voltage from the input voltage. The optional CCC provides an additional means to balance the total charge entering and leaving the SCEB over a line cycle, thereby providing greater flexibility in the operation of the SCEB.

A high-frequency-link converter is proposed in [60] where it is applied to a dual-boost converter to produce ac voltage output without rectifying the high-frequency current avoiding a dc link. Fig. 27 shows the schematic of this converter, which has two ac outputs. Capacitors C_1, C_2, and C_3 are small, providing high-frequency paths for the link current. One phase output, composed by s_1, s_2, C_1, and C_2, injects unity power factor current into the mains, while the second output, composed by s_3 and C_3, which shares s_2 and C_2 with first output, supplies a capacitive load (C) with a waveform that ensures that the instantaneous power remains constant, guaranteeing that the ripple power is avoided at the dc input to the converter.

IV. Bidirectionals

A. Nonisolated Bidirectionals

A topology of single-phase pulse width modulation (PWM) voltage source rectifier is proposed in [61]. This topology, shown in Fig. 28 (blue), consists of a conventional single-phase PWM voltage source rectifier, a pair of additional switches (q_3 and $\bar{q}_3$), and an inductor L_R. The proposed rectifier requires neither a large dc capacitor nor a passive *LC* resonant circuit. The decoupling power is achieved reducing the ripple current on this circuit topology, converting the ripple energy into the magnetic energy in the inductor L_R. Two control methods are proposed for storing magnetic energy into an inductor. While in [62], the same two methods are analyzed and another control method is proposed for a four-leg converter (q_3, $\bar{q}_3$, q_4, $\bar{q}_4$, and L_M), as shown in Fig. 28 (red). These topologies have bidirectional capability in terms of power process, which means that they can be named as voltage source converters (VSCs).

The power circuit of the topology proposed in [63] and [64] for a current source converter (CSC) is illustrated in Fig. 29. On the dc side of the converter, the inductor $L_{\rm dc}$ is used to maintain the current $I_{\rm dc}$ constant. On the ac side of the converter, two phase legs of the bridge are connected to the grid voltage through an *LC* filter that is composed of $L_{\rm ac}$ and $C_{\rm ac}$. In [63], a CSC is analyzed. In [64], the authors analyze both VSC and CSC. The main idea in both papers is to control the current CSC on the capacitor C_R such that the decoupling power can be achieved. The inductor $L_{\rm dc}$ in this proposed topology can be sized according to the switching frequency ripple components.

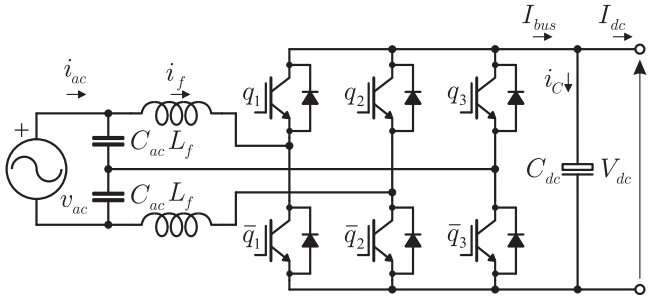

Fig. 30. Proposed in [65].

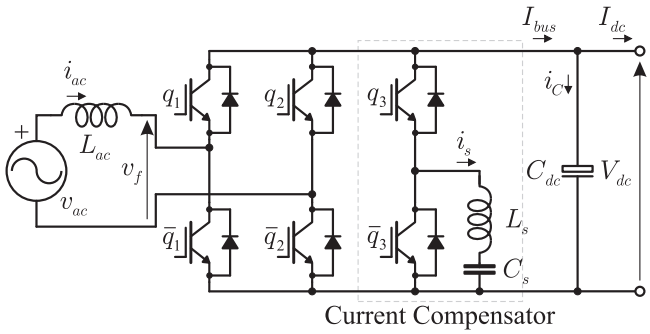

Fig. 31. Proposed in [66] and [67].

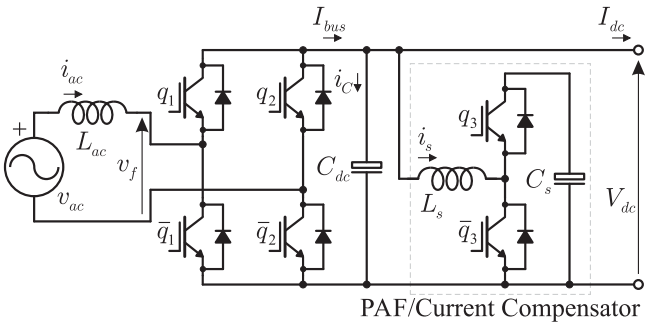

Fig. 32. Proposed in [68]–[72].

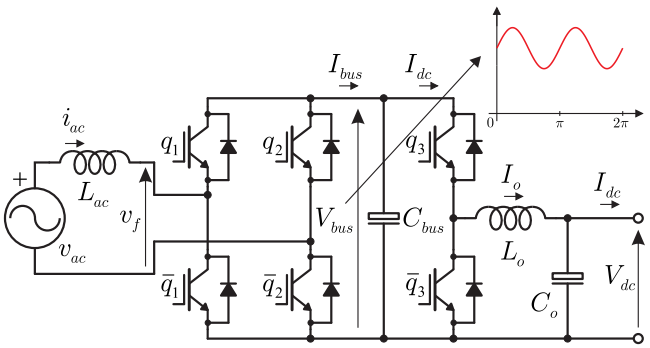

Fig. 33. Proposed in [74].

Hence, the size of the inductor can be significantly smaller than the conventional single-phase CSCs.

A circuit topology for a PWM rectifier is proposed by Shimizu *et al.* [65] and is shown in Fig. 30. The work was focused on achieving unity power factor on the ac supply side and ripple reduction on the dc output side. The main circuit of this rectifier consists of a conventional PWM rectifier and a pair of additional switches (q_3 and $\bar{q}_3$), which are connected to two terminals of the dc output line, and the junction of q_3 and $\bar{q}_3$ is connected to the junction of the two capacitors $C_{\rm ac}$ of the ac input filter. The switches and PWM rectifier are controlled such that the ripple current on the dc link is reduced, and unity power factor is achieved on the ac line. As a result, this circuit does not require a large dc capacitor or a passive *LC* resonant circuit.

Fig. 31 shows the topology proposed in [66] and [67], where a bidirectional buck–boost converter is used as the ripple energy storage circuit. The circuit is composed of one phase leg formed by the switches q_3 and $\bar{q}_3$, an auxiliary capacitor C_s used as the energy storage component, and an inductor L_s that is used to transfer the ripple energy between the auxiliary capacitor and the dc link. The dc link voltage is still controlled by the H-bridge rectifier, while the ripple power that comes from the ac side is controlled by the auxiliary circuit. According to the authors, the proposed topology leads to a 50% volume reduction of the system size.

A current pulsation smoothing parallel active filter (CPS-PAF) was proposed by Saito *et al.* [68]–[70]. This topology is also proposed by Xing *et al.* [71] but in order to provide the large-signal variable frequency ripple current and actively shape the small-signal impedance characteristics of the dc-link interface at the mid-frequency range to increase the system stability margin. The circuit shown in Fig. 32 implements the CPS-PAF. This circuit behaves as a current source equating the value of the current that flows from the dc side ($I_{\rm dc}$) with the average value of the $I_{\rm bus}(\omega t)$. When the $I_{\rm bus}(\omega t)$ value is lower than $I_{\rm dc}$, the PAF behaves as a boost converter (switch q_3 inactive) storing energy to a small capacitor C_s. In the rest time intervals, the PAF behaves as a buck converter (switch q_3 is active) discharging the C_s. According to [70], this approach has the advantage that it requires a small film capacitor with the capacitance approximately 100 times smaller than in the conventional solution. The proposed CPS-PAF is independent from the inverter topology and its operation mode and so it can be applied for various single-stage topologies. An active low-frequency ripple control method based on the virtual capacitor concept (ALFRCD) is proposed in [72]. The ALFRCD, constituted with a buck–boost converter and an energy storage capacitor, introduces an integrator into the control loop to inject the ripple current into the dc link and restrain the dc component of the current reference. With the virtual capacitor, a filter in the detection process is not essential anymore.

The current compensator circuits seen in Figs. 31 and 32 are analyzed in detail in [73], and a load current compensation technique is proposed. As seen before, the proposed technique replaces the second-stage dc–dc converter with a bidirectional dc–dc converter connected in parallel with the dc link, and requires a secondary energy source, i.e., a small-size capacitor.

As shown in Fig. 33, the topology proposed by Dong *et al.* [74] is a two-stage single-phase PWM, in which two

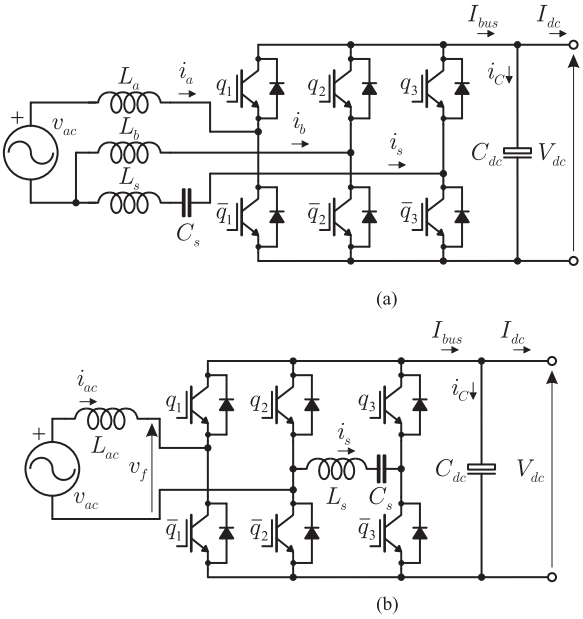

Fig. 34. Proposed in [75], [76], and [78]. (a) Generalization and (b) for $L_b = 0$, which represents a simplification of what is presented in [77].

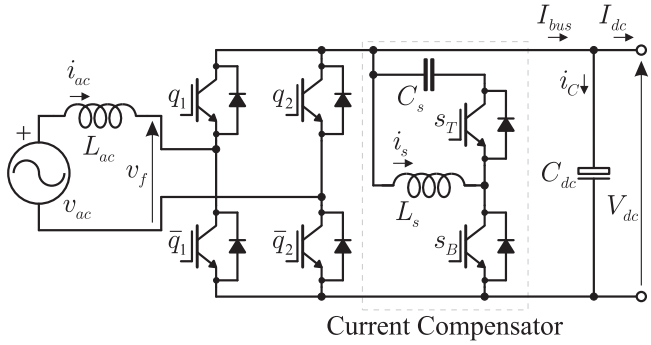

Fig. 35. Proposed in [79].

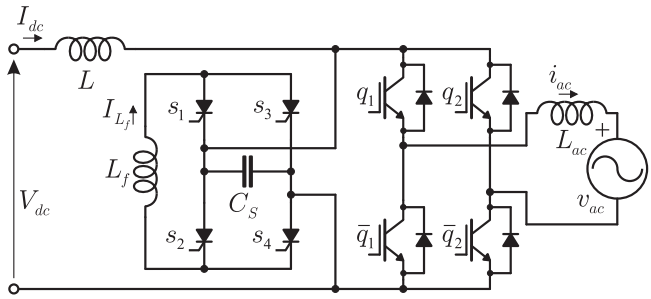

Fig. 36. Proposed in [80].

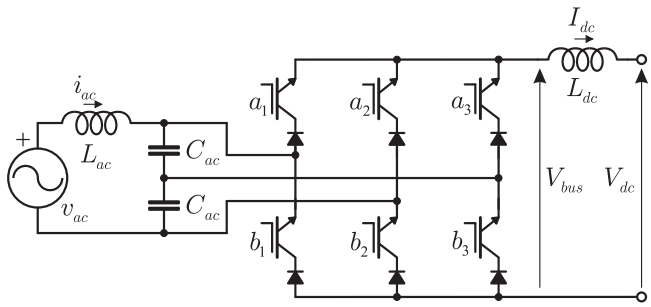

Fig. 37. Proposed in [81] and used by Vitorino *et al.* [82] for single-phase power decoupling.

phase legs are used as the H-bridge to interface with the grid, and the other phase leg is used as a bidirectional dc–dc converter to regulate the dc voltage $V_{\rm dc}$ with a small-voltage ripple to reduce the capacitance $C_{\rm bus}$, thereby leaving a large voltage variation on the dc-link voltage $V_{\rm bus}$. This topology not only reduces the dc-link capacitor $C_{\rm dc}$, but also renders the feasibility of bidirectional power flow.

The circuit shown in Fig. 34 is proposed by Li *et al.* [75], [76]. This circuit consists of a third leg, an energy storage capacitor, and a smoothing inductor. The basic idea is using this circuit to divert the ripple power from the dc link to the capacitor C_s, it provides a high efficiency due to capacitive energy storage as compared with inductance energy storage. The low requirement for switching frequency/control bandwidth, the full utilization of the capacitor energy storage capability, and no excessive current stresses of the power devices are the advantages of the proposed topology. This topology consists of a simplification of what was presented in [77], in which the converter is formed by two H-bridge converters, one for the ac converter and the other for the ripple power compensation. The same H-bridge and the addition phase leg is analyzed together in [78] as an unbalanced three-phase system, and then a space-vector pulse width modulation control is proposed.

Fig. 35 presents the topology proposed by Mollov [79]. This proposed converter behaves as a buck–boost that permits the use of the entire energy stored in C_s, allowing for smaller capacitor. The total energy stored in the reduced capacitor is used more efficiently during dc-link transient mitigation what may eliminate the need to use a large electrolytic capacitor. The capacitor $C_{\rm dc}$ is used to filter the switched current at the switching frequency and stabilizing the dc link. This proposed approach not only effectively mitigates the link voltage transients caused by pulsed power loads, but also contributes to the improvement of the power quality and the stability of the power distribution system.

In [80], a high-frequency current-fed type active filter is used to replace the dc-link electrolytic capacitor, as shown in Fig. 36. This active filter is formed by an inductance L_f, which traps the dc current I_{L_f} which can be switched in either polarity or freewheeled, the power semiconductor devices for the control, and a small capacitor C_S, which filters the high-frequency ripple. In general, this topology permits to absorb the harmonics and provides smooth dc-link voltage. The filtering function is programmable providing flexibility of operation. The topology proposed can be extended to other converter topologies.

In [81], a single-phase PWM CSR with a neutral leg is proposed, but that work was focused in compensate the high-frequency harmonics in the dc-link voltage due the switching. Based in that proposition, in [82], the proposed rectifier (see Fig. 37) was focused in the mitigation of power ripple at

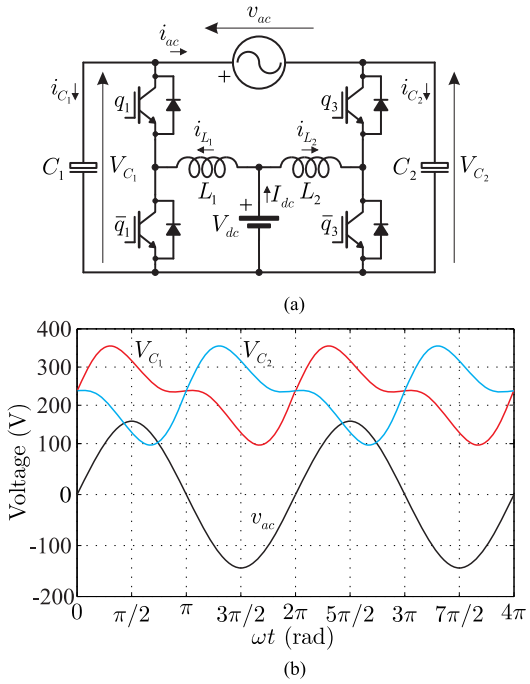

Fig. 38. Proposed in [83]–[86]. (a) Boost-type differential inverter circuit. (b) Waveforms.

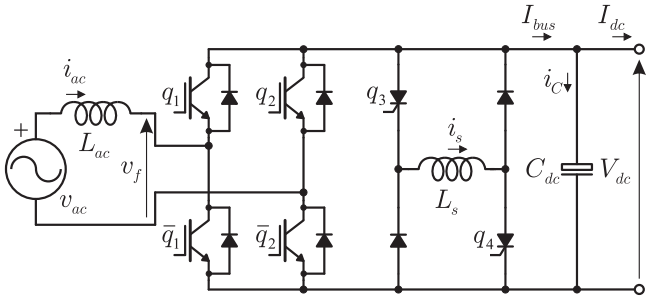

Fig. 39. Proposed in [87].

twice the line frequency. The topology used is a conventional single-phase CSC (switches a_1-b_1 and a_2-b_2) and an extra leg (switches a_3-b_3) to create a converter able to eliminate the single-phase power propagated through the dc link. The output filter made by the two capacitors $C_{\rm ac}$ is responsible to filter the high-frequency harmonics due the switching as well storages the power needed to eliminate the single-phase power oscillation generated by the grid to avoid its propagation through the converter. The neutral leg can introduce new switch states that can be analyzed to find switching sequences that reduces the output voltage distortion and eliminate the power ripple at twice the line frequency. The performance of the proposed topology depends on the correct control applied to the converter.

In [83] and [84], a waveform control method for mitigating low-frequency current ripple in fuel-cell inverter systems is proposed, where a boost-type differential inverter made up of two bidirectional boost converters, as shown in Fig. 38(a), is adopted for describing the proposed waveform control. The objective of the waveform control method is to control the capacitor voltages V_{C_1} and V_{C_2} in such way that they can mitigate the input current ripple. This method achieves significant suppression of the low-frequency current ripple without any additional component, circuit, or electrolytic capacitor, therefore maintaining the overall size and cost. Additionally, the current stress of the switch is decreased and the total efficiency is improved with the use of waveform control. Further, a type of ac–dc differential rectifier system with current-waveform control technique is proposed in [85] for direct rectification applications. The configuration is based on a structure having two bidirectional dc–dc converters in series-input and parallel-output connections. The bidirectional dc–dc converters can be of any type, depending on the required application. To complement the feature of this rectifier configuration, a waveform control is proposed in order to mitigate the double-line-frequency current ripple of the dc output. More analysis about power decoupling is made in [86] for boost-, buck-, and buck–boost-type differential inverters.

The topology proposed by Larsson and Ostlund [87], as shown in Fig. 39, replaces the passive short-circuit link by an active filter consisting of a converter bridge and an inductor. The converter is used to control the inductor current i_s and, thus, the stored magnetic energy. The main idea to keep the dc-link voltage constant is to absorb the excess energy from the supply when the input power is higher than the output power and discharge the energy when the input power is lower than the output power. The active filter is able to operate at both $16 \cdot 2/3$ and 50 Hz without changing its configuration, only a change in the control is necessary, for electric locomotives application.

The topology proposed by Fan *et al.* [88] uses a second ac output as energy buffer in a single-phase converter with six power switches, as is shown in Fig. 40(a). The two-output-port topology of a single-phase converter consists of six switching devices and energy storage components $C_{\rm dc}$, C_2, $L_{\rm ac}$, and L_2. The dc-link capacitor $C_{\rm dc}$ can be very small because it is required for filtering high-order switching harmonics only, and the power decoupling capacitor C_2 is used for storing the double-line-frequency pulsating power in ac side. The idea is to control the capacitor voltage v_{C_2} such that the power in dc side will be constant and the power decoupling of the single-phase converter is achieved. The topology proposed by Vitorino *et al.* [89] is a dual/similar of what is presented in [88] for single-phase power decoupling; however, in [89], the compensation of oscillating power is achieved by using a six-switch CSC topology, which allows independent control for two output ports which share the same dc link, where an energy storage element is responsible to absorb and deliver the oscillating power [see Fig. 40(b)]. The main idea is to control the current that flows through the capacitor C_R such that the power decoupling of the single-phase converter is achieved. As the power decoupling occurs in the ac side, the efficiency is improved compared to the dc-side power decoupling approaches and the dc voltage utilization will not be sacrificed because the grid power control and power decoupling can be controlled completely independent.

Fig. 41 shows an active circuit proposed by Kyritsis *et al.* [90] and Schimpf and Norum [91]. This circuit acts as an interface between the dc link and an additional storage capacitor. The main principle of the circuit is that the dc-link capacitor is

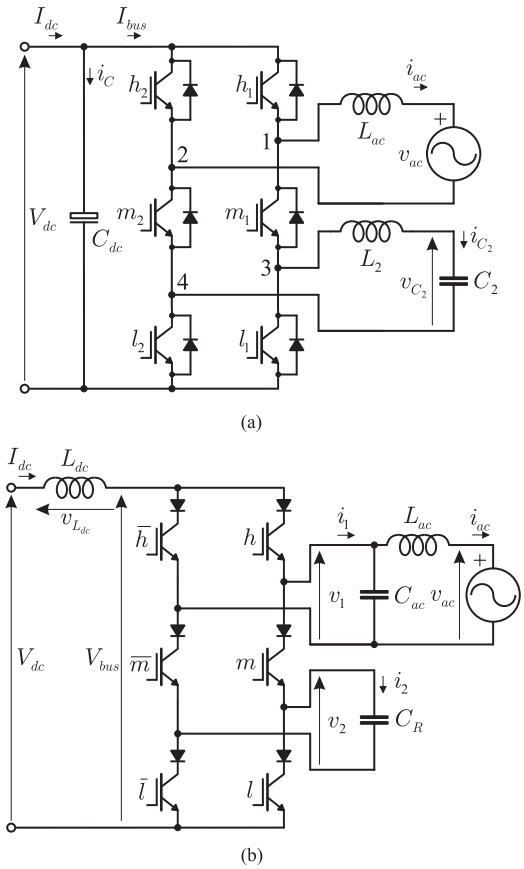

Fig. 40. Topologies using six-switch converter. (a) Voltage source proposed in [88]. (b) Current source proposed in [89].

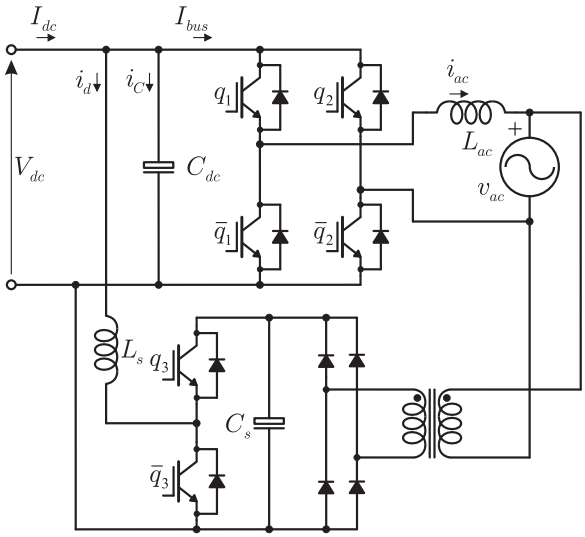

Fig. 41. Proposed in [90] and [91].

separated into two parts, both with relatively low capacity. The capacitors are connected via a bidirectional dc–dc converter, allowing a different voltage at both of them. The dc–dc converter is operated in a way which keeps the voltage at the dc link constant, while the voltage of the second capacitor C_s can have a high ripple. This allows using a larger part of the stored

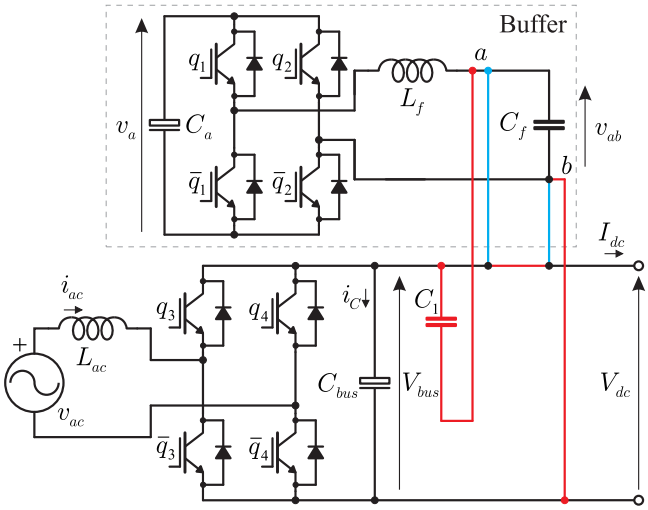

Fig. 42. Proposed in [92]–[94] (blue) and in [95] (red).

energy in the storage capacitor. The bidirectional dc–dc converter operates either as a boost converter (switch q_3 inactive) storing energy to a small capacitor C_s or as a buck converter (switch q_3 is active) discharging C_s. When this active circuit is only controlled by a current controller, the voltage in the storage capacitor C_s can drop to the dc-link voltage while it is being discharged. Then, the marginal PWM operation occurs in the buck operation of the circuit, leading to instability and high ripple in the dc-link voltage. To solve this problem, a combination of a transformer and a diode rectifier proposed by Kyritsis *et al.* [90] in conjunction with a virtual capacitance controller [91] recharge the storage capacitor from the grid, when its voltage drops below a defined limit.

Fig. 42 shows an additional circuit composed by a dc–ac converter consisting of an H-bridge (switches q_1, $\bar{q}_1$, q_2, and $\bar{q}_2$) and an output filter formed by the inductor L_f and capacitor C_f. Its dc side is connected to an energy storage device such as the capacitor C_a. This circuit [see Fig. 42 (blue)], proposed by Wang *et al.* [92]–[94], uses charge and discharge processes by using the stored energy in the capacitor C_a for generating a voltage counteracting $\Delta V_{\rm bus}$ with its dc component equal to zero (i.e., $v_{ab} = \Delta V_{\rm bus}$). Thus, $V_{\rm dc}$ has the same dc value as that across $C_{\rm bus}$, but with a zero-ripple voltage in the ideal situation. This topology can reduce the dc-link capacitance to 10–20% while achieving a very low voltage ripple across its output terminals. Similar buffer structure is used in [95] [see Fig. 42 (red)]; however, the capacitor C_f is connected in series with capacitor C_1, then they are connected in parallel with the dc bus capacitor $C_{\rm bus}$.

A topology for a PWM rectifier is proposed in [96]. Besides the basic function for the PWM rectifier, i.e., transferring the power from ac to dc side, this circuit has a power decoupling function, where the second-order ripple power should be diverted into the decoupling capacitor, in which the voltage can fluctuate in larger range. The proposed circuit is shown in Fig. 43, which divides the ac inductor of the conventional H-bridge PWM rectifier into two parts L_1 and $L_{\rm ac}$. An auxiliary decoupling capacitor $C_{\rm dec}$ is added to absorb the second-order

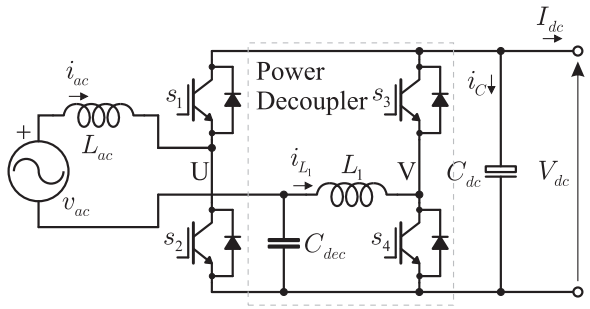

Fig. 43. Proposed in [96].

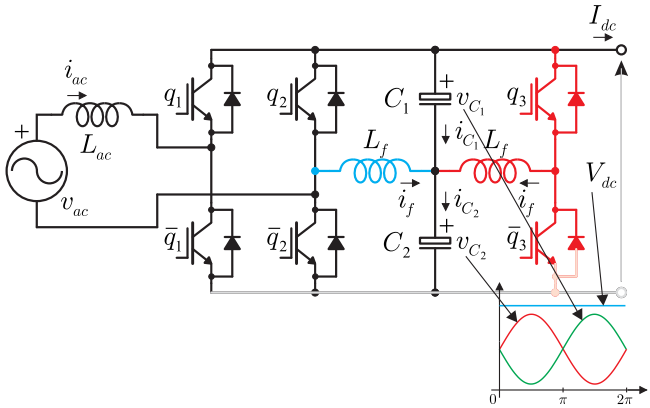

Fig. 44. Proposed in [97]–[99] (blue) and in [100] (red).

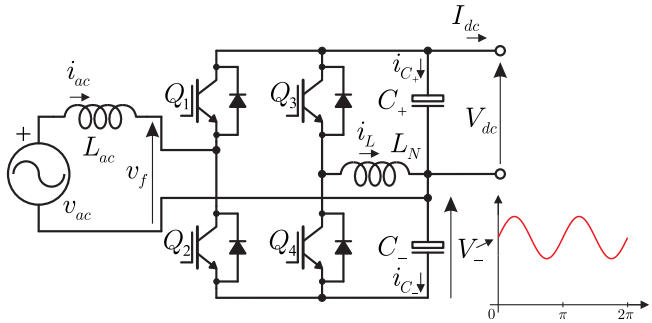

Fig. 45. Proposed in [101], [102], and in [99] where $V_{\rm dc} = v_{C_+} + v_{C_-}$.

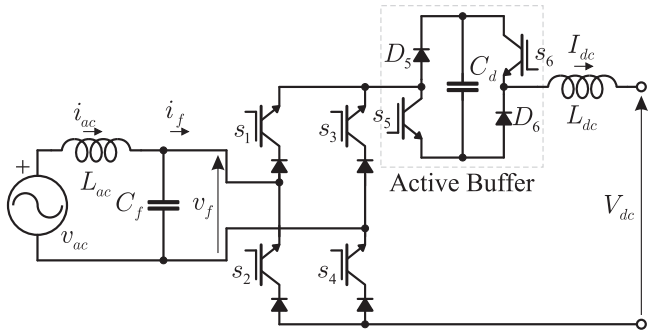

Fig. 46. Proposed in [103].

ripple power. The V-phase leg switches, inductor L_1, and the auxiliary decoupling capacitor $C_{\rm dec}$ constitute the bidirectional buck–boost APF converter, which realizes the function of diverting the second-ripple power into the auxiliary decoupling capacitor. The V-phase switching leg is multiused both as a leg of H-bridge converter and the leg of the buck–boost converter.

In [97]–[99], an active power decoupling circuit is proposed in order to reduce the dc-link capacitance. This is a simple circuit because it does not require any additional active switch or energy storage component for realization of power decoupling, as shown in Fig. 44 (blue). The circuit proposed is a full-bridge rectifier that splits the dc-link capacitor into two identical parts and the midpoint is connected to one leg through a filter inductor. This leg controls the current going into the two output capacitors connected in series. In the ideal situation, the current is controlled such that the voltage on the capacitor cancels the double-line-frequency ripple power that is inherent in single-phase systems. The proposed topology reduces the current stress of the power semiconductors as compared to a conventional H-bridge rectifier, then it can improve the conversion efficiency. Fig. 44 (red) shows an active converter topology proposed by Tang *et al.* [100], which consists of a conventional H-bridge circuit for ac–dc power conversion, and a half-bridge circuit for ripple power compensation. Two identical film capacitors (C_1 and C_2) responsible for the decoupling are connected in series in the dc link, whose midpoint is connected to the half-bridge circuit through a small filtering inductor (L_f). The power decoupling is achieved modulating the half-bridge leg in such a way that the average voltages of the two capacitors are the same, and with its fundamental ac component superposed in each voltage with 180° phase shift. It is noted that in this topology, the only energy storage elements are the dc-link capacitors.

The proposed topology in [99], [101], [102], and as shown in Fig. 45, consists of one single-phase four-switch rectifier. The rectifier is formed by adding two active switches into a conventional half-bridge PWM rectifier by putting a neutral leg consisting of two switches (Q_3 and Q_4) across the dc link with their midpoint connected to the midpoint of the split capacitors (C_+ and C_-) through the inductor L_N. The rectification leg is operated as a half-bridge rectifier to regulate the dc-link voltage, whereas the neutral leg maintains a stable dc output voltage, and by its control, ensures the absorbing of the power pulsating by the capacitor C_-. The two dc voltages, $V_{\rm dc}$ and V_-, provide a possible way to operate the rectifiers to make one of the voltages as the output voltage to supply loads and to make the other voltage as the ripple energy buffer.

In [103], a CSC with power decoupling function is proposed (see Fig. 46). It is constructed by inserting a power buffer circuit in series with the dc link of the conventional CSC circuit. The buffer circuit consists of two switching devices (s_5 and s_6), two diodes (D_5 and D_6), and a capacitor (C_d). As can be seen, the power pulsation with twice the power supply frequency can be absorbed by the active buffer capacitor C_d. The proposed power decoupling circuit could be viewed as a controlled voltage source.

A power decoupling circuit using a flying capacitor dc–dc converter topology is proposed in [104]. The proposed circuit, shown in Fig. 47, has the function of the boost-up and

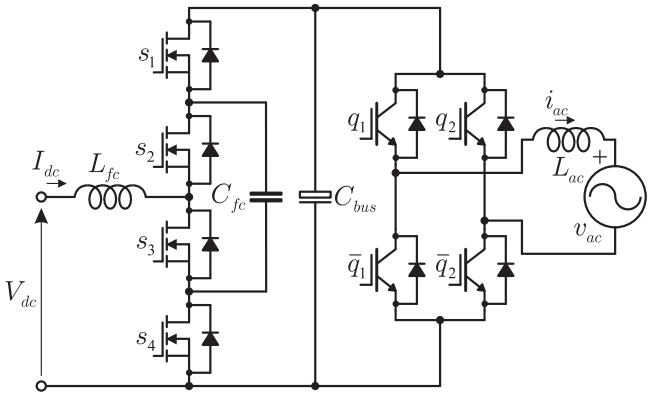

Fig. 47. Proposed in [104].

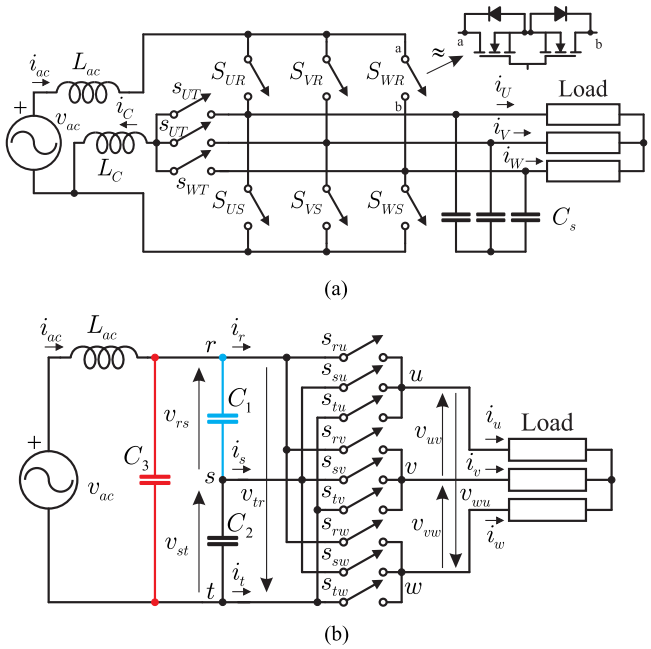

Fig. 48. Single-phase to three-phase matrix converters. (a) Proposed in [105]. (b) Proposed in [106] (blue) and in [107] (red).

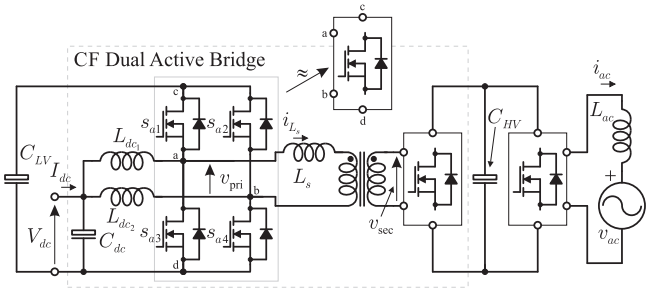

Fig. 49. Proposed in [115]–[117].

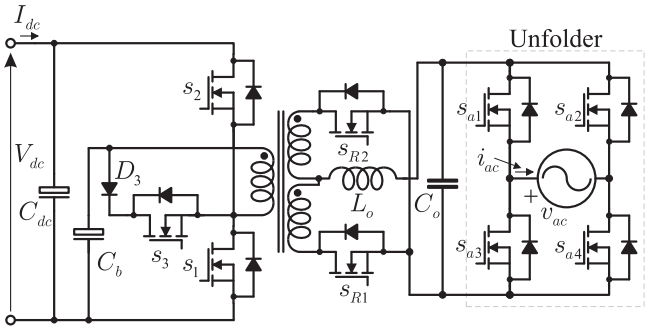

Fig. 50. Proposed in [119].

single-phase power fluctuation compensation. The main idea behind the proposed circuit is to compensate the single-phase power fluctuation controlling the energy on the flying capacitor C_{fc}. In the control strategy, each switching duty is decided by the relationship between input and output power. When the input power is large in comparison with the instantaneous output power, the on duty of charge mode is set widely. On the other hand, when the input power is small, the on duty of discharge mode should be set widely. Besides the simple constitution and easy control, the additional magnetic component for active power decoupling is not required for this topology.

A single-phase to three-phase matrix converter (STMC) with power decoupling capability is proposed in [105]. As can be seen in Fig. 48(a), in order to suppress the ripple on the three-phase voltages and currents, an ac reactor and three bidirectional switches were installed on the conventional single- to three-phase. By using the single-phase instantaneous active and reactive power theory, the ripple component on single-phase instantaneous power is detected and stored in the ac reactor L_C.

In [106], a design method for a single-phase to three-phase matrix converter with compensation for instantaneous power fluctuation is proposed. As shown in Fig. 48(b) (blue), the main circuit of the STMC is similar to the others, but the compensation capacitors C_1 and C_2 for the instantaneous-power fluctuation are connected to the input terminals when the input unity power factor is provided from the single-phase voltage source, i.e., C_1 and C_2 also consist of the *LC* input filter, which suppress harmonic currents, with the input reactor $L_{\rm ac}$. Similar approach is used in [107], which is shown in Fig. 48(b) (red).

A different topology for a matrix converter is proposed in [108], but the proposed converter can instantaneously decouple the single-phase power by installing a small power capacitor in the conventional three/three-phase matrix converter; a similar configuration is shown in Fig. 29 replacing the IGBTs by bidirectional switches. According to the authors, in this proposed system, the size of this capacitor is less than 1/40th of the conventional PWM rectifier/inverter system. The great advantage of the proposed system is to control the motors without vibration in either the steady state or transient state. Continuing talking about ac–dc–ac applications, Vitorino *et al.* [109] proposes to connect in series the topologies shown in Figs. 28 (blue) and 29 to achieve a single-phase to single-phase converter with full power decoupling in both sides. In [110]–[112], single-phase to single-phase conventional back-to-back converter is used such a way that the input and output voltage phases are synchronized by means of the control strategy to minimize the oscillation in the dc link.

TABLE I
OVERVIEW SUMMARY

Direction	Isolation	Fig.	Reference	Storage	Type	Technic	Connec.	Side	Application
		4	[15], [16]	Capacitor	Boost	Control	-	AC	PFC
		5	[17], [18]	Inductor	Boost	Topology	Parallel	Link	AC–DC–AC
		6	[19]	Capacitor	Buck	Topology	Parallel	Link	PFC
	Non-Isolated	-	[20]	Capacitor	Tyristor CSR	Topology	Parallel	Link	PFC
		7	[21]	Capacitor	Boost	Topology	Parallel	Link	PFC
		-	[22]	-	Diode Rect.	Control	-	AC	Motor Drive
		8	[23]	Capacitor	CSR	Topology	Series	Link	PFC
Rectifier		9	[24]	Capacitor	H-Bridge	Topology	Parallel	DC	PFC
		10(a)	[25]	Capacitor	Flyback	Topology	Parallel	Link	PFC
		10(b)	[25]	Capacitor	H-bridge	Topology	Parallel	Link	PFC
		11(a)	[26]	Capacitor	Flyback	Topology	Parallel	Link	LED Driver
	Isolated	11(b)	[27]	Capacitor	Flyback	Top./Cont.	Parallel	Link	LED Driver
		12(red)	[28], [29]	Capacitor	Flyback	Topology	Parallel	DC	LED Driver
		12 (green)	[30]	Capacitor	Flyback	Topology	Parallel	DC	LED Driver
		12 (green)	[31]	Capacitor	Flyback	Topology	Series	DC	LED Driver
		12 (blue)	[32]	Capacitor	Flyback	Topology	Parallel	Link	LED Driver
		13	[33]	Capacitor	CSI	Topology	Parallel	Link	PV
		14	[34]	Capacitor	CSI	Topology	Parallel	Link	PV
	Non-Isolated	15(a)	[35]	Capacitor	ZSI	Control	-	Link	-
		15(b)	[36]–[39]	Capacitor	qZSI	Control	-	Link	PV
		15(b) (blue)	[40]	Capacitor	qZSI	Topology	Parallel	Link	-
		16	[41]	Inductor	VSI	Topology	Parallel	DC	Fuel Cell
		17(a)	[42], [43]	Capacitor	Two-Stage VSI	Control	-	Link	Fuel Cell
		17(a) (red)	[44]	Capacitor	Two-Stage VSI	Topology	Parallel	Link	-
Inverter		18	[45], [46]	Capacitor	Push-pull	Topology	Parallel	Link	Fuel Cell
		19	[47]–[49]	Capacitor	Flyback	Topology	Parallel	DC	PV
		20	[50]	Capacitor	Dual Flyback	Topology	Parallel	DC	PV
	Isolated	21	[51]	Capacitor	Flyback	Topology	Series	DC	PV
		22	[52]–[54]	Capacitor	Flyback	Topology	Parallel	Link	PV
		23	[55]	Capacitor	Push–pull	Topology	Parallel	DC	PV
		23	[56]	Capacitor	Parallel Flyback	Topology	Parallel	DC	PV
		24	[57]	Capacitor	Flyback	Topology	Parallel	DC	PV
		25	[58]	Capacitor	Flyback	Topology	Parallel	Link	PV
		26	[59]	Capacitor	VSI	Topology	Series	DC	PV
		27	[60]	Capacitor	Dual-Boost	Topology	Series	AC	PV
		28	[61], [62]	Inductor	VSC	Topology	Parallel	Link	PFC
		29	[63], [64]	Capacitor	CSC	Topology	Parallel	Link	PV
		30	[65]	Capacitor	VSC	Topology	Parallel	AC	UPS
		31	[66], [67]	Capacitor	VSC	Topology	Parallel	Link	PFC
		32	[68]–[72]	Capacitor	VSC	Topology	Parallel	DC	PFC/PV/Battery
		33	[74]	Capacitor	VSC	Control	-	Link	DC Nanogrid
		34	[75]–[78]	Capacitor	VSC	Topology	Parallel	Link	PFC
		35	[79]	Capacitor	VSC	Topology	Parallel	Link	Aircraft
		36	[80]	Inductor	VSC	Topology	Parallel	DC	Grid-tie
		37	[82]	Capacitor	CSC	Topology	Parallel	AC	-
		38(a)	[83]–[86]	Capacitor	Differ. Inverter	Control	-	AC	Fuel Cell/PFC
		39	[87]	Inductor	VSC	Topology	Parallel	Link	Locomotive
		40(a)	[88]	Capacitor	VSC	Topology	Series	Link	PV
	Non-Isolated	40(b)	[89]	Capacitor	CSC	Topology	Serie	Link	-
		41	[90], [91]	Capacitor	VSC	Topology	Parallel	DC	PV
Bidirectional		42(blue)	[92]–[94]	Capacitor	VSC	Topology	Series	DC	PFC-DC/PV
		42(red)	[95]	Capacitor	VSC	Topology	Parallel	DC	Grid-tie
		43	[96]	Capacitor	VSC	Topology	Series	AC	PFC
		44	[97]–[100]	Inductor	VSC	Topology	Parallel	Link	-
		45	[99], [101], [102]	Capacitor	VSC	Topology	Parallel	Link	Grid-tie/PFC
		46	[103]	Capacitor	CSC	Topology	Series	Link	-
		47	[104]	Capacitor	Fly.-Cap. VSC	Topology	Series	DC	PV
		48(a)	[105]	Inductor	Matrix	Topology	Series	AC	AC-AC
		48(b)	[106], [107]	Capacitor	Matrix	Topology	Parallel	AC	AC-AC/Motor
		-	[108]	Capacitor	Matrix	Topology	Parallel	Link	Motor Drive
		-	[109]	Cap./Ind.	VSC/CSC	Topology	Parallel	Link	AC-DC-AC
		-	[110]–[112]	Capacitor	VSC	Control	-	Link	AC-DC-AC
		-	[113]	Capacitor	DHB	Control	-	Link	Fuel Cell
		-	[114]	Capacitor	DAB	Control	-	Link	PV
	Isolated	49	[115]–[117]	Capacitor	DAB	Top./Cont.	Series	Link	PV
		-	[118]	-	Multi-DAB	Control	-	Link	Fuel Cell
		50	[119]	Capacitor	H. Bri./P.-Pull	Topology	Series	DC	PV

B. Isolated Bidirectionals

In [113], a fuel cell power conditioning system based on the current-fed dual-half-bridge dc–dc converter is proposed. The proposed topology can achieve low-frequency ripple-free input current using a control-oriented power pulsation decoupling strategy. Furthermore, a proportional resonant controller to eliminate fuel cell double-frequency ripple current is developed. The implementation of the proposed pulsation power decoupling control is mainly achieved by the CF-DHB converter phase shift control. Especially, a controller is developed to achieve an extra high control gain at 120 Hz resonant frequency.

A dual active bridge (DAB) with an SHC reduction method is proposed in [114]. The proposal is a voltage-loop-based SHC reduction method which is suited for converters in which duel-loop control is difficult to implement. But this SHC method is not limited to these converters, all the converters with voltage-loop can implement this SHC reduction method. A single-phase grid-connected PV converter based on current-fed dual active bridge (CF-DAB) dc–dc converter is proposed in [115]–[117] (see Fig. 49). The proposed topology uses a small dc-link capacitor with a control method that can achieve minimized low-frequency ripple without adding extra components. The control system of the proposed PV converter is divided into the CF-DAB dc–dc converter control system and the full-bridge inverter control system. At the inverter side, the voltage is regulated by the outer voltage controller in order to mitigate the influence of the double frequency introduced to the control loop, a band-eliminator filter is applied to stop the 120 Hz component.

Various control strategies from an output-impedance viewpoint are discussed in [118], where a bidirectional DAB dc–dc converter modified for multiinput operation is chosen as the platform for analysis. After analysis about the output impedance of the energy storage branch under open-loop condition, as well as, closed-loop conditions with single-voltage loop and dual-loop controls, a proportional-resonant control to effectively compensate for the dc-link voltage variation by generating an extremely low-impedance path for harmonic current flow at specific frequency was proposed. The proposed method control shown to be very effective in suppressing voltage ripples by diverting harmonic current flow from the dc-link capacitor to the energy storage branch.

A three-port converter with power decoupling capability is proposed in [119], as shown in Fig. 50. Without the middle branch of s_3 and D_3, it is a traditional half-bridge two-port converter. By adding these components, it becomes a modified version of the half-bridge converter which includes three basic circuit stages which has two control freedoms, in which the energy storage element is made by C_b. The circuit allows ZVS operation.

V. Comparison and Consideration

Considering all the topologies presented in this paper, a detailed summary is shown in Table I. The comparison is conducted in terms of energy storage element, topology type, auxiliary circuit location, etc., in terms of what is shown in Section I-C.

From this comparison, most of the active method selects the capacitor as the element to store the ripple energy. The reason is because of higher energy density for capacitor compared with inductor. With a certain energy storage requirement and operating frequency, energy storage components size is compared for both inductive and capacitive method [109], [120]. The inductor is found not to be as good as a capacitor in terms of energy density for an application using tens of hertz to few hundred hertz. There are two major reasons for this preliminary conclusion. First, the magnetic material saturation flux will limit the volume. In order to meet the flux saturation requirement for the energy storage inductor, a larger magnetic core size is required. Second, the inductor has more losses compared with the capacitor; in order to meet the temperature rise requirement, more volume is required for thermal dissipation.

Meanwhile, we can notice that most of the active method topologies belong to parallel structure. The reason is because of higher efficiency for parallel structure compared with series structure because only the ripple energy is processed in the parallel topology. For the series structure, the main power has to be processed as well which will create more loss.

VI. Conclusion

Single-phase distributed applications are becoming widely used nowadays. To improve the converter power density, reliability, and life time, many research works have been proposed single-phase power decoupling techniques. This paper presents a comprehensive overview in state-of-the-art on power decoupling techniques for single-phase applications systems highlighting the topologies and structures. In terms of classification, the topologies are divided as: rectifiers, inverters, and bidirectionals. Among them, a second broad classification is related to whether the topology has galvanic isolation or not. Most of the applications are utilized in PV systems and in PFC. Till the data of submission, all proposed ideas exiting in the literature regarding the topic are gathered in this paper. To the ease of study, a summary table is presented containing the references.

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