Load-Dependent Soft-Switching Method of Half-Bridge Current Doubler for High-Voltage Point-of-Load Converter in Data Center Power Supplies

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***Abstract*—With the increased cloud computing and digital information storage, the energy requirement of data centers keeps increasing. A high-voltage point of load (HV POL) with an input series output parallel structure is proposed to convert 400 to 1 V_{DC} within a single stage to increase the power conversion efficiency. The symmetrical controlled half-bridge current doubler is selected as the converter topology in the HV POL. A load-dependent soft-switching method has been proposed with an auxiliary circuit that includes inductor, diode, and MOSFETs so that the hard-switching issue of typical symmetrical controlled half-bridge converters is resolved. The operation principles of the proposed soft-switching half-bridge current doubler have been analyzed in detail. Then, the necessity of adjusting the timing with the loading in the proposed method is analyzed based on losses, and a controller is designed to realize the load-dependent operation. A lossless *RCD* current sensing method is used to sense the output inductor current value in the proposed load-dependent operation. Experimental efficiency of a hardware prototype is provided to show that the proposed method can increase the converter's efficiency in both heavy- and light-load conditions.**

***Index Terms*—Date center power supplies, half-bridge current doubler, load dependent, zero voltage switching (ZVS).**

I. Introduction

EXTENSIVE efforts have been devoted to improve the efficiency of power supplies used in data centers as the data centers' electricity usage keeps increasing, yet most of the power supplies are operated with efficiency below 50% [1]–[3]. In order to improve the overall efficiency of power supply from 400 to 1 V_{DC}, a single power conversion stage converting 400 to 1 V_{DC} directly has been proposed, and the converter performs as the high-voltage point-of-load (HV POL) converter as shown in Fig. 1 [4], [5]. Nowadays, most of the power supply architectures have several conversion stages connected in series [2], [6]. In series-connected architectures, the system overall efficiency from 400 to 1 V_{DC} is the product of each stage's efficiency, which is lower than the lowest converter's efficiency in the power supply chain. HV POL has the potential to increase the overall power conversion's efficiency from 400 to 1 V_{DC} as it eliminates the need to multiply each converter's efficiency to obtain the overall system's efficiency. In addition, high-efficiency power converter design within a HV POL is the key to increasing the system efficiency when converting from 400 to 1 V_{DC}.

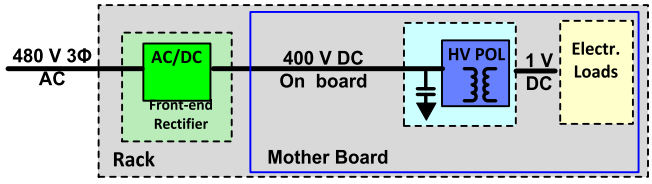

Fig. 1. HV POL architecture.

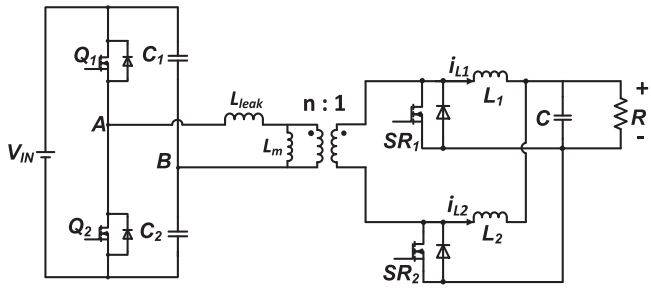

Fig. 2. Half-bridge current doubler converter.

Therefore, in this paper, a load-dependent soft-switching method will be discussed to reduce the devices' switching losses and to improve the efficiency of the converter used in HV POL.

To mitigate the voltage conversion ratio from input to output for a single converter, a six-phase input series output parallel (ISOP) connected system is implemented to fulfill the 400 to 1 V_{DC} conversion [4], [5]. Even with an ISOP system, the step-down ratio for a single converter is still extremely high (66:1); therefore, a half-bridge current doubler (illustrated in Fig. 2) is selected as the converter topology in the HV POL because the voltage gain from output voltage to input voltage of a half bridge is 1/2 [7] compared with full bridge. A current doubler on the secondary side is selected as it simplifies the transformer design and eliminates current flowing through the transformer secondary-side windings during the freewheeling period compared with the full-wave rectifier which requires a center tapped transformer.

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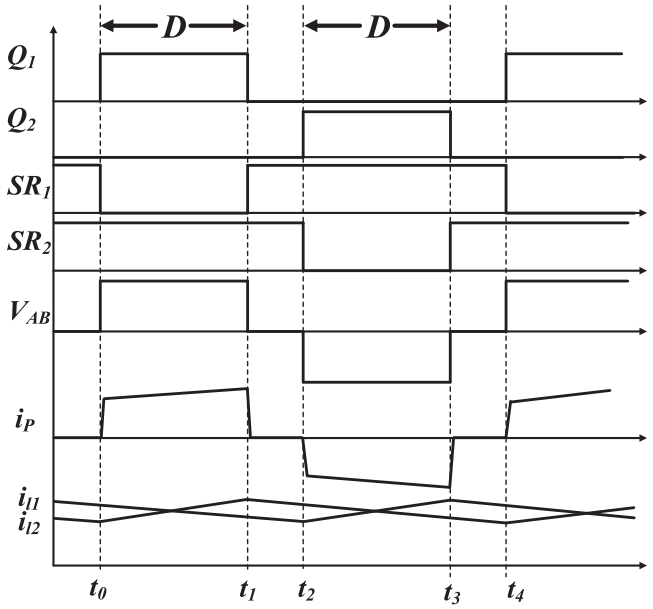


Fig. 3. Key waveforms of symmetrical control of half-bridge current doubler.

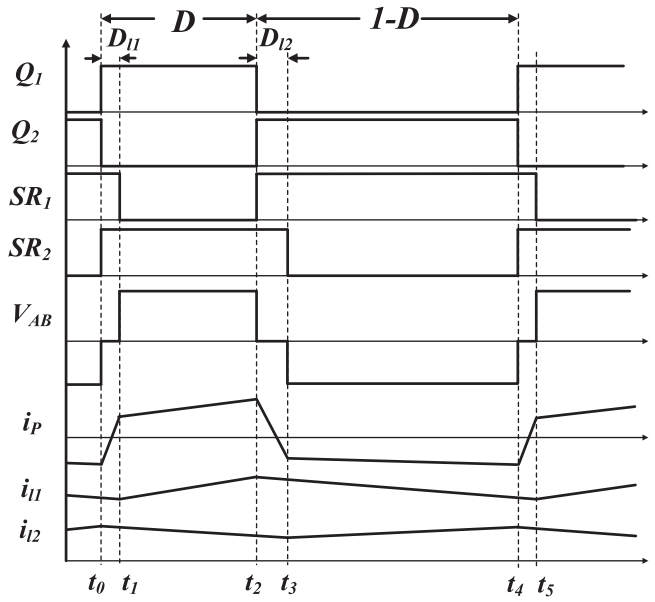


Fig. 4. Key waveforms of asymmetrical control of a half-bridge current doubler.

Because of the high-input voltage and large output current of the half-bridge current doubler, the switching losses of the primary-side MOSFETs (Q_1 and Q_2) and the body diode reverse-recovery losses of the secondary-side MOSFETs (SR_1 and SR_2) will be the dominant loss mechanism which cannot be reduced by device paralleling in the converter. Furthermore, in terms of the switching losses of the primary MOSFETs, turn-on loss would be more severe as extra current is introduced by the body diode reverse recovery and the capacitive losses to discharge the junction capacitances. In order to improve the converter efficiency, zero voltage turn on which can eliminate both turn-on losses of primary MOSFETs and body diode reverse-recovery losses of SRs would be necessary without increasing the conduction losses in the devices and transformer.

Asymmetrical control of a half-bridge current doubler where Q_1 and Q_2 are controlled with complementary gate signals (shown in Fig. 3) [11], [12] is implemented to allow zero voltage switching (ZVS) of primary-side MOSFETs for certain load range with the assistance of leakage inductance ($L_{\rm leak}$). With larger leakage inductance, wider ZVS range can be achieved. However, larger leakage leads to a larger duty cycle loss and higher RMS current in the transformer [8], which is not desirable as the current stress and conduction loss will increase and offset the efficiency benefit by reducing the switching losses. Moreover, eventually, ZVS of primary-side MOSFETs is lost at light loading regardless of the leakage inductance value. Clearly illustrated in Fig. 3, the current stress on the devices is not even and the transformer is biased [8].

Another control method is symmetrical control where Q_1 and Q_2 are controlled with an identical gate signal with 180º phase shift (shown in Fig. 4) [8]–[10]. Symmetrical controlled half-bridge current doubler allows balanced current stress of MOSFETs and nonbiased transformer operation, which is preferred. Since the leakage inductance $L_{\rm leak}$ is minimized in symmetrical control to reduce the resonant current when both Q_1 and Q_2 are OFF, the duty cycle loss and RMS current is much lower in symmetrical control compared with the asymmetrical control, which means the conductive loss is also lower. The major drawback of a symmetrical controlled half-bridge current doubler is that the primary devices are operating with hard switching and the SR device with reverse-recovery current. Therefore, a soft-switching method eliminating the two losses is needed to further improve the efficiency of a symmetrical controlled half-bridge current doubler.

In this paper, a load-dependent ZVS of primary MOSFETs for the entire load range is proposed to improve the efficiency of the half-bridge current doubler with symmetrical control.

II. Soft Switching of a Half-Bridge Current Doubler and Buck Derived Converters

Since the symmetrical controlled half-bridge current doubler is essentially the same as the two-phase interleaved buck converter with isolation, therefore, ZVS methods for a buck converter can be applied to the half-bridge current doubler. Various approaches have been proposed to obtain ZVS of buck and buck-derived converters [8], [13]–[29]. For all the methods, the current at a switching node (*SN* in Fig. 5) during the dead time between turning off Q_2 and turning on Q_1 needs to be the direction in Fig. 5 to achieve ZVS of Q_1 and eliminate the reverse-recovery loss of Q_2. In [8], [13], and [14], smaller output inductance with natural bidirectional current flow is proposed for ZVS, yet the major drawback of this method is that the increased current ripple leads to an increased core loss of the output inductor, increased conduction loss of switching devices, inductor, and capacitor, and increased Q_2 turn-off loss especially at light load.

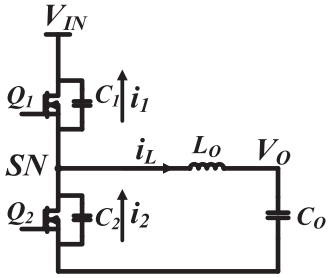


Fig. 5. Synchronous buck converter with current direction of switches and inductor.

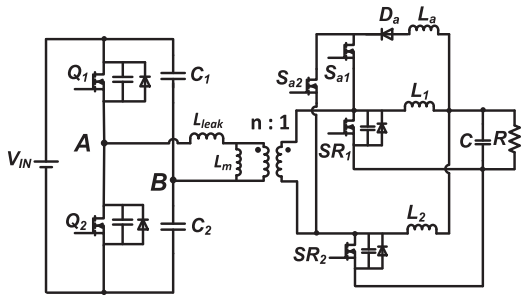


Fig. 6. Proposed ZVS circuit for a half-bridge current doubler.

In order to solve the increased turn-off loss of Q_2, in [15], a clamping circuit is placed in parallel with the output inductor so the current is clamped at a desired value instead of continuing to increase until Q_1 is turned ON. In [16], an emulated diode rectification of a synchronous rectifier is implemented, but it requires a zero-current crossing detection to turn off the SR MOSFET, which increases the complexity of the circuit.

In order to solve the increased core loss of the output inductor, in [17]–[19], an auxiliary inductor is inserted in a two-phase buck converter. The current flowing on the auxiliary inductor helps to reshape the output inductor current to realize ZVS instead of reducing the output inductance; however, the auxiliary inductor is conducting all the time, which introduces considerable conduction loss. In [20]–[24], a coupled inductor is inserted into the converter, together with a diode or an active switch; however, the turn-off losses of Q_2 increase with load reduction.

In [25]–[29], an auxiliary inductor together with unidirectional switch is placed in parallel with the output inductor, and by charging the auxiliary inductor, the desired current direction can be obtained at the switch node. The method in [25]–[29] solves the increased conduction loss of devices; however, all of the methods in [17]–[29] lead to an increased turn-off loss of Q_2; therefore, a snubber capacitor has been placed in parallel with Q_1 or Q_2 to obtain a zero voltage turn off; however, the snubber capacitor paralleled with the MOSFETs essentially requires more energy to achieve ZVS turn on of the MOSFETs, which means more energy needs to be stored in the auxiliary inductor. Therefore, increased auxiliary losses occur when paralleling the snubber capacitor. In the meantime, the time used to charge the auxiliary inductor in [25]–[28] is fixed which means the losses in the auxiliary circuit is also fixed regardless of loading. The constant auxiliary components' losses undermine the benefit of eliminating switching losses when the load reduces. To solve the constant auxiliary components losses, in [29], the timing of the gate signal is adjusted based on load condition through a lookup table; however, it still uses a snubber capacitor in parallel with MOSFETs which increases the auxiliary components losses at the beginning.

When it comes to a half-bridge current doubler, the snubber capacitor cannot be added in parallel with Q_1 or Q_2 as in Fig. 2 even if the additional auxiliary components loss is not an issue. The leakage inductance of the transformer ($L_{\rm leak}$) resonates with the junction capacitance of the MOSFETs when both Q_1 and Q_2 are OFF. Adding the turn-off snubber capacitors in parallel with Q_1 and Q_2 leads to an increased resonant current and higher winding losses in the transformer, which will undermine the efficiency increase by reducing the turn-on losses. One way to damp the oscillation is adding a snubber resistor in series with the snubber capacitor; however, extra snubber losses occur in the converter. Therefore, by adding the snubber capacitor to solve the increased turn-off loss of SR_1 and SR_2, which is widely used in the buck converter, is not feasible in the half-bridge converter.

In this paper, a load-dependent ZVS method shown in Fig. 6 has been proposed to improve the efficiency of the half-bridge current doubler in a wide load range. Besides the power stage of a conventional half-bridge current doubler shown in Fig. 2, the proposed circuit also contains an auxiliary circuit, which includes series-connected MOSFETs (S_{a1} and S_{a2}), a diode (D_a), and an inductor (L_a). The capacitances in parallel with the devices are the junction capacitances drawn explicitly and are not extra discrete components, and these will be used to explain how the proposed method works in the following sections.

In this paper, first, the operation principle of the proposed ZVS method for the half-bridge current doubler converter is presented. In the next section, the load-dependent ZVS method will be described, and a controller design procedure will be given in detail. Then, the converter design to adopt the proposed load-dependent charging method will be provided which is followed by an experimental verification of the proposed load-dependent ZVS method.

III. Operation Principle of a ZVS Half-Bridge Current Doubler

Fig. 7 illustrates the theoretical operation waveforms of the converter's major components. The operation of the load-dependent soft-switching half-bridge current doubler can be divided into 12 intervals as t_0 through t_{11} in Fig. 7. Because the half-bridge converter is a symmetrical converter, only the first six intervals ($t_0 \text{through} t_5$) will be discussed here to indicate how the proposed method works. The magnetizing inductance L_m in the transformer as shown in Fig. 6 is designed to have a large value so that the magnetizing current in the transformer can be greatly reduced. Therefore, the magnetizing inductance and current is ignored from the following discussion to simplify the analysis.

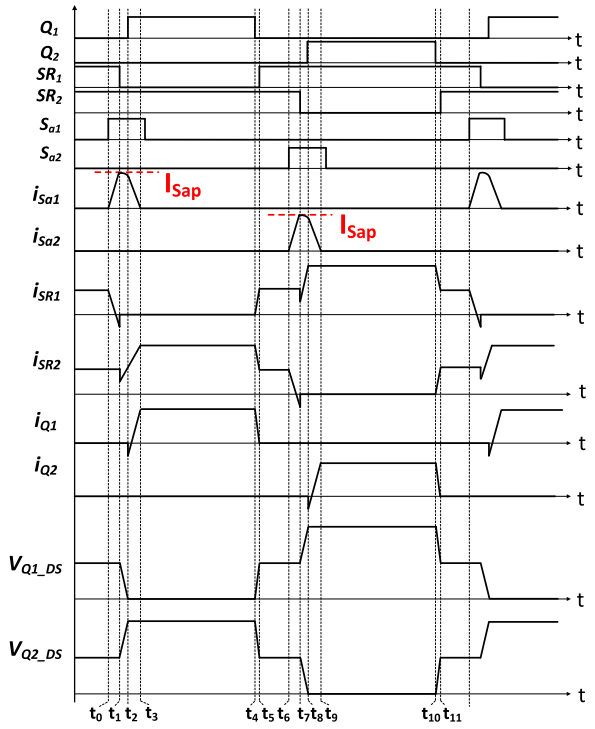


Fig. 7. Operational waveform of the proposed soft-switching method for a half-bridge current doubler.

The equivalent circuits and current directions of the converter are shown in Fig. 8 for each operation interval. The detailed operation principle will be discussed for each interval. Only the switching losses of MOSFETs in the converter are discussed, as the conduction losses and gate driving losses of the power stage MOSFETs are the same as in a conventional half-bridge current doubler. The auxiliary components losses will be discussed in Section V.

A. Interval 1: t_0 to t_1

Before t_0, two inductor currents i_{L1} and i_{L2} are freewheeling through SR_1 and SR_2 as in Fig. 8(a). At time t_0, S_{a1} is turned ON, then a positive voltage is applied across L_a as indicated in Fig. 8(b), and auxiliary current in the direction of the arrow in Fig. 8(b) starts to build up. S_{a1} is turned ON with zero current switching. Based on KCL, the sum of i_{SR1} and i_{Sa1} is equal to the current i_{L1} at any given time; therefore, the current flowing through SR_1 is transferring to the auxiliary inductor L_a. In order to achieve ZVS of primary-side devices and avoid reverse-recovery loss of SRs' body diode, the current direction of i_{SR1} needs to be negative with respect to the current direction shown in Fig. 8(b) when SR_1 is being turned off. The current flowing through the auxiliary inductor can be calculated as in (1), which clearly indicates the current in the auxiliary inductor depends not only on the inductance value but also the time when both SR_1 and S_{a1} are ON. This helps in the design of the proposed load-dependent ZVS method and will be further discussed in a later section

$$i_{\rm sa} = \frac{V_o - V_{F\_D}}{L_a}\ (t - t_0) \tag{1}$$

where V_o is the output voltage and V_{F_D} is the forward voltage drop of the auxiliary diode.

B. Interval 2: t_1 to t_2

At time t_1, SR_1 is turned OFF with the equivalent circuit shown in Fig. 8(c). As the current is flowing from drain to source when SR_1 is turned OFF, the body diode conduction of SR_1 is prohibited together with the reverse-recovery current and loss. Yet, active turn-off loss occurs in the SR_1. Equation (2) is the turn-off loss of SR_1, as a part of the current is used to charge the junction capacitance where no loss is involved, that portion is taken out of the turn-off loss of SR_1. By designing the difference between $(I_{\rm sap} - \frac{1}{2}I_o)$ as small as possible, the actual turn-off losses of *SR* devices are also kept at the minimum value

$$P_{SR\rm off} = \frac{1}{2}V_{\rm SR}\left(I_{\rm sap} - \frac{1}{2}I_o\right)t_{\rm off,sw}f_s - \frac{1}{2}V_{\rm SR}^2 C_{\rm SR} f_s. \tag{2}$$

At the instant SR_1 is turned OFF, the current in the auxiliary inductor is larger than the current in the output inductor. The difference between the two currents is forced to flow through the capacitances in the converter including SR_1, Q_1, and Q_2. The current and voltage relationship during this interval can be expressed as (3) to (6). As indicated in (5), a larger difference between $I_{\rm sap}$ and $\frac{1}{2}I_O$ leads to a faster discharging of voltage across Q_1, which means ZVS can be achieved for a shorter period of resonance

$$\omega_o = \sqrt{\frac{1}{L_{\rm eq}C_{\rm eq}}} \tag{3}$$

$$Z_o = \sqrt{\frac{L_{\rm eq}}{C_{\rm eq}}} \tag{4}$$

$$\begin{aligned} v_{Q1\_\rm DS} = {} & V_{\rm in} - V_o\left(n^2 + \cos\omega_o\left(t - t_1\right)\right)\frac{Z_o - \omega_o L_a}{Z_o} \\ & - \frac{Z_o}{\omega_o^2 C_{\rm SR} L_{\rm leak} + \frac{C_{\rm SR}}{C_{\rm pri}} + 1}\left(I_{\rm sap} - \frac{1}{2}I_o\right) \\ & \times \sin\omega_o\left(t - t_1\right) \end{aligned} \tag{5}$$

$$\begin{aligned} i_{\rm La} = {} & I_o + \frac{V_o}{Z_o}\sin\omega_o\left(t - t_1\right) + \left(I_{\rm sap} - \frac{1}{2}I_o\right) \\ & \times \cos\omega_o\left(t - t_1\right) \end{aligned} \tag{6}$$

where $L_{\rm eq} = L_a + \frac{L_{\rm leak}}{n^2}$, $C_{\rm eq} = \frac{2n^2 C_{\rm pri} C_{\rm SR}}{C_{\rm SR} + 2n^2 C_{\rm pri}}$, and $C_{\rm pri}$ is the junction capacitances of primary MOSFETs, $C_{\rm SR}$ is the junction capacitance of SR MOSFETs, ω_o and Z_o is the resonant frequency and impedance of the *LC* components, respectively.

If Q_1's turn-on signal still has not arrived when the voltage is discharged to zero, the body diode of Q_1 starts to conduct as shown in Fig. 8(d), which is not preferred, as extra body diode conduction loss is being introduced [30] and efficiency is compromised.

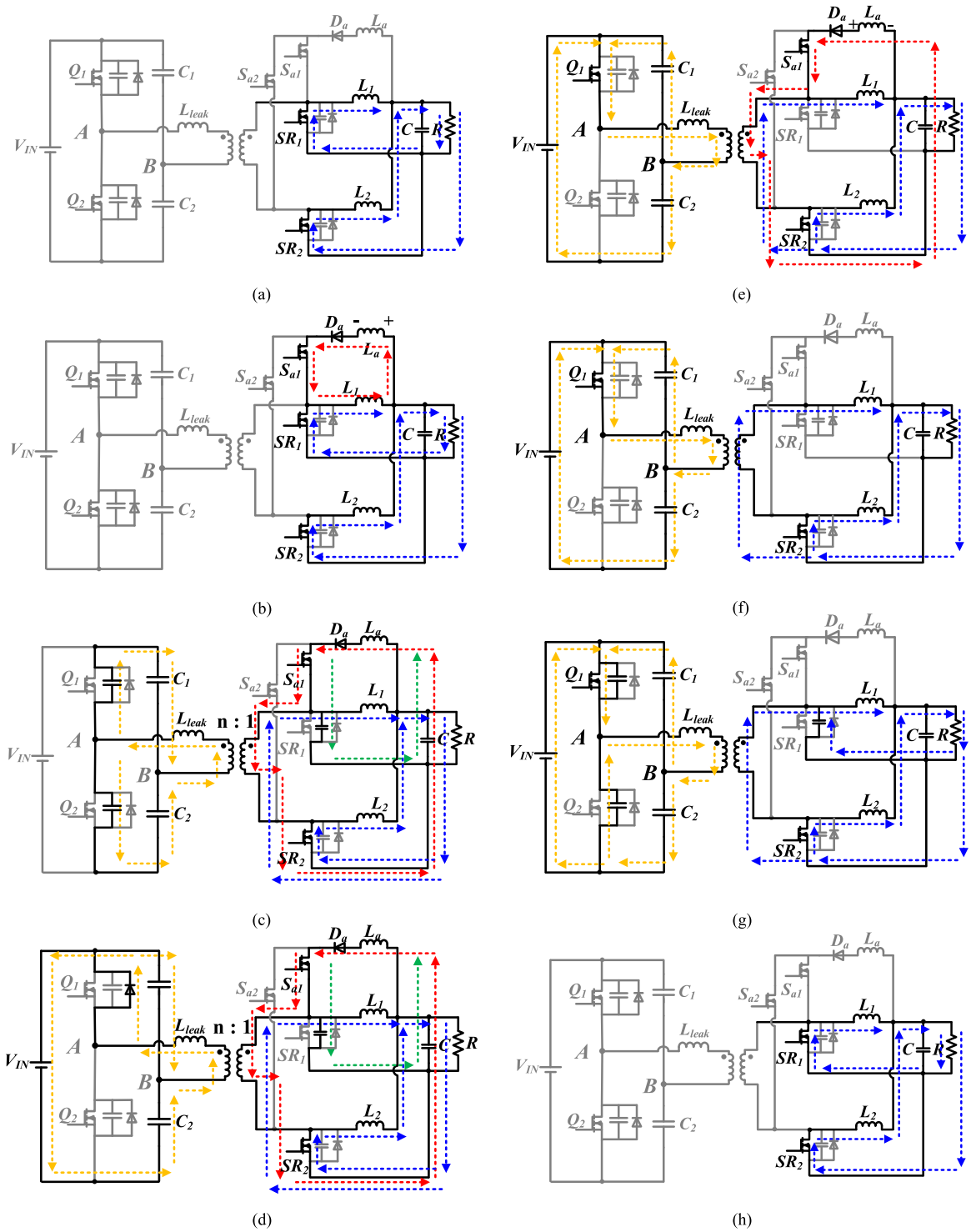


Fig. 8. Equivalent circuits of soft-switching half-bridge current doubler. (a) Prior to t_0, (b) t_0–t_1, (c) t_1–t_2, (d) primary body diode conduction in t_1–t_2, (e) t_2–t_3, (f) t_3–t_4, (g) t_4–t_5, and (h) t_5–t_6.

C. Interval 3: t_2 to t_3

At time t_2, Q_1 is turned ON with zero voltage across it as shown in Fig. 8(e). When Q_1 is conducting, a positive voltage is applied across the transformer while a negative voltage is applied across L_a (the direction is marked in Fig. 8(e)). Therefore, the current in auxiliary inductor starts to reduce linearly as (7). When the current reaches zero, the diode D_a starts to block the voltage and stops conducting current. Clearly, S_{a1} can be turned OFF with zero current through it. The time for the current to reduce to zero can be calculated based on (7) as well. At the same time when S_{a1} stops conduction, the current through Q_1 reaches the inductor current reflected to the primary side

$$i_{\mathrm{sa}} = I_{\mathrm{sat2}} - \frac{\frac{V_{\mathrm{in}}}{2n} - V_o - V_{D_a}}{L_a}(t - t_1) \tag{7}$$

where $I_{\mathrm{sat}2}$ is current in auxiliary inductor at time t_2.

D. Interval 4: t_3 to t_4

During this interval, the converter's operation is the same as the conventional half-bridge current doubler as presented in Fig. 8(f), and the energy is transferring from primary to secondary side. The duration of this interval can be calculated as in (8). Both of the two inductor currents are freewheeling through SR_2

$$t = \left(\frac{2nV_o}{V_{\mathrm{in}}}\right) \times T_s \tag{8}$$

E. Interval 5: t_4 to t_5

At time t_4, Q_1 is turned OFF. The actual turn-off loss can be calculated in (9) where the current charging the junction capacitances is not included the turn-off loss of Q_1 and is being subtracted. For high-input voltage low-input current application here, the actual turn-off losses of Q_1 and Q_2 are much smaller compared with *VI* product calculation as in (9). Also, the actual turn-off losses of Q_1 and Q_2 are smaller than the extra auxiliary components loss if the snubber capacitor was added in parallel with Q_1 and Q_2 to eliminate the turn-off loss as in [25]–[29] for high-input voltage low-input current application

$$P_{\mathrm{prioff}} = \frac{1}{4} V_{\mathrm{in}} I_{\mathrm{off}} t_{\mathrm{off,sw}} f_s - V_{\mathrm{in}} Q_{\mathrm{oss}} f_{\mathrm{sw}} \tag{9}$$

where I_{off} is the current value of Q_1 is turned off and $t_{\mathrm{off,SW}}$ is the turn-off transition time which is found by Saber simulation.

The body diode of SR starts to conduct when the channel of Q_1 starts turning OFF.

F. Interval 6: t_5 to t_6

From time t_5, SR_1 is turned on with zero voltage across it. The converter enters the free-wheeling period, which is the same as the time interval before t_o and Q_2 and SR_2 will be switched for next half-switching cycle. Because of symmetry of the half-bridge current doubler operation, the rest of the switching intervals will not be discussed here.

Even though ZVS can be obtained and switching losses and reverses-recovery loss are eliminated based on the discussion in this section, extra auxiliary components losses occur to the converter. In the next section, the auxiliary losses are analyzed and the method to improve light-load efficiency is discussed.

IV. Load-Dependent Charging Time Analysis and Controller Design

A. Losses Under Constant Charging Time of Auxiliary Inductor

Based on earlier discussion in Section II, the intervals 1 and 2 are the key transitions to realize zero-voltage turn on of primary MOSFETs. During interval 1, energy is stored in the auxiliary inductor, which is released to junction capacitances during interval 2. The current in the auxiliary inductor is discharged during interval 3. Energy losses will occur during the interval charging and discharging the auxiliary inductor, mainly conduction loss of auxiliary MOSFETs and diode which can be calculated as in (10) and (11), receptively. The auxiliary inductor (L_a) is an air core inductor formed with printed circuit board (PCB) traces which will be discussed in detail in a later section; therefore, the conduction losses of L_a is ignored here

$$P_{\mathrm{AUX\_}M} = 2I^2_{\mathrm{RMS\_AUX}} R_{\mathrm{AUX\_}M} \tag{10}$$

$$P_{\mathrm{AUX\_}D} = 2I^2_{\mathrm{RMS\_AUX}} \times R_{\mathrm{AUX\_}D} + 2I_{\mathrm{AVG\_AUX}} \times V_{F\_D} \tag{11}$$

where $I_{\mathrm{RMS_AUX}}$ and $I_{\mathrm{AVG\_AUX}}$ are the RMS and average value of auxiliary current, which can be further calculated in (12) and (13), and $R_{\mathrm{AUX\_M}}$ is the on-state resistance of the auxiliary MOSFETs and V_{F_D} and $R_{\mathrm{AUX\_}M}$ are the forward voltage drop and resistance of the auxiliary diode. Usually the resonant duration is much shorter than the charging and discharging period; therefore, the current value is assumed to be constant from t_1 to t_2

$$\begin{aligned} I_{\mathrm{RMS_{AUX}}} &= \sqrt{\left(\frac{\boldsymbol{I^2_{sap}}\left((\boldsymbol{t_3}-\boldsymbol{t_2})+3\left(\boldsymbol{t_2}-\boldsymbol{t_1}\right)+\left(\boldsymbol{t_1}-\boldsymbol{t_0}\right)\right)}{3\boldsymbol{T_s}}\right)} \\ &= \sqrt{\left(\frac{\boldsymbol{I^2_{sap}}\left(t_c+3t_r+t_{\mathrm{dc}}\right)}{3\boldsymbol{T_s}}\right)} \end{aligned} \tag{12}$$

$$\begin{aligned} I_{\mathrm{AVG\_AUX}} &= \frac{I_{\mathrm{sap}}\left((\boldsymbol{t_3}-\boldsymbol{t_2})+2\left(\boldsymbol{t_2}-\boldsymbol{t_1}\right)+\left(\boldsymbol{t_1}-\boldsymbol{t_0}\right)\right)}{2\boldsymbol{T_s}} \\ &= \frac{I_{\mathrm{sap}}\left(\left(t_c+2t_r+t_{\mathrm{dc}}\right)\right)}{2\boldsymbol{T_s}} \end{aligned} \tag{13}$$

where $t_c, t_r,$ and t_{dc} are the charging time, resonance time, and discharging time of the auxiliary inductor, which is the time duration from t_0 to t_1, t_1 to t_2, and $t_2$tot_3 in Fig. 7, respectively.

For the on-board power supplies, the electric loads demand high current (30 A) at low voltage (1 V), which means a considerable amount of current is flowing through the auxiliary components to achieve ZVS, making the losses in auxiliary components nonnegligible. When the charging timing of the auxiliary inductor is determined and being fixed, the losses of auxiliary components are also fixed regardless of the loading condition of the converter. The constant auxiliary components' losses mean the percentage of the auxiliary components' losses increases as load decreases. Therefore, the light-load efficiency is compromised by the constant charging time method.

In the meantime, the constant auxiliary components' loss is not the only factor that worsens the light-load efficiency, the SR devices turn-off losses also increase as load decreases. Fig. 9 presents the theoretical current waveforms of the output inductor, SR device, and auxiliary inductor with constant charging time of the auxiliary inductor. It clearly indicates that as load reduces, the SR devices are turned off with a larger current through them, resulting in an increased turn-off loss when load is lighter as in (2).

At the same time, if a constant dead time is implemented in the converter, the conduction period of primary MOSFETs' body diode is longer as the load becomes lighter. As indicated in (5), a larger difference between I_{sap} and $\frac{1}{2}I_O$ leads to a faster discharging of junction capacitances. Therefore, the converter

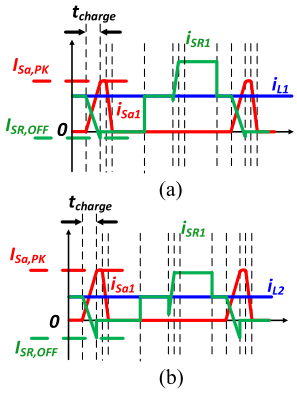


Fig. 9. SR waveforms under different load conditions with constant charging time method. (a) Heavy load. (b) Light load.

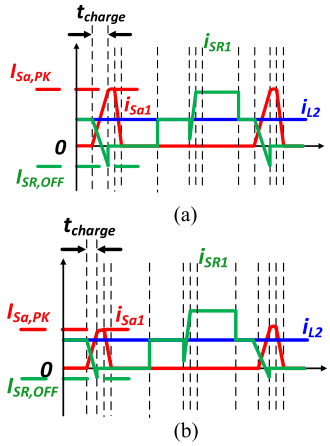


Fig. 10. SR waveforms under different load conditions with load-dependent charging time method.

experiences an increased body diodes conduction loss as load reduces. Adjusting the dead time can solve this issue, but it increases the complexity of the controller.

B. Proposed Load-Dependent Charging Time Method

The essential part to realize ZVS of primary-side MOSFETs is the resonance between MOSFET junction capacitances and auxiliary inductance between t_1 and t_2 discussed in the last section. In order to achieve ZVS, the energy stored in the auxiliary inductance must be equal or greater than the energy stored in the output junction capacitances of MOSFETs expressed as

$$\frac{1}{2}L_{\rm sa}\left(I_{\rm sap}-\frac{1}{2}I_O\right)^2 \geq \frac{1}{2}C_{\rm pri}V_{\rm in}^2+C_{\rm SR}V_{\rm SR}^2. \tag{14}$$

As (14) indicates, the energy stored in the auxiliary inductor is related to the difference between the auxiliary current and output current. Therefore, the optimal design with minimum auxiliary losses is that energy stored in the auxiliary inductor equals to the energy stored in the junction capacitances in all the load conditions. Therefore, the optimum design is to keep a constant$(I_{\rm sap}-\frac{1}{2}I_O)$, which means when load current reduces, $I_{\rm sap}$ reduces correspondingly. For a given auxiliary inductance, it means a shorter charging time of the auxiliary inductor. The desired charging current and corresponding charging time can be calculated as in (15) and (16), which clearly indicates that to store the same amount of energy in the auxiliary inductor as in the junction capacitances, the charging current and charging time is related to the load condition

$$I_{\rm sap}=\sqrt{\frac{C_{\rm pri}V_{\rm in}^2+2C_{\rm SR}V_{\rm SR}^2}{L_{\rm sa}}}+\frac{1}{2}I_O \tag{15}$$

$$t_{\rm charge}=L_{\rm sa}\left(\sqrt{\frac{C_{\rm pri}V_{\rm in}^2+2C_{\rm SR}V_{\rm SR}^2}{L_{\rm sa}}}+\frac{1}{2}I_O\right)\Big/V_o-V_{F\_D}. \tag{16}$$

Fig. 10 is the theoretical current waveforms of output inductor, SR devices, and auxiliary inductor with the proposed load-dependent control. When the output inductor current reduces, the auxiliary MOSFET is triggered to turn on later, which

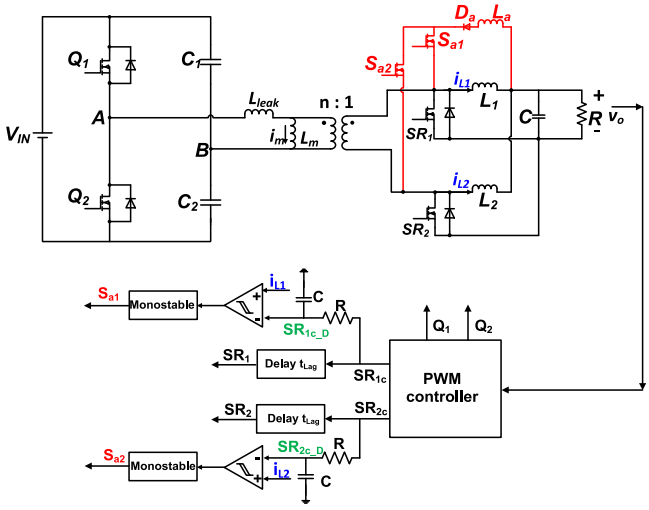


Fig. 11. Control scheme of a load-dependent soft-switching method.

means the auxiliary inductor is charged for a shorter period of time ($t_{\rm charge}$). The difference between the auxiliary inductor and output inductor current is constant regardless of the load. Therefore, the losses in the auxiliary circuit are reduced, the turn-off loss of SR devices is not increasing, and the constant dead time can be used in the converter as the load reduces in the proposed method.

After the necessity of adjusting the charging time being established, Fig. 11 indicates the controller design of the load-dependent ZVS method, and Fig. 12 illustrates the key waveforms of the controller. A commercial half-bridge controller IC (UCC 28250) is used to generate the control signals Q_1, Q_2, SR_{1C}, and SR_{2C}. A large dead time between SR devices' turn off (SR_{1C} and SR_{2C} in Fig. 11) and primary devices' turn on (Q_1 and Q_2 in Fig. 11) is programmed on the controller IC so that the falling edges of SR_{1C} and SR_{2C} can be used to generate gate signals for S_{a1} and S_{a2}. In order to consider the load condition, a comparator between inductor current (i_{L1} and i_{L2} in Fig. 11) and the *RC* delayed falling edge (SR_{1C_D} and SR_{2C_D} in Fig. 11) is used to generate the turn-on

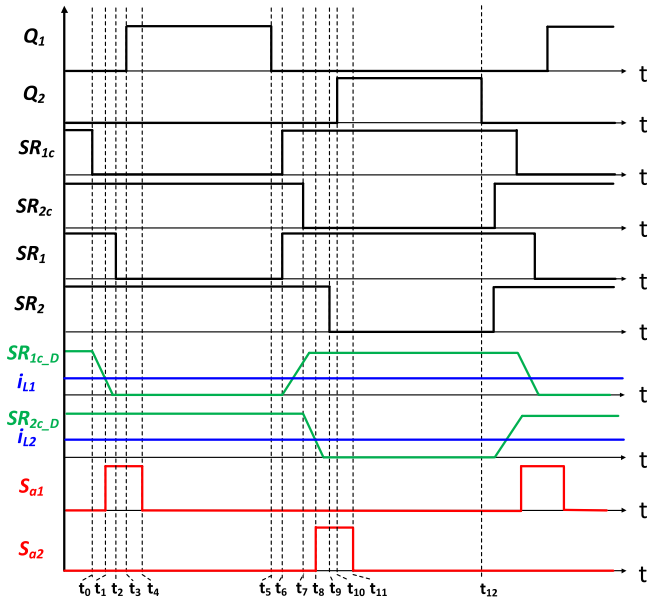


Fig. 12. Gate signal sequence for a load-dependent soft-switching half-bridge current doubler.

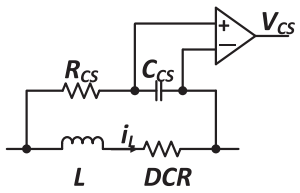


Fig. 13. DCR current sensing of an output inductor current.

signal for S_{a1} and S_{a2}. A larger load leads to a sooner cross over between SR_{1C_D} and I_{L1} (same for SR_{2C_D} and I_{L2}) which will trigger the comparator sooner to create a longer charging time of L_a. The multivibrator is set to be rising edge triggering; therefore, the rising edge of the comparator (when I_{L1} becomes larger than SR_{1C_D} as t_1 in Fig. 12) will trigger the multivibrator to turn on for a given time, the falling edge (whenI_{L1} becomes smaller than SR_{1C_D} as between t_6 and t_7 in Fig. 12) will not trigger the multivibrator. Also, a falling edge delay circuit is implemented so that SR_1 and SR_2 will have a suitable dead-time.

As indicated in Fig. 11 and 12, the inductor current or load current information is necessary to adjust the charging time of the auxiliary inductor. DCR current sensing method (shown in Fig. 13), which is widely adopted for the on-board power supplies, is implemented for the half-bridge current doubler [31]–[33]. The DCR is the dc equivalent resistance of the inductor, which is not added to the circuit as an extra sensing resistor.

When $R_{\rm CS}\ C_{\rm CS} = L/{\rm DCR}$ is satisfied, the voltage across the capacitor, $C_{\rm CS}$, is proportional to the inductor current as (17). Then, the signal is fed to an op amp to get larger signal and become the positive input to the comparator. Therefore, the current information can be obtained with no extra component losses.

$$v_{\rm CS} = {\rm DCR} * i_L \tag{17}$$

TABLE I
SPECIFICATION OF HALF-BRIDGE CURRENT DOUBLER

Parameter	Value/Part number
Input voltage	66 V
Output voltage	1 V
Output power	30 W
Output current	30 A
Switching frequency	280 kHz

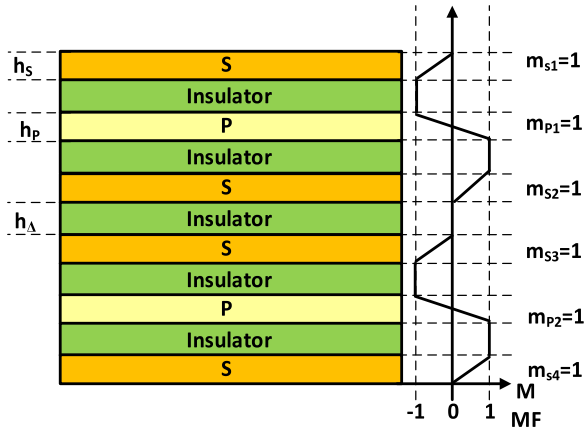


Fig. 14. Interleaved winding structure.

V. CONVERTER DESIGN FOR THE PROPOSED METHOD

A. Power Stage Design

A laboratory prototype has been designed and built to verify the proposed method. The system specifications of half-bridge current doubler are listed in Table I. Under 280-kHz switching frequency, the skin depth of copper used in the planer transformer is around 140 μm (4 oz); therefore, by using 4-oz copper in the planar transformer, the copper depth can be fully utilized [34], [35].

The transformer is designed with PCB winding at 6:1 primary to secondary turns ratio. The winding is designed with primary- and secondary-side interleaved as shown in Fig. 14 [34], [35] to reduce the leakage inductance in the half-bridge current doubler which causes resonance with the junction capacitances. Non-gapped cores are used to obtain large magnetizing inductance to limit the magnetizing current as discussed earlier. Planar cores E/PLT core E 14/3.5/5 and PLT 14/5/1.5 are selected with 4-oz (140 μm) copper windings. The leakage inductance and ac resistance is 63 nH and 76 mΩ at switching frequency, respectively, as presented in Fig. 15. For the symmetrical-controlled half-bridge current doubler, the leakage inductance resonates with the primary MOSFETs' output junction capacitances when both SR MOSFETs are in conduction. The energy earlier stored in the leakage inductance is eventually lost in the circuit during the ringing process; therefore, it is essential to design the transformer with small leakage inductance to reduce the resonant losses. With interleaved winding and the actual leakage inductance around 63 nH, the leakage inductance energy losses ($L_{\rm leak} I_{\rm off}^2 f_{\rm sw}$) can be calculated as 0.22 W under full load

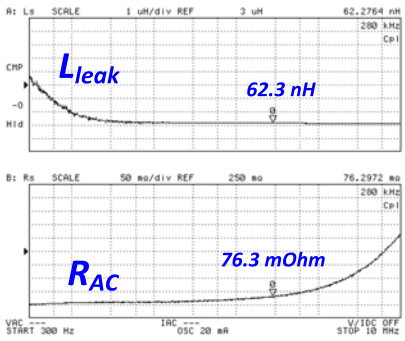


Fig. 15. Measured transformer leakage inductance and ac resistance.

TABLE II
COMPONENTS IN HALF-BRIDGE CURRENT DOUBLER

Components	Part number/Value
Q_1 and Q_2	AON7296
SR_1 and SR_2	BSC010NE2LS
S_{a1} and S_{a2}	BSZ036NE2L
D_a	DSS40-0008D
C_1 and C_2	4.7 μH
Output inductor	220 nH
Output capacitor	500 μF

(30 W), which corresponds to 5.6% of the converter's total loss under full load. As load reduces, the leakage inductance losses would become even less compared with other losses.

Other components including primary- and secondary-side MOSFETs, output inductors, and capacitors used in the half-bridge current doubler are listed in Table II.

B. Auxiliary Circuit Design

The auxiliary inductance together with the charging time (duration $(t_1 - t_0)$ in Fig. 7) determines the auxiliary current ($I_{\rm sap}$ in Fig. 7) and then determines if energy stored in the auxiliary inductor ($\frac{1}{2}L_{\rm sa}(I_{\rm sap} - \frac{1}{2}I_O)^2$) is enough to discharge the junction capacitances completely for the primary MOSFETs. Therefore, the value of the auxiliary inductance is not strictly defined because the charging time can be adjusted to accommodate the actual value of the auxiliary inductance in order to store enough energy.

Fig. 16 shows the relationship of the auxiliary inductance and the ratio of $I_{\rm sap}$ toI_L in order to have enough energy stored. Then, the charging time can be calculated correspondingly as presented in (1). Since the auxiliary inductance is in the range of nanohenry, an air core inductor from turns formed on a PCB with traces is designed. The actual auxiliary inductance based on an impedance analyzer's measurement is 32 nH.

Unlike the buck converter, the leakage inductance ($L_{\rm leak}$) is a part of the resonant network in the half bridge; therefore, it impacts the ZVS behavior of the primary-side devices.–Fig. 17 shows the equivalent circuit during the resonant period (t_2–t_1) and Fig. 18 shows the relationship between the minimum duration of this interval (t_2–t_1) and the ratio of leakage inductance

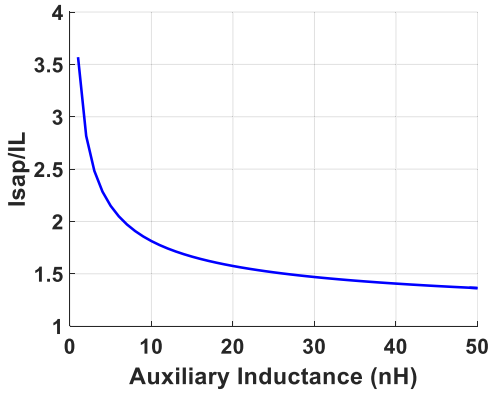


Fig. 16. Relationship between auxiliary inductance and the ratio between desired auxiliary charging current and output inductor's current.

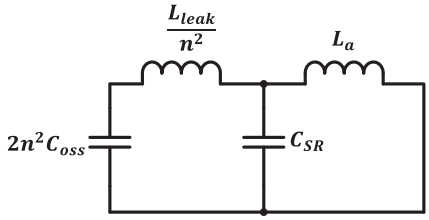


Fig. 17. Equivalent resonant circuit during interval 2 (as in Fig. 7).

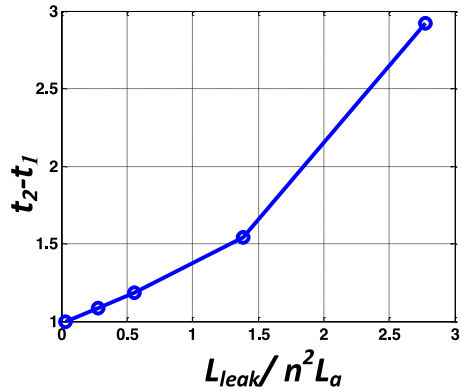


Fig. 18. Relationship between the leakage inductance and resonance time (t_2–t_1) in Fig. 7.

to the auxiliary inductance reflected to the primary side ($L_{\rm leak}/n^2L_{\rm a}$) with zero leakage inductance being unity based on Saber simulation. As a high step-down converter with large transformer turns ratio, the leakage inductance needs to be much larger compared with the auxiliary inductance to impact the resonance. Based on the prototype measured, $L_{\rm leak}/n^2L_{\rm a}$ is less than 0.1, which means it has very limited impact on the resonance. Schottky diode DSS40-0008D and MOSFET BSZ036NE2L are selected as the auxiliary diode and MOSFET, respectively.

C. Loss and Efficiency Comparison Between Proposed and Conventional Method

As discussed earlier, the proposed method can eliminate the turn-on loss of the primary MOSFETs (calculated in (18)) and the body diode reverse-recovery loss of SR MOSFETs

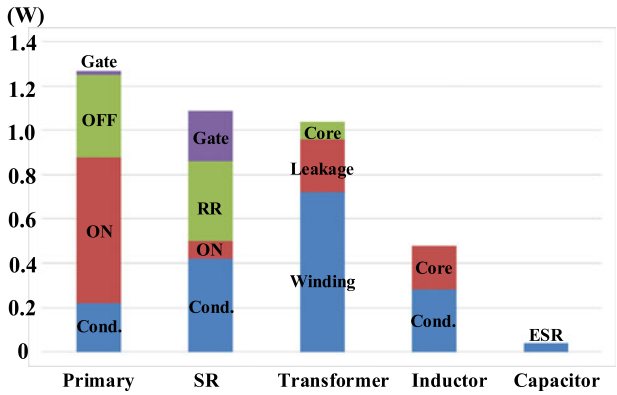


Fig. 19. Loss breakdown of a hard-switching half-bridge current doubler under full-load condition (30 W).

(calculated in (19)), both of which are illustrated in the loss breakdown diagram in Fig. 19. However, at the same time, some other losses are also added to the circuit including the SR MOSFETs active turn-off losses of the main power stage (calculated in (20)); and the auxiliary components losses that includes the conduction losses of auxiliary MOSFETs and diode which can be as in (10) and (11), the gate driver loss, and the turn-on capacitive loss of auxiliary MOSFETs which can be calculated in (21) and (22), respectively. Therefore, it is necessary to compare the losses eliminated by the proposed soft-switching method and losses added to the circuit by the auxiliary components to prove the proposed method can improve the efficiency of the half-bridge current doubler

$$P_{\mathrm{on}\_p} = \frac{1}{4n}V_{\mathrm{in}}\left(\frac{1}{2}I_o - \Delta I + \frac{I_{\mathrm{rr}}}{n}\right)\left(t_{\mathrm{ir}} + t_{\mathrm{vf}}\right) f_{\mathrm{sw}} + V_{\mathrm{in}} Q_{\mathrm{oss}} f_{\mathrm{sw}} \tag{18}$$

$$P_{\mathrm{rr}} = \frac{V_{\mathrm{in}}}{n} Q_{\mathrm{rr}} f_{\mathrm{sw}} \tag{19}$$

$$P_{\mathrm{off}\_SR} = \frac{1}{4n}V_{\mathrm{in}}\left(\frac{1}{2}I_o + \Delta I\right)\left(t_{\mathrm{if\_SR}} + t_{\mathrm{vr\_SR}}\right) f_{\mathrm{sw}} - \frac{1}{n}V_{\mathrm{in}} Q_{\mathrm{oss\_SR}} f_{\mathrm{sw}} \tag{20}$$

$$P_{\mathrm{gate\_AUX}} = 2V_{\mathrm{Drive\_AUX}} \times Q_{g\_\mathrm{AUX}} \times f_{\mathrm{sw}} \tag{21}$$

$$P_{\mathrm{on\_AUX}} = \left(\frac{V_{\mathrm{in}}}{n} - V_{\mathrm{out}}\right) \times Q_{\mathrm{oss\_AUX}} \times f_{\mathrm{sw}} \tag{22}$$

where I_{rr} is the reverse-recovery current of SR MOSFETs, which is added to the turn-on current of the primary-side MOSFETs during the turn on transition of the primary MOSFETs. ΔI is the current ripple. t_{ir} and t_{vf} are the current rising time and voltage falling time during turn on transient of primary MOSFETs, both of which are obtained from Saber simulation. Q_{oss} is the output charge of primary MOSFETs. Q_{rr} is the reverse-recovery charge of the SR MOSFETs body diode. $t_{\mathrm{if\_SR}}$ and $t_{\mathrm{vr\_SR}}$ are the current falling time and voltage rising time during turn off transient of SR MOSFETs, both of which are also obtained from Saber simulation. $Q_{\mathrm{oss\_SR}}$ is the output charge of the SR MOSFETs, $V_{\mathrm{drive\_AUX}}$ is the gate driver's high level voltage of auxiliary MOSFETs, $Q_{\mathrm{g\_AUX}}$ is the gate charge of the auxiliary MOSFETs, and $Q_{\mathrm{oss\_AUX}}$ is the output charge of the auxiliary MOSFETs.

TABLE III
LOSSES AND EFFICIENCY COMPARISON BETWEEN PROPOSED AND CONVENTIONAL METHOD

		30 W	18 W	6 W
Conventional metdod	Primary MOSFETs turn-on (W)	0.66	0.48	0.17
	SR MOSFETs loss (W)	0.32	0.19	0.08
Proposed method	Auxiliary MOSFETs (W)	0.17	0.15	0.11
	Auxiliary diode (W)	0.16	0.10	0.04
	SR MOSFETs turn off (W)	0.09	0.09	0.09
Losses reduction	(conventional method—proposed method) (W)	0.56	0.33	0.01
Efficiency improvement	(percentage point)	1.87	1.83	0.17

Since the other losses, such as transformer winding and core losses, conductive and gate driving losses for the power MOSFETs, and output inductor and capacitor are hardly being impacted by the proposed method; therefore, the losses of those components are not included for the loss and efficiency comparison between the proposed method and conventional hard-switching method as listed in Table III. The losses of the conventional hard switching half-bridge current doubler differing from the proposed method are the turn-on losses of primary MOSFETs and the body diode reverse-recovery losses of the SR MOSFETs. The proposed method eliminates these two losses, yet it introduces other losses which are also listed in Table III as discussed earlier. The benefit of the proposed method is the difference between the reduced main power stage components losses in the conventional hard-switching converter and the extra loss with the auxiliary components in the proposed method. Even though the conduction losses of the auxiliary MOSFETs and diode reduce as load reduces, the gate driving and turn-on capacitive losses stay almost constant under different load conditions, which sacrifice the light-load efficiency improvement as indicated in Table III. From Table III, it is also clear that if the charging time of the auxiliary circuit keeps constant, the light-load efficiency would be poorer compared with the proposed load-dependent methods.

VI. EXPERIMENTAL VERIFICATION

Based on the schematic of the proposed method in Fig. 6, the gate of the auxiliary MOSFETs is connected to the drain of SR MOSFETs, which means a floating gate driver is required. However, as the specification indicates the drain voltage of the SR MOSFETs is below 6 V, therefore a 12 V driving voltage directly connected to ground is used in this paper. Even when the SR MOSFET is off, there is still enough gate voltage to keep the auxiliary MOSFETs on with a slightly higher $R_{\mathrm{ds(on)}}$. The complexity of the gate driver circuit is greatly reduced.

Fig. 20 through Fig. 25 show the ZVS of primary-side MOSFETs under different load conditions with the proposed load-dependent ZVS method as the drain to source voltage (V_{ds}) has been discharged to zero before the arrival of gate voltage(V_{gs}). Neither the MOSFETs' current nor the auxiliary inductor's

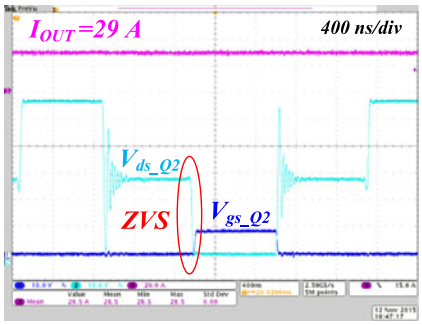


Fig. 20. ZVS for primary device with 29-A load current.

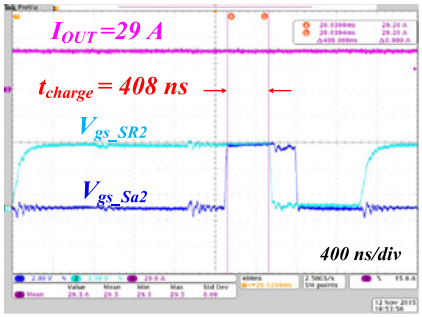


Fig. 21. Charging time for auxiliary inductor with 29-A load current.

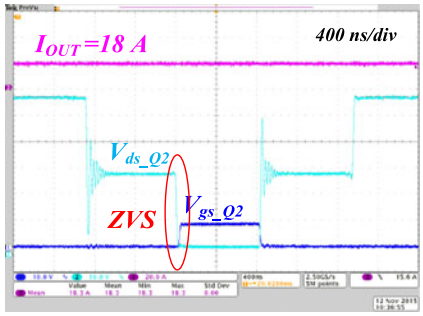


Fig. 22. ZVS for primary device with 18-A load current.

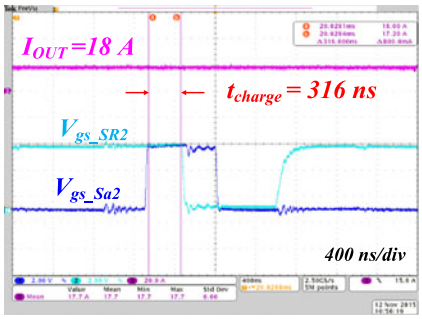


Fig. 23. Charging time for auxiliary inductor with 18-A load current.

current are measured in the experiments directly, mainly because measuring the currents would introduce extra inductance to the circuit. As the leakage inductance of the transformer is 60 nH and auxiliary inductance is around 30 nH, therefore the measuring wire's inductance would make a difference. The charging time is indicated by the overlap between secondary-side devices' ($V_{\mathrm{gs\_SR2}}$) and auxiliary devices' gate signal ($V_{\mathrm{gs\_sa2}}$) as the auxiliary inductor is only being charged when both of them are on. From the experimental results, it can be clearly seen that ZVS of primary-side devices can be achieved over a wide load range, and the charging time is dependent on the load condition as shown in Figs. 21, 23, and 25. which prevents charging the auxiliary inductor to an unnecessarily large value and increasing conduction loss of the auxiliary MOSFETs and diode and turn-off loss of SR devices as in the constant charging time method.

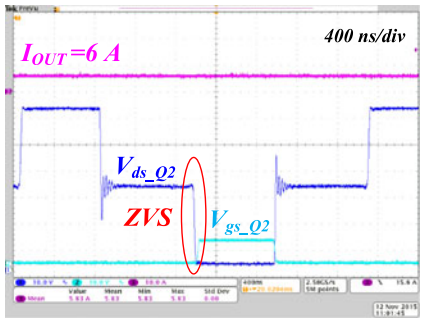


Fig. 24. ZVS for primary device with 6-A load current.

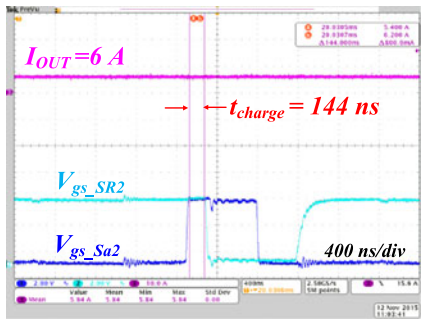


Fig. 25. Charging time for auxiliary inductor with 6-A load current.

In the meantime, constant dead time is implemented in the controller for all the loading conditions. It can be seen the junction capacitances can be completely discharged and almost no body diode conduction of primary-side MOSFET regardless of the load conditions as illustrated in Figs. 20, 22, and 24.

Fig. 26 illustrates the charging time of the auxiliary inductor under different load conditions based on experimental testing. The charging time reduces when load reduces as designed. One thing to notice is that in the experiments, it actually requires longer charging time to achieve ZVS in all the load conditions; therefore, longer charging time is implemented in the experiment compared with analysis. However, this difference does not impact the load-dependent operation; it simply means a larger I_{sap} is needed to obtain ZVS under all load conditions. The longer required charging time is because of the parasitics in the converter which are not being considered in calculation.

Fig. 27 shows the efficiency comparison among different control methods, including conventional hard switching, constant charging time of the auxiliary inductor which is obtained un-

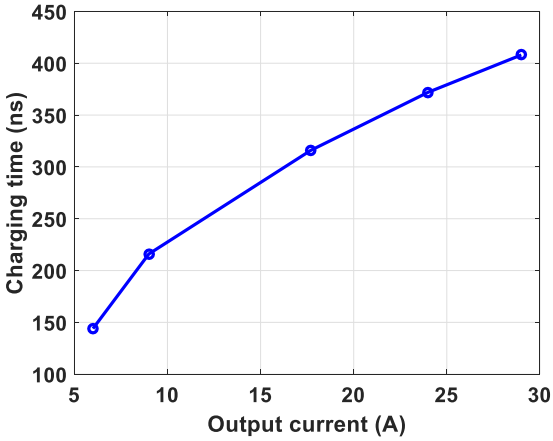


Fig. 26. Experimental charging time under different load conditions.

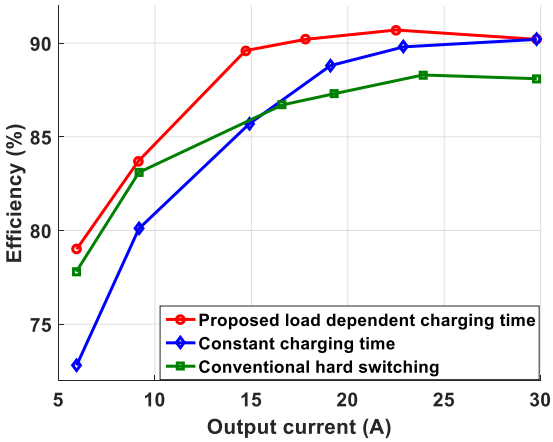
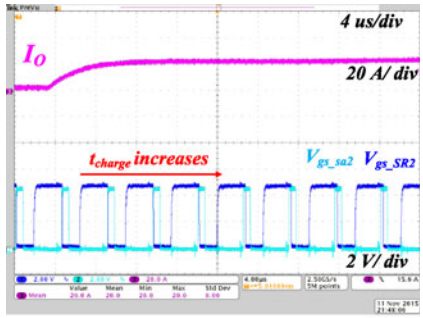


Fig. 27. Experimental efficiency comparison among the proposed load-dependent charging time, constant charging time, and conventional hard switching.

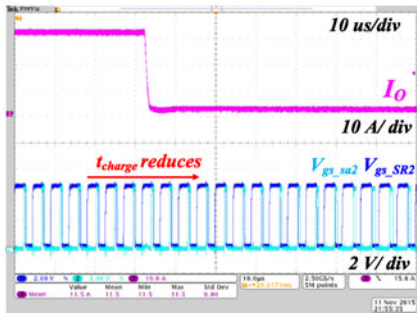
der full-load condition, and proposed load-dependent charging method. Dead time between primary- and secondary-side devices is not being adjusted based on load condition for all three cases. It clearly shows that the proposed method has higher efficiency compared with the other two methods in a wide load range.

Fig. 28 shows the transient performance of the proposed method when load changes. The time scale for load step up is 4 μs/div and for load step down is 10 μs/div. Charging time (t_{charge}) is indicated by the overlap of ON signal between the auxiliary MOSFET ($V_{\mathrm{GS\_Sa2}}$) and SR MOSFET ($V_{\mathrm{GS\_SR2}}$). It can be seen that the charging time changes with the load current changing automatically. It takes several switching cycles for the control to respond to the load change, mainly because inductor current is used for the load condition in the controller, which is not as fast as the output current to the load. However, after several switching cycles, the proposed method can adjust the charging time to a desired value and offers a higher efficiency compared with the constant charging time method.

Based on the experimental results, the proposed load-dependent ZVS method can improve the efficiency of the half-bridge current doubler compared with both hard-switching and



(a)



(b)

Fig. 28. Transient of the proposed load-dependent charging method. (a) Load stepping up. (b) Load stepping down.

constant charging time method. Also, the proposed controller can adjust the charging time automatically when the load changes.

Even though the method is proposed for the half-bridge current doubler in the HV POL converter in power supplies for data centers, the method can easily be applied to the synchronous buck converter (stepping 12 V down to 1 V) used in the POL converter in the conventional power supply architectures where the turn-on loss is also a dominant loss of the converter [15].

The method can also be applied to converters not typically used in power supplies but also a PWM converter, such as boost, buck boost, SEPIC, Cuk, etc.

VII. Conclusion

Half-bridge current doubler with symmetrical control is selected as the converter topology in an ISOP connected system used in the high HV POL converter for data center power supplies in order to improve the overall system efficiency from 400 to 1 $\mathrm{V_{DC}}$.

A control method has been proposed so that ZVS of primary-side MOSFETs can be achieved which eliminates the major drawback of symmetrical-controlled half-bridge converter being a hard-switching converter. A Load-dependent ZVS method has further been proposed and analyzed to indicate the mechanisms which improve light-load efficiency compared with the constant charging time method in particular for the on-board power supply converters.

The converter design including device selection and transformer design together with the auxiliary components selection has been accomplished. A hardware prototype has been built

to verify the proposed soft-switching methods. Based on the experimental results, the proposed method can adjust the charging time of auxiliary inductor automatically based on load condition, and, thus, higher efficiency is observed for the proposed method in comparison with conventional hard-switching and constant charging time method. Therefore, the proposed soft-switching method is an effective method to increase the entire load range efficiency.

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