IR Camera Validation of IGBT Junction Temperature Measurement via Peak Gate Current

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***Abstract*—Infrared measurements are used to assess the measurement accuracy of the peak gate current (I_{GPeak}) method for Insulated-gate bipolar transistor (IGBT)junction temperature measurement. Single IGBT chips with the gate pad in both the center and the edge are investigated, along with paralleled chips, as well as chips suffering partial bondwire lift-off. Results are also compared with a traditional electrical temperature measurement method: the voltage drop under low current ($V_{\mathrm{CE(low)}}$). In all cases, the I_{GPeak} method is found to provide a temperature slightly overestimating the temperature of the gate pad. Consequently, both the gate pad position and chip temperature distribution influence whether the measurement is representative of the mean junction temperature. These results remain consistent after chips are degraded through bondwire lift-off. In a paralleled IGBT configuration with nonnegligible temperature disequilibrium between chips, the I_{GPeak} method delivers a measurement based on the average temperature of the gate pads.**

***Index Terms*—Insulated-gate bipolar transistor (IGBT), power semiconductor devices, temperature measurement.**

I. Introduction

THE junction temperature of a power semiconductor device is a key parameter that influences both performance and reliability. Knowledge of this temperature during operation could improve condition monitoring systems, and allow temperature-based control algorithms that enhance module lifetime [1].

Real-time junction temperature measurement is however often difficult. Physical or contact measurement methods such as optical fibers, on-chip sensors, or infrared (IR) cameras are expensive and require substantial modification to standard power module packaging. For these reasons, electrical measurement methods are often preferred. Using a temperature-sensitive electrical parameter (TSEP), such as the on-state voltage drop or threshold voltage, junction temperature measurements can be performed on standard power modules without modification to their structure [2]–[4].

Electrical methods for junction temperature measurement have been used for many decades on transistors, particularly for offline thermal characterization of devices. Nevertheless, TSEP-based methods face many challenges in online implementation (i.e., during normal transistor operation) [4], [5]. Issues regarding online TSEP usage generally involve the need to compensate for operating conditions other than temperature (such as load current), and the need for complex measurement circuitry or alteration to converter structure or control. Calibration procedures can also present substantial problems when self-heating compensation is required for higher current levels [6], [7].

In the past two years, a significant number of proposals for online TSEP measurements have been presented [8]–[15]. This paper extends on the work displayed in [11] and [12], by providing a detailed evaluation on the accuracy of insulated-gate bipolar transistor (IGBT) temperature measurement using the peak gate current (I_{GPeak}). Although this method claims to resolve some of the TSEP implementation issues highlighted earlier, no validation is currently available regarding whether the measured temperature suitably represents the junction temperature in an operating IGBT.

Validating the accuracy of a TSEP is of fundamental importance if a TSEP is to be considered for real-world use, since a TSEP may not always provide accurate results. In fact, inconsistencies between different TSEP measurements have been found as far back as 1966 [16]. Since then, there is ample research to back up the assertion that TSEPs can deliver widely varying temperature measurements. A notable example is the V_{CE} at high current, which can give vastly erroneous temperatures due to the series resistance contribution of the packaging interconnections [7], [17]. The discrepancies between different TSEPs may also change depending on the device and dissipation conditions [18]—[20]. Nevertheless, many recent TSEP proposals come with little or no validation (perhaps limited to one single chip) of the temperature provided.

As a result, this paper focuses on evaluating the accuracy of the (I_{GPeak}) method for IGBT junction temperature measurement. First of all, IR measurements are used to validate the (I_{GPeak}) method on two equally rated IGBTs from the same manufacturer, with differing geometry (shape and gate pad position). The IGBTs are also investigated in a paralleled configuration—both with and without large temperature disequilibrium between the paralleled IGBTs. Finally, since the electrical parameters of a device are prone to alter throughout its lifetime, a pertinent question is whether the accuracy of a TSEP method is resistant to these effects. To begin a preliminary assessment on this question, an IGBT is investigated both before and after several bondwires are disconnected from the die, which mimics one of the most common degradation mechanisms reported in prior literature.

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All results obtained using the (I_{GPeak}) method are compared to measurements made using a conventional TSEP method, the voltage drop under low current injection ($V_{\mathrm{CE(low)}}$). This TSEP is selected for comparison with I_{GPeak} due to its widespread use and repeated evidence of correlation with mean junction temperature [7], [18], [21].

This paper will first provide a short description of the procedure for junction temperature measurement using both (I_{GPeak}) and ($V_{\mathrm{CE(low)}}$). Details will then be provided on the IGBT chips studied, and the methodology behind the IR measurements. The electrical test bench will also be described, which allows thermal measurements to be conducted on IGBTs operating under constant current injection. The results of each temperature measurement on the variety of IGBT configurations are then presented.

II. TSEP Measurements

A. Peak Gate Current—I_{GPeak}

This measurement method relies on the temperature dependence of the internal gate resistance (R_{Gint}), which is located in the IGBT chip itself. If the peak gate current and voltage swing of the gate driver are known, these values can be used to calculate a value for R_{Gint}. A detailed explanation of this method is provided in [11]; however, the basic measurement principle will be outlined in the following paragraphs.

I_{GPeak} is measured during the normal charging cycle of the gate terminal during turn-on. The time constant for the charging of the gate in a MOS-gated device before the threshold voltage is reached (i.e., during the turn-on delay) can be written as follows [22]:

$$R_G \left[C_{\mathrm{GS}} + C_{\mathrm{GD}} \left(V_{\mathrm{DS}}\right)\right] \tag{1}$$

where R_G is the gate resistance, C_{GS} is the gate–source capacitance (gate–emitter in IGBTs), C_{GD} is the gate–drain capacitance (gate–collector in IGBTs), and V_{DS} is the drain–source voltage (collector–emitter in IGBTs).

During the turn-on delay, the capacitance C_{GD} remains small and constant due to a high and unchanged value of V_{DS} [23], [24]. Thus, if the parasitic gate inductance is kept negligible, the gate current during the turn-on delay can be viewed as a step response of a first-order *RC* circuit where the initial (and peak) charging current into the gate capacitor can be calculated as follows:

$$I = \frac{V}{R} e^{-t/\mathrm{RC}}. \tag{2}$$

The peak current at $t = 0$ can therefore be approximated by using Ohm's law, $I \approx V/R$, where V is the voltage swing of the gate driver, and R is the total gate resistance.

It is possible to monitor (I_{GPeak}) by measuring the peak value of the voltage across the external gate resistor, since this voltage is directly proportional to the gate current. A peak detector circuit is integrated into the gate driver and consists of a differential amplifier, a peak detector, a memory capacitor, and a reset switch that is controlled by the gate voltage signal, as seen in Fig. 1.

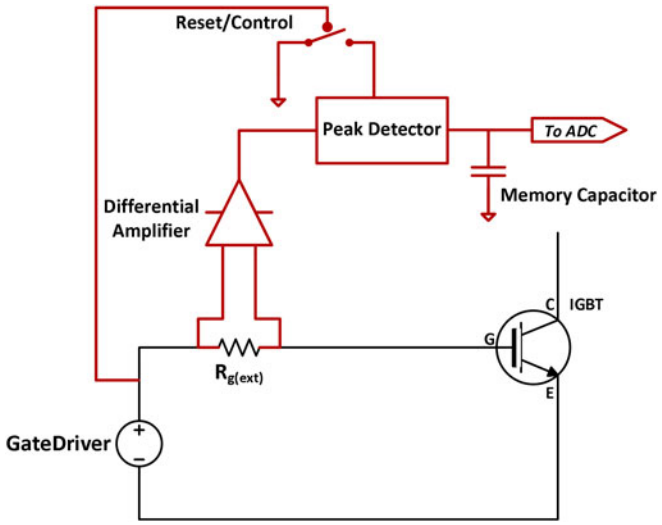


Fig. 1. Peak detector schematic to detect peak voltage over the external gate resistor [11].

Along with the output of the peak detector circuit $V_{\mathrm{Peakdetector}}$, the gate voltage just before turn-on is measured (V_{Gneg}), as well as the positive supply from the gate driver V_{Gpos}. These three values are then used in (3) to calculate a value for R_{Gint}:

$$R_{\mathrm{Gint}} = \frac{V_{\mathrm{Gpos}} - V_{\mathrm{Gneg}}}{\left(V_{\mathrm{peakdetector}}/R_{\mathrm{Gext}}\right)} - R_{\mathrm{Gext}}. \tag{3}$$

This paper uses a prototype measurement circuit previously detailed in [11]. High power verification of the measurement in the form of a double pulse test, along with discussion of several implementation issues can be found in [11]. This paper however focuses on evaluating the fundamental accuracy of the I_{GPeak} method; therefore, implementation issues relating to real-world use in commercial converters will not be extensively discussed.

B. Forward Voltage Under Low Current Injection—$V_{\mathrm{CE(low)}}$

The $V_{\mathrm{CE(low)}}$ has been used for the thermal characterization of bipolar transistors for many decades [3], [16], [21], [25]. By taking advantage of the temperature dependence of the voltage drop across a PN junction, this parameter generally exhibits a negative temperature dependence of approximately –2 mV/°C in silicon devices.

The measurement process is very simple: a constant sensing current generally in the range of 1–100 mA is fed into the power device, and the subsequent voltage drop is measured. Typically, the sensing current is injected into the device after a sufficient delay (up to a few hundred microseconds) once the load current has been removed in order to be sure that excess carriers are completely swept away or recombined. Since the sense current induces negligible self-heating, the voltage drop can be recorded as the device is cooling and a linear regression versus the square root of time used to estimate the temperature value at the moment the load current is switched off [3], [21].

Although the $V_{\mathrm{CE(low)}}$ has been experimentally validated in numerous studies and shown to provide a temperature close to

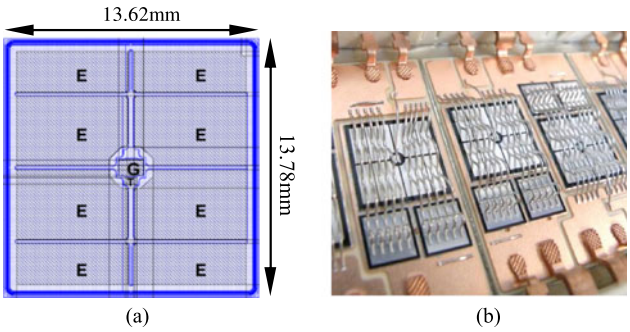


Fig. 2. IGBT A. (a) Geometry of Infineon IGC189T120T8RL bare die. (b) Dies inside FS200R12PT4 module after dielectric gel is removed.

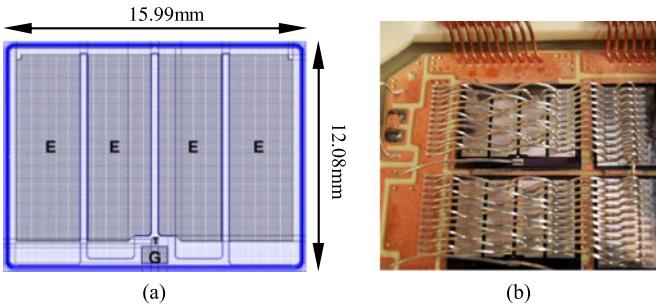


Fig. 3. IGBT B. (a) Geometry of Infineon IGC193T120T8RM bare die. (b) Dies inside FF600R12ME4 module after dielectric gel is removed.

the mean temperature of the chip [7], [18], [21], it is problematic to implement in real switching conditions due to requiring a suitable window to inject the sensing current [26], [27]. Nevertheless, its traditional use and repeated evidence of correlation with mean junction temperature is why the method is chosen as the current state-of-the-art for comparison with the recently proposed (I_{GPeak}) method.

III. TSEP Measurements

A. IGBTs Under Test

Two Infineon IGBTs are chosen for investigation, both rated at 1200 V/200 A. Additionally, each IGBT contains an (R_{Gint}) of 3.5 Ω. Although these IGBTs have identical specifications, the geometry of the chips is dissimilar and is the primary reason for their selection.

The first IGBT (Die: IGC189T120T8RL [28], Module: FS200R12PT4) is square in profile with the gate pad in the center, while the second IGBT (Die: IGC193T120T8RM [29], Module: FF600R12ME4) has a rectangular profile with the gate pad at the side. The geometry and dimensions of the dies are shown in Figs. 2 and 3. These IGBTs will subsequently be referred to as Type A and Type B, respectively.

Because functional dies complete with bondwires and packaging could not be obtained individually, the experiments are performed on individual dies isolated from inside commercial multichip power modules. The module layout for IGBT A (square, gate pad center) also allowed investigation of two

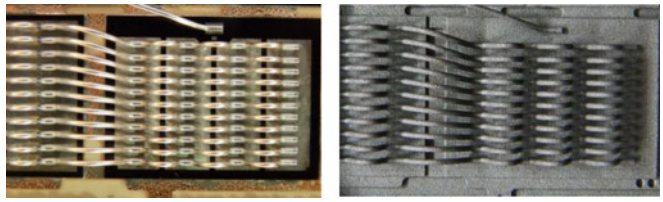


Fig. 4. IGBT B before painting (left) and after painting (right).

IGBTs in parallel. In addition, IGBT A is investigated both with and without bondwire removal.

B. IR Thermal Measurements

To prepare the power modules for IR measurements, the dielectric gel was first removed by soaking for several hours in Ardrox 2312 at 75 °C. The modules were then cleaned with Acetone and deionized water, before being painted with PYROMARK 1200 high temperature paint. Care was taken during the painting process to achieve as consistent emissivity as possible across the chip surface: the paint was filtered to attain a uniform particle size, and microspraying equipment was used that allowed tight control over the paint thickness. Before and after painting photos of IGBT B are shown in Fig. 4.

The thickness of the paint was selected as a tradeoff between achieving uniform emissivity, while minimizing the impact on the thermal behavior of the IGBTs. The paint thickness in all cases is between 10 and 16 μm, compared to the 115–120 μm thickness of the IGBT dies.

The IR camera used is a CEDIP-FLIR SC7500. For each measurement, 100 IR frames (100 Hz frequency) are acquired while the IGBTs conduct a constant current in a thermal steady state. To fix identical positioning for each image acquisition, the position of the camera was controlled by a three-axis positioning system.

C. Test Bench Operation

A panoramic view of the test bench, along with a closeup of the IR camera, power module and gate driver with the I_{GPeak} measurement circuit is shown in Fig. 5. A schematic of the test setup is displayed in Fig. 6, which allowed the TSEPs to be evaluated with IGBTs operating under constant current injection. The operating principle is described below, with the basic premise being a two stage operation: a heating phase and a measurement phase.

The first step is the heating step, where a high current is fed into the device under test (DUT) IGBT from the current source I_1. This induces self-heating in the device, which can last for several minutes until a thermal steady state is reached. The second step is the measurement step. At this point, the IGBT temperature is measured using the three presented measurement methods: IR camera, $V_{\mathrm{CE(low)}}$, and I_{GPeak}.

All electrical measurements are performed using a HBM Gen3i data recorder. To measure I_{GPeak}, the peak detector prototype described in [11] is used, and the circuit output along with

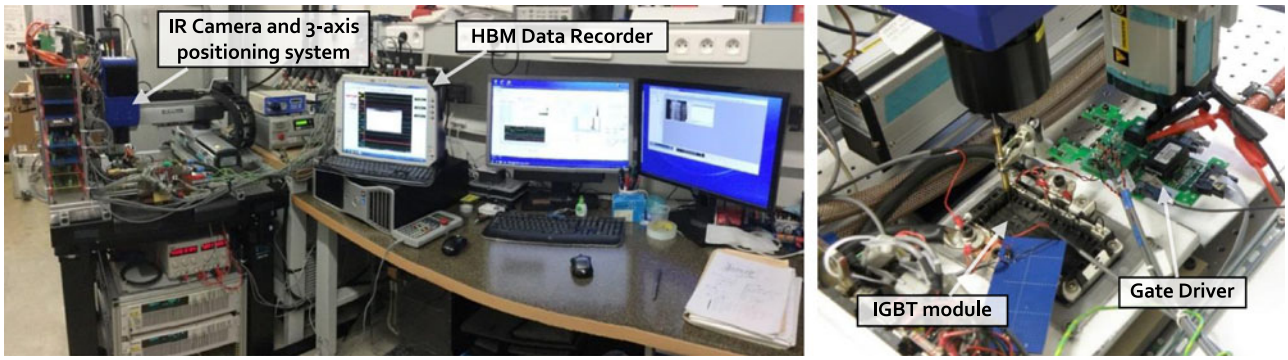


Fig. 5. (a) Panoramic view of test bench (b) Closeup of power module, IR camera, and gate driver with peak detector measurement circuit [11].

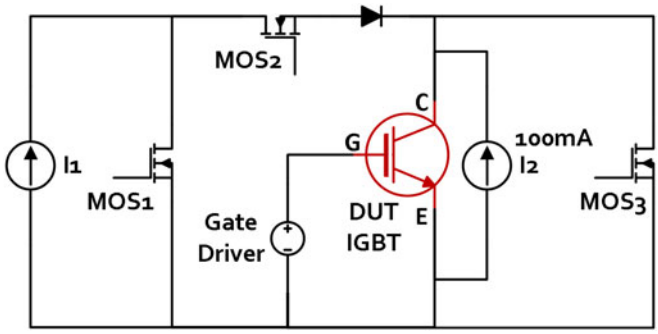


Fig. 6. Test bench schematic.

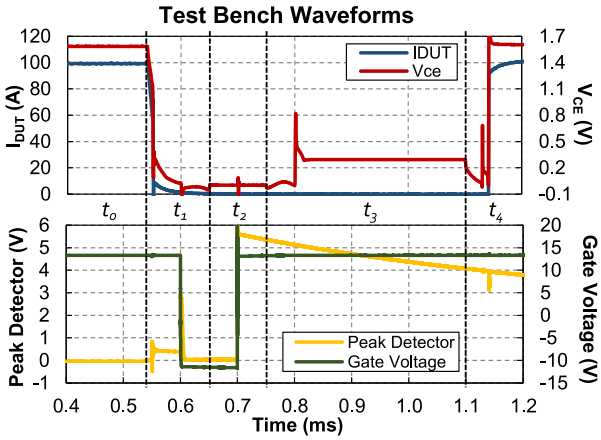


Fig. 7. Synchronization of electrical measurements.

the gate voltage is sampled at 100 MS/s (14-bit resolution). The V_{CE} of the DUT IGBT is recorded at 2 MS/s (16-bit resolution).

It is clear that both $V_{\mathrm{CE(low)}}$ and I_{GPeak} cannot be performed while conducting the full dissipation current: $V_{\mathrm{CE(low)}}$ requires a low sensing current of 100 mA and I_{GPeak} must be recorded during an IGBT turn-on. Therefore, synchronization of MOSFETs MOS1, MOS2, MOS3, and current source I_2 are used in order to facilitate these measurements.

The current source I_2 is fixed at 100 mA and provides the sensing current to perform a temperature measurement using $V_{\mathrm{CE(low)}}$. MOS1 and MOS2 on the other hand are used to control the injection of the high heating current into the IGBT. MOS3 is used to force a zero collector–emitter voltage during measurement of I_{GPeak}.

The general procedure is as follows and depicted in Fig. 7. First of all, t_0 depicts the end of the heating phase which may have been ongoing for several minutes previously, with the DUT IGBT conducting a high current. In this phase, the temperature evolution of the IGBT is monitored using the IR camera. Once a thermal steady state is reached, 100 IR images are sampled at 100 Hz. Following this, t_1 commences with I_{DUT} redirected into MOS1, and the DUT IGBT switched off—a transition that lasts 100 µs in total. In t_2, MOS3 is closed to short the collector and emitter of the DUT IGBT. This fixes the V_{CE} at 0 V and is vital to ensure a stable C_G for the (I_{GPeak}) measurement [11]. The IGBT is turned on again and a measurement of I_{GPeak} occurs using the peak detector circuit. In total, (I_{GPeak}) is measured 200 µs after the heating current is removed. The negative gate voltage and the positive voltage supply of the gate driver are sampled 500 ns before turn-on, while the output of the peak detector is recorded 1 µs after turn-on.

Now that the (I_{GPeak}) measurement is completed, MOS3 is opened and a 100 mA sensing current (I_2) is injected into the DUT IGBT during t_3. The $(V_{\mathrm{CE(low)}})$ is recorded for a period of 250 µs, and a linear regression versus the square root of time is used to estimate the $V_{\mathrm{CE(low)}}$ at the instant the load current is removed from the DUT IGBT [3]. Finally, the original IDUT is returned to the DUT IGBT in t_4.

This procedure is repeated ten times and the mean value of these measurements is used for analysis. For calibration of $V_{\mathrm{CE(low)}}$ and I_{GPeak}, the cooling fluid to the IGBT heatsink is varied from 40 to 180 °C, and the procedure described above is performed with I_{DUT} set to 0 A. A type-K open thermocouple is placed on the copper base of the power module and used as the reference temperature during the calibration procedure.

D. Gate Capacitance Stability at $V_{\mathrm{CE}} = 0$ V

Although the measurement of I_{GPeak} is conducted at a constant V_{CE}, previous assumptions have stipulated that a high V_{CE} is also required for C_G to be stable [11], [23]. Since I_{GPeak} is

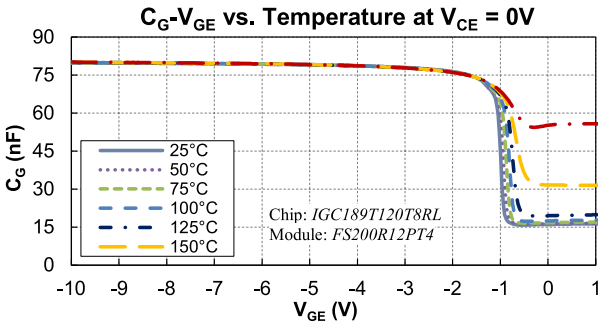


Fig. 8. $C_G - VGE$ versus temperature profile for IGBT A (Infineon FS200R12PT4).

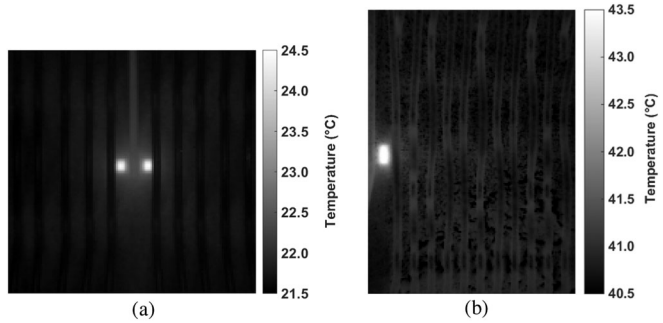


Fig. 10. Self-heating of R_{Gint}. (a) IGBT A. (b) IGBT B.

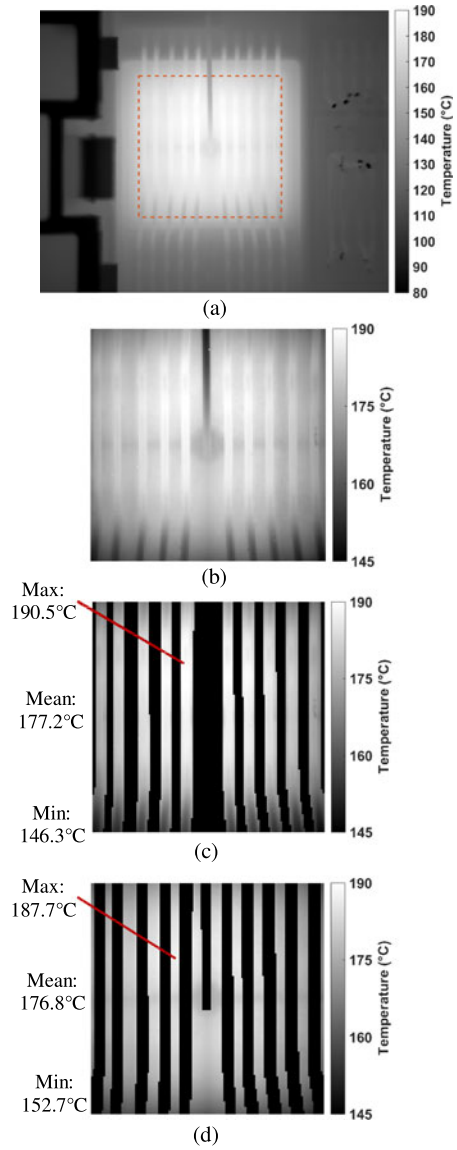


Fig. 9. Processing of IR images to extract the junction temperature. (a) Unedited IR image of IGBT A during dissipation at 140 A. (b) Cropped IR image to the active area of the die. (c) IR image of bondwires with die surface removed via a MATLAB image mask. (d) IR image of die surface with bondwires removed via a MATLAB image mask. This image is used to calculate the mean junction temperature.

measured at a V_{CE} of 0 V in these experiments, a short validation of the stability of C_G in this condition was conducted. Fig. 8 displays a C_{GE}–V_{GE} profile versus temperature on IGBT A with the collector–emitter shorted (i.e., the same conditions for I_{GPeak} measurement in the test bench).

The profile shows that (C_{GE}) is around 80 nF and stable with temperature while V_{GE} remains below approximately –1 V. Given that the Concept2 gate driver used in the peak detector prototype has a negative turn-off voltage of –10 V [30], (I_{GPeak}) should be detected well before the voltage on the gate capacitor reaches –1 V. Therefore, the fluctuation of (C_{GE}) with temperature at a V_{GE} beyond –1 V should not impact the measurement of (I_{GPeak}). For the experiments conducted in this paper, a unipolar gate driver with a turn-off voltage of 0 V (or within temperature-dependent region of Fig. 8) would yield fallacious results.

IV. Results

In the following sections, all raw data values for the dissipation results are included in the tables in the Appendix.

A. *Definition of "Junction Temperature"*

The term "junction temperature" is ambiguous, since the temperature of a power semiconductor cannot be described using a single temperature value. Instead, the junction is made up of a large distribution of temperatures. In prior literature concerning the evaluation of TSEP accuracy, the mean surface temperature and the absolute maximum temperature of the chip are the two most common measurements chosen for comparison with the TSEP measurement. In this paper, the "junction temperature" is assumed to be the mean surface temperature of the emitter metallization on the IGBT die. These emitter pads can be seen in the die datasheets [28], [29] and in Figs. 2 and 3. As a result, the "junction temperature" does not include the entirety of the die area, or any of the attached bondwires.

To extract the mean surface temperature of the emitter pads, the IR images are processed using image masks in MATLAB to remove the undesired pixels. This process is depicted in Fig. 9.

A noteworthy observation from this procedure is that the bondwires experience a wider temperature distribution than the die. From Fig. 9, where IGBT A is conducting 140 A, it can be seen that the bondwires have both a lesser minimum and

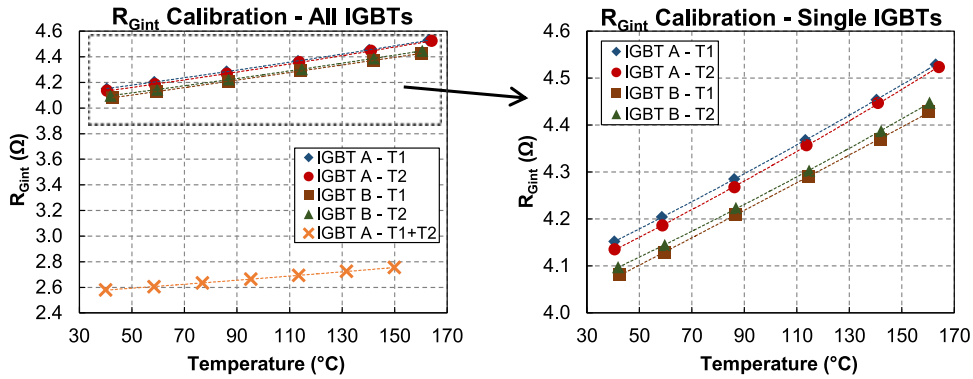


Fig. 11. R_{Gint} versus temperature from calibration data for IGBT A and B (I_{GPeak} used to calculate R_{Gint}).

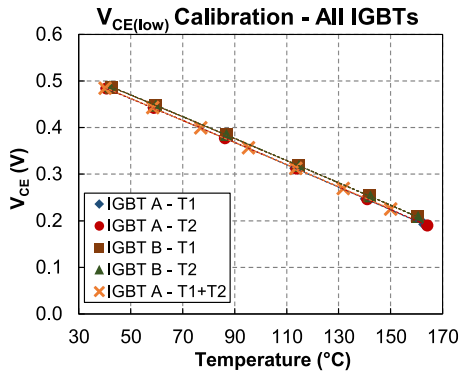


Fig. 12. $(V_{\mathrm{CE(low)}})$ versus temperature from calibration data for IGBT A and B.

a higher maximum temperature. The maximum temperature of the bondwires is close to 3 °C higher than the die, while the minimum is more than 6 °C lower. Nonetheless, the overall mean temperature of both structures is similar, with the mean temperature of the bondwires just 0.4 °C higher than the die surface.

B. Location of R_{Gint}

The IR camera was used to perform a preliminary assessment on the location of the internal gate resistor for each IGBT. To do this, IGBTs were shorted between the collector and emitter, and switched using a gate driver at a frequency of 30 kHz. Fig. 10 displays thermal images of the IGBTs during this procedure. Clear heating in the gate pad of around 3 °C can be seen on both IGBTs, which is assumed to be the result of the self-heating of R_{Gint}.

As a result, image masks were created in MATLAB to extract both the mean surface temperature of the emitter metallization on the IGBT die ($\mathrm{IR_{Mean}}$), as well as the mean temperature of the gate pad ($\mathrm{IR_{Gate}}$).

C. Calibration

Two IGBTs are characterized from each module. In addition, the layout of the FS200R12PT4 module allowed IGBT A to be calibrated with two IGBTs in parallel. In this case, the sensing current for $V_{\mathrm{CE(low)}}$ was accordingly doubled from 100 to 200 mA, while the gate driver remained unchanged.

Calibration curves for the two TSEP measurement methods are shown in Figs. 11 and 12. I_{GPeak} is used in conjunction with the gate voltage swing to calculate R_{Gint}, as specified in (3). Although both (R_{Gint}) and $(V_{\mathrm{CE(low)}})$ display a near linear relationship with temperature, a second-order polynomial fit is in fact used to calculate their respective relationships for when the TSEPs are used during dissipation.

For the traditional $V_{\mathrm{CE(low)}}$, the calibration reveals very little variance between the chips. The temperature sensitivity is approximately –2.4 mV/°C, with only a small offset between IGBT A and B of around 6 mV. Furthermore, the two paralleled chips of IGBT A displayed precisely the same $V_{\mathrm{CE(low)}}$ as when they were calibrated individually.

On the other hand, R_{Gint} has significant variation between IGBTs in spite of each chip having a specified datasheet value of 3.5 Ω. Within chips from the same module, sensitivity was fairly uniform: 3.2 mΩ/°C for IGBT A and 2.9 mΩ/°C for IGBT B. However, an offset of approximately 20–30 mΩ is present between T1 and T2 for both IGBT types. Furthermore, there is a discrepancy of around 50 mΩ between IGBT A and B. This offset could be due to manufacturing tolerances in the production of R_{Gint}. For the paralleled chips of IGBT A, the sensitivity was halved to 1.6 mΩ/°C.

D. Dissipation Results—Single IGBTs

Temperature measurements during dissipation were conducted at a range of current values from 40 to 160 A. The heating current was limited to below the 200 A rating of each IGBT in order to maintain a safe maximum junction temperature of below 200 °C. The input fluid to the heatsink was maintained at 40 °C during all tests.

Fig. 13 displays the temperature measurement results during dissipation on a single IGBT of both Types A and B. Temperature measurements via I_{GPeak} and $V_{\mathrm{CE(low)}}$ are displayed, along with IR measurements regarding the mean surface temperature of the die $(\mathrm{IR_{Mean}})$ and gate pad $(\mathrm{IR_{Gate}})$.

For IGBT A (square, gate pad center), all temperature measurements appear to match closely. On the other hand, the four

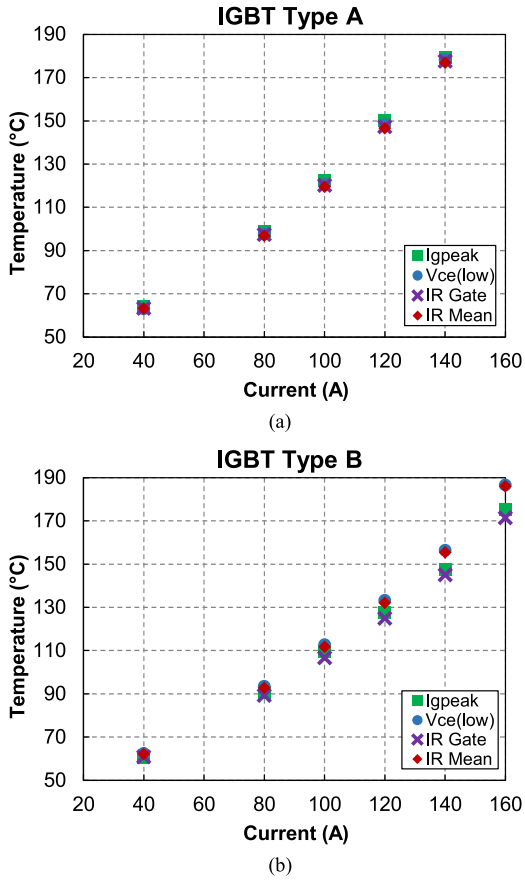


Fig. 13. Temperature measurement results during dissipation from 40 to 160 A. (a) IGBT A. (b) IGBT B.

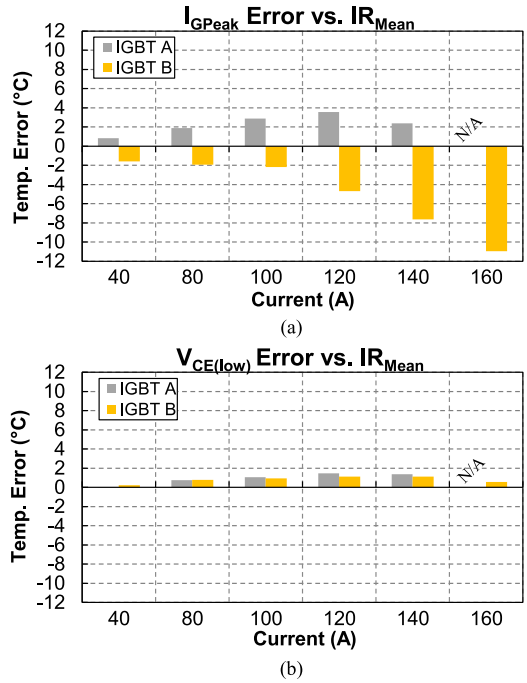


Fig. 14. Measurement error versus mean surface temperature for (a) I_{GPeak} and (b) $(V_{\mathrm{CE(low)}})$.

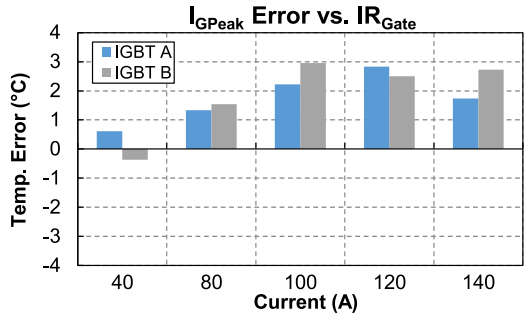


Fig. 15. Temperature measurement via I_{GPeak}: error versus gate pad temperature.

temperature measurement methods show clear divergence on IGBT B—particularly at high current levels. In IGBT B, I_{GPeak} clearly underestimates the mean surface temperature and provides a temperature that is lower than measured via $V_{\mathrm{CE(low)}}$.

To demonstrate these trends more precisely, Fig. 14 compares both TSEP measurements in relation to $\mathrm{IR}_{\mathrm{Mean}}$ for each IGBT. It can be observed that in all cases, $V_{\mathrm{CE(low)}}$ provides a temperature that slightly overestimates the mean surface temperature of the die. The difference between the V_{CElow} and $\mathrm{IR}_{\mathrm{Mean}}$ remains strictly lower than +2 °C. These results are in accordance with several previous studies [18], [21].

The slight overestimation of the mean temperature may be a consequence of the temperature gradient across the chip during dissipation, which is a contrast to the homogenous temperature during calibration. Due to the negative temperature coefficient of $V_{\mathrm{CE(low)}}$, the central and hotter parts of the chip experience an increased current density compared to the colder outer parts of the chip. As the entire current in the chip must equal the total sense current of 100 mA, these hotter areas subsequently contribute a larger weighting in the composition of $(V_{\mathrm{CE(low)}})$.

Meanwhile, I_{GPeak} provided a temperature that differed in comparison to $\mathrm{IR}_{\mathrm{Mean}}$ depending on the chip type. For IGBT A, with a centrally located gate pad, Fig. 14 shows that I_{GPeak} obtained a temperature that was higher than the mean surface temperature by between 1 and 4 °C. These results are comparable to those obtained via $(V_{\mathrm{CE(low)}})$. Conversely, for IGBT B, I_{GPeak} always delivered a temperature lower than $\mathrm{IR}_{\mathrm{Mean}}$. At lower current levels, this underestimation was not severe at around –2 °C. However, this increased to –7.6 and –10.9 °C at higher current (and temperature) levels.

These trends could perhaps be anticipated due to the respective locations of the gate pad. In fact, Fig. 15 shows the correlation of temperature measurement via I_{GPeak} to the temperature of the gate pad measured via IR camera. In almost all cases on both chip types, I_{GPeak} provided a temperature within +1 and +3 °C of the gate pad.

A gate pad at the side experiences a comparatively lower temperature than one in the center due to the temperature gradient across the chip during dissipation. These temperature gradients generally become more significant at higher mean temperatures. This is shown in Fig. 16, which displays the temperature profile

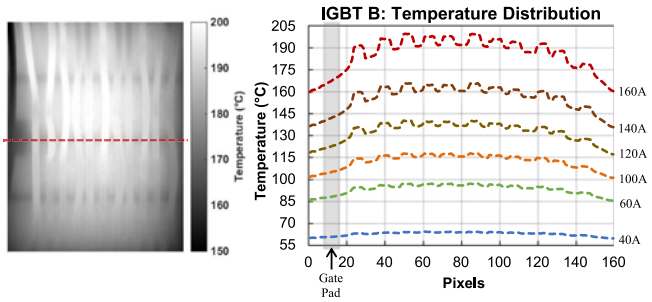


Fig. 16. Temperature profile across IGBT B from 40 to 160 A. Temperature is plotted along the dotted line.

across IGBT B at all investigated current levels. This is therefore an explanation for why I_{GPeak} still delivered a reasonable approximation of $\mathrm{IR}_{\mathrm{Mean}}$ (within –2 °C) on IGBT B up to 100 A dissipation current, while severely underestimating $\mathrm{IR}_{\mathrm{Mean}}$ as the current and temperature increased.

These results infer that use of I_{GPeak} for junction temperature measurement on single IGBTs would require consideration of the gate pad position, as well as the expected operating temperatures and temperature distribution throughout the chip.

The fact that the I_{GPeak} method consistently measures a slight overestimation of the gate pad temperature could indicate a systematic error in the experiment. This may be due to a suboptimal design of the peak detector circuit, or a systematic error in the measurement principle. For example, the gate connection in the IGBTs studied is not a Kelvin connection. Therefore, the collector current and the gate current must share the same path (including bondwires), which could produce a discrepancy between the calibration conditions with 0 A load current, and the dissipation conditions with a high heating current.

E. Dissipation Results: Degraded Single IGBT With Partial Bondwire Removal

To begin an assessment on the robustness of the I_{GPeak} method, temperature measurements were performed on a degraded IGBT suffering bondwire lift-off. The bondwire lift-off mechanism was selected for two reasons. First, it is one of the most common degradation mechanisms written about in academic literature, and second it is easy to emulate without requiring removal of the power modules from the test setup. In this manner, the I_{GPeak} method can be assessed in precisely the same conditions for both the healthy and degraded states.

To achieve the degraded condition, three bondwires on IGBT A were cut with wire clippers, resulting in the complete disconnection of a central emitter pad on the IGBT. An IR image of this condition at 140 A is displayed in Fig. 17, from which clear distortion of the temperature distribution can be seen in comparison to the healthy IGBT. Mean and maximum temperatures of the IGBT are around 5–10 °C higher after bondwire removal.

Temperature measurements on the degraded IGBT A are shown in Fig. 18. The results appear similar to the findings of IGBT A in a healthy condition (see Fig. 13)—all temperature measurements match closely.

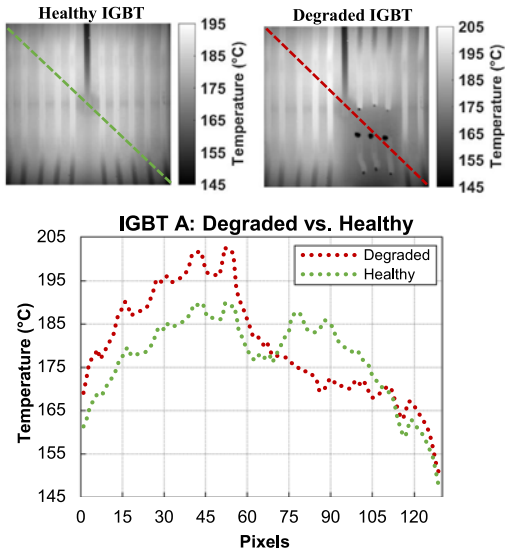


Fig. 17. Comparison of IGBT A temperature profile at 140 A before and after bondwire removal. Temperature is displayed along diagonal lines.

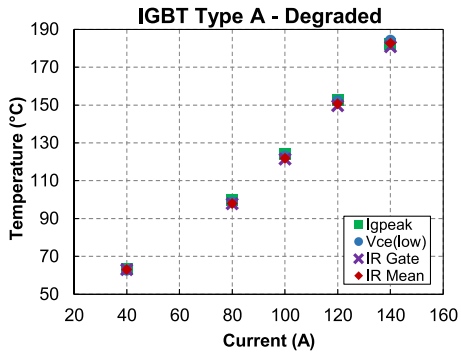


Fig. 18. Temperature measurement results during dissipation on IGBT A with bondwires removed.

For further analysis, Fig. 19 is presented and displays a comparison of I_{GPeak} in relation to $\mathrm{IR}_{\mathrm{Mean}}$ and $\mathrm{IR}_{\mathrm{Gate}}$, both before and after degradation. The correlation between I_{GPeak} and $\mathrm{IR}_{\mathrm{Gate}}$ remains almost unchanged between healthy and degraded conditions. However, a nonnegligible shift can be seen when comparing I_{GPeak} to $\mathrm{IR}_{\mathrm{Mean}}$. In a healthy state, I_{GPeak} typically delivered a temperature between 2 and 3 °C larger than the mean junction temperature. After bondwire removal, this overestimation reduced by 1–2 °C. In fact, a –0.4 °C underestimation of $\mathrm{IR}_{\mathrm{Mean}}$ was observed at the highest heating current of 140 A. Although this adjustment may seem small, it is in clear contrast to $V_{\mathrm{CE(low)}}$, whose correlation with $\mathrm{IR}_{\mathrm{Mean}}$ altered less than ±0.2 °C in all cases, as shown in Fig. 20.

These results again infer that I_{GPeak} is primarily influenced by local conditions in the vicinity of the gate pad, rather than the overall active area of the die as is the case with the traditional $V_{\mathrm{CE(low)}}$.

It is perhaps logical that I_{GPeak} was found to be largely unaffected by bondwire lift-off, since the emitter bondwires may contribute a total resistance of just a few milliohm, as opposed to

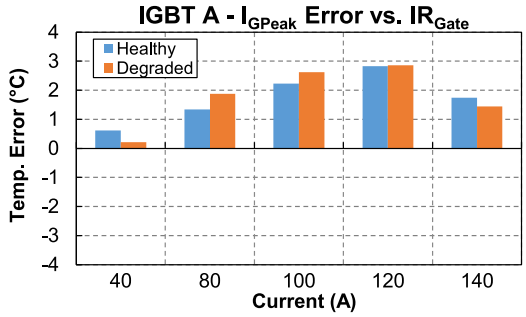


Fig. 19. Temperature measurement via I_{GPeak} in degraded and healthy conditions. (a) Error versus gate pad temperature. (b) Error versus mean surface temperature.

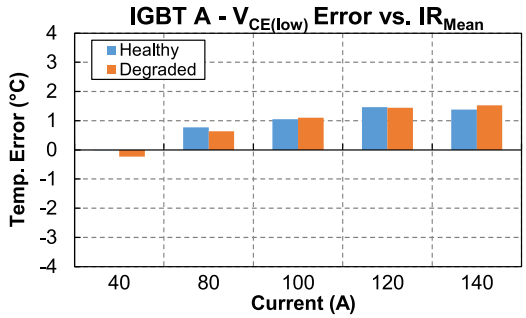


Fig. 20. Temperature measurement via $(V_{\mathrm{CE(low)}})$: error versus mean surface temperature in healthy and degraded condition.

the 3.5 Ω of R_{Gint}. Additionally, since the parasitic gate inductance is mainly comprised of the terminal leads and packaging, the lift-off of just a few bondwires cannot significantly change the total inductance in the circuit [31].

It must also be noted that merely cutting three bondwires on an IGBT is not a realistic representation of a degraded condition. In practical applications, an IGBT can be subject to a wide variety of failure mechanisms, some of which may be far more pertinent in influencing the I_{GPeak} method. To provide more thorough assessment on the robustness of I_{GPeak}, an investigation on IGBTs with a degraded gate oxide or gate capacitance would be relevant, especially as there is data to suggest that IGBT gate capacitances can vary through aging [33], [34].

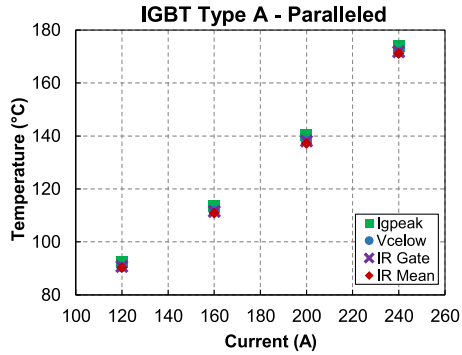


Fig. 21. Temperature measurement results during dissipation for two paralleled IGBTs (IGBT A) from 120 to 240 A.

F. Dissipation Results: Paralleled IGBTs

The module structure for IGBT A allowed investigation of two IGBTs in parallel. For paralleled IGBTs, the heating current ranged from 120 to 240 A, and the sense current for $V_{\mathrm{CE(low)}}$ was accordingly doubled from 100 to 200 mA. The gate driver and peak detector were unchanged from previous investigations, with a single gate driver being used to drive both IGBTs.

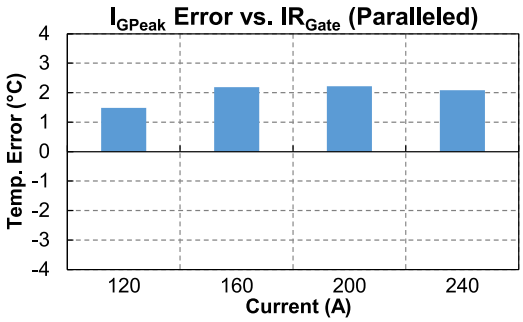
First of all, the paralleled IGBTs were assessed without inducing a temperature imbalance. In this condition, the temperature difference between the mean surface temperatures of each IGBT was a maximum of 2 °C. Temperature measurements in this paralleled state are displayed in Fig. 21. Since the temperature difference between the two IGBTs is minimal, single IR measurements are displayed which is the cumulative mean of both IGBTs (i.e. ,$((IR_{\mathrm{Mean}-T1} + IR_{\mathrm{Mean}-T2})/2)$).

The results on IGBT A in a paralleled configuration follow the same trends as with single IGBTs. Fig. 22 shows that I_{GPeak} delivers a temperature within +2 °C of the gate pad temperature. This leads to an overestimation of $\mathrm{IR}_{\mathrm{Mean}}$ by between +1 and +3 °C. Additionally, $V_{\mathrm{CE(low)}}$ again provides a temperature closely correlated with the mean surface temperature, with measurements at all current levels showing a difference of less than +1 °C.

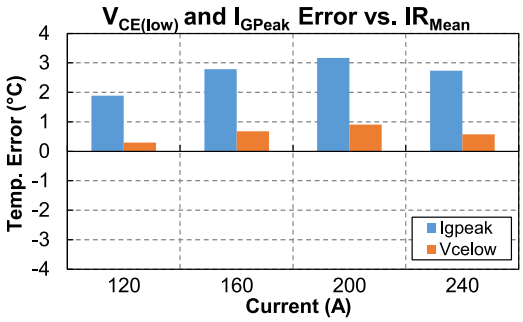
G. Dissipation Results: Paralleled IGBTs With Temperature Disequilibrium

A more interesting scenario is to examine the TSEP methods on paralleled IGBTs that have a large temperature imbalance. To achieve this, the connection from the heatsink to the baseplate was loosened on one side of the power module so that one IGBT suffered a deteriorated thermal contact. The IGBTs were then examined with a heating current of up to 200 A, where the temperature disequilibrium between the two IGBTs reached close to 20 °C.

Fig. 23 displays the temperature measurement results with this thermal imbalance. In this figure, the mean surface temperature measured via IR camera is included for both IGBTs. It can be seen that both I_{GPeak} and $(V_{\mathrm{CE(low)}})$ provide a temperature in between the $\mathrm{IR}_{\mathrm{Mean}}$ of IGBT 1 and IGBT 2.



(a)



(b)

Fig. 22. Temperature measurement error for two paralleled IGBTs (IGBT A). (a) I_{GPeak} error versus gate pad temperature. (b) I_{GPeak} and $(V_{\mathrm{CE(low)}})$ errors versus mean surface temperature.

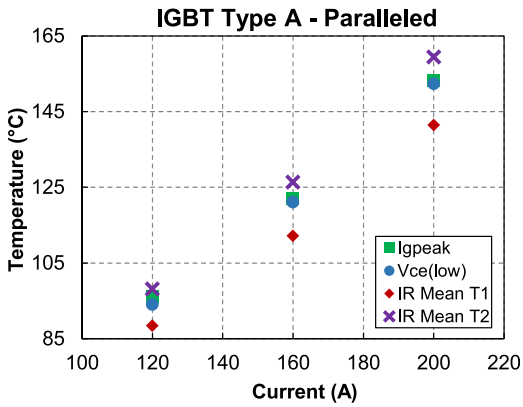


Fig. 23. Temperature measurements during dissipation on two paralleled IGBTs (IGBT A) with a temperature disequilibrium.

I_{GPeak} delivers a temperature within +2 °C of the cumulative mean temperature of the gate pad, as shown in Fig. 24.

The temperature profile of the two IGBTs with a 200 A heating current is shown in Fig. 25. Here, the I_{GPeak} and $(V_{\mathrm{CE(low)}})$ measurements are within 1 °C of each other and appear to correspond closely with the combined mean temperature profile of the two IGBTs. In fact, both TSEP measurements overestimate the cumulative mean surface temperature by between +1 and +3 °C, as shown in Fig. 26.

These results suggest that I_{GPeak} can provide an adequate assessment of the mean temperature of IGBT chips in a paralleled condition, at the least in line with results provided by the traditionally used $(V_{\mathrm{CE(low)}})$. This is providing that the IGBTs contain a centrally located gate pad.

For a more detailed assessment on the performance of I_{GPeak} with paralleled chips, a number of additional studies could be carried out. Clearly, immediate steps would be to assess I_{GPeak}

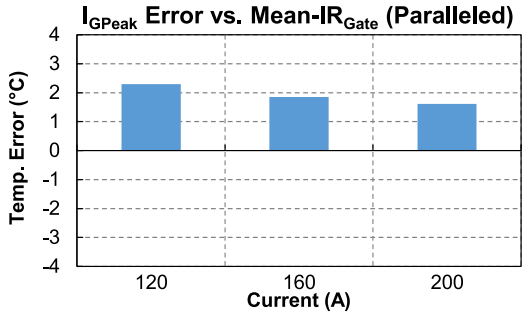


Fig. 24. I_{GPeak} on two paralleled IGBTs (IGBT A) with a temperature disequilibrium: error versus cumulative mean of gate pad temperature.

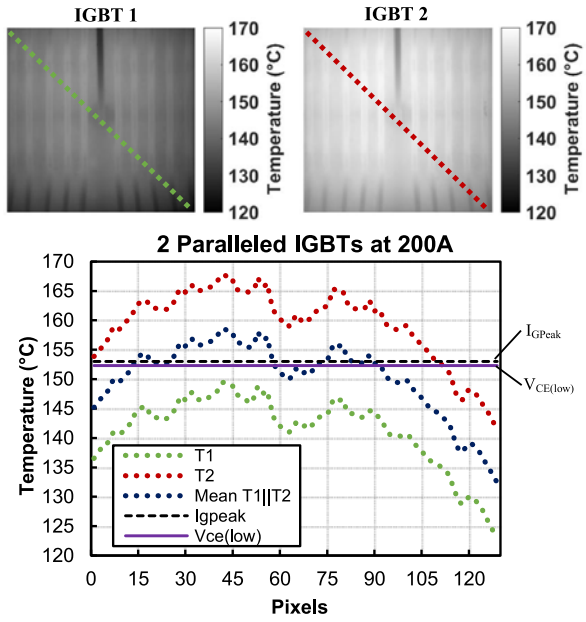


Fig. 25. Temperature profile of two paralleled IGBTs (IGBT A) with 200 A heating current. Temperature is plotted along diagonal lines.

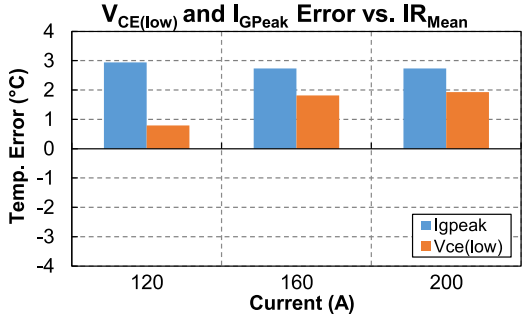


Fig. 26. I_{GPeak} and $(V_{\mathrm{CE(low)}})$ on two paralleled IGBTs (IGBT A): error versus cumulative mean surface temperature.

on a greater number than two IGBTs in parallel, as well as on paralleled IGBTs with the gate pad at the edge of the die. Other relevant studies would be to investigate the impact different paralleling layout techniques such as grouping IGBTs into "cells" [32].

V. Conclusion

This paper uses IR measurements to experimentally evaluate the accuracy of the peak gate current (I_{GPeak}) method for IGBT junction temperature measurement. The accuracy of I_{GPeak} is compared to a traditional electrical temperature measurement method, the voltage drop at low current ($V_{\mathrm{CE(low)}}$). The investigation is performed with IGBTs operating under constant current injection and temperature measurements are taken while the IGBT is in a thermal steady state.

The I_{GPeak} method is found to correlate closely with the temperature conditions in the vicinity of the gate pad. This is in contrast to the $V_{\mathrm{CE(low)}}$, which is influenced by the entire area of the die. As a result, I_{GPeak} provided a slight overestimation of the mean surface temperature of the die in IGBTs with a centrally located gate pad, while underestimating the mean surface temperature in IGBTs with a gate pad located at the side. These trends became more pronounced as the overall temperature of the dies increased, as a result of more pronounced temperature gradients.

The I_{GPeak} method is found to be largely unaffected by partial bondwire lift-off, which is a common degradation mechanism in IGBTs. In this respect, the I_{GPeak} method continued to provide a temperature associated with the gate pad temperature when the IGBT was in a degraded condition. However, since the temperature distribution in the die was modified due to this degradation, the correlation with the mean surface temperature was slightly altered.

In paralleled IGBTs where the gate pad is centrally located, I_{GPeak} was found to have similar averaging properties as the traditional $V_{\mathrm{CE(low)}}$ method, and provided a temperature slightly overestimating the cumulative mean temperature when a large temperature imbalance is present between the IGBTs.

As a general conclusion, using and interpreting measurement results provided by I_{GPeak} requires a good knowledge of the gate pad position, as well as likely operating temperatures and the temperature gradient in the chip.

Future work should primarily involve extending the validation to real functional conditions that are not experienced during constant current injection, and to a statistically significant number of IGBTs with differing power ratings and manufacturer. An assessment of the I_{GPeak} method tracking fast dynamic changes in temperature should also be a priority. Finally, an evaluation of robustness toward gate-oxide degradation introducing non-negligible gate leakage currents should also be carried out.

Appendix

Complete table of temperature measurement results from experiments performed.

IGBT A—Healthy

Current (A)	I_{GPeak} (°C)	$(V_{\mathrm{CE(low)}})$ (°C)	$\mathrm{IR}_{\mathrm{Gate}}$ (°C)	$\mathrm{IR}_{\mathrm{Mean}}$ (°C)	$\mathrm{IR}_{\mathrm{Max}}$ (°C)
0	42.1	42.0	41.7	41.8	42.1
40	63.9	63.0	63.3	63.1	65.3
80	98.7	97.6	97.4	96.8	102.1
100	122.3	120.5	120.1	119.4	126.7
120	150.1	148.0	147.2	146.5	156.5
140	179.2	178.2	177.5	176.9	190.5

IGBT A—Degraded

Current (A)	I_{GPeak} (°C)	$(V_{\mathrm{CE(low)}})$ (°C)	$\mathrm{IR}_{\mathrm{Gate}}$ (°C)	$\mathrm{IR}_{\mathrm{Mean}}$ (°C)	$\mathrm{IR}_{\mathrm{Max}}$ (°C)
0	40.9	40.5	40.8	40.9	41.3
40	63.1	62.7	62.9	63.0	65.8
80	99.6	98.6	97.7	98.0	105.1
100	123.9	122.9	121.3	121.8	132.2
120	152.5	152.1	149.6	150.6	165.3
140	182.1	184.0	180.7	182.5	203.1

IGBT B

Current (A)	I_{GPeak} (°C)	$(V_{\mathrm{CE(low)}})$ (°C)	$\mathrm{IR}_{\mathrm{Gate}}$ (°C)	$\mathrm{IR}_{\mathrm{Mean}}$ (°C)	$\mathrm{IR}_{\mathrm{Max}}$ (°C)
0	41.8	41.6	41.5	41.6	41.8
40	60.6	62.4	60.9	62.2	64.3
80	90.8	93.5	89.2	92.7	97.6
100	109.5	112.7	106.6	111.7	118.4
120	127.4	133.2	124.9	132.1	140.7
140	147.6	156.4	144.9	155.3	166.5
160	175.0	186.5	171.3	186.0	201.5

IGBT A—2× Paralleled without temperature disequilibrium

Current (A)	I_{GPeak} (°C)	$(V_{\mathrm{CE(low)}})$ (°C)	$\mathrm{IR}_{\mathrm{Gate}}$ T1 (°C)	$\mathrm{IR}_{\mathrm{Gate}}$ T2 (°C)	$\mathrm{IR}_{\mathrm{Mean}}$ T1 (°C)	$\mathrm{IR}_{\mathrm{Mean}}$ T2 (°C)
120	92.2	90.6	90.7	90.8	90.3	90.4
160	113.7	111.6	110.5	112.6	110.0	111.9
200	140.3	138.1	136.7	139.5	135.7	138.6
240	173.9	171.7	171.0	172.6	170.1	172.2

IGBT A—2× Paralleled with temperature disequilibrium

Current (A)	I_{GPeak} (°C)	$(V_{\mathrm{CE(low)}})$ (°C)	$\mathrm{IR}_{\mathrm{Gate}}$ T1 (°C)	$\mathrm{IR}_{\mathrm{Gate}}$ T2 (°C)	$\mathrm{IR}_{\mathrm{Mean}}$ T1 (°C)	$\mathrm{IR}_{\mathrm{Mean}}$ T2 (°C)
120	96.2	94.1	89.2	98.6	88.4	98.1
160	122.0	121.1	113.1	127.1	112.2	126.3
200	153.1	152.3	142.5	160.5	141.4	159.4

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