Development of a High-Temperature Gate Drive and Protection Circuit Using Discrete Components

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***Abstract*—This paper presents a high-temperature (HT) gate drive and protection circuit for Silicon–Carbide (SiC) power MOSFETs entirely built from commercial off-the-shelf HT discrete components. To estimate cost reduction, a brief comparison was made between the proposed circuit and a commercial circuit using silicon-on-insulator integrated circuits. To evaluate performance, power tests were conducted up to 180 °C in a thermal chamber. Eventually, the proposed circuit achieved a 90% cost reduction, and all functions were validated by experiments at 180 °C. This demonstrated that the proposed circuit is a cost-effective solution for contemporary HT applications.**

***Index Terms*—Commercial off-the-shelf, desaturation protection, galvanic isolation circuit, gate drive circuit, high temperature, SiC MOSFET, under voltage protection.**

I. Introduction

SILICON–CARBIDE (SiC) power devices are very promising candidates for the next generation of power devices due to their fast switching and (high-temperature) HT operating capabilities [1], [2]. The HT operating capability of SiC power devices significantly improves their applicability for power electronics circuits in HT environments such as hybrid electrical vehicles (HEV) and down-hole drilling tools [3]–[8]. Specifically for HEV applications, HT operation of power electronics circuits demands less heat dissipation. Because of this, separation of cooling systems for electronics and engine thermal management becomes unnecessary [4].

Although SiC power devices provide HT operating capability, it is still challenging to develop HT power circuits since many of the components for the gate drive circuits are not rated for HT environments [9]–[13]. Recently, researchers have developed some gate drive and protection circuits to drive and protect SiC power devices in HT environments [14]–[24].

CISSOID and XREL Semiconductor Company are major suppliers of gate drive and protection circuits using HT SOI integrated circuits (ICs). The ICs from CISSOID and XREL are designed for a maximum operating junction temperatures of 225 and 230 °C, respectively, and both have an absolute maximum junction temperature of 250 °C [14], [15]. In their solutions, pulse transformer circuits provide the galvanic isolation between control electronics and power electronics. Other researchers have also proposed a gate drive and protection IC based on a silicon-on-insulator (SOI) process [16], [17]. The IC was successfully tested at 200 °C.

The HT SOI processes improve the maximum junction temperature significantly and allow the HT SOI ICs to work up to 250 °C. However, due to the band-gap energy of silicon, the junction temperature limit will always remain below 300 °C theoretically [3]. It should be noted that as of this writing, the prices of HT SOI ICs are more than ten times the prices of conventional silicon ICs [29], [30].

Alternative solutions utilizing wide band-gap materials, such as SiC, could be made to work all the way up to 600 °C and have already been demonstrated in laboratory prototypes [3], [23]–[28]. However, it is difficult to predict when SiC ICs will become mature enough for commercialization in real-world applications.

Although advanced IC fabrication processes have made a large difference in increasing the operating junction temperature, the price and maturity of advanced IC fabrication processes are major barriers to the proliferation of HT ICs. Furthermore, the low volume of the current applications for HT ICs largely influences the optimization of advanced IC fabrication processes. As of this writing, the HT ICs suffer from prohibitively high prices and immature fabrication processes.

In some cases, it is unnecessary to use ICs in HT gate drive and protection circuits. A gate drive circuit based on commercial off-the-shelf (COTS) discrete components can be built to drive SiC MOSFETs in HT environments [19]. This was modified from a pulse transformer topology [18]. With similar pulse transformer topologies, other researchers also designed gate drive circuits utilizing both SOI ICs and COTS discrete components [20]–[22]. The decent performance of the COTS discrete components has been initially demonstrated by these HT gate drive circuits. Additionally, current market prices of HT ICs are about 500 times the price of HT discrete components [29], [30]. These performance and price factors make it very attractive to develop gate drive and protection circuits using COTS HT discrete components.

By using COTS discrete components, this paper proposes a novel gate drive and protection circuit for HT applications. Generally, gate drive and protection circuits are required to be compact. However, it is quite challenging to design a compact circuit solely using discrete components. To achieve a balance between size and function, the proposed circuit cuts nonessential functions and only retains: gate drive, desaturation protection, under voltage protection, and galvanic isolation. To further reduce circuit area, simplifications are made by creatively composing

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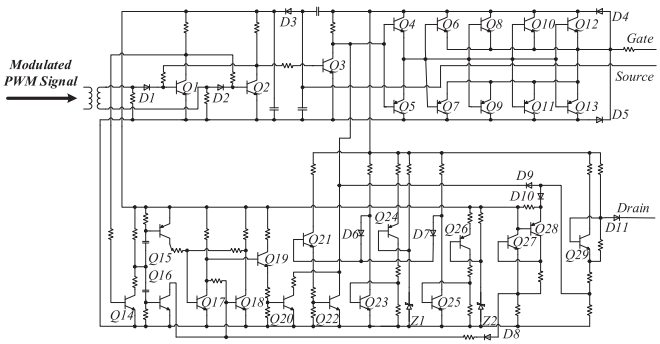

Fig. 1. Schematic of the proposed HT gate drive and protection circuit.

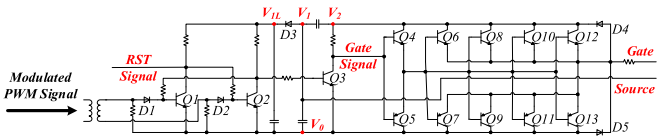

Fig. 2. Schematic of the isolation and gate drive circuit.

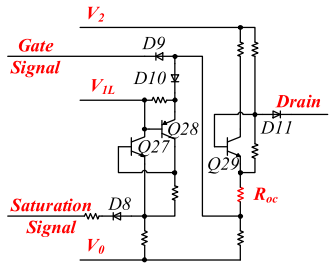

Fig. 3. Schematic of the saturation detection circuit.

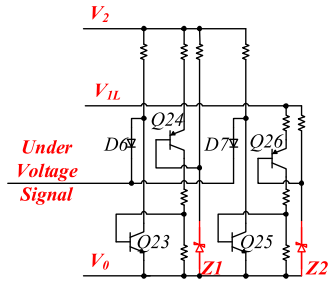

Fig. 4. Schematic of the under voltage detection circuit.

classic bipolar junction transistor circuits, the details of which will be discussed in the following sections.

Based on these principles, a prototype was built and initially tested at room temperature. Then, HT power tests were conducted in an 180 °C thermal chamber. Furthermore, a dummy load was used to investigate the proposed design's temperature dependence and stability. Finally, conclusion was drawn from the results and future work was considered.

II. Circuit Development

The proposed HT gate drive and protection circuit is presented in Fig. 1. To achieve low cost and compact size, the proposed circuit is composed of only 29 COTS HT discrete transistors. In following sections, the schematic will be broken into function blocks to discuss the operating principle in detail.

A. Gate Drive Circuit

Gate drive and galvanic isolation circuits are composed of Q_1 to Q_{13} in Fig. 2. In normal operation, the *Gate* voltage swings between V_2 and V_0, and the *Source* voltage is clamped to V_1. The logic circuit is powered by V_{1L}.

On the control electronics side, a pulse width modulation (PWM) signal from the controller is modulated to trigger pulses, where the trigger pulses are sent to the pulse transformer. On the power electronics side, a latch circuit composed of Q_1 and Q_2 catches the trigger pulses from the pulse transformer and demodulates the trigger pulses to PWM signal with a magnitude of $(V_{1L} - V_0)$. Then, the PWM signal is amplified by Q_3 and the *Gate Signal* is generated with a magnitude of $(V_2 - V_0)$. The *Gate Signal* drives Q_4 and Q_5 and Q_4 and Q_5 compose a buffer to drive Q_6 to Q_{13}. Eventually, Q_6 to Q_{13} drive the *Gate* of the driven SiC MOSFET. Since the *Source* is clamped to V_1, $V_{\rm GS}$ high is $(V_2 - V_1)$ and $V_{\rm GS}$ low is $(V_0 - V_1)$. As a result, the gate drive circuit provides both a positive and negative $V_{\rm GS}$ for the SiC MOSFET. In the schematic, the *RST Signal* is a reset signal generated for protection logic which will be further discussed in *Part D*.

B. Saturation Detection Circuit

Saturation detection is accomplished by Q_{27} to Q_{29} in Fig. 3. The saturation fault is triggered by $V_{\rm DS}$ of the driven SiC MOSFET, since $V_{\rm DS}$ of the driven SiC MOSFET increases as current increases. When an overcurrent event occurs, the level of saturation is detected by monitoring *Drain* voltage.

In the schematic, Q_{29} converts *Drain* voltage to a conditioned *Drain* voltage with a ratio set by tuning the resistance of $R_{\rm oc}$. Saturation detection is accomplished by comparing the conditioned *Drain* voltage to the logic voltage V_{1L}. Q_2 is adopted to replace a comparator circuit by using its transistor characteristic. Specifically, Q_{28} is turned ON when the conditioned *Drain* voltage at its emitter becomes higher than the reference voltage at its base. This approach significantly reduces the number of transistors required by a comparator circuit.

At *Gate Signal* high, if the conditioned *Drain* voltage becomes higher than the logic voltage V_{1L}, Q_{28} will be turned ON and saturation is detected. Consequently, Q_{27} generates a *Saturation Signal* by converting the Q_{28} collector voltage to an acceptable voltage for Q_{18} base. When the *Gate Signal* is low, the *Saturation Signal* is cleared since the conditioned *Drain* voltage is pulled down and Q_{27} is turned OFF.

C. Under Voltage Detection Circuit

Under voltage detection circuit is composed of Q_{23} to Q_{26} in Fig. 4. Zener diodes Z_1 and Z_2 are used to provide reference voltages for the specified under voltage situation. An under voltage fault is triggered when V_2 or V_{1L} falls below its corresponding reference voltage.

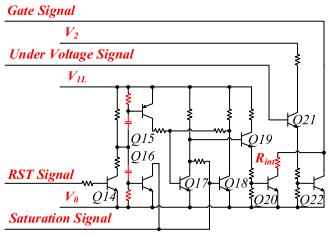

Fig. 5. Schematic of the protection logic circuit.

In the under voltage detection circuit, when V_2 drops under the Z_1 zener voltage, the base to emitter voltage of Q_{24} will be clamped to zero by resistors and Q_{23} will lose the base current provided by Q_{24}. As a result, Q_{23} is turned OFF and the *Under Voltage Signal* becomes high. After V_2 becomes higher than Z_1 zener voltage, the *Under Voltage Signal* will be back to low. The same operation principle applies to detect the under voltage of V_{1L}. As for the temperature dependence of zener diodes, in a wide temperature range of 200 °C, the maximum voltage drift is approximately 7.5% in reference to the voltage at the median temperature [31]. If the reference voltage is properly chosen, the slight voltage drift is acceptable as long as it doesn't affect the normal operation of the gate drive circuit.

D. Protection Logic Circuit

The protection logic circuit is composed of Q_{14} to Q_{22} in Fig. 5. Q_{14} to Q_{20} are designed for desaturation protection and Q_{21} and Q_{22} are placed for under voltage protection.

Q_{14} is used to synchronize the gate drive circuit and the desaturation protection circuit. When a turn-ON signal arrives, the *RST Signal* becomes high and Q_{14} is turned ON. At the Q_{14} collector, a pulse is generated to turn ON Q_{15}. Consequently, the Q_{15} collector pulls up the Q_{17} base, and the Q_{17} collector clamps the Q_{19} base to low. As a result, Q_{20} is forced to OFF status by Q_{19} and a blanking time is created at the turn-ON transient. The blanking time is set by the RC network connected to Q_{15}. When a saturation fault is detected, the *Saturation Signal* turns on Q_{18} and establishes a fault status in the latch circuit composed of Q_{17} and Q_{18}. At fault status, the Q_{18} collector is registered as low and the Q_{17} collector is registered as high. Consequently, Q_{17} turns ON Q_{19} and Q_{19} turns ON Q_{20}. When Q_{20} is ON, the Q_3 collector, *Gate Signal*, is pulled down to an intermediate voltage set by R_{int}. In this design, the intermediate voltage is adjusted to a value around *Source* voltage, V_{1L}. When a turn-OFF signal comes, Q_3 pulls down *Gate Signal* to V_0 and V_{GS} is forced to a negative value. A two-step desaturation protection scheme has been accomplished to reduce V_{GS} undershoot and V_{DS} overshoot during the turn-OFF process. Meanwhile, the *RST Signal* turns OFF Q_{14} and a pulse is generated to turn ON Q_{16}. The Q_{16} collector pulls down the Q_{18} base and Q_{18} turns ON Q_{17}. At this time, the fault status of the latch circuit is cleared, and the desaturation protection is ready for the next turn-ON signal. For under voltage protection, when *Under Voltage Signal* is high, Q_{21} is turned ON and then Q_{22}. As a result, the *Gate Signal* is immediately pulled down to V_0 and the driven SiC MOSFET is forced to OFF status.

TABLE I
MAJOR COMPONENTS SELECTION

Components	Part Number	Temperature
Transistors	Q2N2222A, Q2N2907A Q2N2219A, Q2N2905A	200 °C
Signal Diode	FDLL485B	200 °C
Zener Diode	BZV55-B15	200 °C
High Voltage Diode	DSA2-18A	180 °C

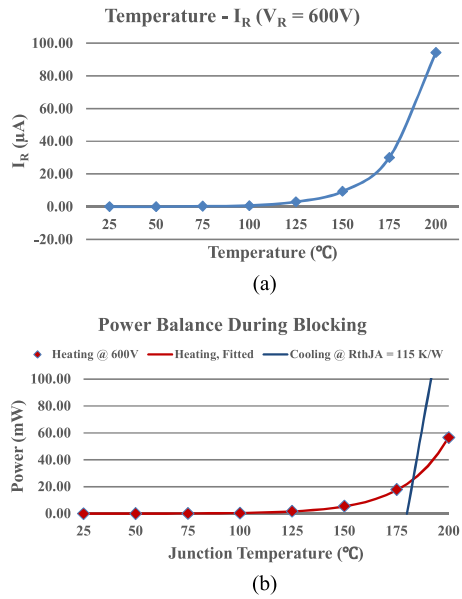

Fig. 6. (a) Leakage current and (b) power balance during blocking of DSA2-18A at 600V.

E. Prototype Development

In prototype development, component selection is contained in [18] and [19], and board material selection is well documented in [21]. As shown in Table I, all active components are COTS components, which have been massively produced and used for decades. At the time of this writing, the listed transistors are distributed at $0.928/piece at a 1k quantities [29].

The high voltage diode listed has a rated junction temperature of only 180 °C. It should be noted that for higher temperature applications, the diode can be replaced by a SiC schottky diode in a HT package and rated at low reverse leakage current. To take full advantage of the high voltage diode, the operating temperature limit of the prototype was set to its maximum of 180 °C; since the diode operates near its limit, proper deration needs to be considered. To define a proper operating condition for the high voltage diode, characterization and analysis were conducted at elevated temperatures. Results from multiple tests suggest the voltage limit to be 600 V for operating temperature around 180 °C.

Under such a condition, leakage currents at different temperatures are presented in Fig. 6(a). The highest reverse leakage current is still one order of magnitude lower than the forward conducting current, which is on the order of 1 mA. As a result, switching states are distinguishable and operating logic is still

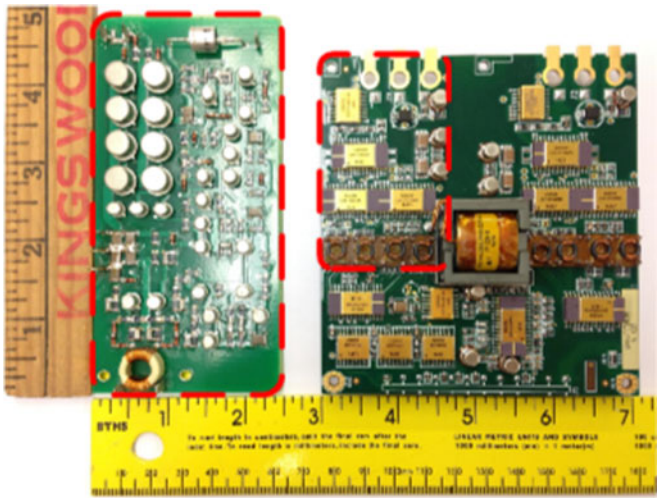

Fig. 7. Comparison of the proposed discrete component circuit (left) and the commercial IC circuit (right).

TABLE II
COMPARISON OF COMPARABLE PARTS (IN RED BOXES)

Factor	Prototype	Commercial
Size of Comparable Parts	12 in^2	4.6 in^2
Type of Active Components	COTS Discrete	HT SOI IC
Cost of Active Components	$50 in total	$2250 in total
Gate Drive	Yes	Yes
Galvanic Isolation	Yes	Yes
Desaturation Protection	Yes	Yes
Under Voltage Protection	Yes	Yes
Active Miller Clamp	No	Yes

correct. On the other hand, power balance has been investigated at the 180 °C ambient temperature. Around 180 °C, the heating power during conducting is approximately 0.6 mW, which is negligible compared to the 20-mW heating power during blocking [32]. In this case, the heating power during blocking represents total heating power. In Fig. 6(b), it is shown that the heating and cooling power reach a balance at junction temperature around 183 °C, which is slightly higher than the rated junction temperature. As a result, thermal runaway does not happen and the high voltage diode is still usable with a potential deration of lifetime.

In Fig. 7, the proposed circuit is compared to a commercial circuit built with HT SOI ICs in [14]. The comparable parts are highlighted in red boxes. A comparison of comparable parts is summarized in Table II. Although the size of the proposed circuit is optimized by cutting auxiliary protection functions and communication channels, the size of the proposed circuit is still 2.6 times as large as the size of the commercial circuit. However, the cost of the proposed circuit is less than 10% of the cost of the commercial circuit [29], [30]. Overall, the major functions are achieved at a competitive cost.

III. EXPERIMENTAL EVALUATION

In experimental evaluation, the prototype was tested in room and high temperature environments. The test schematic and setup are shown in Fig. 8(a) and (b). The ceramic capacitor dc link is composed of AVX SXP47C105KAA rated at 500 V, 200 °C. The SiC power MOSFET module is CREE CAS300M12BM2 rated at 1200 V, 300 A, and 150 °C. For operation at 180 °C, the lifetime of CAS300M12BM2 is definitely compromised. However, no failure has been observed during experiments in 180 °C environments. The performance is acceptable for the purpose of gate drive and protection circuit evaluation.

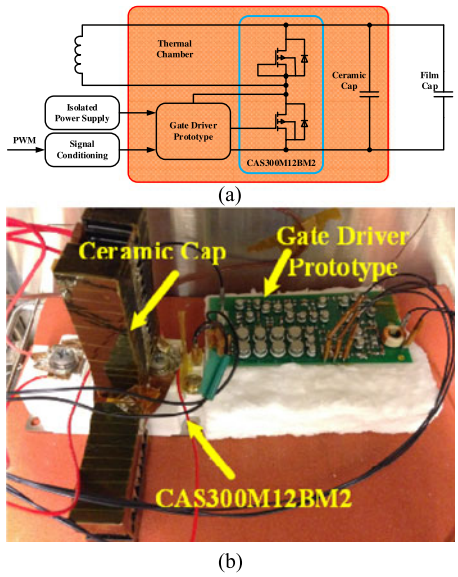

Fig. 8. (a) Schematic and (b) photograph of the circuit under test.

When the proposed circuit was tested in the thermal chamber, $V_{\rm GS}$, $V_{\rm DS}$, and I_D were measured by probes placed outside of the thermal chamber since HT probes were not available. I_D was directly measured from the load inductor outside the thermal chamber. $V_{\rm GS}$ and $V_{\rm DS}$ were measured through HT wires connected to test points in the thermal chamber. The effect from these wires was evaluated by comparing the thermal chamber tests to additional test conducted outside the chamber.

The environment temperature was monitored and recorded by OMEGA data logger RDXL4SD with original Type K thermocouple probe. During the tests, temperatures were recorded every minute. The recorded temperature is hardly affected by switching noise since double pulse and overcurrent tests are not continuous operating tests. Experimental results of continuous operating tests can be found in a relevant publication [33].

A. Room Temperature Evaluation

At room temperature, the double pulse test waveform is shown in Fig. 9(a) and (b). Fig. 9(a) was recorded by directly measuring the circuit outside the chamber. Fig. 9(b) was obtained by measuring HT wires connected to the circuit in the chamber. Once the wires were added to facilitate measurement in the chamber, the observed oscillation on $V_{\rm GS}$ and $V_{\rm DS}$ became stronger during switching at nonzero current. This was due to a large amount of noise induced in the wires. However, for the purpose of circuit evaluation, the results are still acceptable as long as the oscillation does not cause false switching transients.

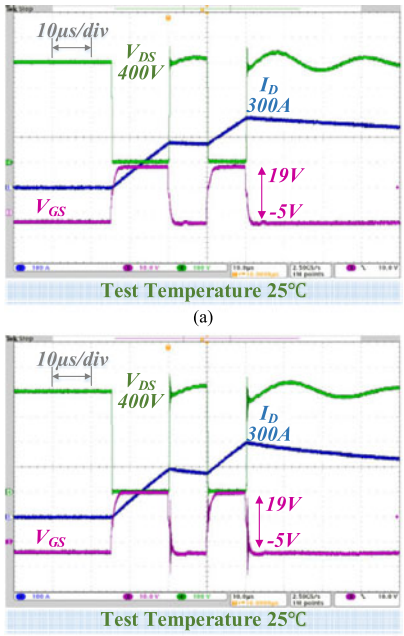

Fig. 9. Room Temperature double pulse test waveform from (a) directly testing the circuit out of the thermal chamber, and (b) measuring through HT wires connected to the circuit in the thermal chamber.

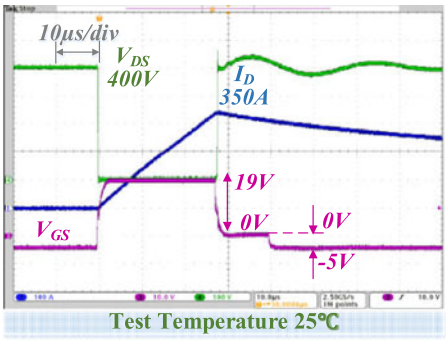

Fig. 10. Room temperature overcurrent test waveform.

The desaturation protection waveform is presented in Fig. 10. When the defined overcurrent occurred, $V_{\rm GS}$ was pulled down to an intermediate voltage 0 V, set by $R_{\rm int}$ in Fig. 5, and then pulled down to off-state voltage, -5 V. The desaturation protection turned OFF the SiC MOSFET with a two-step scheme. Compared to the oscillation during the turn-OFF process from Fig. 9(b), though the turn-OFF process occurred at higher current in Fig. 10, the oscillation from $V_{\rm GS}$ and $V_{\rm DS}$ was successfully reduced to lower amplitude by the two-step protection scheme.

The measured trigger voltages for under voltage protection were 17.1 V for $(V_2 - V_0)$ and 4.2 V for $(V_1 - V_0)$. When under voltage fault was detected, the gate voltage was clamped to V_0 immediately.

B. High Temperature Evaluation

At 180 °C ambient temperature, the prototype was evaluated by a double pulse test and an overcurrent test. At 180 °C, the driven SiC MOSFET causes more voltage drop at the same current

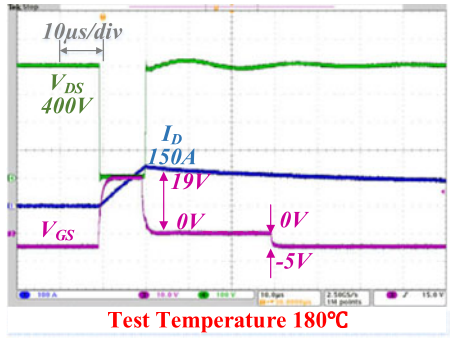

Fig. 11. HT overcurrent test waveform.

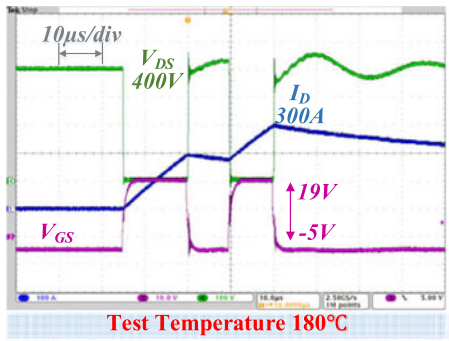

Fig. 12. HT double pulse test waveform after $R_{\rm oc}$ is tuned.

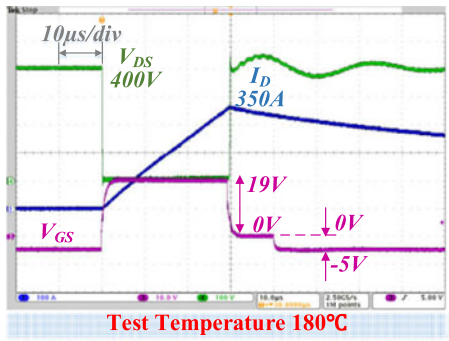

Fig. 13. HT overcurrent test waveform after $R_{\rm oc}$ is tuned.

value since its on-resistance increases with increasing temperature [34]. As a result, the desaturation protection is triggered at a lower current value, which is presented in Fig. 11.

In following tests at 180 °C, $R_{\rm oc}$ in Fig. 3 was tuned to a proper value so that the defined overcurrent value at 180 °C became close to that at room temperature. The double pulse test waveform is shown in Fig. 12 and the desaturation protection waveform is presented in Fig. 13. Once overcurrent occurred, the two-step protection scheme forced $V_{\rm GS}$ to 0 V and eventually pulled down $V_{\rm GS}$ to -5 V.

The measured trigger voltages for under voltage protection were 17.9 V for $(V_2 - V_0)$ and 3.5 V for $(V_1 - V_0)$. Compared to those values at room temperature, the trigger voltage for $(V_2 - V_0)$ was increased and the trigger voltage for $(V_1 - V_0)$ was decreased at 180 °C. That is mainly caused by temperature drifts in working voltages of the zener diodes [31].

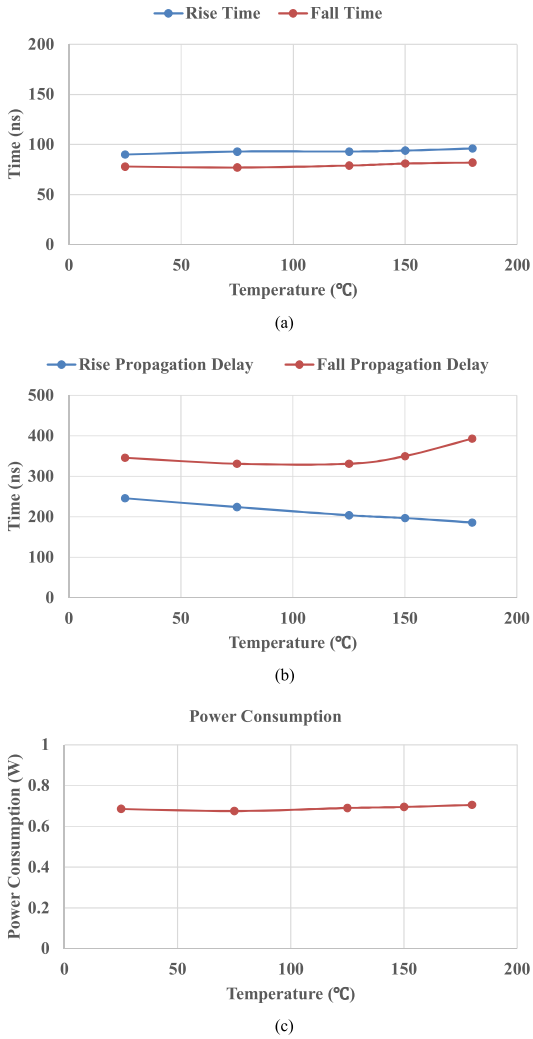

Fig. 14. Evaluation of temperature dependence (a) rise/fall time (b) rise/fall propagation delay (c) power consumption.

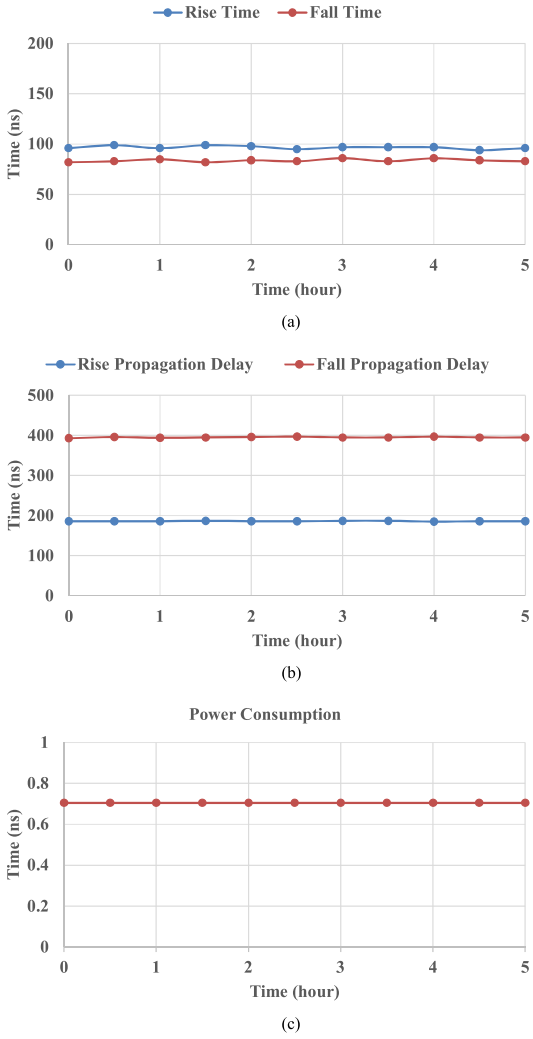

Fig. 15. Evaluation of stability (a) rise/fall time (b) rise/fall propagation delay (c) power consumption.

Specifically, temperature coefficients are negative for zener diodes with working voltages lower than 5.6 V and positive for zener diodes with higher working voltages. Overall, the temperature drifts in trigger voltages are acceptable since they do not affect the normal operation as shown in Figs. 12 and 13.

C. Evaluation of Temperature Dependence and Stability

The prototype was evaluated by driving a dummy load ($R_G = 5\Omega$, $C_{\text{load}} = 10\,\text{nF}$) at a frequency of 10 kHz and a duty ration of 50%. Temperature dependence was obtained by testing the prototype from 25 °C to 180 °C. Stability was validated by testing the prototype at 180 °C for 5 h. Rise/fall time, rise/fall propagation delay, and power consumption of the prototype were recorded in Figs. 14 and 15.

Fig. 14 presents temperature dependence of the prototype. From 25 to 180 °C, the rise time is increased slightly from 90 to 96 ns and the fall time is increased from 78 to 82 ns. Meanwhile, the rise and fall delay times vary with the changing temperature. The range of rise delay time is from 186 to 246 ns. The range of fall delay time is from 331 to 393 ns. The variation is less than 62 ns. The change of power consumption is less than 50 mW.

Fig. 15 shows stability of the prototype at 180 °C ambient temperature. In 5 h, the variation of rise time is less than 5 ns, and the variation of fall time is less than 4 ns. Meanwhile, the variation of rise delay time is less than 2 ns, and the variation of fall delay time is less than 4 ns. The variation of power consumption is less than 25 mW.

IV. Conclusion and Future Work

By using COTS HT discrete components, a gate drive and protection circuit was proposed and developed. The performance of the prototype was validated by driving and protecting a 1200-V 300-A SiC MOSFET module at 180 °C ambient temperature. Additionally, temperature dependence and stability were evaluated over temperature and time.

Compared to other solutions, the proposed circuit does not need any HT SOI ICs. Furthermore, the proposed circuit also achieves most functions of a commercial circuit using HT SOI ICs. As a result, the proposed circuit significantly reduces the

number of active components and successfully removes the barrier of HT gate drive circuits, high cost.

With the proposed circuit, performance of SiC MOSFETs can be evaluated at high temperature and low cost. Meanwhile, great cost reduction is also expected in prototyping of HT power electronics circuits. In future work, a three-phase inverter will be developed for HT operation where the cost reduction will be scaled by six.

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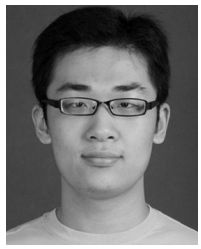

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