Conducted EMI Mitigation Schemes in Isolated Switching-Mode Power Supply Without the Need of a Y-Capacitor

Yongjiang Bai, *Student Member, IEEE*, Xu Yang, *Member, IEEE*, Dan Zhang, Xinlei Li, Wenjie Chen, *Member, IEEE*, and Weihao Hu, *Senior Member, IEEE*

***Abstract*—In order to construct a low-impedance loop for common-mode electromagnetic interference (EMI) signals, traditional method is to use Y-capacitors as filtering components. However, in the commonly used isolated ac–dc switching-mode power supplies (SMPS), the Y-capacitors branch also behaves as a terrible leakage current loop. For the safety of human beings, this leakage current is not allowed in commercial used equipment, such as chargers, medical instruments, etc. Therefore, certain works should be done to both acquire good EMI performance and satisfy the strict leakage current limitation. The goal of this paper is try to meet these two demands at the same time. In this paper, a novel non-Y-capacitor EMI design concept for SMPS is proposed for the first time. By getting rid of traditional EMI filtering component—the Y-capacitors, the leakage current can be eliminated entirely. Meanwhile, to face with EMI design challenge, optimized transformer architecture is presented. Analysis of the transformer architecture as well as the auxiliary winding has been carried out. Then, a novel topology suitable for non-Y-capacitors converter is proposed and the design procedure of the proposed topology is discussed in detail. The proposed concept is applied to several popular converter topologies. The experiment results demonstrated the effectiveness and feasibility of the proposed non-Y-capacitor design schemes.**

***Index Terms*—Balanced-winding topology, common-mode noise, electromagnetic interference (EMI), non-Y-capacitor, transformer architecture.**

I. Introduction

ELECTROMAGNETIC interference (EMI) filters have been widely used for decades to solve conducted EMI problems for switching-mode power supplies. However, the common-mode Y-capacitor filtering components will also introduce an unsafe by-pass for the low-frequency (50 Hz) current for many battery charger applications. On the one hand, consumer who uses a charging cell phone with a metal case will have the risk of getting an electric shock due to the existence of Y-capacitor branch. On the other hand, the leakage current will also affect the performance of the touch screen too. To protect the safety of human beings and to prevent the user from becoming part of a path for leakage current, strict leakage current standards were developed. Table I shows some leakage current limits for IT equipment [1], [2].

TABLE I
Maximum Leakage Current

Equipment		Condition	Limit
Information Technology (IEC60950)	All equipment	From protective earth ground to accessible parts not connected to protective ground	0.25 mA
	Handheld	From protective earth ground terminal (earth conductor) to protective ground	0.75 mA
	Portable	From protective earth ground terminal (earth conductor)to protective ground	3.5 mA
	Stationary		
Medical (IEC60601-1)		Patient leakage	100 μA

TABLE II
Test Results of Leakage Current Relationship With Value of Y-Cap

Capacitance of Y-caps	3300 pF	2200 pF	1000 pF	470 pF
Leakage current	1.02 mA	0.94 mA	0.43 mA	0.34 mA
Capacitance of Y-caps	220 pF	100 pF	Non-Y-caps	–
Leakage current	0.29 mA	0.21 mA	0.075 mA	–

Traditional method to minimize this kind of leakage current is to use small-scale EMI filter by-pass components. Table II shows a tested result of the relationship between leakage current and Y-capacitor value based on a 5-V 2.1-A power supply. It can be seen if smaller value Y-capacitors are used, larger impedance of the Y-cap branch will be achieved. Therefore, the value of leakage current will become smaller. However, limited Y-cap value will inevitably result in EMI design challenge for the whole system. During the past decade, various types of EMI solutions, based on improved converter topologies [3]–[5], controlling or modulation algorithm [6]–[8], driving schemes [9]–[12], and filtering methods [13]–[18] have been reported. Based on 1000–2000-pF limited Y-cap value, the EMI noise can either be reduced from the beginning of the noise source [3]–[12] or be blocked from the coupling path [13]–[30]. These publications are very important to power electronics and EMI

Manuscript received February 2, 2016; revised April 14, 2016; accepted May 31, 2016. Date of publication June 10, 2016; date of current version January 20, 2017. This work was supported by the National Natural Science Foundation of China under Project 51277145. Recommended for publication by Associate Editor F. Costa.

Y. Bai, X. Yang, and W. Chen are with the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: baiyj@mail.xjtu.edu.cn; yangxu@mail.xjtu.edu.cn; cwj@mail.xjtu.edu.cn).

D. Zhang and X. Li are with Silergy, Corp., Xi'an 710075, China (e-mail: zhangdan-1023@163.com; matt_x_lee@163.com).

W. Hu is with the Department of Energy Technology, Aalborg University, Aalborg 9100, Denmark (e-mail: whu@et.aau.dk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2579679

research. Nevertheless, there is still a lack of manuscript which treats the EMI noise and leakage current simultaneously, or could acquire both excellent leakage current value and good EMI performance. In [25], a shielding-cancelation technique is presented by combining the shielding technique and the winding cancelation method together. The shielding layer is adjusted to have the same turn number and winding direction with its adjacent windings. However, using shields may lead to large power losses, and this is not practical in the structure of multiple-layer transformer windings because many of the shields are needed. In [17], a redesign of low-power single- phase EMI filter where less than 100 μA of leakage current is presented. A 3-Y capacitor method is suggested by using additional capacitor in series with the existing Y-capacitor between phase and ground. Although the leakage current is diminished to meet the standard, this makes the system complex with increased cost and size. Moreover, this is not a common method for all the switching-mode power supply application. In a word, it is widely believed that this line of research has not yet been reached completely.

In this paper, a novel non-Y-cap EMI design concept is proposed. There is not any common-mode grounding path in the proposed EMI filter structure. The motivation of this study is to first get rid of the by-pass EMI components in order to eliminate the leakage current which flows through it. Then, to deal with the EMI challenge, an efficient non-Y-cap EMI mitigation design procedure is put forward on. The novelty of the proposed method lies in two aspects. On the one hand, it could reduce the EMI noise passively. That is, optimized transformer architecture is presented, which is able to reduce the EMI noise from transmission path. On the other hand, the proposed method could minimize the EMI noise actively. That is, a novel topology suitable for non-Y-capacitor converter is proposed to solve the EMI issue from the noise source. This method has the merit of low cost and easy to be fabricated in massive production.

This paper is organized as follow: Section II discusses the motivation for reduction of Y-capacitor in medical and handheld or some dedicated portable equipment in detail. Then, non-Y-cap EMI design concept is proposed. Section III describes optimized transformer structure to reduce the conduction EMI noise. Section IV proposes a new topology with balanced winding which has excellent conducted EMI performance, and the experimental results are presented in Section V. Section VI is the conclusion of this paper.

II. Motivation and Proposed Design Procedure for Non-Y-capacitor Design

A. Case A. Charger Interference to Touch Screen

Touch screen has been widely used in many applications, such as industrial control computers, mobile phone, PDA, GPS, PMP, MP3, MP4, etc. There are mainly eight different touch screen technologies which can be sorted in two types according to whether they need Indium Tin Oxide (ITO) or not. At present, resistance type and surface capacitive which need the ITO are widely used. Multitouch operation based on surface capacitive type can be implemented by calculating the fingers position according to capacitance change. In this kind of applications,

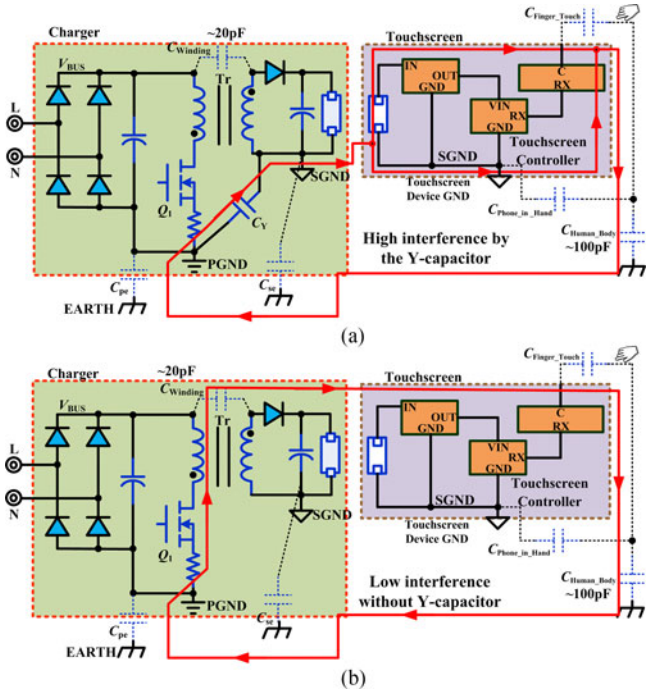


Fig. 1. Charger interference coupling mode. (a) With Y-capacitor. (b) Without Y-capacitor.

the EMI has to be considered to prevent the interference to the system.

The charger of the touch screen device is a potential interference source. As shown in Fig. 1(a), the interference can be coupled to the touch screen by the finger when people using the phone which is connected to the charger in the wall. If the charge has two-wire ac input connector without connecting to the power ground, the finger including the human body turns to be a low-impedance return path of the charger EMI interference. With the low impedance of Y-capacitor, C_Y, there will be a high interference loop shown by the red arrow mark in Fig. 1(a). If there is no Y-capacitor in the system, the charger interference is only coupled by the transformer parasitic capacitors (~20 pF) between the primary windings and the secondary windings. Due to high impedance of transformer parasitic capacitors, C_{winding}, there will be only a low interference loop shown by the red arrow mark in Fig. 1(b). This kind of little capacitance coupling can be cancelled by the charger and equipment itself parasitic capacitors in paralleled. However, if a Y-capacitor is added between the primary winding and secondary winding in the charger, the coupling is impossible to be cancelled by the parasitic capacitor of the portable device. The interference is easy to be transferred to the portable device with this low-impedance loop, and the normal working of touch screen may be interrupted. If the portable device is operated with multifingers of people on the touch screen, the interference will turn to be even more serious.

In order to improve the electromagnetic susceptibility performance, the Y-cap is not allowed to use in chargers from the world-famous company, such as Apple, Samsung, and Huawei, etc. So, a non-Y-cap EMI design for SMPS is urgent for the need of market.

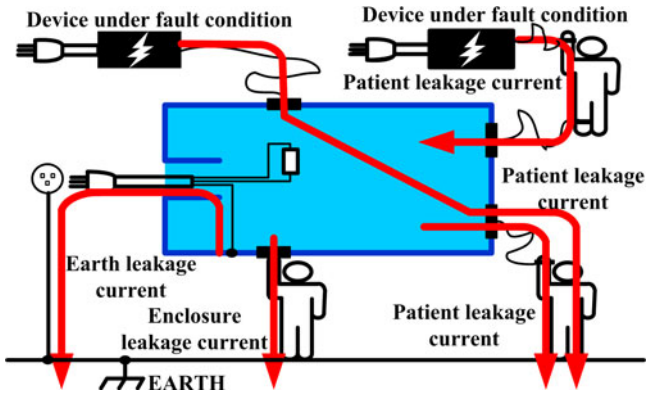


Fig. 2. Leakage current test mode in the medical equipment.

TABLE III
LEAKAGE CURRENT AND PATIENT AUXILIARY CURRENT (μA)

Leakage current (LKC)	B Type		BF Type		CF Type	
	Normal State	Single Failure State	Normal State	Single Failure State	Normal State	Single Failure State
Earth LKC	5	10	5	10	5	10
Enclosure LKC	100	500	100	500	100	500
Patient ac LKC	100	500	100	500	10	50
Patient dc LKC	5	50	5	50	5	50
Patient Aux. dc current	5	50	5	50	5	50
Patient Aux. ac current	100	500	100	500	10	50

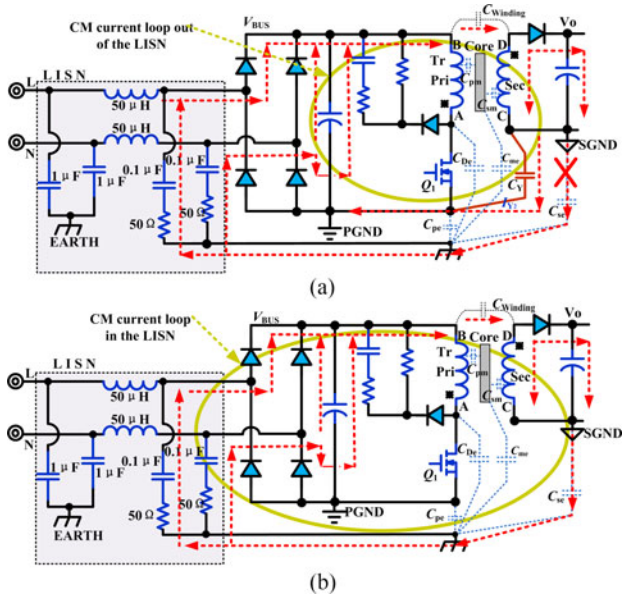


Fig. 3. Shunting effects of C_Y for the CM noise when Q_1 is being turned-off: (a) With Y-capacitor. (b) Without Y-capacitor.

B. Case A. Charger Interference to Touch Screen

As we know, the quality of the power supply will influence the stability and reliability of the medical equipment. Bad power source will even lead to medical accidents and cause huge economic losses.

The case of the most medical equipments can be touched easily since it is installed very close to the patient and operator. Security and isolation of power supply are two significant specifications compared with the commonly used power supply. The isolation voltage between input and output should be more than 4000 V and the leakage current should be as low as possible to meet the requirements. The leakage current test mode in the medical equipment is shown in Fig. 2. Generally, the leakage current limitation of medical equipments defined in the IEC601 standard is only one-tenth of that of the commonly used power supply, and it is lower than 100 μA as described previously. The maximum leakage current is defined for three main types of power supply equipment as follow.

1) Class B—No electrical contact with patient and maybe earthed.
2) Class BF—Electrically connected to patient but not directly to heart.
3) Class CF—Electrically connected to the heart of patient.

The detail leakage current limitation is shown in Table III. As we known, the Y-capacitors branch behaves as a terrible leakage current loop. So in the medical equipment switching power supply, the Y-capacitor is limited to a very small value. Or it is even been prohibited in order to prevent the patients and medical personnel to get an electric shock. Meanwhile, the power supply should pass the standards, such as FCC-B, CISPR22-B, EN55011/EN55022/61204/61000, etc. In order to eliminate the leakage current and obtain better EMI performance, non-Y-cap EMI design is urgent in the power supply for medical equipment.

C. Impact of Y-capacitors on the EMI Noise and Stabilization

Differential mode (DM) noise is mainly caused by the pulsating converter current, and is attenuated by the input filter capacitor. Since this capacitor is generally an electrolytic one with large ESL and ESR, it is only effective for the reduction of DM noise up to the switching frequency [31]. The DM noise current is not changed if adding or removing the Y-capacitor and only the CM noise current is related to the Y-capacitor. In this paper, the non-Y-cap design is focused, so the CM noise is analyzed, measured, and compared in following sections.

It is well known that CM conducted EMI is caused by the CM current flowing through the parasitic capacitance of transistors, diodes, and transformers to earth in the power circuit. The CM noise is accounted by the current flowing through the line-impedance stabilization network (LISN) resistor as shown in Fig. 3(a). To find solution to reduce the CM current, the secondary-side CM noise current propagation path is also illustrated. When a Y-capacitor C_Y is added between the primary return terminal PGND and secondary return terminal SGND, the CM noise current will change original path from C_{se} to C_Y and it changes to be the DM noise which is much easier to be solved by the filter. By means of this method, the CM noise has low impedance with C_Y branch and better EMI performance can be acquired. On the contrary, if the Y-capacitor is removed for the leakage current standard requirements, all the CM noise has only one path through the C_{se}, and this will cause the worse EMI results as shown in Fig. 3(b).

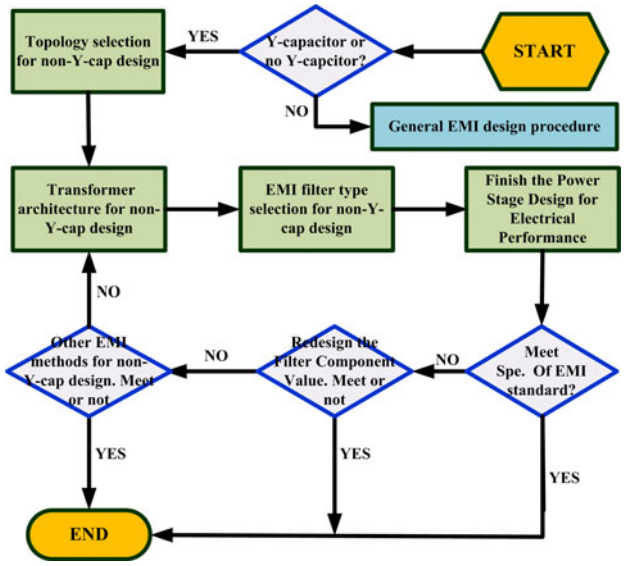


Fig. 4. Proposed design procedure for the non-Y-cap SMPS.

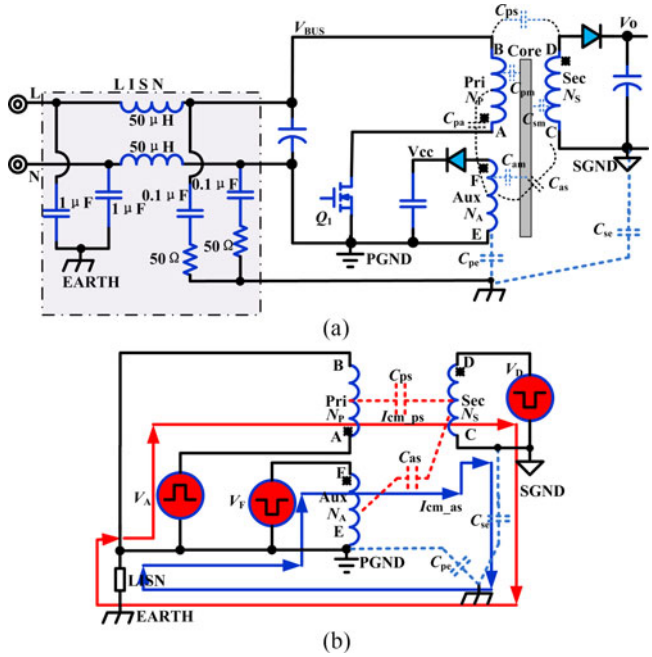


Fig. 5. Flyback converter: (a) Simple CM noise source model of (b) Major paths for the CM noise current from primary to secondary side.

In the non-Y-cap SMPS design, although the leakage current is eliminated sharply, the EMI will be worse than the SMPS with Y-capacitor. So, it is urgent to find a non-Y-cap EMI design method for SMPS.

D. Proposed EMI Design Procedure for Non-Y-capacitor SMPS

In the non-Y-cap EMI design, it is both very difficult and expensive to solve the EMI problem based on the traditional EMI design process. In order to obtain a better EMI performance, a brand new design procedure is proposed in this paper as shown in Fig. 4. First, whether it is necessary to carry out a non-Y-cap design for a SMPS should be fully understood. If not, it will be fine to follow the general EMI design procedure. If yes, the topology has to be selected considering the EMI. The control and driving unit is also needed to be selected considering the EMI performance. Thus, the transformer architecture suitable for EMI reduction is applied and the EMI filter to suppress the CM noise is designed. Then, the electrical performance of SMPS is optimized to meet the specification. After that the EMI is checked whether it can meet the standard. If not, then redesign the EMI filter or other method suitable for the non-Y-capacitor should be applied until it passes the EMI certification.

In this paper, following the proposed design procedure, two effective methods, one is to reduce EMI noise passively, one is able to reduce the EMI noise from transmission path, are applied for the non-Y-cap SMPS design. Excellent EMI performance can be obtained as well as the leakage current at microampere level.

II. Optimizing Transformer Structure to Reduce CM Noise for Non-Y-Cap EMI Design

The transformer provides power transmission path and galvanic isolation for SMPS. However, it is a key EMI noise source of the power supply. In order to reduce this noise, corresponding research has been studied on the transformer parasitic capacitance analysis. For simplification, this paper takes the flyback converter as an example. In a flyback converter, the transformer has three windings, such as primary winding, secondary winding, as well as auxiliary winding. Sandwich structure transformer is very popular in those applications for its smaller leakage inductance and higher efficiency. However, for the non-Y-cap design, this means much larger parasitic capacitance which is harm to reduce the CM noise. On the contrary, the non-sandwich has smaller parasitic capacitance and it means better EMI. So following analysis is based on nonsandwich transformer structure.

In most applications, the CM noise of a power converter is dominated by displacement currents which are the results of voltage pulsating (*dv/dt*) on the converter parasitic capacitances. In an isolated power converter, the interwinding capacitances of power transformer are critical parasitic capacitances of the converter in the CM noise perspective. Such capacitances are distributed along the windings with different voltage pulsating (*dv/dt*) [21]. The CM noise current generated by the noise sources propagates through interwinding capacitance of the transformer and goes into LISN through the grounding wire of secondary side output, as shown in Fig. 5(a).

The total CM noise current going through the interwinding capacitors is determined by the distribution of voltage pulsating along the windings. It is determined by both the voltage pulsating on the transformer terminals and the winding structure of the transformer. The CM noise current introduced by the voltage pulsating can be calculated as in following equation [23]:

$$i_{\mathrm{cm}} = \Sigma C \frac{dv}{dt}. \tag{1}$$

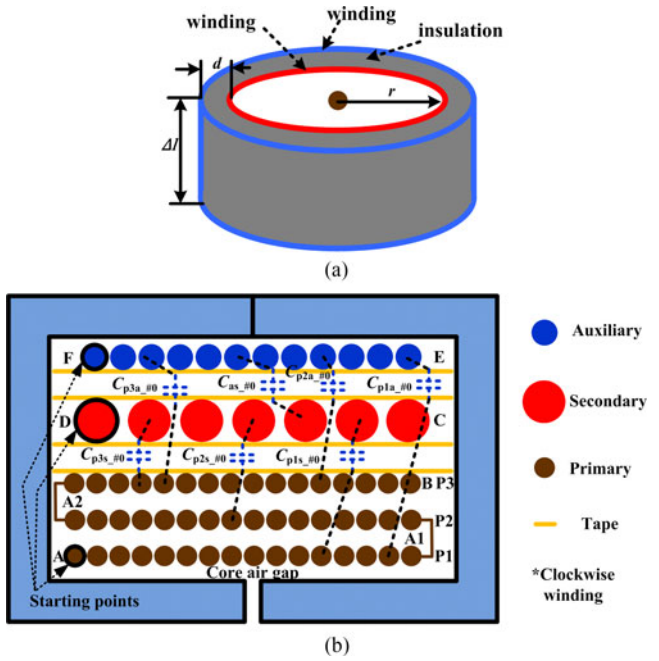


Fig. 6. (a) Model of two adjacent winding layers. (b) Parasitic capacitors of two adjacent winding layers of transformer #0.

There are distributed parasitic capacitances between every two layers. Those capacitances between primary winding layers or between primary winding and auxiliary winding do not contribute to the CM noise because the displacement currents between them are confined within the primary side of the converter. These parasitic capacitors only contribute to the DM noise current. So the displacement current of primary winding to the auxiliary winding $C_{\rm pa}$ does not contribute to the CM noise current. The distributed parasitic capacitances $C_{\rm ps}$ between primary winding and secondary winding, $C_{\rm as}$ between auxiliary winding to secondary winding provide the major paths for the CM noise current from primary to secondary side of the converter as shown in Fig. 5(b). This paper only focuses on primary side to the secondary side which related to the Y-capacitor between them.

It is easy to calculate the *dv/dt* of the winding pulse voltage to the earth ground. How to evaluate the capacitance is key problem here. As presented in [32]–[34], the two adjacent winding layers can be modeled as two conductors of the shape of a hollow cylinder which share the same center as shown in Fig. 6(a). The space between them is filled with insulation material. Parasitic capacitance ΔC between them can be calculated as follows:

$$\Delta C = \varepsilon_{\rm r} \frac{2\pi r \Delta l}{d} \tag{2}$$

where $\varepsilon_{\rm r}$ is the permittivity of the insulation material between layers. Δl is the height of the winding layer, and d is the distance between two winding layers.

To verify above assumption, the half window of the transformer #0 with the three different windings is illustrated in Fig. 6(b). The primary winding is evenly divided into three layers. Meanwhile, the auxiliary winding and secondary winding are distributed symmetrically in a standalone layer. The terminals A, D, and F are dotted terminals. Based on above transformer architecture, the interwinding capacitance can be measured as follows in Table IV.

TABLE IV
MEASUREMENT RESULTS OF INTERWINDING PARASITIC CAPACITOR VALUE

Parasitic capacitors	$C_{\rm p1s\_\#0}$	$C_{\rm ps\_\#0}$ $C_{\rm p2s\_\#0}$	$C_{\rm p3s\_\#0}$	$C_{\rm as\_\#0}$
Capacitor value	16 pF	18.3 pF	20.7 pF	24.4 pF
Average capacitor value		19.8 pF		
Parasitic capacitors	$C_{\rm p1a\_\#0}$	$C_{\rm pa\_\#0}$ $C_{\rm p2a\_\#0}$	$C_{\rm p3a\_\#0}$	–
Capacitor value	11.3 pF	11.8 pF	12.4 pF	–
Average capacitor value		12 pF		

According to [23], the capacitor between the winding and core can be neglected due to the smaller capacitance, and the primary winding inner layers capacitors can also be neglected because they do not contribute to the CM noise. So only capacitors between different windings should be considered and analyzed. According to the current formula of capacitor $I_C = C * dv/dt$, the displacement current between primary side and secondary side only depends on the voltage jump slope and the parasitic capacitor value. First, to analyze the intercapacitor between windings, in Fig. 7(a), the half window of the transformer #1 with the three different windings is illustrated. The primary winding is evenly divided into three layers. Meanwhile, the auxiliary winding and secondary winding are distributed symmetrically in a standalone layer. The terminals A, D, and F are dotted terminals, while identify the positive current orientation by the voltage between two winding layers from high to low.

Supposing the positive current orientation is from primary side to the secondary side, if the current orientation is opposite to the positive current orientation, then adds a minus before plus to the total current.

When the Q_1 is in switching mode, point A can be considered as a pulse voltage source which the amplitude is $V_{\rm A}$ from turned-on state to turned-off state, and it can be expressed following:

$$V_{\rm A} = V_{\rm BUS} + V_{\rm O} * \frac{N_{\rm P}}{N_{\rm S}} \tag{3}$$

where $V_{\rm BUS}$ is the rectified voltage of the flyback converter, $V_{\rm O}$ is the output voltage of the flyback converter. The $N_{\rm P}$ and $N_{\rm S}$ are turns of primary winding and secondary winding, respectively.

Similarly, the point D can be considered as a pulse voltage source which the amplitude is $V_{\rm D}$ from turned-on state to turned-off state, and it can be expressed as follows:

$$V_{\rm D} = V_{\rm O} + V_{\rm BUS} * \frac{N_{\rm S}}{N_{\rm P}} = V_{\rm A} * \frac{N_{\rm S}}{N_{\rm P}}. \tag{4}$$

In the same way, the point F can also be considered as a pulse voltage source which amplitude is $V_{\rm F}$ from turned-on state to turned-off state, and it can be expressed following:

$$V_{\rm F} = V_{\rm O} * \frac{N_{\rm A}}{N_{\rm S}} + V_{\rm BUS} * \frac{N_{\rm A}}{N_{\rm P}} = V_{\rm A} * \frac{N_{\rm A}}{N_{\rm P}} \tag{5}$$

where $N_{\rm A}$ is the turn's of auxiliary winding.

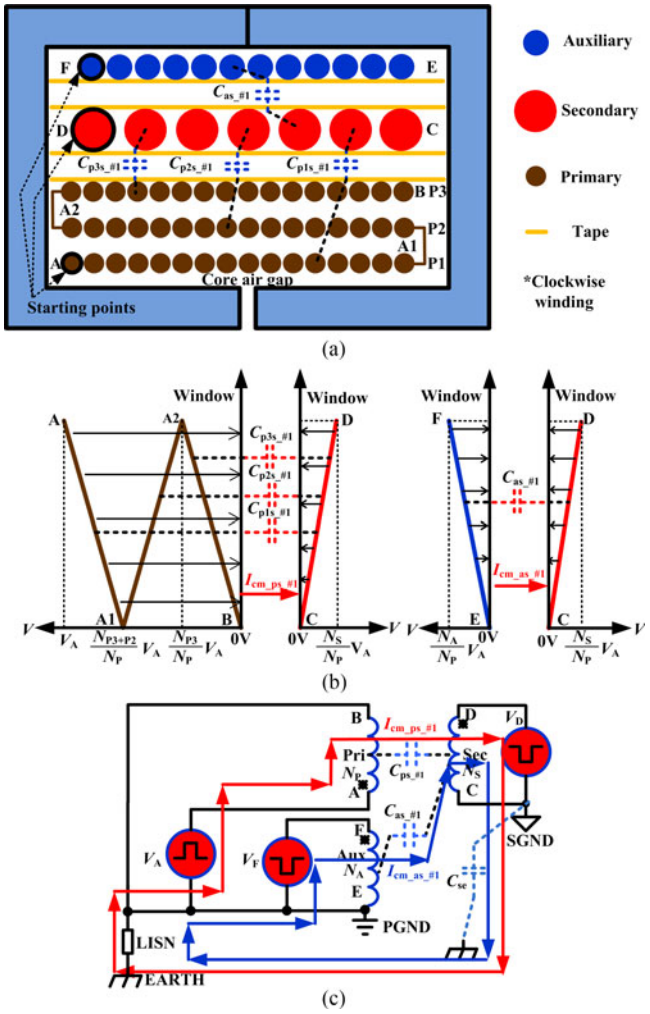


Fig. 7. Transformer #1: (a) Interwinding. (b) Voltage and current distribution. (c) CM current propagation.

The voltage distribution of the three windings is shown in Fig. 7(b). When the Q_1 is turned off, the voltage of points A, F, and D is rising up relative to points B, E, and C, respectively. By means of the above equations, the displacement current propagation path is shown by the arrow in Fig. 7(c).

The displacement current between primary winding and the secondary winding is given as

$$\begin{aligned} I_{\mathrm{cm\_ps\_\#1}} = & \frac{C_{\mathrm{p3s\_\#1}}}{2}\left(\frac{N_{\mathrm{P3}}}{N_{\mathrm{P}}}\frac{V_{\mathrm{A}}}{\Delta t}-\frac{N_{\mathrm{S}}}{N_{\mathrm{P}}}\frac{V_{\mathrm{A}}}{\Delta t}\right) \\ & +\frac{C_{\mathrm{p2s\_\#1}}}{2}\left(\frac{N_{\mathrm{P3}}+N_{\mathrm{P2}}+N_{\mathrm{P3}}}{N_{\mathrm{P}}}\frac{V_{\mathrm{A}}}{\Delta t}-\frac{N_{\mathrm{S}}}{N_{\mathrm{P}}}\frac{V_{\mathrm{A}}}{\Delta t}\right) \\ & +\frac{C_{\mathrm{p1s\_\#1}}}{2}\left(\left(\frac{N_{\mathrm{P3}}+N_{\mathrm{P2}}}{N_{\mathrm{P}}}+1\right)\frac{V_{\mathrm{A}}}{\Delta t}-\frac{N_{\mathrm{S}}}{N_{\mathrm{P}}}\frac{V_{\mathrm{A}}}{\Delta t}\right) \end{aligned} \quad (6)$$

where $N_{\mathrm{P1}}, N_{\mathrm{P2}}$, and N_{P3} are turns of three primary winding layers from inner to outer, respectively. $C_{\mathrm{p1s\_\#1}}, C_{\mathrm{p2s\_\#1}}$, and $C_{\mathrm{p3s\_\#1}}$ are parasitic capacitors between the three primary winding layers from inner to outer and secondary winding, respectively. Δt is the transient time of the voltage jumping.

The displacement current between auxiliary winding and the secondary winding is also given as follows based on the same analysis method

$$I_{\mathrm{cm\_as\_\#1}} = \frac{C_{\mathrm{as\_\#1}}}{2}\left(\frac{N_{\mathrm{A}}}{N_{\mathrm{P}}}\frac{V_{\mathrm{A}}}{\Delta t}-\frac{N_{\mathrm{S}}}{N_{\mathrm{P}}}\frac{V_{\mathrm{A}}}{\Delta t}\right) \quad (7)$$

where $C_{\mathrm{as\_\#1}}$ is the parasitic capacitor between the auxiliary winding and secondary winding.

Some assumptions are made to simplify the equations according the physical distance between different layers as follows:

$$\begin{aligned} C_{\mathrm{p3s\_\#1}} &= C_{\mathrm{as\_\#1}}, C_{p2s\_\#1} = \frac{C_{\mathrm{as\_\#1}}}{2}, C_{\mathrm{p1s\_\#1}} = \frac{C_{\mathrm{as\_\#1}}}{3} \\ N_{\mathrm{P1}} &= N_{\mathrm{P2}} = N_{\mathrm{P3}} = \frac{N_{\mathrm{P}}}{3}. \end{aligned} \quad (8)$$

Substituting (8) into (6) and (7), the total displacement current from primary to secondary can be expressed by

$$\begin{aligned} I_{\mathrm{cm\_\#1}} &= I_{\mathrm{cm\_ps\_\#1}} + I_{\mathrm{cm\_as\_\#1}} \\ &= C_{\mathrm{as\_\#1}}\left(0.694+0.5\frac{N_{\mathrm{A}}}{N_{\mathrm{P}}}-1.42\frac{N_{\mathrm{S}}}{N_{\mathrm{P}}}\right)\frac{V_{\mathrm{A}}}{\Delta t}. \end{aligned} \quad (9)$$

If the total displacement current is decreased, the better EMI will be obtained. To reduce the displacement current, the parasitic capacitance of the primary winding and secondary winding has to be decreased by increasing the physical distance between the primary side windings to secondary winding, although the voltage pulsation between them is very large. While adding several turns of tapes may not be feasible considering the window area limitation. To solve this problem, the auxiliary winding can be placed in middle layer as shown in Fig. 8(a).

By means of this method, some assumptions are made to simplify the equations in view of the distance between different layers as follows:

$$\begin{aligned} C_{\mathrm{p3s\_\#2}} &= \frac{1}{2}C_{\mathrm{as\_\#2}}, C_{\mathrm{p2s\_\#2}} = \frac{1}{3}C_{\mathrm{as\_\#2}}, \\ C_{\mathrm{p1s\_\#2}} &= \frac{1}{4}C_{\mathrm{as\_\#2}}, \\ N_{\mathrm{P1}} &= N_{\mathrm{P2}} = N_{\mathrm{P3}} = \frac{1}{3}N_{\mathrm{P}}. \end{aligned} \quad (10)$$

Therefore, based on the above analysis methods, the total displacement current formula from primary and secondary can be expressed by

$$\begin{aligned} I_{\mathrm{cm\_\#2}} &= I_{\mathrm{cm\_ps\_\#2}} + I_{\mathrm{cm\_as\_\#2}} \\ &= C_{\mathrm{as\_\#2}}\left(0.458+0.5\frac{N_{\mathrm{A}}}{N_{\mathrm{P}}}-1.04\frac{N_{\mathrm{S}}}{N_{\mathrm{P}}}\right)\frac{V_{\mathrm{A}}}{\Delta t}. \end{aligned} \quad (11)$$

In order to better understand the effectiveness of our process, the voltage pulsation and displacement current are analyzed in Fig. 8(b). Then, the displacement current propagation path is shown by the arrow in Fig. 8(c).

Compared $I_{\mathrm{cm\_\#2}}$ with $I_{\mathrm{cm\_\#1}}$, $C_{\mathrm{as\_\#2}}$ is equal to the $C_{\mathrm{as\_\#1}}$ from the above theory, in case of $N_{\mathrm{S}}/N_{\mathrm{P}} < 17/27$ in the general low-voltage output application ($N_{\mathrm{S}} << N_{\mathrm{P}}$), the

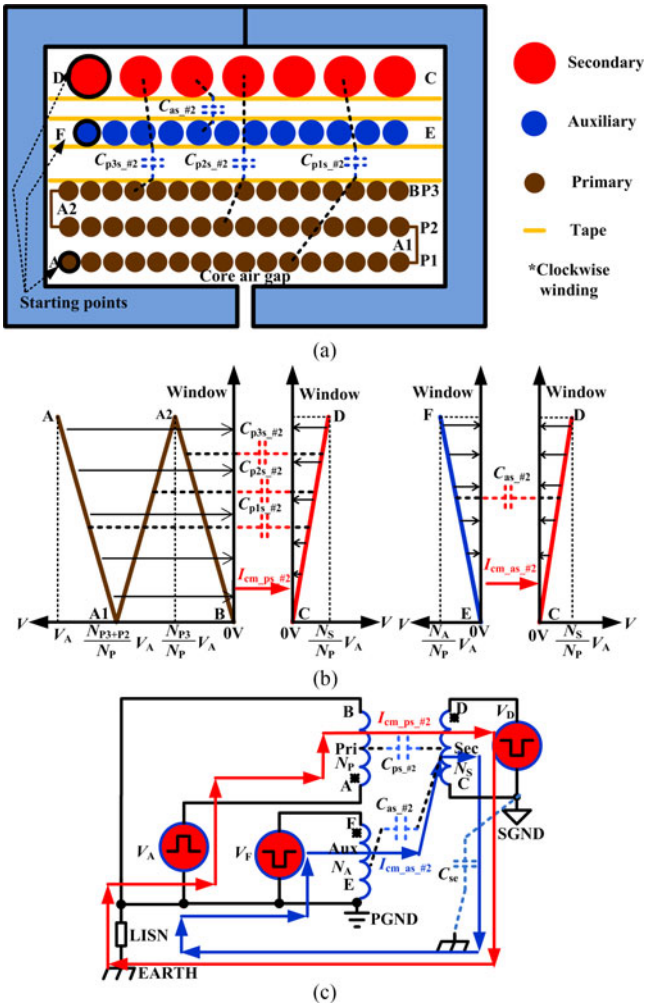


Fig. 8. Transformer #2: (a) Interwinding. (b) Voltage and current distribution. (c) CM current propagation.

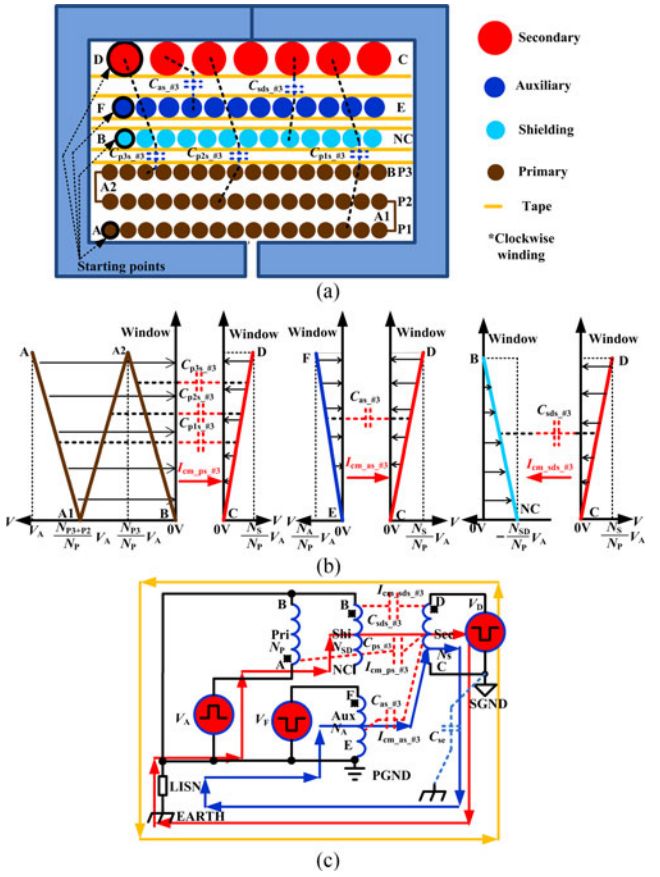


Fig. 9. Transformer #3: (a) Interwinding. (b) Voltage and current distribution. (c) CM current propagation.

displacement current has been reduced greatly. So, placing the auxiliary winding in the middle of primary winding and secondary winding is an effective method to mitigate the EMI noise in the non-Y-cap design.

Further on to reduce the displacement current, a shield winding is inserted between primary winding and auxiliary winding based on above transformer #2 as shown in Fig. 9(a). The starting point of the shielding winding is connected to point B, and the end point is disconnected to any electrical node.

Based on the similar analysis method, the displacement current between the primary winding and secondary winding $I_{\mathrm{cm\_ps\_\#3}}$ is as follows:

$$\begin{aligned} I_{\mathrm{cm\_ps\_\#3}} &= \frac{C_{\mathrm{p3s\_\#3}}}{2}\left(\frac{N_{\mathrm{P3}}}{N_{\mathrm{P}}}\frac{V_{\mathrm{A}}}{\Delta t}-\frac{N_{\mathrm{S}}}{N_{\mathrm{P}}}\frac{V_{\mathrm{A}}}{\Delta t}\right) \\ &+\frac{C_{\mathrm{p2s\_\#3}}}{2}\left(\frac{N_{\mathrm{P3}}+N_{\mathrm{P2}}+N_{\mathrm{P3}}}{N_{\mathrm{P}}}\frac{V_{A}}{\Delta t}-\frac{N_{\mathrm{S}}}{N_{\mathrm{P}}}\frac{V_{\mathrm{A}}}{\Delta t}\right) \\ &+\frac{C_{\mathrm{p1s\_\#3}}}{2}\left(\left(\frac{N_{\mathrm{P3}}+N_{\mathrm{P2}}}{N_{\mathrm{P}}}+1\right)\frac{V_{\mathrm{A}}}{\Delta t}-\frac{N_{\mathrm{S}}}{N_{\mathrm{P}}}\frac{V_{\mathrm{A}}}{\Delta t}\right) \end{aligned} \quad (12)$$

The displacement current between the auxiliary winding and secondary winding $I_{\mathrm{cm\_as\_\#3}}$ has the same equation as in (7):

$$I_{\mathrm{cm\_as\_\#3}} = \frac{C_{\mathrm{as\_\#3}}}{2}\left(\frac{N_{\mathrm{A}}}{N_{\mathrm{P}}}\frac{V_{\mathrm{A}}}{\Delta t}-\frac{N_{\mathrm{S}}}{N_{\mathrm{P}}}\frac{V_{\mathrm{A}}}{\Delta t}\right). \quad (13)$$

In the new power architecture, an additional displacement current between shielding winding and secondary winding is formed to cancel the displacement current which is given as follows:

$$I_{\mathrm{cm\_sds\_\#3}} = \frac{C_{\mathrm{sds\_\#3}}}{2}\left(\frac{N_{\mathrm{SD}}}{N_{\mathrm{P}}}+\frac{N_{\mathrm{S}}}{N_{\mathrm{P}}}\right)\frac{V_{\mathrm{A}}}{\Delta t}. \quad (14)$$

For simplification, some assumptions can be made as to the parasitic capacitance according the layers distance as follows:

$$\begin{aligned} C_{\mathrm{sds\_\#3}} &= \frac{1}{2}C_{\mathrm{as\_\#3}}, C_{\mathrm{p3s\_\#3}} = \frac{1}{3}C_{\mathrm{as\_\#3}}, \\ C_{\mathrm{p2s\_\#3}} &= \frac{1}{4}C_{\mathrm{as\_\#3}}, \\ C_{\mathrm{p1s\_\#3}} &= \frac{1}{5}C_{\mathrm{as\_\#3}}, N_{\mathrm{P1}} = N_{\mathrm{P2}} = N_{\mathrm{P3}} = \frac{1}{3}N_{\mathrm{P}}. \end{aligned} \quad (15)$$

Obviously, the $I_{\mathrm{cm\_sds\_\#3}}$ flows from secondary side to primary side, and it has the different current orient, so it can cancel a part of the total current. Therefore, the total displacement current formula from primary and secondary can be expressed

by

$$I_{\mathrm{cm\_\#3}} = I_{\mathrm{cm\_ps\_\#3}} + I_{\mathrm{cm\_as\_\#3}} - I_{\mathrm{cm\_sds\_\#3}}$$
$$= C_{\mathrm{as\_\#3}}\left(0.35 + 0.5\frac{N_{\mathrm{A}}}{N_{\mathrm{P}}} - 1.26\frac{N_{\mathrm{S}}}{N_{\mathrm{P}}} - 0.25\frac{N_{\mathrm{sds}}}{N_{\mathrm{P}}}\right)\frac{V_{\mathrm{A}}}{\Delta t}. \quad (16)$$

To better understand the effectiveness of the process, the voltage pulsation and displacement current are analyzed in Fig. 9(b). Thus, the displacement current propagation path is shown by the arrow in Fig. 9(c).

Compared $I_{\mathrm{cm\_\#3}}$ with $I_{\mathrm{cm\_\#2}}$, $C_{\mathrm{as\_\#3}}$ is equal to the $C_{\mathrm{as\_\#2}}$ from the above theory, the $I_{\mathrm{cm\_\#3}}$ is much smaller than $I_{\mathrm{cm\_\#2}}$, and the displacement current has been reduced greatly. Based on above analysis, the shielding winding not only increases the physical distance between primary winding and secondary winding, but also cancels a part of the displacement current from primary side to secondary side. If a proper N_{sd} is selected, the total displacement current could even be reduced to zero; thus, the CM noise will be reduced and better EMI performance will be obtained.

Obviously, the transformer optimized method is effective to reduce the CM noise in the non-Y-cap design. Actually, it is not only suitable for the flyback converter, and it is suitable for almost all isolated converter, such as forward converter, half-bridge converter, and *LLC* converter. To verify it, the transformer optimized method is applied to the *LLC* converter as follows.

The simple model of the *LLC* converter is shown in Fig. 10(a). Based on the transformer optimization method in the non-Y-cap design, three different transformers, such as transformer #4, #5, and #6 are designed for the *LLC* which is shown in Fig. 10(b)–(d) respectively. The primary winding is evenly divided into two layers and the auxiliary winding and secondary winding are distributed symmetrically in a standalone layer. The transformer #4 structure has the same structure as transformer #1. This is primary-secondary-auxiliary winding structure. The transformer #5 structure is primary-auxiliary-secondary winding structure as transformer #2. The transformer #6 structure is primary-shielding-auxiliary-secondary winding structure the same as the transformer #3. Based on above analysis, the transformer #6 has the best EMI performance among the three transformers. Due to the limited length, it is not analyzed in detail.

In short, in the non-Y-cap EMI design, the inner parasitic capacitors among different windings as well as the different layer consideration of power transformer are analyzed. Accurate relationship is built based on the layer distance for analysis. The distribution of voltage along layer is studied to calculate the CM current. The CM displacement current from the primary side to the secondary side is analyzed and modeled. Based on the built model, three different optimized transformers are presented in detail and are proved to be effective methods for the non-Y-cap EMI design whatever the topology is applied. The optimized method is also verified by the experiment both in flyback converter and *LLC* converter in Section V.

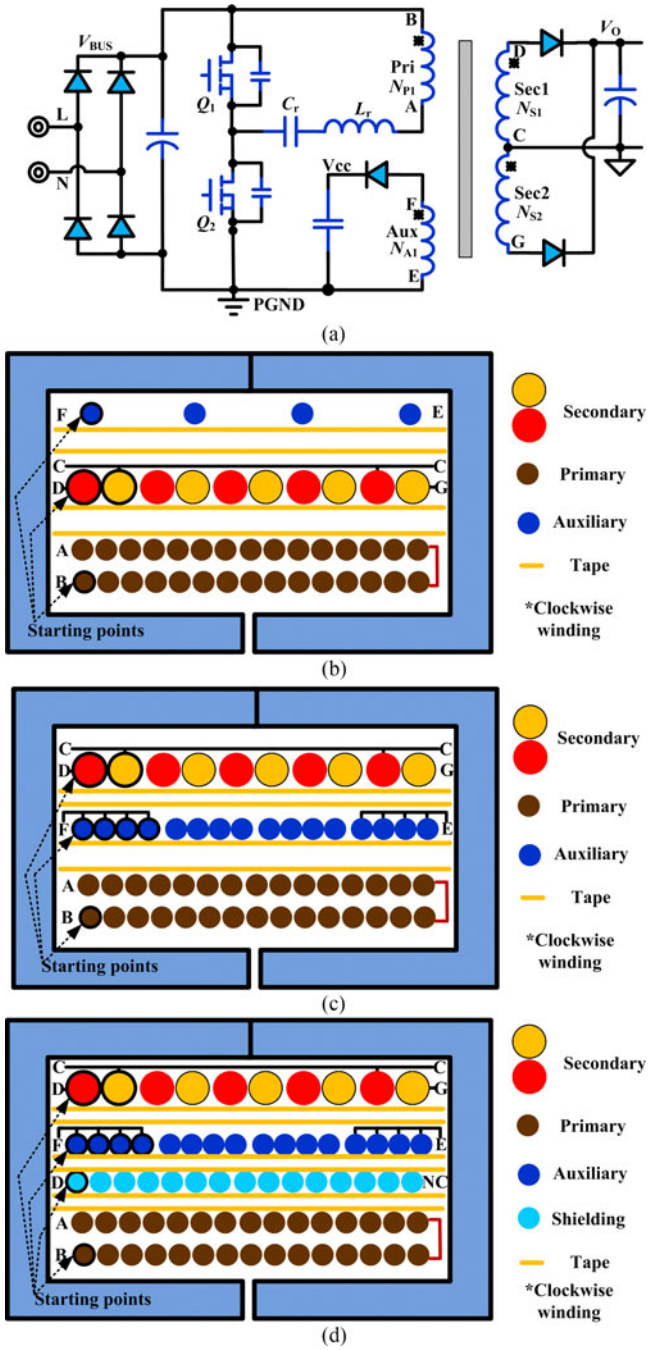


Fig. 10. *LLC* converter: (a) Simple model. (b) Interwinding of transformer #4. (c) Interwinding of transformer #5. (d) Interwinding of transformer #6.

IV. Proposed Topology With Balanced Windings for Non-Y-Cap EMI Design

Although the optimized transformer architecture is able to reduce the EMI noise from the transmission path, a better way of solving the EMI issue from the noise source, it has the merit of low cost and easy to be fabricated in massive production.

In this section, a new topology suitable for non-Y-capacitor converter is proposed to solve the EMI issue actively from the noise source. It is better EMC behavior along with other desirable converter parameters considered in the topology

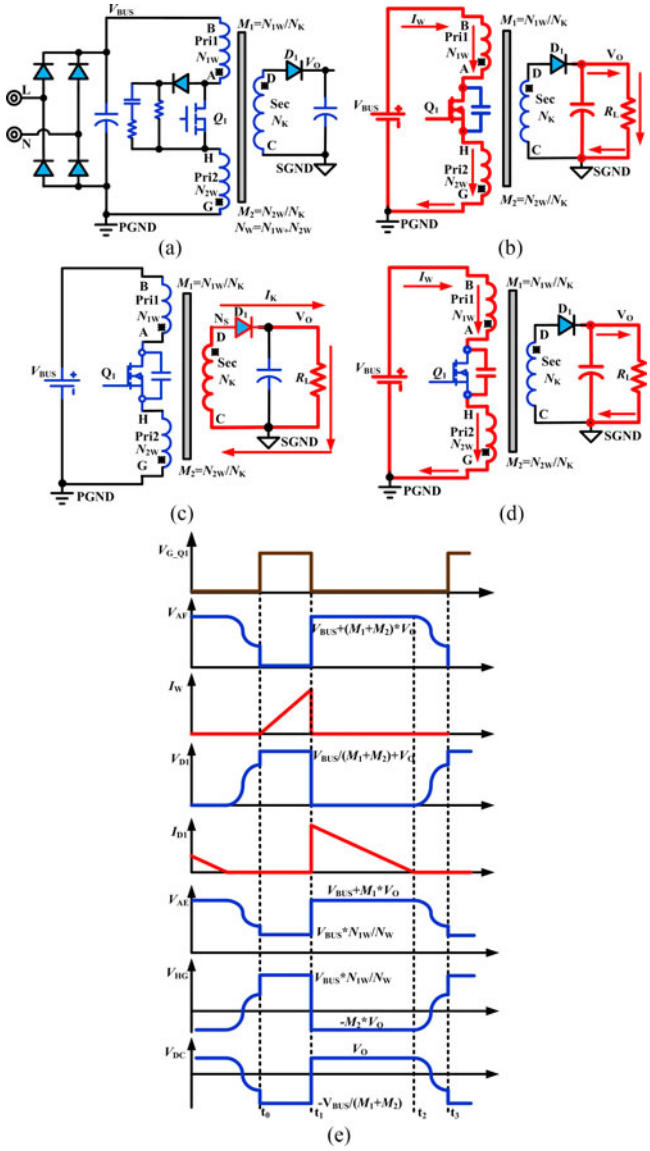


Fig. 11. (a) Proposed flyback topology with balanced windings. (b) Q_1 is turned-on. (c) Q_1 is turned-off. (d) Q_1 body diode is turned-on. (e) Operation waveforms.

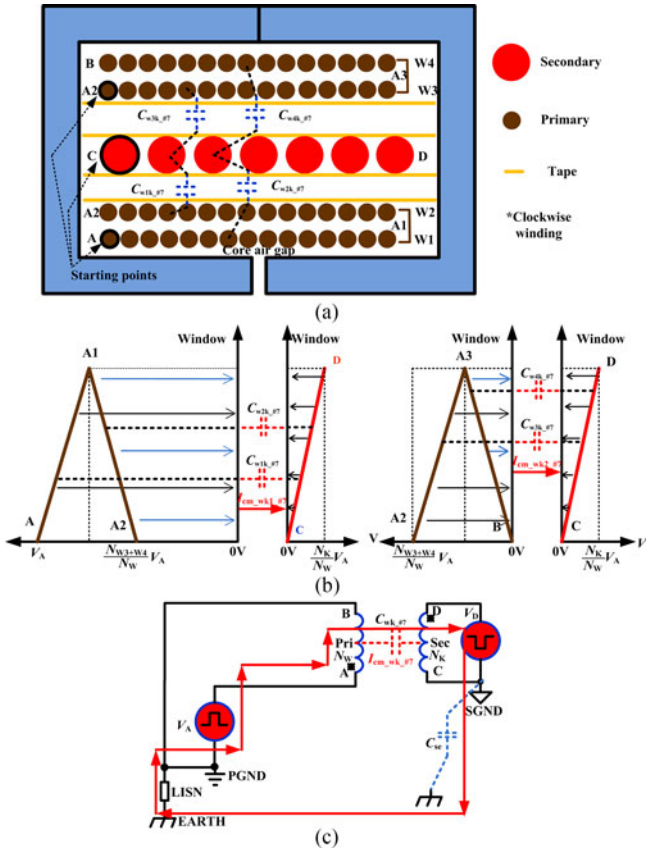


Fig. 12. Transformer #7: (a) Interwinding. (b) Voltage and current distribution. (c) CM current propagation.

design. Since the flyback converter is widely used as an isolated switching-mode power supply, this paper takes it as an example to introduce the proposed topology with balanced windings as shown Fig. 11(a). It just operates as a flyback with primary winding divided into two branches, and the switch and control logic branch is placed in the middle. Based on an optimized transformer structure, the EMI CM noise current in the two branches has been cancelled entirely. So it has excellent EMI performance and the Y-capacitor can be removed easily for strict leakage current limitation.

First, the operational principle of the proposed topology is introduced. At the switch Q_1 turning on moment, the magnetic current increases linearly from zero. The energy stores in two primary windings just like inductors. The voltage across the two windings Pri1 and Pri2 is proportional to V_{BUS}. After a certain time, the switch Q_1 turns off and then the energy stored in the primary winding will transfer to the secondary through output rectifier diode. Then, the switch Q_1 voltage will be $V_{\mathrm{BUS}} + (M_1 + M_2) * V_{\mathrm{O}}$ (M_1 and M_2 are the transformer ratios of the two balanced windings). Until the secondary winding current goes to zero, the primary switch voltage will be clamped to V_{BUS}. The current transmission paths of the proposed topology at different intervals are shown in Fig. 11(b)–(d), respectively. The real-time waveforms of the voltage and current are shown in Fig. 11(e).

A traditional flyback converter without auxiliary winding is analyzed first as a guideline. It is used as a guideline to compare the proposed balance winding effectiveness. The primary winding is evenly divided into four layers, while the secondary winding is distributed symmetrically in a standalone layer. The half window of the transformer structure implemented with EE core is shown in Fig. 12(a) and the terminals A and C are dotted terminals. According to [23], the capacitor between the winding and core can be neglected due to the smaller capacitance, and the primary winding inner layers capacitors can also be neglected because they do not contribute to the CM noise. For simplification, this paper supposes all the winding layers cover the whole window width and there is two-layer taps between different windings. Then, the parasitic capacitance is different in view of different distance between the different primary winding layers to the secondary winding layer

and a k ratio can be represented for the difference. According to current formula of capacitor $I_{\rm C} = C * dv/dt$, the displacement current between primary side and secondary side only depends on the voltage jump slope and the parasitic capacitor value.

When the Q_1 is in the switching mode, the point A can be considered as a pulse voltage source which amplitude is $V_{\rm A}$ from turned- on state to turned-off state and it can be expressed as follows:

$$V_{\rm A} = V_{\rm BUS} + \frac{N_{\rm W}}{N_{\rm K}} * V_{\rm O} \tag{17}$$

where $N_{\rm W}$ and $N_{\rm K}$ are turns of primary winding and secondary winding respectively.

Similarly, the point D can also be considered as a pulse voltage source which amplitude is $V_{\rm D}$ from turn on state to turn off state and it can be expressed following:

$$V_{\rm D} = V_{\rm O} + \frac{N_{\rm K}}{N_{\rm W}} V_{\rm BUS} = \frac{N_{\rm K}}{N_{\rm W}} V_{\rm A}. \tag{18}$$

The voltage curve of the four layers winding at different points is illustrated in Fig. 12(b) assuming that the voltage is evenly distributed. At the Q_1 turned-off moment, the voltage of point A_1 and D is rising up relative to points B and C, respectively. By the means of the above equations, the displacement current is shown in Fig. 12(c). Assuming that the current orient to primary side is positive, the displacement current between inner primary winding and the secondary winding can be expressed by

$$I_{\rm cm\_wk1\_\#7} = C_{\rm w1k\_\#7} \frac{N_{\rm W2} + 2 * (N_{\rm W3} + N_{\rm W4}) - N_{\rm K}}{2 * N_{\rm W} * \Delta t} V_{\rm A} + C_{\rm w2k\_\#7} \frac{N_{\rm W} + N_{\rm W2} + N_{\rm W3} + N_{\rm W4} - N_{\rm K}}{2 * N_{\rm W} * \Delta t} V_{\rm A} \tag{19}$$

where $N_{\rm W1}$, $N_{\rm W2}$, $N_{\rm W3}$, and $N_{\rm W4}$ are turns of three primary winding layers from inner to outer respectively. $C_{w1k\_\#7}$ is parasitic capacitor between the second primary winding layer and secondary winding. Δt is the transient time of the voltage jumping.

Similarly, the displacement current between outer primary winding and the secondary winding is calculated as follows:

$$I_{\rm cm\_wk2\_\#7} = C_{\rm w3k\_\#7} \frac{N_{\rm W3} + 2 * N_{\rm W4} - N_{\rm K}}{2 * N_{\rm W} * \Delta t} V_{\rm A} + C_{\rm w4k\_\#7} \frac{N_{\rm W4} - N_{\rm K}}{2 * N_{\rm W} * \Delta t} V_{\rm A} \tag{20}$$

where $C_{\rm w3k\_\#7}$ is the parasitic capacitor between the third primary winding layer and secondary winding layer.

Substituting (17), (18) into (19) and (20), and supposing $N_{\rm W1} = N_{\rm W2} = N_{\rm W3} = N_{\rm W4} = 1/4 * N_{\rm W}$, $C_{w3k\_\#7} = C_{w1k\_\#7}$, $C_{w2k\_\#7} = k * C_{w1k\_\#7}$, and $C_{w4k\_\#7} = k * C_{w3k\_\#7}$, the total displacement current from primary to secondary can be expressed by

$$I_{\rm cm\_wk\_\#7} = I_{\rm cm\_wk1\_\#7} + I_{\rm cm\_wk2\_\#7} = C_{\rm w1k\_\#7} \left(1 - \frac{N_{\rm K}}{N_{\rm W}}\right)(k+1) \frac{V_{\rm A}}{\Delta t} \tag{21}$$

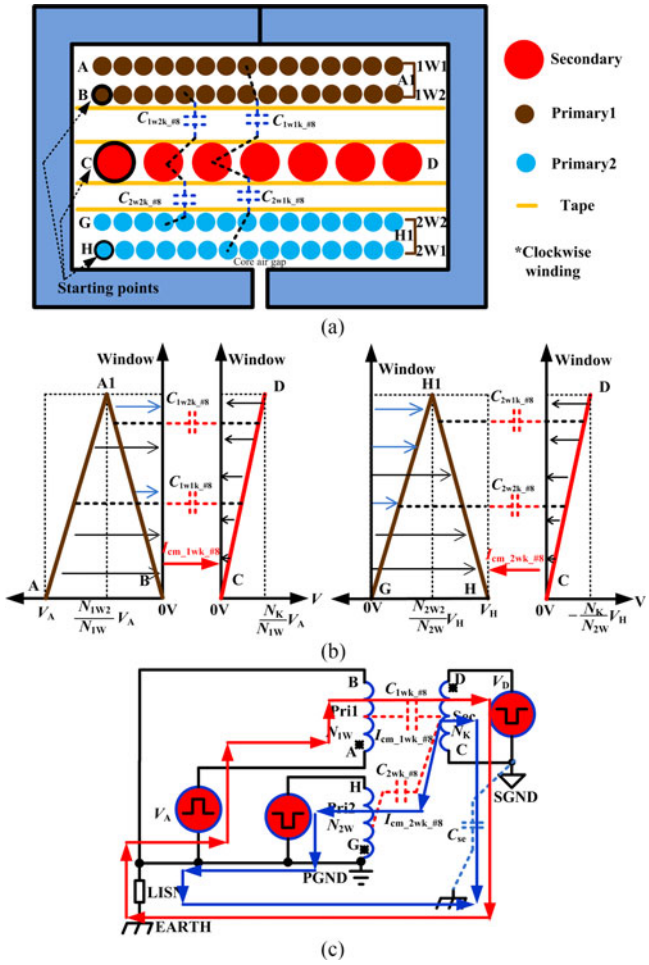


Fig. 13. Transformer #8: (a) Interwinding. (b) Voltage and current distribution. (c) CM current propagation.

where k is the ratio of the capacitance difference between the first primary layer W1 to secondary winding layer and the second primary layer W2 to the secondary winding layer.

Therefore, based on the above equation, $N_{\rm K}$ is much smaller than $N_{\rm W}$ in the traditional low-output voltage flyback converter, the CM displacement current is very large and the EMI turns to be worse if the Y-capacitor is removed to eliminate the leakage current.

With the similar research method, the proposed topology with balanced winding is analyzed as follow. The transformer structure is just the same as the above traditional structure of flyback which is shown in Fig. 13(a).

In the proposed topology, when the Q_1 is in switching mode, the point A can be considered as a pulse voltage source which amplitude is $V_{\rm A}$ from turned-on state to turned-off state and it can be expressed following:

$$V_{\rm A} = V_{\rm BUS} * \frac{N_{\rm 1W}}{N_{\rm 1W} + N_{\rm 2W}} + M_1 * V_{\rm O} \tag{22}$$

where $N_{\rm 1W}$ and $N_{\rm 2W}$ are the turns of two primary windings, respectively. M_1 is the turn ratio of the Pri1 to the secondary winding.

In the same way, the point H can be considered as a pulse voltage source which amplitude is $V_{\rm H}$ from turn-on state to turned-off state and it can be expressed as follows:

$$V_{\rm H} = -(V_{\rm BUS} * \frac{N_{2\rm W}}{N_{1\rm W} + N_{2\rm W}} + M_2 * V_{\rm O}) \qquad (23)$$

where M_2 is the turn ratio of the Pri2 to the secondary winding.

Meanwhile, the point D can be considered as a pulse voltage source which amplitude is $V_{\rm D}$ from turned-on state to turned-off state and it can be expressed by

$$V_{\rm D} = V_{\rm O} + \frac{V_{\rm BUS}}{M_1 + M_2} = \frac{V_{\rm A}}{M_1} = -\frac{V_{\rm H}}{M_2}. \qquad (24)$$

The voltage of the different winding layers at different point is shown in Fig. 13(b). At the Q_1 turned-off moment, the voltage of points A and D is rising up relative to points B and C, respectively. However, the voltage of point H is decreasing down relative to point G. Then, the displacement current between the primary and secondary is shown in Fig. 13(c). The displacement current between primary winding Pri1 and the secondary winding is given as

$$I_{\rm cm\_1wk\_\#8} = C_{1w2k\_\#8}\frac{N_{1\rm W2} - N_{\rm K}}{2 * N_{1\rm W} * \Delta t}V_{\rm A} + C_{1w1k\_\#8}\frac{N_{1\rm W} + N_{1\rm W2} - N_{\rm K}}{2 * N_{1\rm W} * \Delta t}V_{\rm A} \qquad (25)$$

where $N_{1\rm W2}$, $N_{1\rm W}$, and $N_{\rm K}$ the turns of primary winding Pri1 inner layer 1W2, Pri1 winding layer and secondary winding, respectively. $C_{1w2k\_\#8}$ is the parasitic capacitor between the Pri1 inner layer 2W2 and secondary winding.

Similarly, the displacement current between primary winding Pri2 and the secondary winding is given as

$$I_{\rm cm\_2wk\_\#8} = C_{2\rm w2k\_\#8}\frac{N_{2\rm W2} + N_{\rm K}}{2 * N_{2\rm W} * \Delta t}V_{\rm H} + C_{2\rm w1k\_\#8}\frac{N_{2\rm W} + N_{2\rm W2} + N_{\rm K}}{2 * N_{2\rm W} * \Delta t}V_{\rm H} \qquad (26)$$

where $N_{2\rm W2}$ is the turns of primary winding Pri2 inner layer 2W2. $C_{2w2k\_\#8}$ is the parasitic capacitor between the primary winding Pri2 outer layer 2W2 and secondary winding.

Substituting (22), (23) into (24) and (25), and supposing $N_{1\rm W1} = N_{1\rm W2} = 1/2 * N_{1\rm W}$, $N_{2\rm W1} = N_{2\rm W2} = 1/2 * N_{2\rm W}$, and $C_{2w2k\_\#8} = C_{1w2k\_\#8}$ in view of the power architecture, the total displacement current from primary to secondary can be expressed by

$$I_{\rm cm\_wk\_\#8} = I_{\rm cm\_1wk\_\#8} + I_{\rm cm\_2wk\_\#8} = \frac{C_{1\rm w2k\_\#8}}{4 * \Delta t} * [(3k+1)(M_1 - M_2) - 4(k+1)] \times \left(\frac{V_{\rm BUS}}{M_1 + M_2} + V_{\rm O}\right). \qquad (27)$$

With a proper design of M_1 and M_2, the CM noise from the primary to secondary can be reduced even to zero. Therefore, there is no difference whether the Y-cap is removed or not. At the same time, due $V_{\rm A}$ and $V_{\rm H}$ has the different voltage pulsating, so the CM noise from the point A and point H will be partial cancelled. So the proposed topology with balanced winding has excellent EMI performance and suitable for the non-Y-cap EMI design.

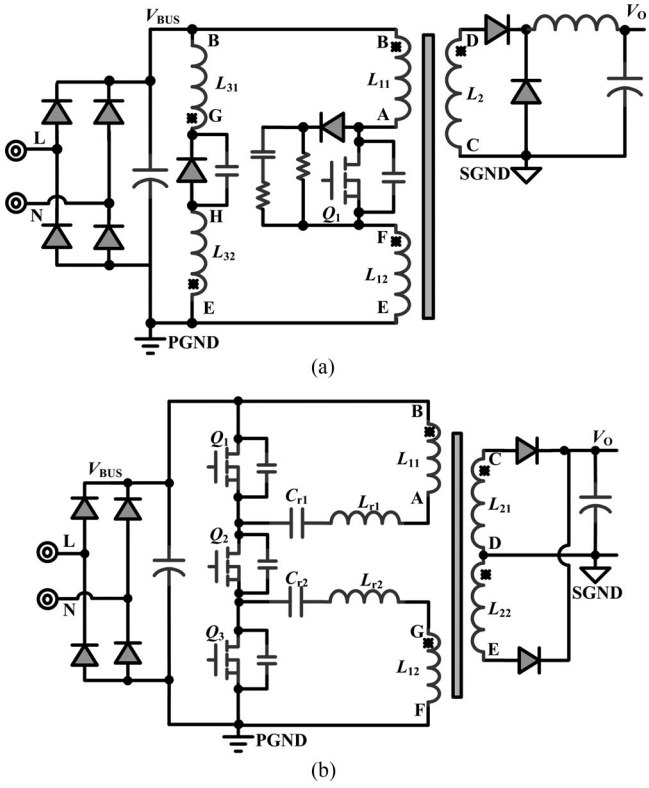


Fig. 14. (a) Proposed forward topology with balanced windings. (b) Proposed *LLC* topology with balanced windings.

Further on, the balanced winding method can also be applied the forward converter and *LLC* converter which is shown in Fig. 14(a) and (b). However it is complex and not analyzed in detail due to limited length.

In short, in the non-Y-cap SMPS EMI design, a balanced winding method is proposed and suitable for various types of isolated topologies. With a proper winding turn number designed for the balanced winding, the CM noise current is even reduced to zero. However, it is complex with high BOM cost, and it is low reliability due to so many components. The power rating is also limited by the radiation performance. So it is suitable for lower power rating application, and experimental results demonstrated verify the effectiveness of the proposed methods in the non-Y-cap EMI design in following Section V, and a dedicated prototype based on the optimized transformer method is also demonstrated to compare with the proposed balanced winding method.

V. Experimental Results

In this section, experimental results are presented in order to validate the theoretical predictions. All the experimental results are based on the following test platform as shown in Fig. 15. This is test environment for conducted EMI of home information technology device, as governed by European Union. Normally

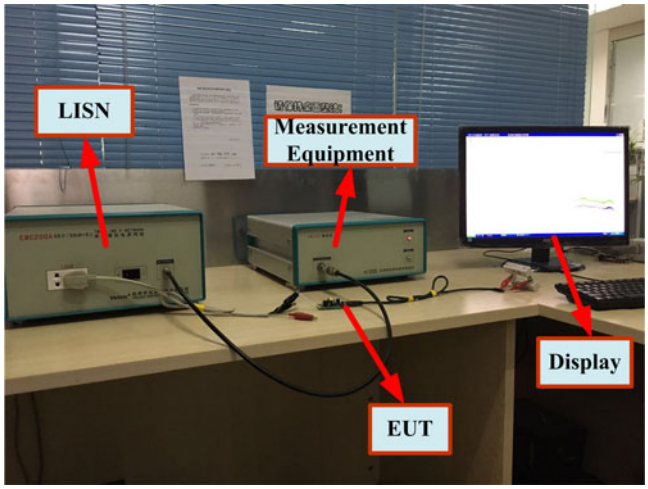


Fig. 15. Conducted EMI measurement platforms.

TABLE V
BASIC SPECIFICATION OF THE FLYBACK PROTOTYPE

Input	L and N Two-wire, 85–264 Vac 47–63 Hz,
Output	5 V, 2.1 A, $V_{\rm ripple} < 100$ mV and $I_{\rm OCP} < 2.5$A with USB port
Efficiency	Energy star Level 6 and No load loss <70 mW
EMC and leakage current	EN55022 Class B limits; Leakage current $<100\ \mu$A
Size	$W \times L \times H = 31.5$ mm $\times$ 40 mm $\times$ 19.6 mm
Switching frequency	Quasi-Resonant flyback with 70 kHz at full load in 115 Vac
Transformer	EE16 core: $N_{\rm P} = 102Ts$, $N_{\rm A} = 16Ts$, $N_{\rm S} = 6Ts$

quasi-peak level limits as well as average level limits are applied to take EN55022 Class B limits as the standard.

A. *Case A—Flyback Converter With Optimized Transformer Architecture to Reduce an EMI Noise in the Non-Y-cap Design*

In order to verify the optimized transformer structure to get rid of the Y-capacitor, a flyback converter prototype is first built. This is a 5-V 2.1-A charger for smart phone or touch Pads. The basic specification of the prototype is shown in Table V.

The prototype is shown in Fig. 16(a) and the flyback converter operation waveforms are shown in Fig. 16(b). More specifically, the voltage of pulsating points $V_{\rm A}$, $V_{\rm ISEN}$, $V_{\rm O}$, and $V_{\rm D}$ are shown as CH1, CH2, CH3, and CH4, respectively.

The measured leakage current of this prototype is 75 μA and it meets the leakage current standard.

The conducted EMI spectrum of a traditional sandwich transformer with 1000-pF Y-capacitor between the primary and secondary measured at 220 Vac at 50 Hz is shown in Fig. 17(a). With the help of Y-capacitor, the conducted EMI can meet the EN55022 Class B limits standard easily. If the Y-capacitor is removed for the limited leakage current benefit, the EMI changes to be worse and hard to meet the standard which is shown in Fig. 17(b). It is over the limitation line about 10 dB. To satisfy

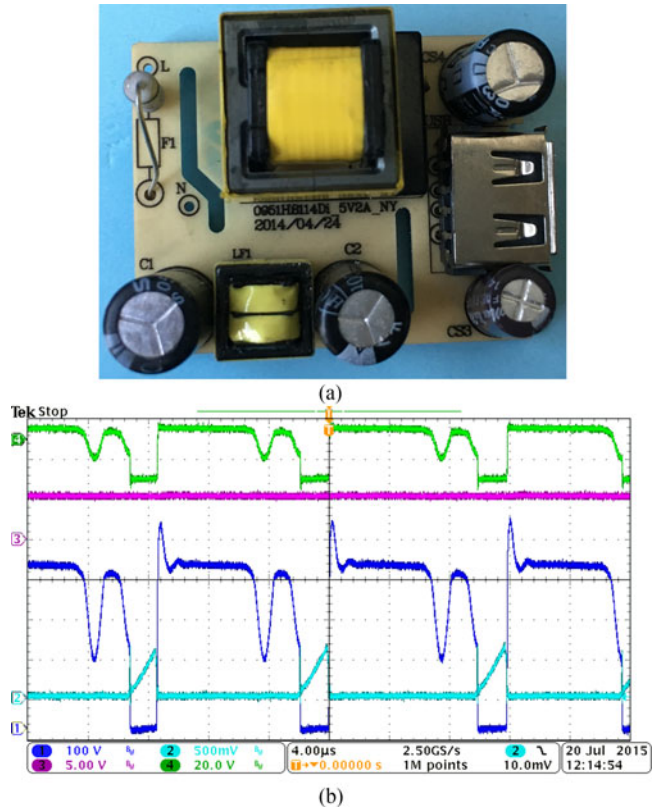


Fig. 16. 5-V 2.1-A flyback: (a) Prototype. (b) Operation waveforms.

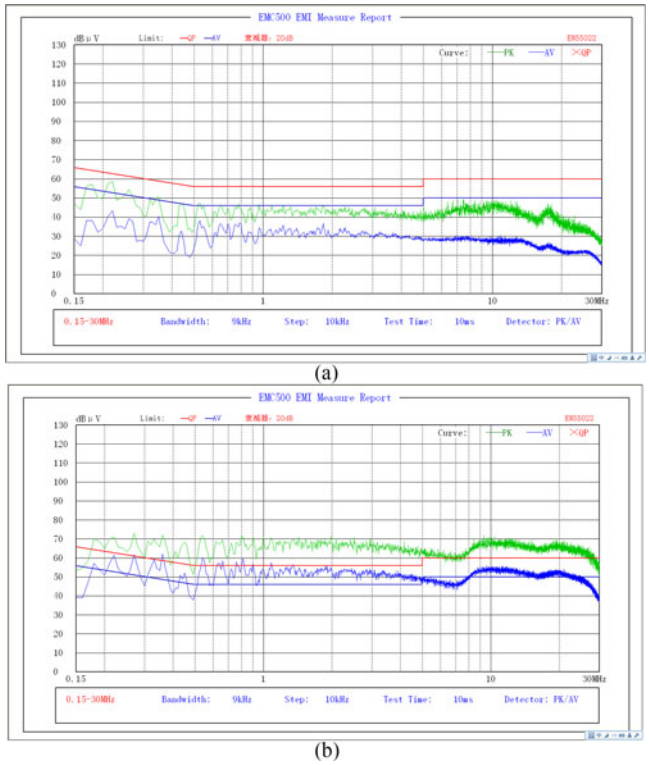


Fig. 17. 5-V 2.1-A EMI spectrum of sandwich transformer #0: (a) With Y-cap. (b) Without Y-cap.

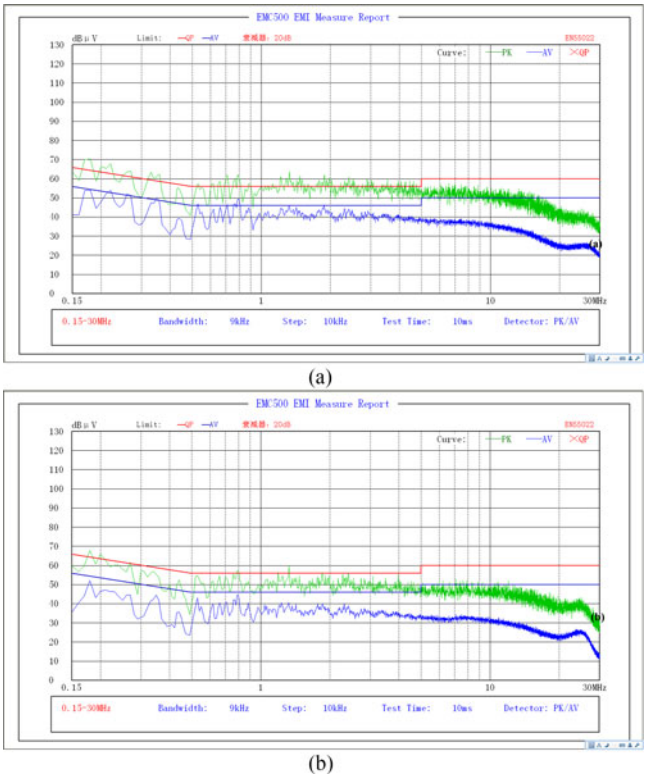


Fig. 18. 5-V 2.1-A EMI spectrum: (a) Nonsandwich transformer #1 without Y-cap. (b) Nonsandwich transformer #2 without Y-cap.

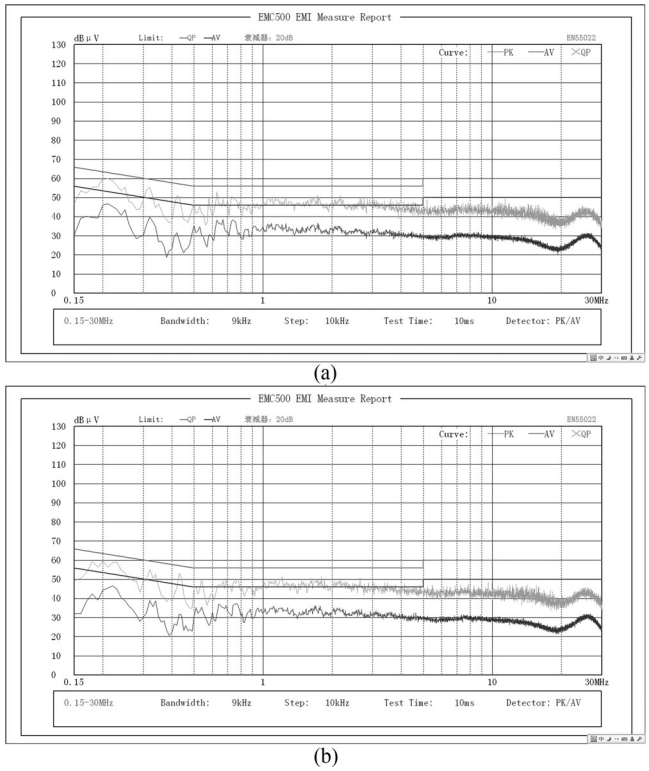


Fig. 19. 5-V 2.1-A EMI spectrum of transformer #3 without Y-cap: (a) L-line at 220 V. (b) N-line at 220 V.

the strict leakage current limitation and acquire good EMI performance, the transformer structure needs to be optimized.

According the transformer optimized method presented in Section III, the CM noise can be significantly reduced in the non-Y-capacitor SMPS. The conducted EMI spectrum by the transformer #1 is shown in Fig. 18(a). With the improved transformer #2 by exchanging the secondary-side winding and auxiliary winding position, the EMI spectrum shown in Fig. 18(b) is about 3 dB improved than Fig. 18(a) as expected.

When a shielding layer is inserted to the transformer #2 to be the transformer #3, the conducted EMI is improved greatly compared with above two transformers as expected. The CM noise is significantly reduced and it can pass the EN55022 Class B limits certification. The EMI spectrums measured at L-line at 220 V and N-Line at 220 V are shown in Fig. 19(a) and (b).

B. Case B—LLC Converter With Optimized Transformer Architecture to Reduce an EMI Noise in the Non-Y-cap Design

Further on, to verify the proposed transformer structure to get rid of the Y-cap, an *LLC* converter prototype is built as well. This is a 20-V 3-A adapter for medical equipment. The basic specification of the prototype is shown in Table VI.

The *LLC* prototype is shown in Fig. 20(a) and the *LLC* converter operation waveforms are shown in Fig. 20(b). More specifically, the voltage of pulsating points resonant current I_{R}, low-side switch V_{DS}, low-side switch gate drive V_{Gate}, and the secondary-side winding voltage V_{D} are shown as CH1, CH2, CH3, and CH4, respectively.

TABLE VI
BASIC SPECIFICATION OF THE *LLC* PROTOTYPE

Input	L and N Two-wire, 230 Vac 47–63 Hz,
Output	20 V, 3 A ,$V_{\mathrm{ripple}} < 200$ mV
Efficiency	Energy star Level 6 and No load loss < 100 mW
EMC and leakage current	EN55022 Class B limits; Leakage current $< 100\ \mu$A
Size	$W \times L \times H = 46$ mm $\times$ 98 mm $\times$ 24 mm
Switching frequency	*LLC* with 180 kHz at full load in 230 Vac
Transformer	PQ2020: $L_{\mathrm{m}} = 400\ \mu$H, $N_{\mathrm{P1}} = 50$Ts, $N_{\mathrm{A1}} = 4$Ts, $N_{\mathrm{S1}} = N_{\mathrm{S1}} = 6$Ts
Resonant inductor and capacitor	$L_{\mathrm{r}} = 30\ \mu$H, $C_{\mathrm{r}} = 13.6$ nF

The measured leakage current of this prototype is 75 μA and it meets the leakage current standard.

The conducted EMI spectrum based on the transformer #4 is shown in Fig. 21(a). With the improved transformer #5 by exchanging the secondary-side winding and auxiliary winding position, the EMI spectrum shown in Fig. 21(b) is about 3–5 dB improved comparing with Fig. 21(a) as expected.

When a shielding layer is inserted to the transformer #5 to be the transformer #6, the EMI is improved greatly compared with above two transformers as expected. The CM noise is significantly reduced and it can pass the EN55022 Class B limits certification. The EMI spectrums measured at

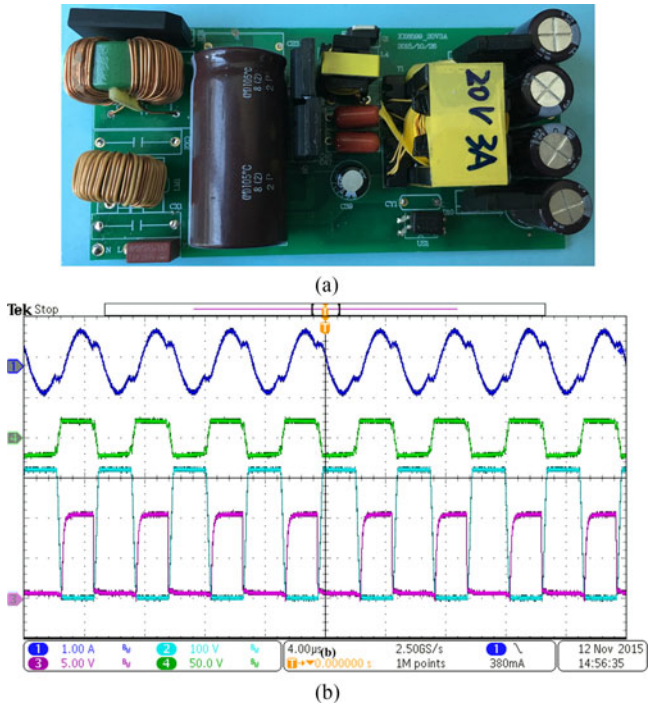


Fig. 20. 20-V 3-A *LLC* converter: (a) Prototype. (b) Operation waveforms.

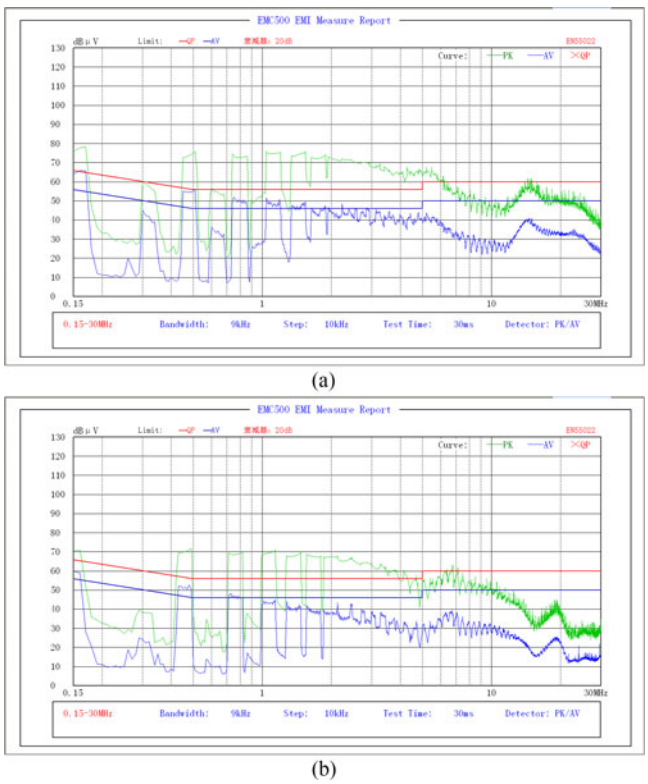


Fig. 21. *LLC* EMI spectrum of: (a) transformer #4 without Y-cap. (b) Transformer #5 without Y-cap.

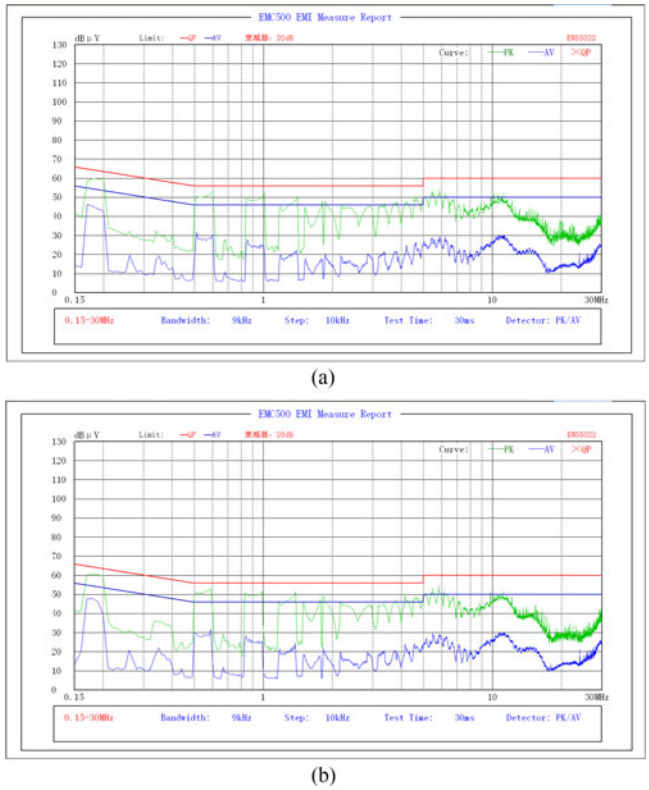


Fig. 22. *LLC* EMI spectrum of transformer #6 without Y-cap: (a) L-line at 220 V. (b) N-line at 220 V.

TABLE VII
BASIC SPECIFICATION OF THE FLYBACK PROTOTYPE

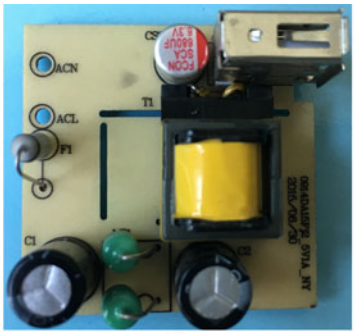
Input	L and N Two-wire, 85 Vac ~ 264 Vac 47 Hz ~ 63 HZ,
Output	5 V, 1 A, $V_{\rm ripple} < 100$ mV and $I_{\rm OCP} < 1.3$ A with USB port
Efficiency	Energy star Level 6 and No load loss <70 mW
EMC and leakage current	EN55022 Class B limits; Leakage current <100 μA
Size	$W \times L \times H = 36$ mm $\times$ 36 mm $\times$ 18 mm
Switching frequency	Quasi-Resonant flyback with 70 kHz at full load in 115 Vac
Transformer	EE13 core: $N_{1W} = 98$Ts, $N_{2W} = 62$Ts, $N_K = 10$Ts

L-line at 220 V and N-line at 220 V are shown in Fig. 22(a) and (b).

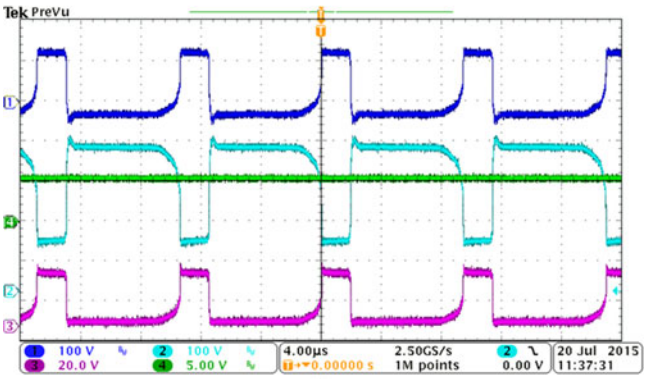
C. Proposed Balanced Winding Method for the Non-Y-cap EMI Design

In order to verify the proposed balanced winding method to get rid of the Y-cap, a flyback converter prototype is built. This is a 5-V 1-A CCCV charger operating in quasi-resonant mode for smart phone or touch Pads. The basic specification of the prototype is shown in Table VII.

The prototype is shown in Fig. 23(a) and the flyback converter operation waveforms are shown in Fig. 23(b).

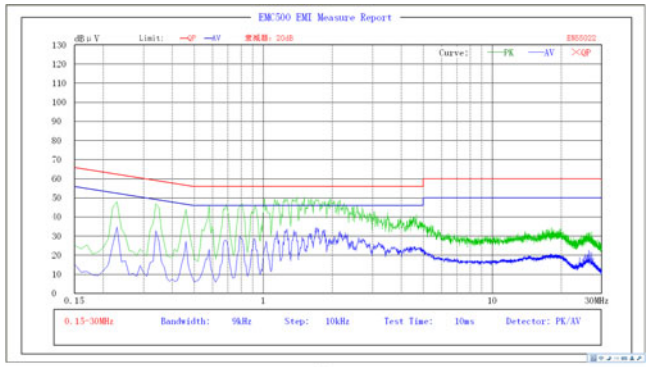


(a)

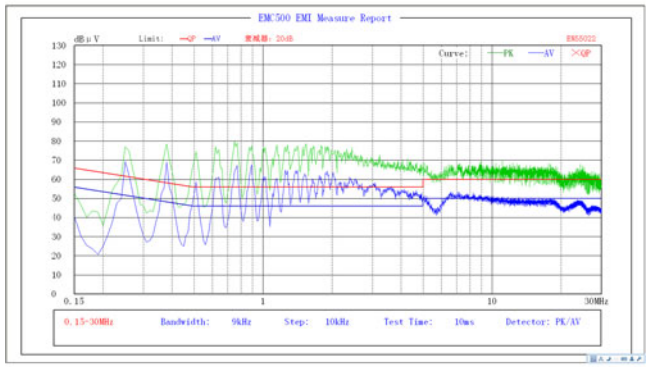


(b)

Fig. 23. Proposed flyback with balanced windings: (a) Prototype. (b) Operation waveforms.



(a)



(b)

Fig. 24. 5-V 1-A EMI spectrum of transformer #7: (a) With Y-cap. (b) Without Y-cap.

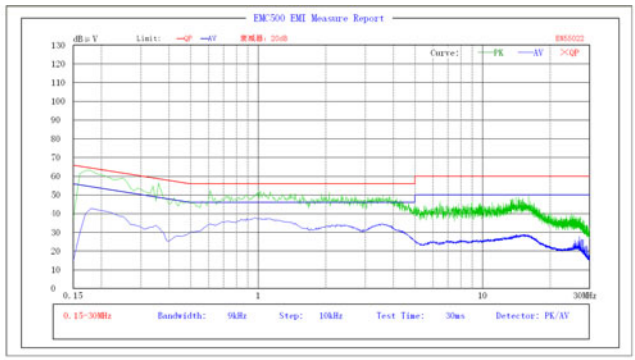
More specifically, the voltage of pulsating points V_H, V_A, V_D, and V_O are illustrated in CH1, CH2, CH3, and CH4, respectively.

The measured leakage current of this prototype is 75 μA and it meets the leakage current standard.

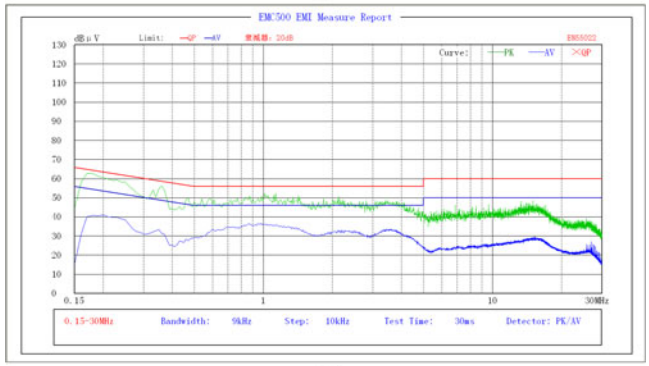
The conducted EMI spectrum of a traditional sandwich transformer with 470-pF Y-capacitor between the primary and secondary which is measured at 220 Vac at 50 Hz is shown in Fig. 24(a). With the help of Y-capacitor, the EMI can meet the EN55022 Class B limits standard easily. If the Y-capacitor is removed for the limited leakage current benefit, the EMI changes to be worse and hard to meet the EMC standard which is shown in Fig. 24(b). It is over the limitation line about 20 dB. To satisfy the strict leakage current limitation and acquire good EMI performance, the proposed balanced windings should be applied to solve it.

First, with the optimized transformer method, the EMI performance is improved greatly. The EMI spectrums measured at L-line at 220 V and N-line at 220 V are shown in Fig. 25(a) and (b). It can pass the EMI standard without Y-cap.

As expected, the CM noise is significantly reduced by the proposed balanced windings method in the non-Y-cap EMI design. The CM noise is significantly reduced and it can pass the EN55022 Class B limits standard certification. The EMI spectrums measured at N-line at 115 V and N-line at 220 V are shown in Fig. 26(a) and (b).



(a)



(b)

Fig. 25. Optimized transformer EMI spectrums without Y-cap: (a) L-line at 220 V. (b) N-line at 220 V.

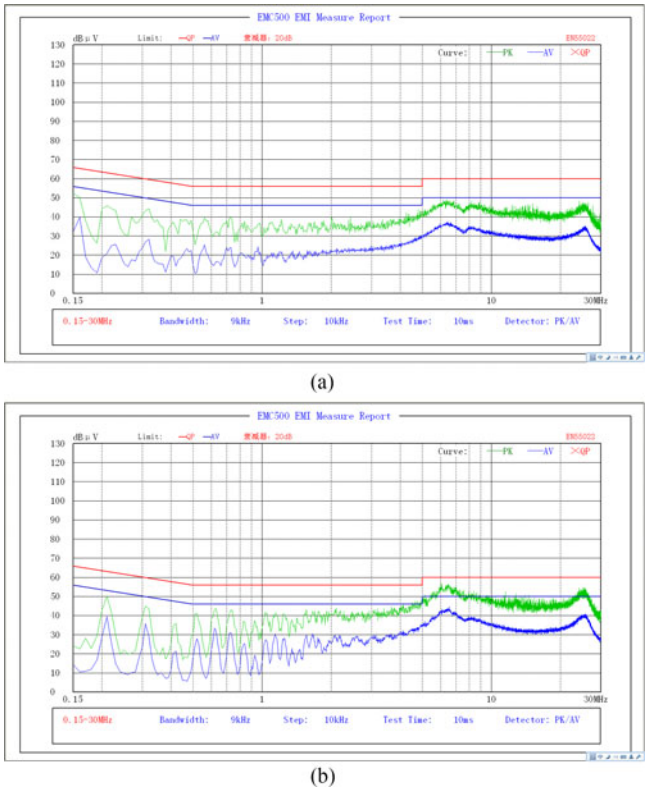


Fig. 26. Proposed topology EMI spectrums without Y-cap of transformer #8: (a) N-line at 115-V ac. (b) N-line at 220-V ac.

VI. Conclusion

In this paper, the motivation for the non-Y-cap design is presented first. In the commonly used isolated switching power supplies, the Y-capacitors branch behaves as a terrible leakage current loop. For the safety of human beings, this leakage current is not allowed in power supplies, such as chargers, medical instruments, etc. Therefore, in order to both acquire good EMI performance and satisfy the strict leakage current limitation, a novel non-Y-capacitor EMI design concept for SMPS is proposed. Following the proposed new design procedure, it is easier to meet the EMI standard and leakage limitation specification. To eliminate the leakage current entirely, optimized transformer architecture is present first. Analysis of the transformer architecture as well as the auxiliary winding has been carried out. Both flyback converter and *LLC* converter are built to verify this method. Then, a novel topology suitable for non-Y-capacitors converter is proposed. The design procedure of the proposed topology is discussed in detail as the flyback converter an example. The proposed concept is also applied to several popular converter topologies, such as forward, half-bridge converter.

In conclusion, a novel non-Y-capacitor EMI design concept is proposed to satisfy the strict leakage current limitation. Optimized transformer architecture and proposed balanced winding topology are verified to be two effective methods for non-Y-cap design to eliminate the leakage current entirely.

References

[1] *Information Technology Equipment—Safety—Part 1: General Requirements*, International Standard IEC 60950-1.

[2] *Information Technology Equipment—Safety—Part 8: Medical Electrical Equipment*, International Standard IEC 60950-1.

[3] F. Costa, E. Laboure, F. Forest, and S. Lefebvre, "Quantification and minimization of conducted interferences generated in hard switching and zero current switching cells," in *Proc. IEEE Appl. Power Electron. Conf.*, Orlando, FL, USA, 1994, pp. 615–621.

[4] M. R. Yazdani, H. Farzanefard, and J. Faiz, "EMI analysis and evaluation of an improved ZCT flyback converter" *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2326–2334, Jun. 2012.

[5] Y. P. Chan, B. M. H. Pong, N. K. Poon, and J. C. P. Liu, "Common-mode noise cancellation in switching-mode power supplies using an equipotential transformer modeling technique" *IEEE Trans. Electronmagn. Compat.*, vol. 54, no. 3, pp. 594–602, Jun. 2012.

[6] K. K. Tse, H. S. H. Chung, S. Y. R. Hui, and H. C. So, "A comparative study of carrier-frequency modulation techniques for conducted EMI suppression in PWM converters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 3, pp. 618–627, Jun. 2002.

[7] D. Gonzalez, J. Balcells, A. Santolaria, J. C. L. Bunetel, J. Gago, D. Magnon, and S. Brehaut, "Conducted EMI reduction in power converters by means of periodic switching frequency modulation" *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2271–2281, Nov. 2007.

[8] J. Balcells, A. Santolaria, A. Orlandi, D. Gonzalez, and J. Gago, "EMI reduction in switched power converters using frequency modulation techniques" *IEEE Trans. Electromagn. Compat.*, vol. 47, no. 3, pp. 569–576, Aug. 2005.

[9] M. Rose, J. Krupar, and H. Hauswald, "Adaptive dv/dt and di/dt control for isolated gate power devices," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 927–934.

[10] J. D. Kagerbauer and T. M. Jahns, "Development of an active dv/dt control algorithm for reducing inverter conducted EMI with minimal impact on switching losses," in *Proc. IEEE Power Electron. Spec. Conf.*, 2007, pp. 894–900.

[11] W. T. Ng and A. Shorten, "Efficiency enhancement and EMI suppression via dynamically adjustable gate driving strength," in *Proc. IEEE 54th Int. Midwest Symp. Circuits Syst.*, 2011, pp. 1–4.

[12] N. Idir, R. Bausiere, and J. J. Franchaud, "Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 849–855, Jul. 2006.

[13] F.-Y. Shih and D. Y. Chen, "A procedure for designing EMI filters for AC line applications," *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 170–181, Jan. 1996.

[14] K. Raggl, T. Nussbaumer, and J. W. Kolar, "Guideline for a simplified differential-mode EMI filter design," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 1031–1040, Mar. 2010.

[15] W. Chen, X. Yang, J. Xue, and F. Wang, "A novel filter topology with active motor CM impedance regulator in PWM ASD system," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6938–3946, Dec. 2014.

[16] H. I. Hsieh, J. Li, and D. Chen, "Effects of X capacitors on EMI filter effectiveness," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 949–955, Feb. 2008

[17] L. Carmody and U. Vichate, "Design and measurement of μA leakage current EMI filter," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, 2003, vol. 2, pp. 622–625.

[18] M. R. B. M. Shariff, M. F. L. Abdullah, M. Y. B. A. Latiff, G. B. M. Tion, Z. A. Haron, and A. Johari, "Impact of EMI filter installed in AC UPS system to earth leakage current," in *Proc. IEEE 8th Int. Power Eng. Optim. Conf.*, 2014, pp. 647–652.

[19] X. Pingfan, Q. Dongyuan, and Z. Bo, "Conducted EMI suppression method based on obstructing grounding loops," in *Proc. IEEE 6th Int. Power Electron Motion Control Conf.*, 2009, pp. 2669–2672.

[20] J.-H. Choi, M. Madafshar, and K. Parmenter, "Designing common-mode (CM) EMI noise cancellation without Y-capacitor" in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2007, pp. 936–940.

[21] Y. P. Chan, B. M. H. Pong, N. K. Poon, and J. C. P. Liu, "Common-mode noise cancellation in switching-mode power supplies using an equipotential transformer modeling technique" *IEEE Trans. Electronmagn. Compat.*, vol. 54, no. 3, pp. 594–602, Jun. 2012.

[22] Y. Yang, D. Huang, F. C. Lee, and Q. Li, "Transformer shielding technique for common mode noise reduction in isolated converters" in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 4149–4153.

[23] P. Kong and F. C. Lee, "Transformer structure and its effects on common mode EMI noise in isolated power converters" in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2010, vol. 2, pp. 1424–1429.
[24] H.-I. Hsieh and S.-F. Shih, "Effects of transformer structures on the noise balancing and cancellation mechanisms of switching power converters" in *Proc. Int. Power Electron. Conf.*, 2014, pp. 2380–2384.
[25] L. Xie, X. Ruan, Q. Ji, and Z. Ye, "Shielding cancelation technique for suppressing common-mode EMI in isolated power converters" *IEEE Trans. Electron.*, vol. 62, no. 5, pp. 2814–2822, May 2015.
[26] Z. Lu and W. Chen, "Common mode EMI noise reduction technique by noise path configuration of high frequency power transformer," in *Proc. IEEE Conf. Power Electron. Motion Control*, 2009, pp. 954–956.
[27] D. Cochrane, D. Y. Chen, and D. Boroyevic, "Passive cancellation of common-mode noise in power electronic circuits," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 756–763, May 2003.
[28] M. Shoyama, G. Li, and T. Ninomiya, "Balanced switching converter to reduce common-mode conducted noise," *IEEE Trans. Ind. Electron.*, Vol. 50, no. 6, pp. 1095–1099, Dec. 2003.
[29] S. Wang, P. Kong, and F. C. Lee, "Common mode noise reduction for boost converters using general balance technique," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1410–1416, Jul. 2007.
[30] S. Wang and F. C. Lee, "Analysis and applications of parasitic capacitance cancellation techniques for EMI suppression," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3109–3117, Sep. 2010.
[31] M. M. Jha, K. B. Naik, and S. P. Das, "Types of electromagnetic interferences in SMPS and using Y-capacitor for mitigation of mixed mode noise," in *Proc. Int. Conf. Power, Control Embedded Syst.*, 2010, pp. 1–6.
[32] P. Kong, S. Wang, F. C. Lee, and Z. Wang, "Reducing common-mode noise in two-switch forward converter," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1522–1533, May 2011.
[33] D. Fu, S. Wang, P. Kong, F. C. Lee, and D. Huang, "Novel techniques to suppress the common-mode EMI noise caused by transformer parasitic capacitances in DC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4968–4977, Nov. 2013.
[34] K. Nguyen-Duy, Z. Ouyang, L. P. Petersen, A. Knott, O. C. Thomsen, and M. A. E. Andersen "Design of a 300-W isolated power supply for ultrafast tracking converters," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3319–3333, Jun. 2015.

Yongjiang Bai (S'15) received the B.S. and M.S. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2004 and 2007, respectively, where he is currently working toward the Ph.D. degree in electrical engineering.

From 2007 to 2012, he was a Research Engineer with FSP-Powerland, Xi'an. His main research interests include electromagnetic interference, control technology, and power electronic integration. He has applied for more than ten China and the United States patents in this area.

Xu Yang (M'02) received the B.S. and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 1994 and 1999, respectively.

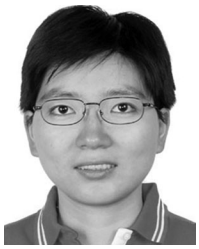
Since 1999, he has been a Member at the Faculty of School of Electrical Engineering, Xi'an Jiaotong University, where he is currently a Professor. From November 2004 to November 2005, he was with the Center of Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, as a Visiting Scholar. He then came back to Xi'an Jiaotong University, and involved in the teaching and researches in power electronics and industrial automation area. His research interests include soft-switching topologies, PWM control techniques and power electronic integration, and packaging technologies.

Dan Zhang received the B.Sc. degree from the Nanjing University of Science and Technology, Nanjing, China, in 2009, and the M.Eng. degree from Xi'an Jiaotong University, Xi'an, China, in 2011.

She is currently a System Engineer at the Department of Application Engineer, Silergy, Corp., Xi'an. Her work includes the solution to EMI issue in low-power SMPS. She has applied for three China and the United States patents in this area. In the period of graduate study, her research interests include the power electronics integration and high-power density converter.

Xinlei Li received the B.S. and M.S. degrees in electrical engineering from Yanshan University, Hebei, China, in 2007 and 2010, respectively.

From 2010 to 2012, he was a Researcher Engineer with FSP-Powerland, Xi'an, China. He is currently a System Engineer at the Department of Application Engineer, Silergy, Corp., Xi'an. His work includes the solution to EMI issue in low-power SMPS. In the research period of graduate study, his research interests include the power electronics integration and soft-switching techniques.



Wenjie Chen (S'06–M'08) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 1996, 2002, and 2006, respectively.

Since 2002, she has been a Member at the Faculty of School of Electrical Engineering, Xi'an Jiaotong University, where she is currently a Professor. From January 2012 to January 2013, she was with the Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville, TN, USA, as a Visiting Scholar. She then came back to Xi'an Jiaotong University, and involved in the teaching and researches in power electronics. Her main research interests include electromagnetic interference, active filters, and power electronic integration.

Weihao Hu (S'06–M'13–SM'15) received the B.Eng. and M.Sc. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2004 and 2007, respectively, and the Ph.D. degree from Aalborg University, Aalborg, Denmark, in 2012.

He is currently an Associate Professor at the Department of Energy Technology, Aalborg University, where he is the Vice-Program Leader of the Wind Power System Research Program. He has participated in several national and international research projects and he has more than 75 publications in his technical field. His research interests include wind power generation and intelligent energy systems.

Dr. Hu is currently serving as the Secretary and Treasurer of the Power and Energy Society Chapter, IEEE Denmark Section.