Capacitance Minimization in Offline LED Drivers Using an Active-Ripple-Compensation Technique

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***Abstract*—This study proposes a novel approach for low-frequency output current ripple minimization in offline light-emitting diode (LED) drivers. This strategy is based on the large-signal modulation of the LED converter duty-cycle so that the output ripple can be reduced and, consequently, the required filtering capacitances of the converter can be somehow decreased. This technique is devised to be used on converters in which a single control loop is employed, such as offline integrated converters, where a single control loop is responsible to control the output current while maintaining the high power factor at the input (mains). The duty-cycle modulation is used to change the shape of the main waveforms of the converter, especially input and output currents. This allows for a reduction of the output current peak-to-peak ripple while the harmonic content of the input current is increased but kept within the limits imposed by the IEC standard. An application example for an integrated two-stage converter based on the cascade connection of two buck–boost converters is shown. Experimental results from a 70-W laboratory prototype supplied from a 115-V grid were carried out and compared with conventional approaches in order to verify the feasibility of the proposed technique.**

***Index Terms*—Active ripple compensation, capacitance reduction, electrolytic capacitor avoidance, high reliability, light-emitting diode (LED) drivers, offline operation, power factor correction (PFC), power supplies.**

I. Introduction

THE solid-state lighting concept arises with the promise of being an efficient, durable, and environmentally friendly technology. Recent researches and also commercially available products already show that LEDs can achieve a very high luminous efficacy as well as a long lifespan [1]–[2]. However, in order to maximize the benefits of this technology, the LED driver must be designed to ensure a tightly controlled current through the LEDs. This includes both the control of the average value and the limitation of the peak-to-peak current ripple. The latter could be a problem when the driver circuit is fed from the mains, since usually a large low-frequency ripple must be filtered to compensate the input-to-output instantaneous power imbalance [3]. Other requirements for offline LED driving includes power factor correction (PFC) and high efficiency [3]–[17].

It was shown in [17]–[20] that the photometrical performance of the LEDs is not only directly related to the thermal management of the devices, but also to the nature and regime of the current that flow through them.

Therefore, for most applications, it is mandatory to keep the current ripple of the LEDs within a certain limit, thus guaranteeing that the light output achieves the desired performance whereas also avoiding stroboscopic and flickering effects, which could be noticeable to the human eye in some circumstances [20].

The task of low-frequency ripple filtering is normally accomplished by using bulky storage elements, usually electrolytic capacitors, which are known to reduce the driver lifespan, or alternatively by using a bank of metalized film capacitors, which have better lifespan, but decrease the power density of the drivers [21]. This could be a problem in applications where the available space for the electronic driver is limited. Another solution consists on using higher temperature long-life electrolytic capacitors, which are much more expensive than conventional ones.

In order to overcome those problems, several works have proposed different techniques to reduce the required filtering capacitances in offline converters [3], [8]–[17] and [22]–[23]. Some of these techniques are based on the reduction of the instantaneous power unbalance between the input and the output of the converter, which causes a reduction of the output current ripple. In [15] and [16], the injection of harmonic components in the input current is proposed, aiming for reducing the peak-to-average ratio of the instantaneous input power. This task was accomplished by modifying the standard control loop of a current-mode controlled PFC converter in order to provide a nonsinusoidal reference for the input current, including a certain amount of third [15] and fifth [16] harmonics so that the output ripple was decreased.

A similar strategy was proposed in [23], using also a current-mode controlled PFC converter with a nonsinusoidal input current reference, aiming the reduction of the output ripple. However, differently from [15] and [16], the analysis presented in [23] took into account the limits of harmonic injection imposed by the IEC-61000-3-2 standard [24] in order to generate the reference for the input current.

One drawback of the harmonic injection techniques presented in [15], [16], and [23] is that two control loops are needed. Furthermore, the complexity of the control structure is increased when compared to the conventional current-control mode.

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On the other hand, the approaches presented in [3], [8], [10]–[14], and [17] all focus on alternative topologies or design procedures to reduce the required filtering capacitances. Most of them propose the use of two-stage drivers, where the first stage is the PFC preregulator and the second one controls the power delivered to the load (PC stage) and minimizes the output current ripple. Furthermore, some proposals addressed the use of integrated converters, where the PFC and PC stage are integrated so that the number of active switches could be reduced, allowing for a reduction of the cost and volume of the converter. The converter integrations also allow an increase of the reliability of the system by reducing the amount of subsystems (e.g., MOSFET drivers, sensors, control loops, and controllers).

Regarding the integrated converters, the use of a front-end converter operating in discontinuous conduction mode (DCM) to perform the PFC function is quite suitable, since it simplifies the implementation of the control loop and minimizes the number of auxiliary circuits. Therefore, the voltage-mode control (VMC) is used in the majority of applications that use integrated LED drivers, as can be observed in [8], [10]–[12], and [17].

On the other hand, the strategy of reducing the instantaneous power imbalance presented in [15]–[16] and [23] is implemented in converters operating with current-mode control, in which two control loops are needed: one outer loop for controlling the output variable and an inner loop to control the magnitude and shape of the input current. Therefore, these strategies are not suitable for integrated converters, since the input stage is normally operating in DCM, as already mentioned.

In this paper, a novel active ripple compensation technique (ARCT) applied to an offline integrated LED driver is proposed. The approach allows for a further current ripple reduction by means of a proper modulation of the converter duty-cycle. This task can be done by adding an additional branch to the traditional control structure and, therefore, it does not require any extra sensor, thus resulting in a low cost, easily implementable solution.

Since in integrated converters the PFC and the PC stage are controlled by a single control loop, the modulation of the duty-cycle will affect both the output variable (i.e., the LED current ripple) and the input variables (i.e., the power factor and the input current distortion). Bearing in mind these limitations, the design methodology proposed in this study deals with this issue by calculating the elements of the converter and the control loop so that the output ripple can be minimized while also ensuring that the input current harmonics remain in compliance with the IEC-61000-3-2 standard.

The remainder of this paper is organized as follows. Section II introduces the double buck–boost: the converter in which the technique was applied. Section III presents the design strategy using the proposed technique. In Section IV, the design of the control system is shown. Section V presents experimental results from a laboratory prototype. Finally, the conclusions of this work are detailed in Section VI.

II. Integrated Double Buck–Boost

As already mentioned, this paper proposes a strategy for current ripple minimization in off-line LED drivers. In this study, the proposed approach was applied to an Integrated Double Buck–Boost (IDBB) converter operating in full DCM. Operation in full DCM means that both stages operate in DCM [12]. This converter has been chosen because it is a simple cascade connection of two buck–boost converters operating in DCM and, under this operating condition, the input current of each stage does not depend on its output voltage. This characteristic dramatically simplifies the derivation of the functions that describe the converter operation, as will be shown in the following analysis. Despite the choice of the IDBB converter, it is important to highlight that the proposed technique can be also applied to other PWM integrated converters in which the PFC stage is also operating in DCM, such as the SEPIC Buck-Boost [17] and the Buck–Flyback [22].

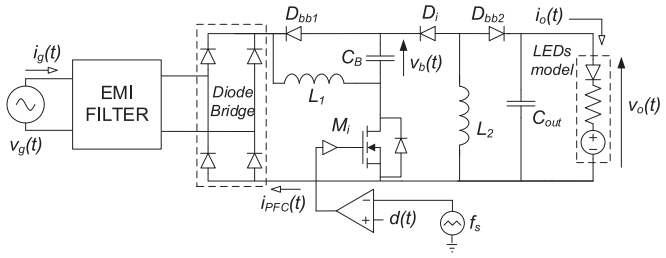


Fig. 1. Integrated Double Buck–Boost converter as an offline HPF LED driver.

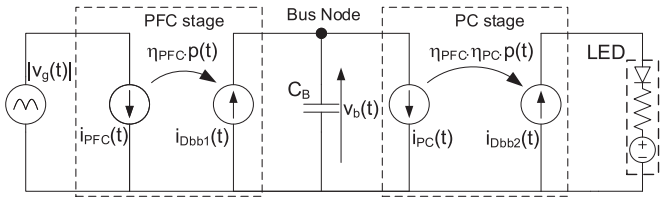


Fig. 2. Large-signal low-frequency model of the IDBB converter

Fig. 1 shows the topology of the IDBB converter. In this circuit, the bus capacitor C_B is the element responsible for filtering the low-frequency ripple of the circuit. Therefore, C_B is the bulkiest capacitance in the IDBB converter. Fig. 1 also shows that the duty-cycle of the converter is modulated according a command signal $d(t)$, whose characteristic might allow for the compensation of the low-frequency ripple of the output current.

The integration of the PFC and the PC stages in the IDBB converter used a method called "graft-scheme" [25]. This technique allows the analysis of the PFC and the PC stages independently, just by considering that the frequency and the duty-cycle of these stages are the same.

In offline converters, it is well-known that the main variables (e.g., the output current) oscillate at twice the line frequency. Therefore, it is suitable to derive a low-frequency large-signal circuit model in order to analyze the IDBB converter and highlight the input and the output variables of the driver. This model can be seen in Fig. 2, in which it is possible to observe that the energy transfer in the converter is performed in two stages. At first, the input power $d(t)$ is delivered to the dc bus via the PFC stage and then the PC stage transfers the dc bus power to the output. The losses in the power conversion process are

represented by the efficiencies of the input and the output stages, which are η_{PFC} and η_{PC}, respectively.

The instantaneous power at the input of the converter $p(t)$ is defined in (1) as the multiplication of the rectified input voltage, $|v_g(t)|$, defined in (2), by the input current $i_{\mathrm{PFC}}(t)$, whose definition is stated in (3) [12]

$$p(t) = |v_g(t)|\, i_{\mathrm{PFC}}(t) \tag{1}$$

$$|v_g(t)| = \left|\sqrt{2}V_G \sin(\omega_L t)\right| \tag{2}$$

$$i_{\mathrm{PFC}}(t) = \frac{|v_g(t)|\, d(t)^2}{2L_1 f_s} \tag{3}$$

where V_G and w_L are the RMS value and the angular frequency of the mains voltage, L_1 is the inductance related to the PFC stage and f_s is the switching frequency of the converter.

As already mentioned, the main variables of the converter oscillate at twice the line frequency. Therefore, a duty-cycle signal having a $2\omega_L$ component was chosen, allowing it to influence the large-signal behavior of the converter. So, the duty- cycle has the form as defined by (4). Note that this parameter has a dc component, which has a major influence on the average variables (e.g., the average output current), and a component oscillating at twice the line frequency with a magnitude D_1 and a phase shift ϕ_{c1} in relation to the first harmonic component of the rectified line voltage. D_1 and ϕ_{c1} will be called ARCT parameters because they govern the behavior of the active compensation technique

$$d(t) = D_0 + D_1 \sin(2\omega_L t + \phi_{c1}). \tag{4}$$

By using the definition of the duty-cycle given by (4) in (3), the input current of the converter can be calculated as shown in (5).

The analysis of the input current was carried out considered that the EMI filter has no effect on the input current harmonics, in other words, the cutoff frequency of the EMI filter is much higher than the line frequency

$$\begin{aligned} i_g(t) = \frac{\sqrt{2}V_G}{2L_1 f_s} \big[& {D_0}^2 \sin(\omega_L t) \\ & + 2D_0 D_1 \sin(\omega_L t)\sin(2\omega_L t + \phi_{c1}) \\ & + {D_1}^2 \sin(\omega_L t)\sin^2(2\omega_L t + \phi_{c1})\big]. \end{aligned} \tag{5}$$

In order to obtain the harmonic components of the input current, it is necessary to simplify (5) using trigonometric relationships and Fourier expansion. This mathematical manipulation yields

$$\begin{aligned} i_g(t) = {} & I_1 \sin(\omega_L t + \phi_1) + I_3 \sin(3\omega_L t + \phi_3) \\ & + I_5 \sin(5\omega_L t + \phi_5) \end{aligned} \tag{6}$$

where the magnitudes and phases of the harmonic components are given by

$$I_1 = \frac{\sqrt{2}V_G}{2L_1 f_s} \left[\begin{array}{c} \left({D_0}^2 + \dfrac{{D_1}^2}{2} - D_0 D_1 \sin(\phi_{c1}) \right)^2 \\ + (D_0 D_1 \cos(\phi_{c1}))^2 \end{array} \right]^{\frac{1}{2}} \tag{7}$$

$$\phi_1 = tg^{-1}\left(\frac{2D_0 D_1 \cos(\phi_{c1})}{2{D_0}^2 + {D_1}^2 - 2D_0 D_1 \sin(\phi_{c1})} \right) \tag{8}$$

$$I_3 = \frac{\sqrt{2}V_G}{4L_1 f_s} \left[\begin{array}{c} \left(2D_0 D_1 \sin(\phi_{c1}) + \dfrac{{D_1}^2}{2}\cos(2\phi_{c1}) \right)^2 \\ + \left(\begin{array}{c} \dfrac{{D_1}^2}{2}\sin(2\phi_{c1}) \\ - 2D_0 D_1 \cos(\phi_{c1}) \end{array} \right)^2 \end{array} \right]^{\frac{1}{2}} \tag{9}$$

$$\phi_3 = tg^{-1}\left(\frac{\frac{{D_1}^2}{2}\sin(2\phi_{c1}) - 2D_0 D_1 \cos(\phi_{c1})}{2D_0 D_1 \sin(\phi_{c1}) + \frac{{D_1}^2}{2}\cos(2\phi_{c1})} \right) \tag{10}$$

$$I_5 = \frac{\sqrt{2}V_G {D_1}^2}{8L_1 f_s} \tag{11}$$

$$\phi_5 = 2\phi_{c1} + \pi. \tag{12}$$

As can be seen, with the proposed duty-cycle signal given by (4), only the harmonics 1, 3, and 5 are present in the input current.

From the analysis of the harmonic components of the input current it is possible to note that average value of $d(t)$, D_0, is related to the active power delivered to the load. This assumption can be verified by means of (7), in which it is noticeable that if D_0 is much greater than D_1, the first harmonic of the input current will depend mostly on D_0. Thus, the active power will be mostly controlled by the average value of the duty-cycle.

The current sources $i_{\mathrm{Dbb1}(t)}$ and $i_{\mathrm{PC}}(t)$ of the model presented in Fig. 2 can be obtained by equating the current through D_{bb1} and the current at the input of the PC stage. These variables are defined in

$$i_{\mathrm{Dbb1}}(t) = \eta_{\mathrm{PFC}} \frac{v_g(t)^2 d(t)^2}{2L_1 f_s v_b(t)} \tag{13}$$

$$i_{\mathrm{PC}}(t) = \frac{v_b(t)\, d(t)^2}{2L_2 f_s} \tag{14}$$

where $v_b(t)$ is the instantaneous bus voltage and L_2 is the inductor of the PC stage.

The current through C_B can be calculated as follows:

$$i_{C_B}(t) = C_B \frac{dv_b}{dt} = i_{\mathrm{Dbb1}}(t) - i_{\mathrm{PC}}(t). \tag{15}$$

By manipulating (13)–(15), the differential equation of the bus voltage is found, as shown in

$$\frac{dv_b(t)}{dt} = \frac{1}{2C_B f_s}\left(\eta_{\mathrm{PFC}} \frac{v_g(t)^2 d(t)^2}{L_1 v_b(t)} - \frac{v_b(t)\, d(t)^2}{L_2} \right). \tag{16}$$

Regarding the output current of the IDBB converter, it can be found by evaluating the instantaneous power balance in the

second stage of the LED driver, which is described by

$$p_b\left(t\right) = \frac{p_o\left(t\right)}{\eta_{\mathrm{PC}}}. \tag{17}$$

The instantaneous bus power is obtained by multiplying the bus voltage and the input current of the second stage, which yields

$$p_b\left(t\right) = \frac{v_b(t)^2 d(t)^2}{2L_2 f_s}. \tag{18}$$

The expression of the power delivered to the LEDs is found by means of the equivalent load model—the threshold voltage V_T and the dynamic resistance r_d of the LED string, thus resulting in

$$p_o\left(t\right) = V_T i_o\left(t\right) + r_d i_o(t)^2. \tag{19}$$

By replacing (19) and (18) in (17) and solving for the output current, the expression of the current through the LED string is found, as shown in

$$i_o\left(t\right) = \sqrt{\left(\frac{V_T}{2r_d}\right)^2 + \eta_{\mathrm{PC}}\frac{v_b(t)^2 d(t)^2}{2L_2 f_s r_d}} - \frac{V_T}{2r_d}. \tag{20}$$

The inexistence of a closed-form solution for the bus voltage implies that both the bus voltage and the output current must be solved numerically. The instantaneous bus voltage $v_b(t)$ must be found by using some numerical integration technique. In this paper in particular, the composite rectangular rule was chosen, which yields

$$v_b(t_f) = \int_{t_1}^{t_f} \frac{dv_b(t)}{dt}dt \approx s_t \sum_{n=0}^{N-1} \frac{\Delta v_b(t_n)}{\Delta t} \tag{21}$$

where t_1 and t_f are the initial and final time of the solution procedure, respectively, s_t is the time step size used and *N* is the number of steps, defined in (22). The variable t_n is *n*th time step, defined in (23). In this study, a step size s_t of one thousandth of the line period was used, the initial time t_1 was zero and the final time t_f was equal to five line periods

$$N = \frac{t_f - t_1}{s_t} \tag{22}$$

$$t_n\left(n\right) = t_1 + n s_t. \tag{23}$$

The solution of the output current was then obtained simultaneously with the bus voltage. In other words, for each $v_b(t_n)$, an output current value $i_o(t_n)$ is calculated by using (20).

III. Design Procedure

This section shows a procedure for designing the IDBB converter with the large-signal duty-cycle modulation proposed in this paper. This procedure can be extended to other topologies just by obtaining the description of the input and output currents for such converters and by applying the presented design procedure in a similar way.

The input parameters for this design example are shown in Table I. Since the output current ripple varies with the input voltage, the converter must be designed under worst-case conditions, which occur for the lowest mains voltage (90 V in this case). Thus, the analysis in this section will consider this voltage level.

TABLE I
Input Parameters of the Design Example

Item	Description	Value
V_G	RMS value of the mains voltage	90-140 V
f_L	frequency of the mains voltage	60 Hz
f_s	switching frequency	50 kHz
I_o	output current	500 mA
V_o	output voltage	139.9 V
P_o	output power	70 W
V_T	threshold voltage of the LED string	130.2 V
r_d	dynamic resistance of the LED string	19.34 Ω
$\Delta_{\mathrm{Io\_LF\_max}}$	maximum peak-to-peak ripple of the output current	250 mA (50%)
$\Delta_{\mathrm{Io\_HF\_max}}$	maximum high frequency ripple of the output current	30 mA
$V_{\mathrm{B\_max}}$	Maximum bus voltage	180 V
η_{PFC}	Efficiency of the PFC stage	0.922
η_{PC}	Efficiency of the PC stage	0.922

A. Definition of the Operating Point and Calculation of the Inductances

As mentioned in Section I, the converter is devised to operate in full DCM. Therefore, the design of the inductors L_1 and L_2 must ensure this operating condition so that all the relationships established in the theoretical analysis are valid. Furthermore, the maximum bus voltage allowed for this application cannot exceed the maximum value defined in Table I. This is done in order to avoid large voltage stresses on the semiconductors.

In order to ensure DCM operation for both stages, it is necessary to define a critical value of the duty-cycle. According to [12], the expressions (24) and (25) can be used to find the critical duty-cycle for the PFC and PC stages, respectively

$$D_{C\_\mathrm{PFC}} = \frac{V_{B\_\min}}{V_{B\_\min} + \sqrt{2}V_{G\_\min}} \tag{24}$$

$$D_{C\_\mathrm{PC}} = \frac{V_o}{V_o + V_{B\_\min}} \tag{25}$$

where $V_{G\_\min}$ is the lowest RMS value of the input voltage (i.e., 90 V), V_o is the output voltage, defined in (26) and $V_{B\_\min}$ is the minimum bus voltage, given by (27)

$$V_o = V_T + r_d I_o \tag{26}$$

$$V_{B\_\min} = V_{B\_\max}\frac{V_{G\_\min}}{V_{G\_\max}} \tag{27}$$

where $V_{G\_\max}$ is the maximum RMS value of the input voltage (i.e., 140 V).

Equation (27) states that the bus voltage varies linearly with the input voltage. This characteristic is a result of the integration of the PFC and the PC stages in DCM [12]. The bus voltage of an integrated converter operating in full DCM depends only on a relationship between the inductances of both stages, as

expressed by (28) and demonstrated in [12]

$$V_B = V_G \sqrt{\frac{L_2}{L_1}}. \tag{28}$$

The inductance L_1 can be calculated using (29), which is derived from the converter power balance relationship. As it can be seen, this expression depends on the global efficiency of the converter $\eta_G = \eta_{\mathrm{PFC}} \cdot \eta_{PC}$ and also on the value of D_0. This equation has been obtained by supposing that the active power of the converter is dependent only on the dc value of the duty-cycle, which is a reasonable assumption, as it has previously been commented

$$L_1 = \eta_G \frac{{D_0}^2 {V_{G\_\min}}^2}{2 V_o I_o f_s}. \tag{29}$$

In order to obtain the value of L_1, it is necessary to choose an operating point for D_0 that satisfies the expression defined in (30). This condition ensures DCM operation for both converters in all situations, because it takes into account the maximum allowable magnitude of the ac component of the duty-cycle, $D_{1\_\max}$. Thus, the sum of D_0 and D_1 will never exceed the critical value of the duty-cycle. Finally, the inductor L_2 can be designed by using $V_{G\_\min}$ and $V_{B\_\min}$ in (28)

$$D_0 < D_C - D_{1\_\max} \tag{30}$$

where the critical duty-cycle D_C is defined in

$$D_C = \min\left(D_{C\_\mathrm{PFC}}, D_{C\_\mathrm{PC}}\right). \tag{31}$$

It is important to highlight that if D_0 is chosen much lower than the critical duty-cycle, the peak current of the inductors will increase dramatically. Owing to this operational constraint, $D_{1\_\max}$ was chosen to be about 10% of the critical duty-cycle, allowing the use of a D_0 closer to D_C. Considering $D_{1\_\max}$ equals to 0.05, the chosen value for D_0 was 0.36.

The calculation of the inductances can be performed by using the values of Table I in (29) and then by using (28) considering $V_G = V_{G\_\min}$ and $V_B = V_{B\_\min}$. Moreover, the calculated global efficiency is 85%, as obtained from the product of the efficiencies of the PC and the PFC stages stated in Table I. The described calculation procedure yields $L_1 = 127\ \mu$H and $L_2 = 204\ \mu$H.

B. Calculation of the IDBB Capacitances and the ARCT Parameters

The calculation of the ac component of the duty-cycle signal must be performed in two steps. The first one is the evaluation of the behavior of the input current owing to variations of the magnitude and phase of the oscillating portion of $d(t)$. This analysis yields the allowable limits for D_1 and ϕ_{c1} based on the constraints imposed by the IEC-61000-3-2 standard. The definition of the ARCT parameters is then done, in which the bus capacitor (C_B) is designed simultaneously with D_1 and ϕ_{c1} so that the output ripple is below the desired limits constrained in Table I (i.e., 50% peak-to-peak), whereas the value of C_B is chosen to be the lowest possible.

Since the input current waveform does not depend on the bus capacitance, the behavior of its harmonic content according to the variations in D_1 and ϕ_{c1} can be graphically visualized. By using the parameters defined in Table I and also those calculated in Section III-A, the input current third and fifth harmonics can be plotted, as shown in Fig. 3. This illustration shows that the third harmonic component is closer to its IEC limit than the fifth and, therefore, it restricts the range of D_1 and ϕ_{c1}. Nevertheless, if D_1 is kept below $D_{1\_\max}$, the converter will comply with the IEC-61000-3-2 regardless the value of ϕ_{c1}, as clearly seen in Fig. 3(a).

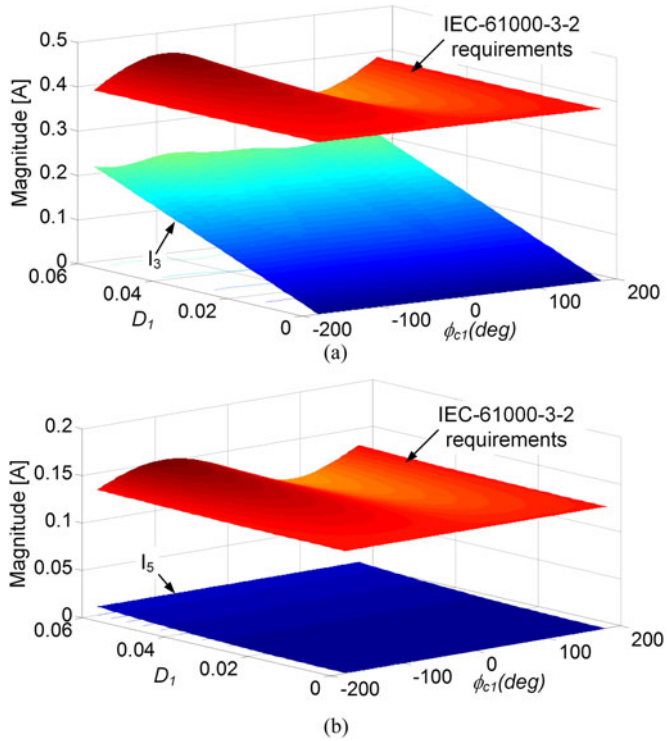


Fig. 3. Harmonic content of the input current according to the oscillating component of the duty cycle: (a) third harmonic component; (b) fifth harmonic component.

Fig. 4 shows these curves. The low-frequency output current ripple behavior according variations in D_1 and ϕ_{c1} for several values of C_B are plotted. As can be seen, for each value of C_B, a family of curves is generated, being each one parameterized by a certain value of D_1, with values ranging from $D_1 = 0$ up to $D_1 = D_{1\_\max}$ in steps of 0.005.

From Fig. 4 it is possible to observe that the ARCT parameters have a high influence on the output current ripple value, as expected. Furthermore, one can also notice the behavior of the

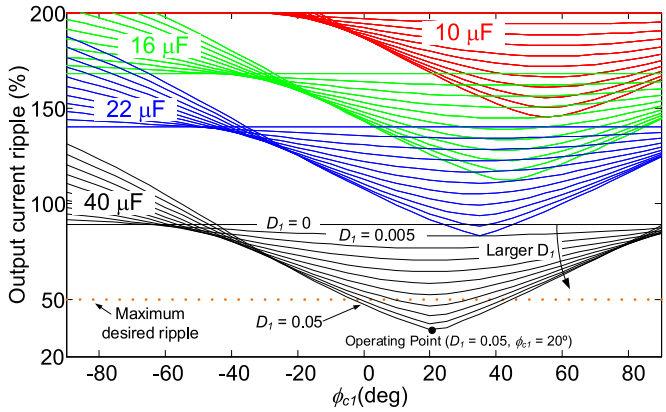


Fig. 4. Behavior of the peak-to-peak output current ripple according to the ARCT parameters for several values of C_B.

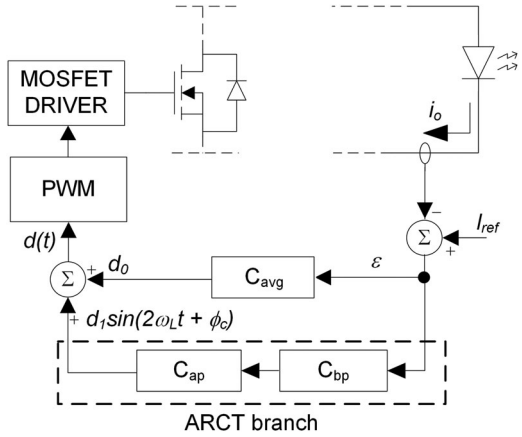


Fig. 5. Diagram of the proposed closed-loop system.

converter without the ARCT, analyzing those curves in which D_1 value is zero (no large-signal modulation whatsoever).

As can be seen, if C_B is chosen to be equal to 10, 16 or 22 μF, the ripple criterion will not be met regardless of the ARCT parameters. However, if a capacitance of 40 μF is selected, the output ripple will be lower than $\Delta_{\mathrm{Io\_LF\_max}}$ if $D_1 \geq 0.04$ and $0° \leq \phi_{c1} \leq 40°$. By using this graphical analysis, the chosen ARCT parameters were $D_1 = 0.05$ and $\phi_{c1} = 20°$ because this operating point makes the output current ripple to be at its minimum for $C_B = 40\,\mu$F. Furthermore, this choice maximizes the robustness of the system: even if D_1 decreases by 20% and ϕ_{c1} varies by $\pm 20°$, the output ripple will remain below the maximum desired value of 50%.

Fig. 4 also shows that without employing the ARCT (i.e., $D_1 = 0$), a 40 $-$ μF bus capacitor would be insufficient to meet the ripple requirements. This shows that such effectiveness of the proposed technique.

The bus capacitance value can be further decreased if a larger value of V_B is chosen. However, such choice would affect negatively the efficiency of the converter, since the voltage stresses in the semiconductors would be larger.

Finally, the output capacitor of the PC stage must be designed to filter the high-frequency component of the output current, which is described by (32) for the buck–boost converter [17]. Taking into account this equation, the constraints stated in Table I (i.e., $\Delta I_{o\_\mathrm{HF}} < 30$ mA) and the laboratory availability, the chosen output capacitor was 16 μF

$$\Delta I_{o\_\mathrm{HF}} = \frac{1}{f_s C_{\mathrm{out}} r_d}\left(I_o + \frac{\Delta I_{o\_\mathrm{LF}}}{2}\right)\left(1 - D_0 \frac{V_{B\_\mathrm{min}}}{V_o}\right). \tag{32}$$

IV. Control System Design

The analysis performed in the previous sections considered that the converter operates in open-loop configuration and only returns, which are the values for the modulating signal (i.e., the large-signal duty-cycle $d(t)$). However, in real applications, a closed-loop control system is desired allowing the driver to deal with load and mains voltage disturbances while keeping the system under desired goals. The theoretical analysis and the design of such system is outlined in the next sections.

A. Control Loop Arrangement

Owing to the characteristic of the duty-cycle signal, it is necessary to derive a special structure for the control loop, which must be able to synthetize the signal described by (4), that is, both the average value D_0 (responsible for the maintaining constant the average LED current) and the ARCT parameters (responsible for reducing output ripple).

A control circuit structure that is able to synthetize the two terms of the duty-cycle signal has been developed, meeting the performance parameters of the application. Fig. 5 shows the diagram of the proposed closed-loop system, which is able to provide the desired duty-cycle function, solely from the output current error. As can be seen, no extra sensor or control loop is required for this system. Some symbols in the Fig. 5 were written in lower case indicating that these variables varies according to the operating conditions (e.g., d_0 varies with the line voltage). Moreover, in this application, the sensor of the output current has a unity gain and does not insert any phase shift in the measured current.

In this control structure, a band-pass filter C_{bp} was used to isolate the ripple portion at $2\omega_L$, so that the control loop was composed by two frequency-independent branches. Because of this characteristic, each branch is responsible for synthetizing one portion of the whole duty-cycle function. The d_0 component is generated by C_{avg}, which must ensure that the output average current follows the reference with null steady-state error. This controller must be tuned to be slow enough to compensate only the average value of the error signal. It could be a classical proportional-integral controller or even a pure integrator.

The band-pass filter C_{bp} is tuned to twice the line frequency in order to obtain the $2\omega_L$ component of the error signal. It is important to highlight that this component is present in the error signal because the output current oscillates at twice the line frequency due to the inherent input–output instantaneous power imbalance. Regarding C_{ap}, it is an all-pass filter, which provides the oscillating component of the duty-cycle by giving

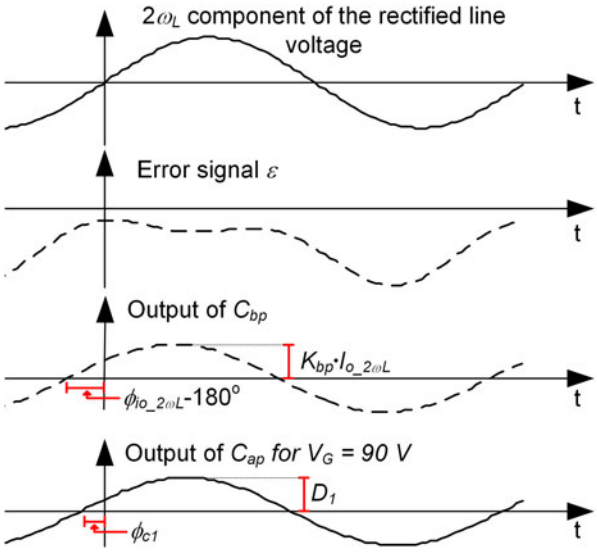


Fig. 6. Theoretical waveforms of the ARCT branch of the control structure.

the correct gain and phase-shift to the $2\omega_L$ component of the error signal.

Fig. 6 shows the theoretical waveforms in the ARCT branch of the proposed control structure. As can be seen, the output of the band-pass filter is the $2\omega_L$ component of the error signal. Therefore, the input of the all-pass filter is directly related to the $2\omega_L$ component of the output current: the magnitude is multiplied by the gain of the band-pass filter and the phase is shifted by 180° (the phase shift of the band-pass filter is zero at $2\omega_L$). One can note that $C_{\rm ap}$ is responsible for conditioning the output of the band-pass filter in order to yield the desired ac component of the duty-cycle (i.e., D_1 and ϕ_{c1}).

It must be pointed that the output of Cap is directly related to the magnitude of the $2\omega_L$ component of the error ε (which is also related to i_o), since it is generated from the output current through a constant gain branch. Therefore, when the output current ripple increases, the value of d_1 will also increase and vice versa. So, the ARCT branch parameters must be calculated so that the condition $d_1 = D_1$ (calculated in Section III-B) is achieved in the worst ripple condition (i.e., when $V_G = 90$ V). This strategy ensures that the ripple never exceeds its maximum desired value (stated in Section III).

It is important to highlight that the control loop shown in Fig. 5 can be applied to any single-stage LED driver based on the VMC, including converters such as the flyback and the Ćuk topology. However, the performance of the ARCT tends to be worse in such cases. This occurs because sole converters (e.g., flyback) normally require higher capacitances than integrated converters and the output-to-control transfer function has a smaller bandwidth [25]–[26]. These characteristics cause a reduction of the effectiveness of the $2\omega_L$ duty-cycle modulation of the ARCT. Therefore, in order to obtain a similar level of capacitance reduction, the magnitude of d_1 in sole converters will be higher than in the integrated topologies, leading to a larger distortion in the input current.

B. Design of the Control loop

One of the advantages of this approach is that both control branches operate independently so that they can also be designed separately. However, the calculation of the elements of these two branches differs from the conventional design procedure of control loops (e.g., the one employing phase and gain margins criteria). The blocks $C_{\rm avg}, C_{\rm bp}$, and $C_{\rm ap}$ can be understood as filters that are responsible for conditioning the "input" signal, which in this case is the current error signal ε, to generate a desired output signal, i.e., the duty-cycle function $d(t)$, as described by (4) and indicated in Fig. 5.

The only constraint regarding $C_{\rm avg}$ is that it must generate a value of d_0 from ε that ensure null steady-state error and it must attenuate all the other frequencies so that d_0 is a pure dc signal. This can be achieved by using a simple integrator, which meets these requirements provided that its crossover frequency is designed to be much lower than $2f_L$. The transfer function of $C_{\rm avg}(s)$ is described by

$$C_{\rm avg}(s) = K_a \frac{1}{s} \tag{33}$$

where it was chosen $K_a = 20$, resulting in a crossover frequency of 3.18 Hz (which is far below $2f_L$).

The expression for $C_{\rm bp}(s)$ was calculated based on a second order band-pass filter tuned at the center angular frequency of $2\omega_L$, thus ensuring that the oscillating component of the duty-cycle presents the desired frequency. Thus, the transfer function of $C_{\rm bp}$ is given by (34), where $K_{\rm bp}$ is the gain at center frequency and B is the bandwidth of the filter

$$C_{\rm bp}(s) = K_{\rm bp} \frac{Bs}{s^2 + Bs + 4{\omega_L}^2}. \tag{34}$$

Finally, the all-pass filter $C_{\rm ap}$ must be designed by considering the magnitude and phase of the output current at the frequency of interest ($2\omega_L$). These values can be obtained from (20) by using Fourier expansion. Thus, the transfer function of $C_{\rm ap}(s)$ is shown in (35) and its parameters must be chosen aiming to ensure that the output waveform of this filter is the desired oscillating component of the duty-cycle signal. This condition is fulfilled by (36) and (37), which were devised from the analysis of the diagram of Fig. 5 and the waveforms shown in Fig. 6

$$C_{\rm ap}(s) = K_{\rm ap} \frac{s + z_{\rm ap}}{s + p_{\rm ap}} \tag{35}$$

$$|C_{\rm ap}(2\omega_L)| = \frac{D_1}{I_{o\_2\omega L} K_{\rm bp}} \tag{36}$$

$$\angle C_{\rm ap}(2\omega_L) = \phi_{c1} - \phi_{io\_2\omega L} - 180^\circ \tag{37}$$

where $I_{o\_2\omega L}, \phi_{io\_2\omega L}$ are the magnitude and the phase of the output current, respectively.

The transfer functions of the filters can be evaluated using the design results presented in Section III. As already mentioned, the values of $I_{o\_2\omega L}$ and $\phi_{io\_2\omega L}$ were obtained from the Fourier analysis of the theoretical output current waveform, which can be evaluated using the values of C_B, D_1, and ϕ_{c1} in (20). Table II summarizes the parameters of the control circuit.

TABLE II
CONTROL CIRCUIT PARAMETERS

Parameter	Value
K_a	20 Hz
$K_{\rm bp}$	1
B	125.66 rad/s
$K_{\rm ap}$	$6.33 \cdot 10^{-1}$
$z_{\rm ap}$	$8.72 \cdot 10^{2}$ rad/s
$p_{\rm ap}$	$6.52 \cdot 10^{2}$ rad/s

C. Digital Implementation

In this study, the control loop was implemented digitally by means of a TIVA C-Series microcontroller. The discretization of the controllers was performed using the Bilinear transformation [27]. The difference equations that represents the compensator $C_{\rm avg}(s)$, the band-pass filter $C_{\rm bp}(s)$, and the all-pass filter $C_{\rm ap}(s)$ are shown in (38)–(40), respectively. Finally, the duty-cycle of the discrete-time system at the *k*th instant is calculated by (41)

$$y_{\rm avg}(k) = N_{a1}\varepsilon(k) + N_{a2}\varepsilon(k+1) - N_{a3}y_a(k+1) \quad (38)$$

$$y_{\rm bp}(k) = N_{\rm bp1}\varepsilon(k) + N_{\rm bp2}\varepsilon(k+2) - N_{\rm bp3}y_{\rm bp}(k+1) - N_{\rm bp4}y_{\rm bp}(k+2) \quad (39)$$

$$y_{\rm ap}(k) = N_{\rm ap1}y_{\rm bp}(k) + N_{\rm ap2}y_{\rm bp}(k+1) - N_{\rm ap3}y_{\rm ap}(k+1) \quad (40)$$

$$d_k(k) = y_a(k) + y_{\rm ap}(k) \quad (41)$$

where $y_{\rm avg}, \varepsilon, y_{\rm bp}, y_{\rm ap}$, and d_k are the discrete variables representing the output of the average current compensator, the error signal, the band-pass filter, the all-pass filter, and the duty-cycle, respectively. The variable *k* is the index of the *k*th sample of the discrete system.

In order to calculate the coefficients of the (38)–(40), a sampling frequency $f_{\rm sam}$ of 5 kHz was considered. According to [28], this choice ensures that a discretization error is lower than 3%, since the largest noticeable frequency in the output current is two decades below the sampling frequency. It is important to highlight that in the experimental evaluation an antialiasing filter at the ADC input was used in order to attenuate the switching harmonics from the measured signal. In this application, the antialiasing filter is a first-order low-pass filter with a cutoff frequency of 2.5 kHz.

The definition and values for each coefficient of (38)–(40) are summarized in Table III.

The flowchart of the algorithm implemented in the microcontroller is shown in Fig. 7. The first two steps concern the configuration of the peripherals of the microcontroller, such as PWM and ADC initialization and setup, and then the initialization of the control variables. Thereafter, the main loop is executed periodically at 5 kHz. The control algorithm is performed in only six straightforward steps, which are the direct implementation of the equations shown in Section IV. Owing to its simplicity, the proposed strategy can be implemented using low-cost microcontrollers, increasing the economic attractiveness of the proposal.

TABLE III
COEFFICIENTS USED IN THE DISCRETE IMPLEMENTATION

Coefficient	Definition	Value
N_{a1}	$\frac{K_a}{2f_{\rm sam}}$	0.002
N_{a2}	$\frac{K_a}{2f_{\rm sam}}$	0.002
N_{a3}	-1	-1
$N_{\rm bp1}$	$\frac{K_{\rm bp}\cdot B\cdot f_{\rm sam}}{2{f_{\rm sam}}^2 + B\cdot f_{\rm sam} + 2{\omega_L}^2}$	0.012341
$N_{\rm bp2}$	$-\frac{K_{\rm bp}\cdot B\cdot f_{\rm sam}}{2{f_{\rm sam}}^2 + B\cdot f_{\rm sam} + 2{\omega_L}^2}$	-0.012341
$N_{\rm bp3}$	$\frac{4{\omega_L}^2 - 4{f_{\rm sam}}^2}{2{f_{\rm sam}}^2 + B\cdot f_{\rm sam} + 2{\omega_L}^2}$	-1.953
$N_{\rm bp4}$	$\frac{2{f_{\rm sam}}^2 + 2{\omega_L}^2 - B\cdot f_{\rm sam}}{2{f_{\rm sam}}^2 + B\cdot f_{\rm sam} + 2{\omega_L}^2}$	0.97532
$N_{\rm ap1}$	$\frac{K_{\rm ap}(2f_{\rm sam} + z_{\rm ap})}{2f_{\rm sam} + p_{\rm ap}}$	0.646
$N_{\rm ap2}$	$\frac{K_{\rm ap}(z_{\rm ap} - 2f_{\rm sam})}{2f_{\rm sam} + p_{\rm ap}}$	-0.5424
$N_{\rm ap3}$	$\frac{p_{\rm ap} - 2f_{\rm sam}}{2f_{\rm sam} + p_{\rm ap}}$	-0.8776

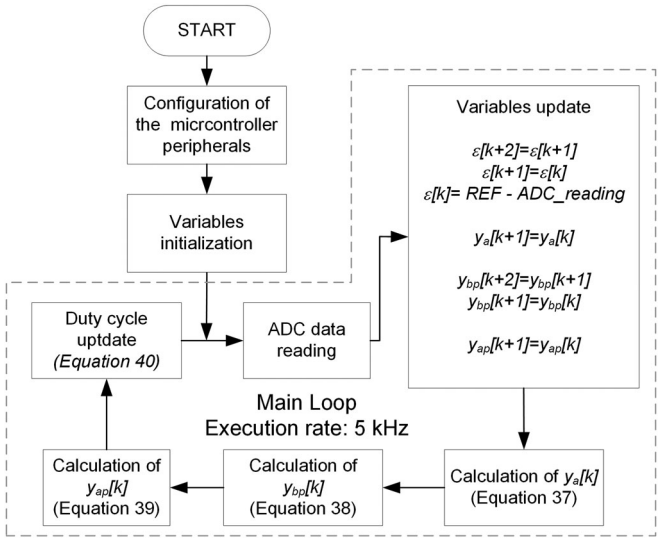


Fig. 7. Flowchart of the control algorithm.

V. EXPERIMENTAL RESULTS

In order to show the actual feasibility of the proposed technique and the validity of the analytical approach outlined, a laboratory prototype was built. The prototype's components values are given in Table IV. Fig. 8 shows a photograph of the laboratory prototype. The LED string has not been included in the photo, but the luminaire employed is composed by a module of LUXEON Rebel LEDs connected in series. Furthermore, all in all, only metalized film capacitors were employed in the power

TABLE IV
PROTOTYPE PARAMETERS

Item	Description	Value
$L_{\mathrm{DM1}}\,L_{\mathrm{DM2}}$	differential-mode inductors of the EMI filter	1 mH
C_{f1}, C_{f2}	capacitors of the EMI filter	33 nF/400 V (polyester film)
L_{CM}	common-mode choke	10 mH
DB	diode bridge	GBU4J
L_1	PFC inductor	$127\ \mu$H (E30 core)
L_2	PC inductor	$204\ \mu$H (E30 core)
C_B	bus capacitor	$40\ \mu\mathrm{F}/450$ V (polypropylene film)
C_{out}	output capacitor	$16\ \mu\mathrm{F}/450$ V (polypropylene film)
Mi	main switch	SPP08N80C3
D_{bb1}	PFC diode	MUR 460
D_{bb2}	PC diode	MUR 460
D_{i}	diode of the integrated stages	MUR 460
U_1	microcontroller	TM4C123G

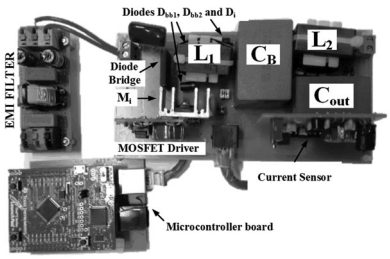
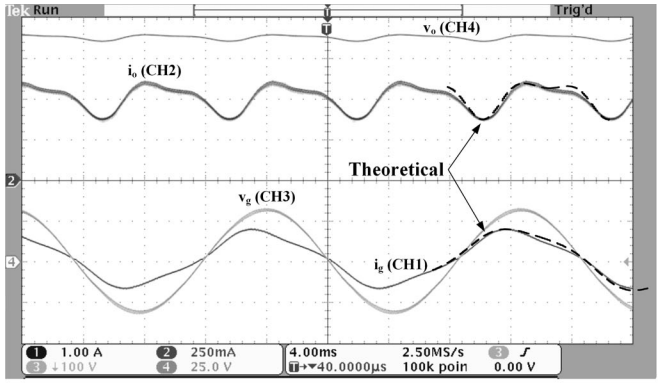
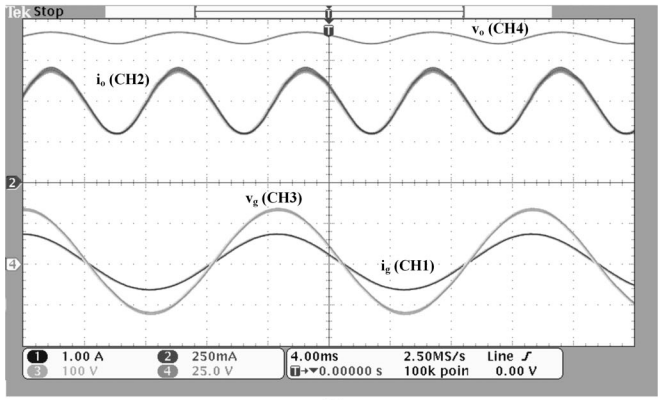


Fig. 8. Top view of the complete prototype, showing both power and digital control circuitry, along with the MOSFET driver and current sensor boards (mounted vertically).



(a)



(b)

Fig. 9. Experimental waveforms obtained with ARCT (a) and without ARTC (b) for an input voltage of 90 V RMS. Input current ($\mathrm{CH1}-1\ \mathrm{A/div}$), output current ($\mathrm{CH2}-250\ \mathrm{mA/div}$), mains voltage ($\mathrm{CH3}-100/\mathrm{div}$), and output voltage ($\mathrm{CH4}-25\ \mathrm{V/div}$). Horiz. Scale: 4 ms/div.

circuitry, thanks to the ARCT ability to reduce the capacitances needed to achieve the desired output ripple level.

As can be seen, the capacitance reduction provided by the ARCT allowed for the use of polypropylene film capacitors, which are commercially available in the required values. However, if the application is cost sensitive, the use of long-life electrolytic capacitors could be suitable, since they are cheaper than film ones. However, even in such applications, the ARCT improves the cost effectiveness of the system by reducing the value of capacitance and consequently the price. Furthermore, the proposed technique also enlarges the reliability of the driver because lower capacitance leads to a higher mean time between failures [29].

Fig. 9(a) shows some selected experimental results for 90-V RMS, which is the worst case in terms of output current ripple. The theoretical behavior, predicted from the analytical analysis of Section II, for the input and the output currents has been sketched in dashed lines, as a reference, on top of the oscillograms. There is only a slight deviation between the theoretical and the experimental waveforms, which could be attributed in part to the simplifications that might have been adopted in part of the mathematical modeling. However, the general behavior is very similar, proving the validity of the presented technique and analysis. In order to compare the proposed control technique with the conventional approach, Fig. 9(b) shows the same experimental results for the converter without the ARCT. The low-frequency ripple in Fig. 9(a) was 44% while in Fig. 9(b) it was 80%. This means that an IDBB converter with the same elements, but without using the ARCT, have an output ripple 36% larger.

Fig. 10 shows the efficiency of the converter according to variations in both the input voltage [see Fig. 10(a)] and the output load [see Fig. 10(b)]. The curve of Fig. 10(a) was obtained for the nominal load and the values of Fig. 10(b) were gathered at the nominal value of the input voltage (i.e., 115 V). These curves show that the efficiency of the converter improves when the input current of the converter is lower, which occur for higher input voltages or light load conditions. This behavior is expected since the integration scheme used to derive the IDBB converter leads to higher current stresses in the main switch [25], increasing the losses in this semiconductor. Furthermore, owing to the chosen bus voltage for this application, the voltage stresses at this input voltage level do not have a major impact on the efficiency as the current stresses do.

Fig. 11 shows the harmonic content of the input current of the converter in two distinct cases: the behavior when the ARCT is used and when no modulation of the duty-cycle is present (i.e., without ARCT). As it can be seen, the input current is in compliance with the IEC-61000-3-2 for both cases, and the

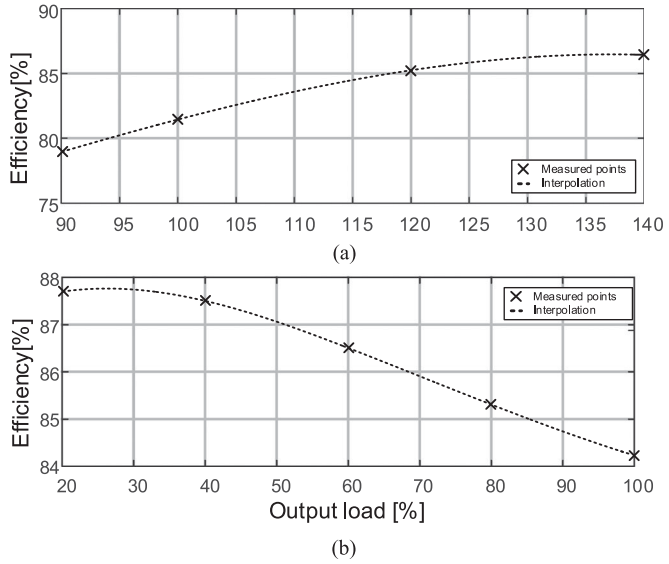


Fig. 10. Efficiency of the converter. (a) Behavior for variations of the input voltage at full load; (b) behavior for variations of the output load with $V_G = 115$ V.

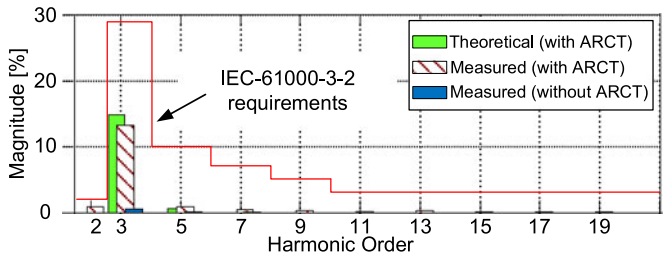


Fig. 11. Harmonic content of the input current compared to the limits imposed by the IEC-61000-3-2 standard (class C equipment).

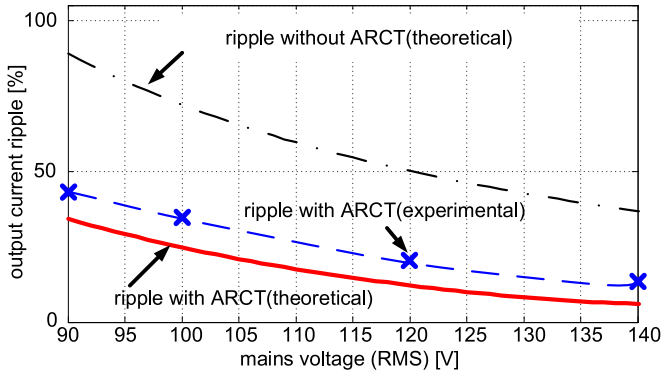


Fig. 12. Behavior of the output current ripple for variations in the mains voltage magnitude.

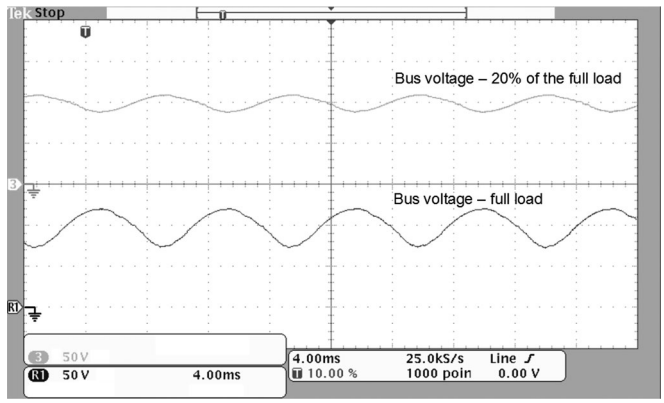


Fig. 13. Behavior of the bus voltage according load variations for an input voltage of 90 V. Bus voltage for 20% of the full load (CH3 − 50 V/div); Bus voltage for full load (R1 − 50 V/div). Time scale: 4 ms.

magnitudes of the harmonic components are also similar to those predicted. Note that the harmonics from 21st to 39th were omitted in this graph since their values were negligible.

Although a lower harmonic content on input current is obtained when the ARCT is not used (classical solution), not modulating the duty-cycle in a controlled manner (as the ARCT does) leads to undesirably high output current ripple, as shown in Fig. 12.

The behavior of the output current ripple for the input voltage range desired (90–140 V, that is, 115 V mains ± 20% variation) is shown in Fig. 12 also for both conditions, with and without the proposed ARCT. The theoretical characteristic of the converter if only the average current compensator (C_{avg}) is present was also plotted along, i.e., when using a conventional control scheme. The results show that the output current ripple is lower when the ARCT is used regardless the input voltage.

By using the theoretical analysis as presented in Section III, if one choses $D_1 = 0$ (no ARCT whatsoever), it is possible to show that a capacitance of c.a.76 μF would be necessary at the bus (C_B) for the conventional system to achieve an output current ripple lower than 50%. This result means that the proposed system provided a reduction of 46.3% in the required filtering capacitance when compared to a conventional system.

The differences between the theoretical prediction and the experimental results occur mainly due to the efficiency of the converter, which varies according to the input voltage (see Fig. 10), whereas it was considered constant in the theoretical analysis (i.e., 85%). Another source of error is the discrete implementation of the band-pass and all-pass filters, which can generate values of D_1 and ϕ_{c1} a little different of those calculated. Nevertheless, the output ripple was kept below the maximum desired level for the whole operating range, which shows the robustness of the proposed system even when considering some typical implementation deminors.

Fig. 13 shows the bus voltage for two load conditions. In order to analyze the ripple behavior, these waveforms were obtained for the lowest value of the input voltage (see 90 V), for which the higher ripple should be expected. In Fig. 13, both conditions were compiled in a single picture by using a memory function of the oscilloscope. As can be seen, the average value of the bus voltage was similar in both cases (about 98 V), which is in compliance with (28). The figure also shows that the low-frequency ripple of the bus voltage dramatically reduces with light loads.

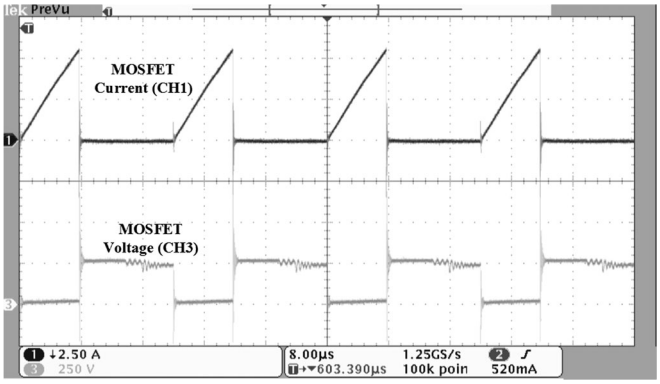


Fig. 14. Current (CH1, 2.5 A/div) and voltage (CH3, 250 V/div) measured at the MOSFET in the peak of the rectified voltage.

Finally, Fig. 14 shows current and voltage waveforms of the main switch M_i, showing full DCM operation since the MOSFET current ramps up from zero. This is because the current through M_i is the sum of the currents through both inductors during the on-time, and can only be observed once both stages are in DCM.

VI. Conclusion

This study has devised a technique to design DCM integrated offline LED drivers allowing further reduction in the filtering capacitances so that not only the reliability but also the power density of the driver can be increased. The presented concept is based on a novel ARCT, in which a single-loop, VMC, converter is subjected to a controlled low-frequency large-signal modulation of the duty-cycle. The resulting output current ripple can then be reduced, at the cost of increasing the input current harmonic distortion, but in a predictable and controlled manner.

A parametric duty-cycle function was proposed, whose characteristic allowed for the change of the conventional low-frequency behavior of the converter. The mathematical analysis showed that by using the proposed modulation scheme it is possible to reduce the required filtering capacitances of the integrated LED driver while still maintaining the harmonic content of the input current in compliance with the IEC-61000-3-2.

Since there is no parallel with classical VMC control, a novel control loop scheme has been proposed for the converter and its implementation aspects were addressed.

An experimental evaluation was carried out and it has been demonstrated the accuracy of the theoretical analysis here outlined. It was shown that the ripple in the output current has been reduced by an amount of 36% when compared with a conventional control strategy. Furthermore, the experimental results showed that the harmonic content of the converter employing the ARCT was indeed in compliance with the IEC-61000-3-2, even though distorted input current results in a reduced output current ripple.

In this particular implementation, the proposed technique allowed for a 46.3% reduction in the required filtering capacitance when compared to a conventional system.

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