Accurate SPICE Modeling of Reverse-Conducting IGBTs Including Self-Heating Effects

Michele Riccio, Giuseppe De Falco, Paolo Mirone, Luca Maresca, Marianna Tedesco, Giovanni Breglio, and Andrea Irace, *Senior Member, IEEE*

***Abstract*—In this paper, a temperature-dependent compact SPICE model of reverse-conducting IGBTs (RC-IGBTs) is presented. The proposed solution is based on a quasi-two-dimensional (2-D) approach, with the use of IGBT and p-i-n diode subcircuits suitably connected to take into account the inner interactions among the two devices. The resulting device model is derived through physical considerations on the RC-IGBT internal behavior, carried out by means of wide area TCAD 2-D simulations. Transversal current path, localized lifetime control effects, and turn-on dynamics are also included into the model. The model shows good robustness properties, even in demanding numerical conditions. Validation of the SPICE model with experiments performed on a 1.2-kV 30-A commercial device, in both static and dynamic conditions, demonstrates its remarkable correctness and accuracy. To further confirm the applicability of the proposed model in real-operating conditions, a quasi-resonant converter has been realized and the measurements on the realized circuit have been successfully compared with the results obtained with the proposed model.**

***Index Terms*—Electro-thermal, quasi-resonant converter, reverse-conducting (RC) insulated gate bipolar transistor (IGBT), SPICE model.**

I. Introduction

TODAY reverse-conducting IGBTs (RC-IGBTs) represent an interesting solution to increase power density in IGBT modules, to reduce packaging dimensions, bonding, and silicon costs in fabrication. As a matter of fact, the design on the same chip of the IGBT with a monolithically integrated body diode requires less area for a given power rating. In addition, the temperature swings of the chip are considerably reduced leading to improved reliability of power modules. Nevertheless, due to difficulty to optimize the same silicon for both IGBT's and diode's conduction modes, a large recovery current and switching losses are responsible of reverse conductive RC-IGBT devices limitation to low-voltage soft-switching applications. In the last years, many papers have described the theory and design of RC-IGBT [1]–[3] with particular focus on the initial snapback phenomenon and secondary multiple snapbacks formation [4]. Different strategies and device layouts were successfully proposed to reduce these problems [5]–[7]. Recently, a new device based on innovative design, the bi-mode insulated gate transistor [8], has brought a significant improvement in the electrical behavior in both soft and hard-switching conditions, ensuring an increased diffusion in the applications [9]. Consequently, to this recent trend, a useful and robust compact model for circuit simulators becomes very attractive from the application point of view. However, at present time, a SPICE model for RC-IGBT is not present neither in PSPICE nor in other SPICE simulator. Therefore, the only solution consists to simulate an IGBT with antiparallel diode, neglecting their internal interaction. In this work, we introduce, for the first time, a compact SPICE model for the RC-IGBT including the lateral interaction between the IGBT and the diode regions taking also into account self-heating effects. The proposed model also includes the primary snapback phenomenon and lateral turn-on dynamic that characterizes the device. The modeling strategy has been chosen to maximize the accuracy and yet to have robust convergence properties. The paper is organized as follows: in Section II, an in-depth analysis of the RC-IGBT physical behavior along with Technology Computer Aided Design, better known as Technology CAD (TCAD) 2-D simulation are used to properly model the device with a compact circuital approach. In Section III, the results of model calibration on a commercial device are given together with a validation in an electro-thermal application.

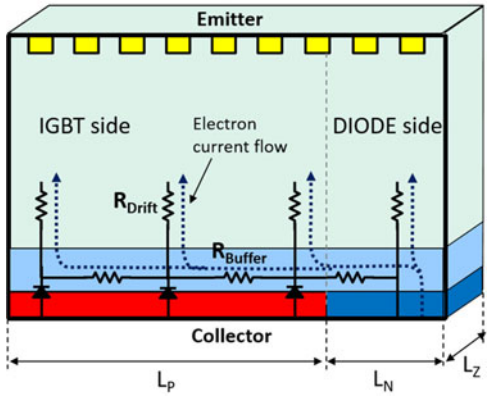

Fig. 1. Simplified internal structure for an RC-IGBT, with electron current path on a resistive distributed network.

II. Model Description

The schematic structure of a basic RC-IGBT is shown in Fig. 1. A resistive network, responsible of the initial snapback phenomenon [10], is also depicted together with the corresponding electron current path. Due to the intrinsic two-dimensional

Manuscript received March 8, 2016; revised April 27, 2016; accepted May 30, 2016. Date of publication June 8, 2016; date of current version January 20, 2017. Recommended for publication by Associate Editor J. Rabkowski.

The authors are with the Department of Electrical Engineering and Information Technologies, University of Naples Federico II, Naples 80125, Italy (e-mail: michele.riccio@unina.it; g.defalco@unina.it; paolo.mirone@unina.it; luca.maresca@unina.it; marian.tedesco@studenti.unina.it; breglio@unina.it; a.irace@unina.it).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org

Digital Object Identifier 10.1109/TPEL.2016.2578363

(2-D) device structure, the electrical behavior could not be modeled with a mathematical one-dimensional approach. In particular, the flowing of lateral currents between the IGBT and the diode regions should not be neglected to obtain a correct model. However, the main drawback of 2-D mathematical formulation for a SPICE model is the complexity growth in the compact device description affecting the convergence properties and simulation speed. Therefore, the approach proposed in this paper is based on a quasi-2-D model, derived from a coupling of properly modified IGBT and diode models.

The structure of the developed SPICE model is depicted in Fig. 1(a). A subcircuit consisting of nonlinear-controlled current and voltage sources and standard SPICE elements (MOSFET, diode, etc.) is realized. The voltages of the input thermal nodes correspond to the temperature increase for the IGBT and diode sides due to self-heating effects [11]. All the physical quantities used into the model are temperature dependent.

The RC-IGBT SPICE model was developed taking into account the lateral interaction between the IGBT and the diode subcircuits by means of additional output nodes. An improved version of the Kraus model [12], [13] was used for the IGBT side [14]. Further enhancements were introduced to better describe Field-Stop (FS) Trench devices, improving both calculation speed and convergence properties. The diode part was described with an electro-thermal version of the Strollo model [15], [16], accounting for an effective carrier lifetime as a function of the device structure and carrier lifetime optimization technique. For reader convenience, in the following we will refer to the intrinsic IGBT terminals as *collector*, *emitter,* and *gate*; while for the diode, *anode* and *cathode* will be used. It is implied that the anode terminal coincides with the emitter and the cathode with the collector. In principle, the strategy used to model the RC-IGBT can be extended using any kind of SPICE models for IGBT and diode regions. The only assumption is the possibility to access to internal nodes and modify properly the equation used to evaluate the IGBT current, as will be explained in this section. As visible in the schematic of Fig. 2(a), the IGBT and the diode subcircuit models were connected using their internal nodes to reproduce the physics structure of an RC-IGBT. Referring to a structure with a buffer-layer at the collector side, i.e., Punch-Through (PT), Soft-PT (SPT), FS, a resistor R_{BUF} can be used to describe a lateral electron current flow [10]. The resistor value can be approximated as [17]

$$R_{\mathrm{BUF}}\left(T\right)=\frac{L_P\left(L_P+L_N\right)}{\mu_n qN_B AW_B}\left(\frac{T}{T_0}\right)^{1.5} \tag{1}$$

where the factor $A/(\mathrm{L_P}+\mathrm{L_N})$ is used to evaluate the dimension L_Z. A further connection is present between nodes *D* and *J*, where a nonlinear resistor R_{MOD} takes into account a transversal current path into the epi-layer. A function of the base charge Q_{B} is used to evaluate this resistor [18]. The longest transversal current path $(\mathrm{L_P})$ has been assumed in order to take into account the worst-case condition, as indicated in the following equation:

$$R_{\mathrm{MOD}}=\frac{L_P^2}{\mu_n Q_n+\left(\mu_n+\mu_p\right)Q_B} \tag{2}$$

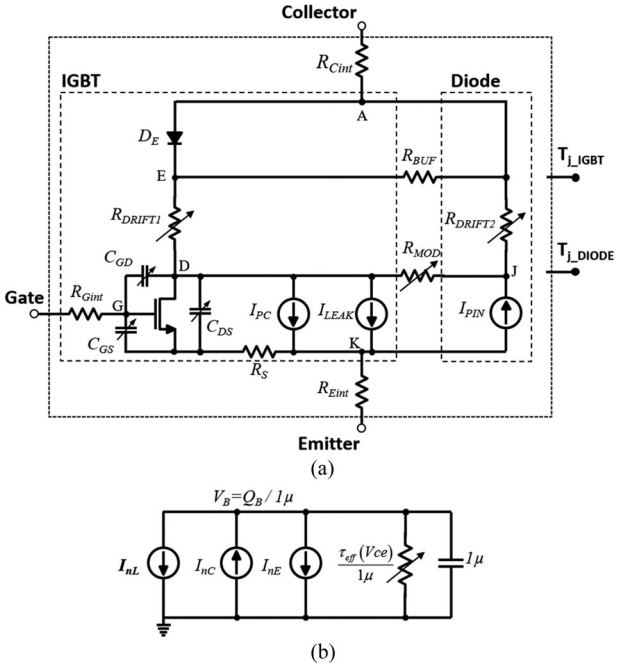

Fig. 2. (a) Developed SPICE subcircuit, with electrical and thermal nodes. (b) Charge-stored subcircuit for IGBT side, modified to take into account lateral current path from the diode side.

being $Q_n=qAN_BW$ the background mobile carriers base charge. Its temperature dependence is implicit through the carrier mobility and Q_B.

A. IGBT Model

The IGBT is described with an enhanced version of the model presented in [14], in which the use of explicitly evaluated solution for steady-state carriers charge Q_{b0}, linear-region transconductance gain factor K_F, and avalanche multiplication factor M_{AV} were introduced. In this work, the use of a linear-region transconductance gain factor K_F [19] was optimized in order to avoid the discontinuity that occurs at the transition between the MOSFET linear and saturation regions. This guarantees a better modeling of the transition region, improving at the same time the model convergence. To this purpose, a smoothing function was defined as follows:

$$K_{\mathrm{Feff}}\left(V_{\mathrm{gs}},V_{\mathrm{ds}}\right)=\frac{1}{2}\{\left(K_F-1\right)\tanh\left[\alpha_{\mathrm{KF}}\left(V_{\mathrm{gs}}-V_{\mathrm{th}}-V_{\mathrm{ds}}\right)\right]+K_F+1\} \tag{3}$$

where α_{KF} is a fitting parameter that defines the transition region extension.K_{Feff} is equal to K_{F} in linear region and gradually approaches unity into the saturation region. The equation for the MOSFET current in linear region becomes the following:

$$I_{\mathrm{MOS}}=\frac{K_{F\mathrm{eff}}K_p\left[\left(V_{\mathrm{gs}}-V_{\mathrm{th}}\right)V_{\mathrm{ds}}-\frac{K_{F\mathrm{eff}}V_{\mathrm{ds}}^2}{2}\right]}{2\left[1+\vartheta_1\left(V_{\mathrm{gs}}-V_{\mathrm{th}}\right)\right]\left(1+\vartheta_2V_{\mathrm{ds}}\right)} \tag{4}$$

In this case, the new boundary condition between the linear and saturation region is defined with the relation shown

$$K_{F\mathrm{eff}}V_{\mathrm{ds}}\le V_{\mathrm{gs}}-V_{\mathrm{th}} \tag{5}$$

With this approach the reduced overall on-resistance of the device, due to the p-i-n injection effect in conduction mode [13], can be accounted in an effective way increasing the electron current I_{nC}.

A further improvement to the modeling of the IGBT bipolar part involves the introduction of an effective carrier lifetime ($\tau_{\rm eff}$) that is function of the high-level injection lifetime in the drift region (τ_{HL}) and low-level injection lifetime in the buffer layer ($\tau_{\rm BF}$). The IGBT tail current evolution during the turn-off phase is determined by recombination in the low-doped epi-layer, recombination in the high-doped buffer layer, and by injection of electrons into the collector. This means that $\tau_{\rm eff}$ depends on how wide is the depletion region and, as a consequence, on the external voltage [20], [21]. The current tail decay rate at different clamping voltage can be used to extract the parameters τ_{HL} and τ_{BF}. To fit the dependence of $\tau_{\rm eff}$ from the collector–emitter voltage, the following empirical expression was introduced:

$$\tau_{\rm eff}\left(T, V_{\rm ce}\right) = \left[\left(\tau_{\rm HL} - \tau_{\rm BF}\right)\exp\left(-\delta_\tau V_{\rm ce}\right) + \tau_{\rm BF}\right]\left(T/T_0\right)^{\beta_\tau} \tag{6}$$

where δ_τ is the decay rate of the effective carrier lifetime, while the temperature dependence is accounted with a power law through the model parameter β_τ. In terms of device capacitances, in addition to the C_{gd}, other two voltage-dependent capacitances were added to the IGBT model: $C_{\rm gs}$ and $C_{\rm ds}$. A constant gate–source capacitance was found to be a good approximation if the gate–source voltage is not driven negatively. On the other hand, when a negative V_{ge} is applied, the capacitance value increases to its maximum value equal to C_{OX} [23]. Since in most current applications the gate–driver circuit makes use of a negative voltage to turn-off the device [24], $C_{\rm gs}$ was modeled with a novel expression suited to fit the high-frequency MOS capacitance behavior, shown

$$C_{\rm GS}\left(V_{\rm GS}\right) = \frac{1}{2}\left[\left(C_{\rm GSP} - C_{\rm GSN}\right)\tanh\left(\frac{V_{\rm gs} - V_{\rm th}/2}{V_{\rm gs}^*}\right) + C_{\rm GSP} + C_{\rm GSN}\right] \tag{7}$$

The parameters $C_{\rm GSP}$ and C_{GSN} are the corresponding values for positive and negative gate–emitter voltage, while $V_{\rm gs}^*$ is a fitting parameter. The voltage-dependent behavior of the $C_{\rm ds}$ capacitance reported in [25] was modeled introducing the following formula for $V_{\rm ds} > 0$, and it is kept constant for negative $V_{\rm ds}$

$$C_{\rm DS}\left(V_{\rm ds}\right) = \frac{C_{\rm DS0}\left[\frac{\pi}{2} + \arctan\left(-\frac{V_{\rm ds}}{V_{\rm ds}^*}\right)\right]}{\pi/2} \tag{8}$$

In this expression, $C_{\rm DS0}$ is the maximum $C_{\rm ds}$ value and $V_{\rm ds}^*$ is a fitting parameter.

The solutions that have been adopted so far in this section aim to a better description of the device IGBT-part behavior. In the following, the solutions referred to the RC-IGBT are considered. The significant difference between a common IGBT and RC-IGBT is that the latter device behaves as a Power MOSFET for low currents until the initially reverse-biased $P^+_{\rm collector}/N^+_{\rm buffer}$ junction is turned ON when the voltage drop produced by the electron current reaches a sufficient value. This behavior is experimentally evident on the *I–V* static characteristic that shows a snapback on the collector voltage. However, also if the design of the device guarantees the absence of the snapback phenomenon, the presence of the MOSFET parallel path influences the dynamic turn-on performances. With particular reference to the case of zero-voltage switching (ZVS) operation, when an RC-IGBT turns ON, the forward recovery phenomenon that commonly takes place in the IGBT is enhanced due to the alternative current path, therefore, producing an initial larger voltage overshoot. To get a better insight, the turn-on behavior is investigated by means of 2-D multicellular TCAD simulations for an RC-IGBT structure and for an IGBT structure in order to compare the behavior of two devices. Then, the results are used to properly modify the IGBT SPICE model, accounting these additional phenomena. The RC-IGBT structure was designed with reference values reported in literature and listed in Table I. The IGBT structure was designed with same features of the RC-IGBT without the diode part. The area factors have been taken into account in order to have the same current density. Simulations were performed for the analysis of turn-on behavior, by means of mixed-mode approach in Synopsis Sentaurus device simulator. Fig. 3(a) reports the collector–emitter voltage and the hole current at the collector side either for the RC-IGBT and for the IGBT. In both cases, the collector voltage presents the characteristic forward recovery spike. As has been already discussed in [26], this effect depends on the finite time that is needed for the onset of conductivity modulation in the epitaxial layer. The time needed for the voltage to reach the peak value is the same for the two devices as it only depends on the rate of rise of external current [27]. In the RC-IGBT, however, the voltage spike is more evident because the electron current that contributes to increase the charge concentration in the epitaxial layer is lower than in the IGBT, as a significant part flows initially in the MOSFET region. As a confirmation, the hole current measured at the collector contact is lower for the RC-IGBT due to the lower conductivity modulation. Fig. 3(b) reports the carriers' densities along a horizontal cutline, taken at five time instants of the analyzed turn-on transient, and normalized to the total current density. At the beginning of the turn-on (100 ns), the overall current is produced only by electron flow as the

TABLE I
STRUCTURE PARAMETERS FOR THE RC-IGBT TCAD SIMULATION

Symbol	Quantity	Value
L	Total length	400 μm
L_P	IGBT length	345 μm
L_N	Diode length	55 μm
W	Epi-layer thickness	100 μm
W_B	Buffer thickness	1.5 μm
$N_{\rm epi}$	Epi-layer doping concentration	1×10^{14} cm^{-3}
N_B	Buffer doping concentration	5×10^{16} cm^{-3}
p_i	Cell pitch	5 μm
W_P	Anode P-well depth	4 μm
N_P	Anode P-well concentration	1.5×10^{17} cm^{-3}
$t_{\rm ox}$	Oxide thickness	181 nm
t_d	Trench depth	7.56 μm

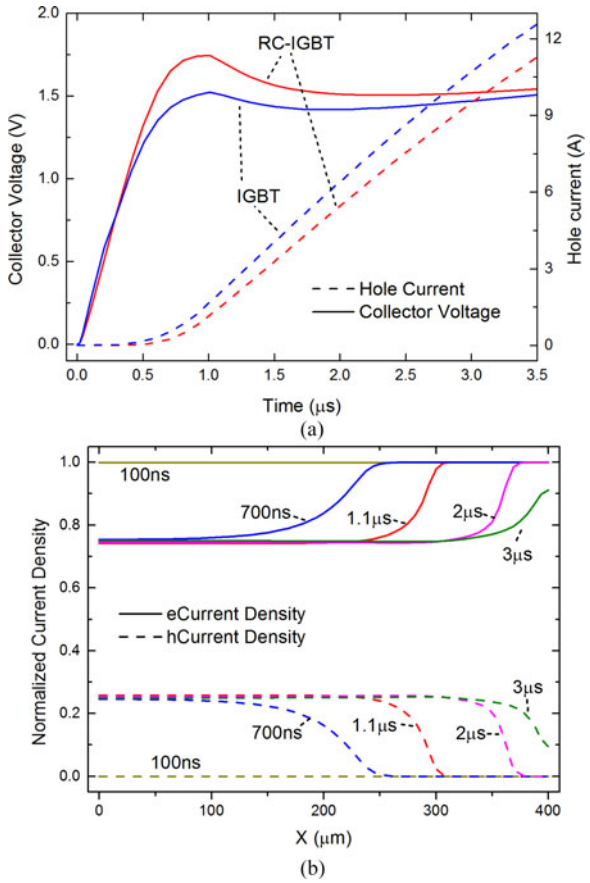

Fig. 3. (a) Simulated collector–emitter voltage and collector hole current during ZVS turn-on for both RC-IGBT and IGBT. (b) Normalized electron and hole current density of the RC-IGBT during ZVS turn-on transient.

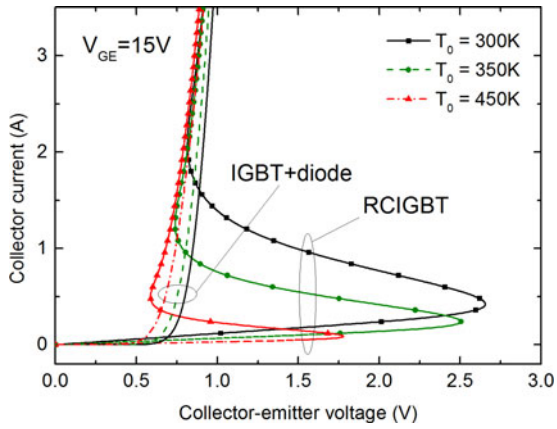

Fig. 4. Forward output characteristics from RC-IGBT model (lines + scatter) and parallel of IGBT and diode (lines) function of junction temperature.

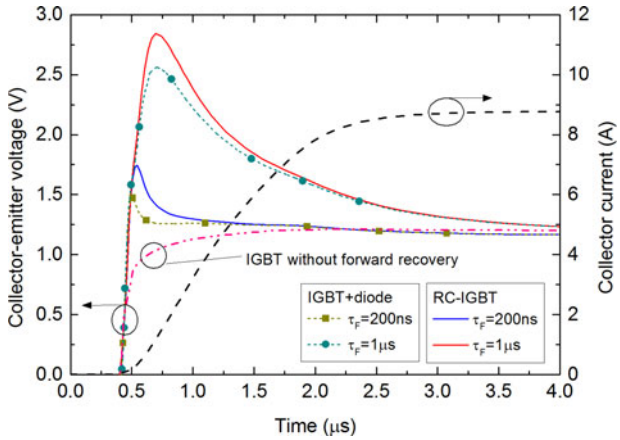

Fig. 5. SPICE simulations of inductive turn-on for both an RC-IGBT and IGBT: collector voltage and current waveforms.

$P^{+}_{\text{collector}}/N^{+}_{\text{buffer}}/N^{-}_{\text{epi}}$ junction is not forward biased yet. At 700 ns, the hole current density is the indication that the conductivity modulation has taken place only in half of the structure, where potential is sufficient to trigger the injection of holes in the epitaxial layer. Therefore, at this time, only half of the device shows a low resistivity but the electron current flow in the unmodulated part is still significant and so is the voltage drop. For larger times, the conductivity modulation spreads along the overall device and the voltage drop reduces and approaches that of the IGBT. These results have shown that, in order to replicate the correct behavior of the RC-IGBT, additional modifications must be included in the original base charge subcircuit [12]. To describe the snapback phenomenon, referring to the circuit in Fig. 2(a), the initial electron current, flowing into R_{BUF} and in the MOSFET (I_{nC}), should not contribute to the collected hole current (I_{pC}), and to the modulation of R_{DRIFT1} through the base-charge Q_B. To take into account this effect, an additional current generator, I_{nL}, was added to the base-charge subcircuit as showed in the schematic of Fig. 2(b)

$$I_{\text{nL}} = I_{\text{RBUF}} + I_{\text{RMOD}} \tag{9}$$

The static forward output characteristic of the RC-IGBT SPICE model is reported for different operative temperatures in Fig. 4. The model parameters were set to standard reference values, while the R_{BUF} resistance has been chosen in order to have a nonsnapback-free device. As expected, the snapback voltage reduces with temperature, as well as the snapback current [1]. In the same picture, the results obtained with a standard approach with IGBT and antiparallel diode, have been also depicted. In this case, the snapback phenomenon is not modeled, and also the device behavior at low current differs due to the absence of the additional electron current path.

The second modification in the model is needed to take into account the forward recovery behavior. For this reason, the voltage drop V_{epi} on the conductivity-modulated *epi-layer* region of the IGBT should not depend instantaneously on the base-charge Q_B [28]. In the proposed model, the nonlinear resistors R_{EPI1} and R_{MOD} are functions of a quantity Q_{Bd} computed according to the following equation:

$$\tau_F \frac{dQ_{\text{Bd}}}{dt} + Q_{\text{Bd}} = Q_B \tag{10}$$

In this way, the turn-on dynamic is modeled with the two resistors, through the instantaneous time-dependent charge in the base (Q_{bd}) and the time constant τ_F. This allows a good

modeling of the RC-IGBT turn-on in ZVS application, where conductivity modulation does not take place immediately in the drift region, resulting in sensible turn-on losses [29]. Fig. 5 shows the results of SPICE simulations during inductive turn-on transients for both RC-IGBT and IGBT with antiparallel diode. The model parameters were set to standard reference values to obtain a snapback-free device. As expected, it can be observed that increasing the τ_F parameter the forward peak voltage increases with a higher value in the case of RC-IGBT. In the same picture, it is also shown the voltage curve obtained with the standard IGBT Kraus model in which the forward recovery phenomenon is not modeled.

B. Diode Model

The diode electric model used for the RC-IGBT is based on the moment-matching approximation of the ambipolar diffusion equation and follows the implementation proposed in [30].

However, in our case the model is improved and provided of four terminals: *anode*, *cathode*, an internal node (into the *epi-layer*, after the p^+n^- junction), and temperature increase. The main improvement to this model involves the carrier lifetime parameter into the *epi-layer*. Several SPICE models have been proposed in literature for silicon power diodes [31]. All of them make use of a constant parameter for the carrier lifetime in the low-doped *n* region. In [32], a solution based on the equivalent lossy transmission lines was introduced, which describes the transport of the injected minority carrier through the quasi-neutral drift region.

Despite a more accurate device description, the higher number of model parameters and the mandatory knowledge of design details (dimensions, doping profiles, etc.) impose a severe limitation to the purely physical modeling of new generation power diodes. Nowadays, the main targets of power diode design consist in achieving low-power losses, soft recovery characteristics, and high reverse recovery safe operating area. To this extent, the local lifetime-control technique is widely used to obtain improved performance p-i-n diodes [33]. In [34], the on state electron–hole distribution is controlled with a double He^{++} irradiation on both the anode and cathode sides, without additional homogenous lifetime control in the n^--base. The cathode-sided He^{++} peak is used to control the tradeoff between diode losses and softness. It is also possible to relax the tight restrictions imposed by the softness requirement, introducing Field Charge Extraction diode concept [35] based on the presence of P^+ islands on the cathode side. Specifically, at the end of the reverse recovery phase, the P^+ islands start to emit holes, which support the reverse recovery current and prevent a snappy behavior. This last mechanism is particularly present in RC devices, where the hole injection is provided by the p^+ *collector*--n^+ *buffer* junction. This allows a further reduction of the excess carrier concentration on the cathode side, ensuring a faster reverse recovery phase [36]. To embed this behavior in the diode SPICE model, our approach consists to define an effective carrier lifetime function. During the turn-off transient, as the voltage across the diode begins to increase, the depletion region starts to form. Then, the reverse recovery tail current occurs sweeping out the remaining excess carriers from the drift region. We introduce a τ_{eff} function of the V_{ak} voltage

$$\tau_{\text{eff}}\left(V_{ak}\right) = \frac{1}{2}\left[\left(\tau_{HL}-\tau_{LO}\right)\tanh\left(V_{ak}/V_{\tau}^{*}+\pi\right) + \tau_{HL}+\tau_{LO}\right] \tag{11}$$

In this way, when the diode operates in forward condition, the model experience a carrier lifetime equal to τ_{HL}, an integral value of the high-injection level carrier lifetime in the *epi-layer*. During the inductive phase and reverse recovery phase [36], when the depletion region increases ($V_{ak} \ll 0$), the carrier extraction mechanism becomes faster with τ_{eff} approaching a lower value τ_{LO}. The parameter V_{τ}^{*} is used to fit the change rate of τ_{eff}. Fig. 6 shows the effect of τ_{eff} model on the current waveforms derived from SPICE simulation during a diode turn-off for different τ_{LO} values. As can be observed, the reverse current peak does not changes, while the current dynamic when the negative voltage increases can be modeled using the two parameters τ_{LO} and V_{τ}^{*}.

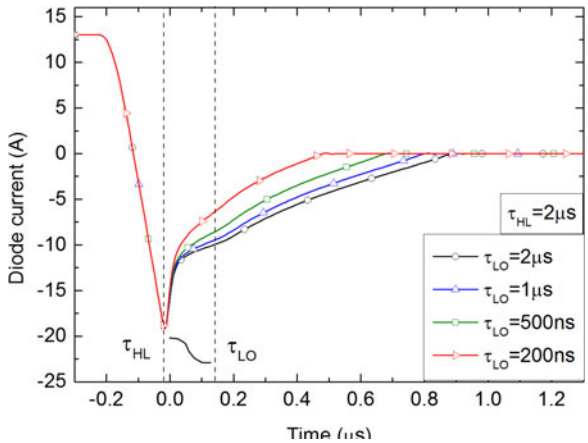

Fig. 6. SPICE simulations of diode inductive turn-off for different τ_{LO} values: current waveforms.

III. Results

The complete RC-IGBT model consists of a SPICE netlist which defines a subcircuit. It is provided of seven interface nodes, namely *Anode*, *Gate*, *Cathode*, $T_{\text{IGBT}}, T_{\text{DIODE}}$ (IGBT, diode temperatures), $P_{\text{IGBT}}, P_{\text{DIODE}}$ (IGBT, diode dissipated electrical power). The diode part of the netlist is the same as reported in [15, Appendix B], with the addition of the function related to the effective carrier lifetime and temperature dependence of the physical parameters. The core of the IGBT netlist is obtained from schematic and analytical expressions reported in [13]. All the improvements described in the previous section have been added to this netlist by means of SPICE behavioral functions. Also in this case, all the physical parameters have been defined as nonlinear function of the junction temperature. Finally, the RC-IGBT netlist is obtained following the connection depicted in Fig. 2. The final model was validated with measurements on different RC-IGBTs that are currently available in the market. As an example, the results obtained with a

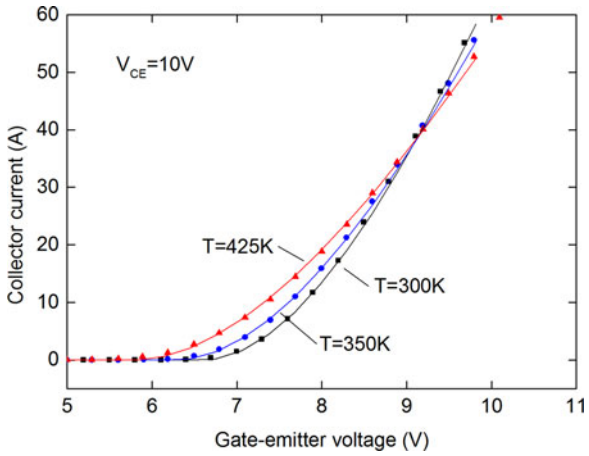

Fig. 7. Transfer characteristics at different temperatures from SPICE simulations (solid lines) and measurements (symbols), $V_{\rm CE}= 10{\rm V}$.

device from the third generation of RC-IGBT manufactured by Infineon Technologies are presented. It is a 30-A 1.2-kV-rated device (IHW30N120R3 [37]) designed for resonant converters and soft-switching applications. It was characterized in both static and dynamic conditions, for different operating temperatures. To avoid the self-heating effect during the dc characterization an in-house developed current pulse circuit was used. The pulse width was set to 80 μs with a repetition time of 1 s, while the backside temperature was controlled by a temperature controller. The developed SPICE model was calibrated on experimental data using a two-step calibration procedure. At first stage, the IGBT and the diode subcircuits were fitted separately to experimental data. For the IGBT, a procedure presented in [21] was used for the main model parameters. The effective lifetime carrier $\tau_{\rm eff}$ was calibrated using the current tail decay rate at different clamping voltage (i.e., from 10 V to 2/3 $V_{\rm Breakdown}$). In particular, the parameters τ_{HL} was extracted at low-clamping voltage, while τ_{BF} is evaluated at high-clamping voltage. For both values, the analytical approach reported in [21] is used. Finally, the decay rate δ_τ is evaluated to best-fit the $\tau_{\rm eff}$ voltage behavior. Additional parameters were obtained with an automatic multivariable optimization routine implementing an iterative feedback with the PSPICE simulator [22]. The $C_{\rm gs}$ capacitance was fitted minimizing the distance between experimental and SPICE waveforms of the V_{ge} during inductive turn-on and turn-off transients, using a bipolar gate driver circuit (±15 V). Similarly, the $C_{\rm ds}$ capacitance was fitted on the V_{ce} curve during the IGBT inductive turn-off. The diode subcircuit was calibrated using the same approach described in [16] and [38]. The new introduced parameters, used for $\tau_{\rm eff}$, were obtained using experimental forward *I–V* curve and the reverse recovery waveforms at different switching voltage. The τ_{HL} is used to fit the *I–V* forward curve as indicated in [16], while $\tau_{\rm LO}$ *and* V_τ were evaluated to best-fit the reverse recovery time for high supply voltage (i.e., $2/3V_{\rm Breakdown}$).

Due to the lateral interaction between the IGBT and the diode, the second step consists to optimize the full RC-IGBT model by means of a best-fitting procedure on the dc curves, starting from the parameters obtained at the first step. In particular,

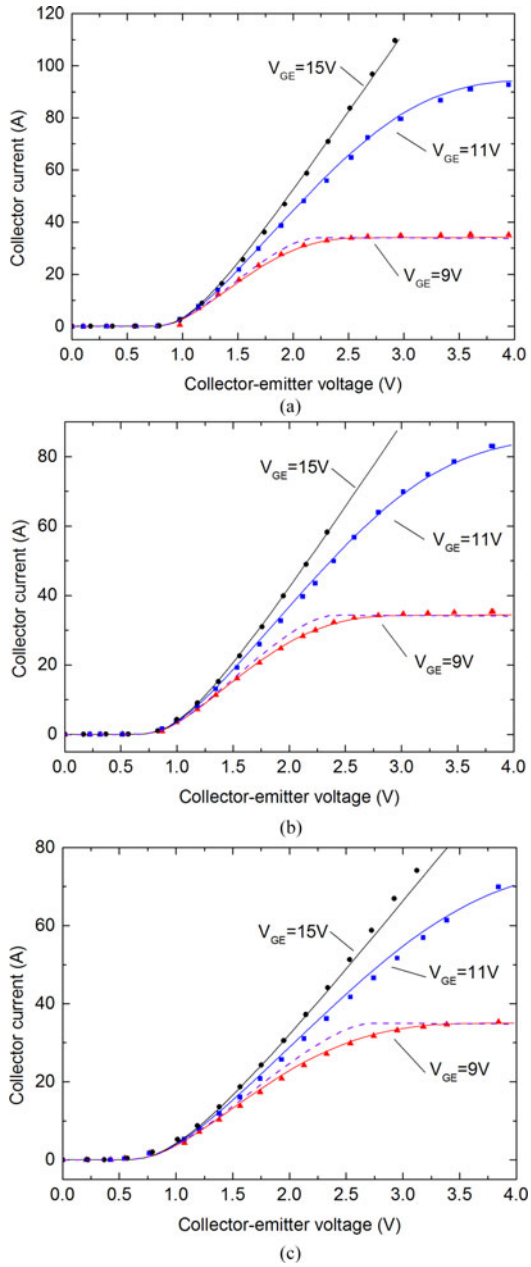

Fig. 8. Output characteristics at different temperature: (a) $T_0= 300{\rm K}$, (b) $T_0= 350{\rm K}$, (c) $T_0= 425{\rm K}$. Solidlines SPICE model; scattered lines experiments; dashed lines SPICE model without $K_{\rm F\,eff}$ smoothing function for $V_{\rm GE}= 9{\rm V}$.

in the second step are involved only a subset of parameters affecting the on-voltage for IGBT $({\rm K_{eff}},{\rm I_{se}},{\rm R_{drift}},\tau_{\rm HL})$ and diode $({\rm I_s},{\rm R_{drift}},{\rm N},\tau_{\rm HL})$. The $R_{\rm BUF}$ and $R_{\rm MOD}$ resistances are evaluated with the (1) and (2), respectively. The resulting values are optimized comparing experimental and numerical static $I_C-{\rm V_{CE}}$ characteristics at low current. Finally, the τ_F parameter is obtained fitting the V_{ce} waveform during an inductive IGBT turn-on transient. The first step of the calibration procedure, which involves the separated calibration of the IGBT and diode subcircuit, is then repeated for a different operating temperature (i.e., 400 K). Afterwards, the unknown temperature coefficients are extracted, enabling calibrated electro-thermal simulations.

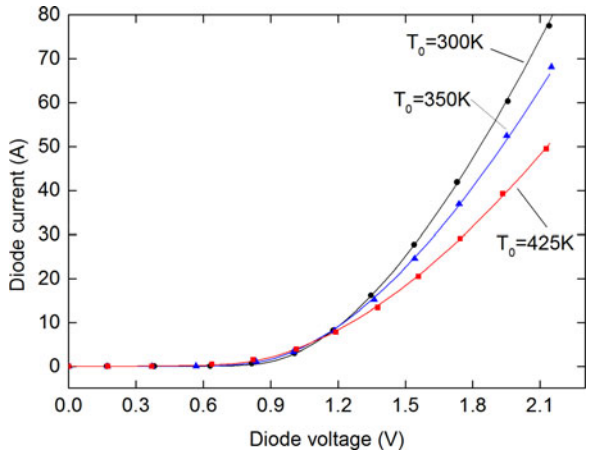

Fig. 9. Forward diode static curves depending on the junction temperature: solid lines SPICE model, scattered lines experiments.

A. Comparison of Model Simulation and Measurement

Fig. 7 shows the experimental and simulated transfer characteristics for different backside temperatures. The temperature compensation point on the $I_C - \mathrm{V_{GE}}$ curves occurs for $V_{\mathrm{GE}} \approx 9.15$ V as correctly predicted by the model. Fig. 8 reports the output characteristics at room temperature, 350 and 425 K, respectively. It can be seen the excellent agreement between SPICE model curves and experimental data. As an example $I_C - \mathrm{V_{CE}}$ curves for $V_{GE} = 9\mathrm{V}$ are also reported disabling the K_{Feff} function, clarifying the relevance of the proposed model for the transition between the linear and saturation region of the MOSFET. In Fig. 9, the SPICE forward diode *I–V* curves are compared with measurements, for different junction temperatures. The results confirm that the model can correctly predict the diode electrical dc behavior. The switching behavior was investigated with a typical double-pulse test circuit. A high-side device acts as a freewheeling diode, with gate and cathode terminals shorted. The test voltage was set to $\mathrm{V_{BATT}} = 500\mathrm{V}$, and a load inductance $\mathrm{L_{LOAD}} = 2$ mH was used. The stray inductance L_σ was estimated to be 300 nH. In the simulated circuit, all the parasitic elements of the devices package and the connections between the components are fitted to the experimental waveforms. Fig. 10(a) and (b) report experimental and numerical electrical waveforms resulting from a double-pulse test operated at ambient temperature. Also in this case, the proposed RC-IGBT model exhibits an excellent agreement with measurements in terms of IGBT tail current and diode reverse peak current. To perform a comparison with a standard model (i.e., nonRCIGBT) the PSPICE *Z-BreakN* and *D-Break* models [39] were fitted on the device under test (DUT) measured curves (for both forward and reverse conduction mode).

Despite nearly sufficient results from the dc calibration, the dynamic behavior gives not acceptable results. In particular, the *Z-BreakN* standard model is not appropriate to describe PT/SPT and FS IGBT neither trench structure. This implies wide oscillations on current and voltage waveforms at turn-off, avoiding correct evaluation of tail current and peak voltage overshoot. On the other hand, the *D-Break* model does not take into account

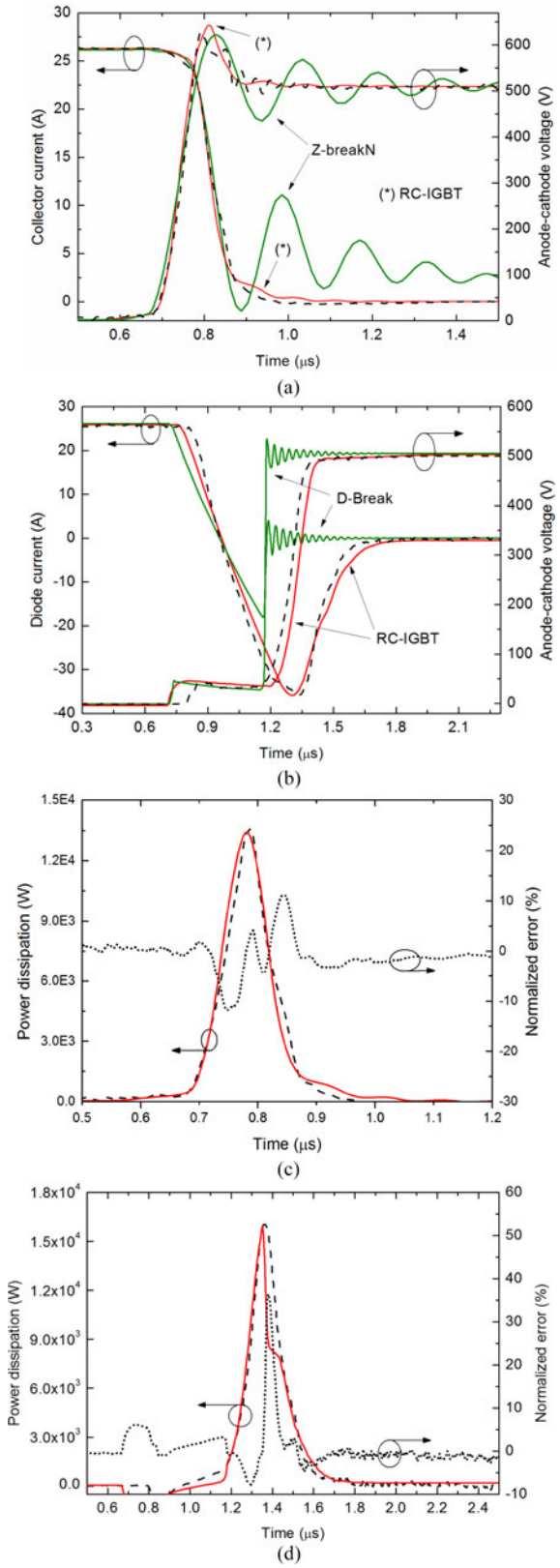

Fig. 10. Comparison between experimental and numerical waveforms during the double-pulse test at $T_0 = 300\mathrm{K}$. (a) Current and voltage during IGBT turn-off. (b) Current and voltage during diode turn-off. (c) Power dissipation during IGBT turn-off and SPICE model error normalized to maximum power value. (d) Power dissipation during diode turn-off and SPICE model error normalized to maximum power value. — denotes measurement, — denotes simulation.

the reverse recovery phenomenon with a critical error in the turn-off power dissipation evaluation. To further confirm the effectiveness of our developed model in dynamic condition, the power dissipation for both IGBT and diode turn-off transitions are shown in Fig. 10 (c) and (d). On the same pictures, the difference between numerical and experimental curves is reported. The results confirm from a quantitative point of view the good description of the device dynamics in both forward and reverse operation. The same experiment was repeated for a different operating temperature T= 400 K and the comparison between experimental and numerical waveforms is reported in Fig. 11(a) and (b). The error plots shown in Fig. 11(c) and (d) confirm that the model correctly predicts the temperature dependence of the IGBT tail current and the diode reverse recovery current. The only differences are due to a slight delay between numerical and experimental curves. The dynamic characterization was completed with a turn-on transient showed in Fig. 12 for two temperatures. In this picture, an inductive load turn-on exhibits the forward recovery phenomenon discussed in the previous section for the IGBT. The forward peak voltage was correctly fitted using $\tau_F = 2$ µs. Fig. 12(c) and (d) report also the SPICE model error.

B. Quasi-Resonant Converter Application

In order to show that the proposed model can replicate the electro-thermal behavior of the RC-IGBT in a real application, a dc–ac converter has been realized using a quasi-resonant converter topology. In this circuit, the device operates in a common emitter configuration whilst an *LC* resonant network is the high-side load, as depicted in Fig. 13(a). The circuit is fed either with a dc voltage or with ac-rectified voltage. This topology is commonly used for induction cookers where the resonant inductance is composed by a heating coil and a cookware which is made of ferromagnetic material and which is heated due to an alternating electromagnetic field generated by the heating coil [40]. For the reader convenience, the basic circuit operation is resumed in the following. The converter action can be divided into three phases [41]: in the first phase, IGBT is ON, and the current in the inductor rises up to a desired peak value. When the IGBT turns OFF, the energy stored into the inductor starts to commute to the capacitor and the resonant phase occurs. Here, the collector voltage evolution is dictated by the resonant capacitor and it finally becomes negative, driving the diode of the RC-IGBT to conduct. In this third phase, current starts to flow from the diode to the inductor and it increases up to crossing zero and the diode turns naturally OFF avoiding reverse recovery effects. At this point, if the converter is designed to work in continuous current mode, the current starts to flow into the IGBT that is naturally turned ON at zero voltage with very low switching losses.

A 50-kHz switching frequency with a duty cycle of 70% was chosen for the circuit prototype. The resulting waveforms, after the initial transient, are shown in Fig. 14. Oscillations of the gate voltage and the device current occur when diode turns ON, and are produced by the stray inductance on the collector side. The DUT steady-state temperature, measured with a thermocouple, reaching about 372 K. In order to perform a reliable SPICE

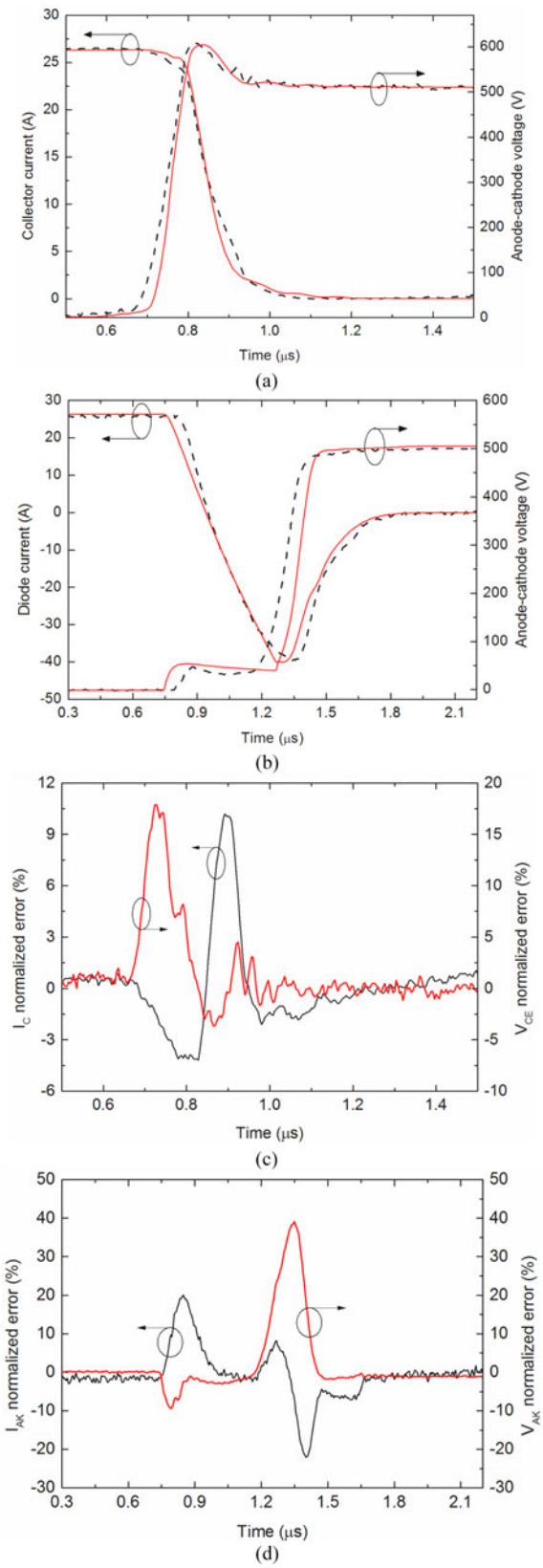

Fig. 11. Experimental and numerical waveforms during the double-pulse test at T_0 = 400 K. (a) Current and voltage during IGBT turn-off. (b) Current and voltage during diode turn-off. (c) SPICE normalized error during IGBT turn-off. (d) SPICE normalized error during diode turn-off. — denotes measurement, — denotes simulation.

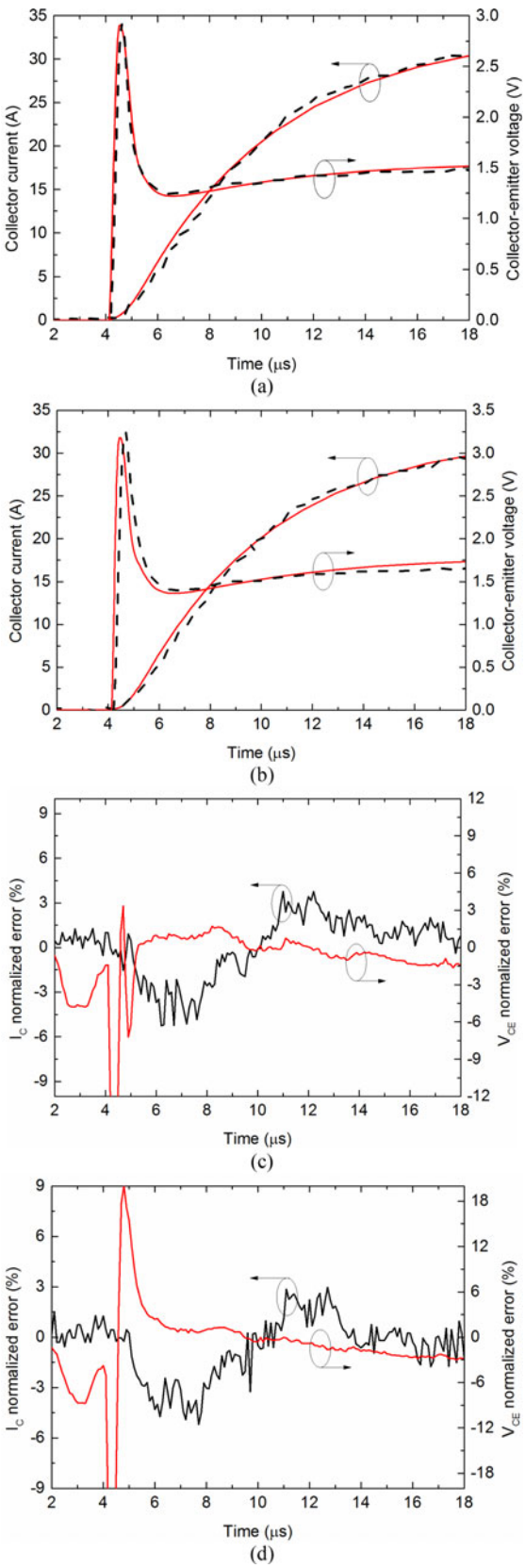

Fig. 12. Inductive turn-on waveforms with $V_{\mathrm{BATT}}= 10\mathrm{V}$, $R\sigma= 200\mathrm{m}\Omega$, $L\sigma= 1.5\mu\mathrm{H}$, $V_{\mathrm{GG}}= 15\mathrm{V}$. — denotes measurement, — denotes simulation. (a) $T= 300\mathrm{K}$, (b) $T= 380\mathrm{K}$. (c) SPICE normalized error at $T= 300\mathrm{K}$. (d) SPICE normalized error at $T= 380\mathrm{K}$.

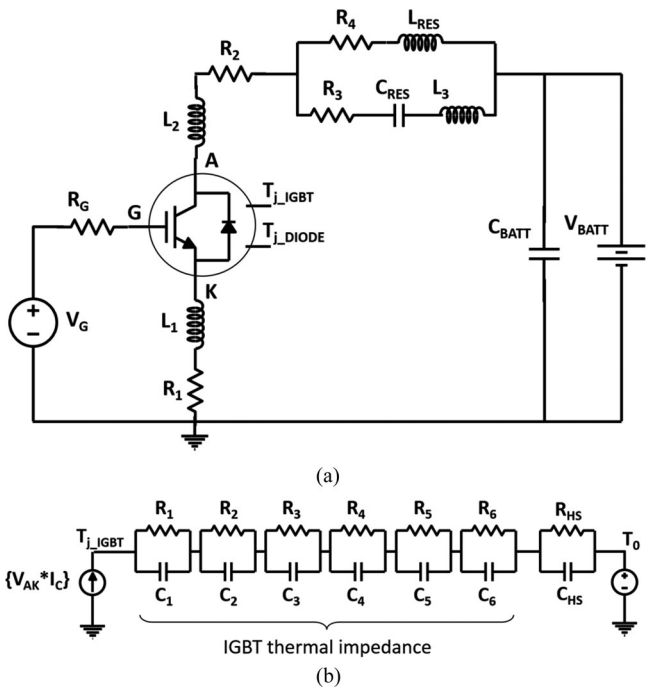

Fig. 13. Single-ended quasi-resonant converter circuit used for simulations and experiments: $R_{\mathrm{G}}= 15\Omega$, $L_{\mathrm{RES}}= 30\mu\mathrm{H}$, $C_{\mathrm{RES}}= 6\mathrm{nF}$, $V_{\mathrm{BATT}}= 50\mathrm{V}$. (b) IGBT equivalent thermal network used for the SPICE ET simulation [37].

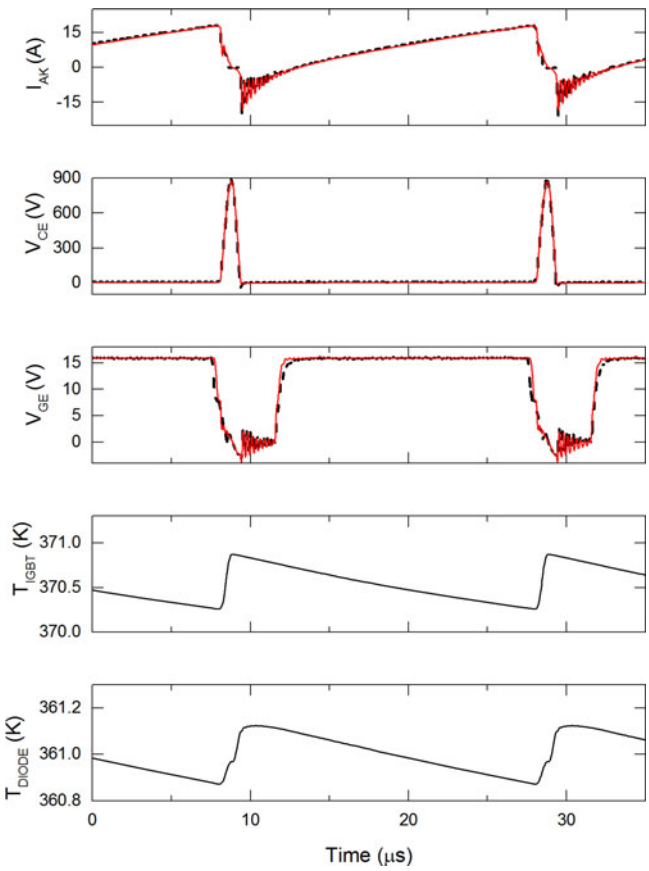

Fig. 14. Comparison between steady-state experimental waveforms and numerical results for the circuit in Fig. 13. — denotes measurement,— denotes simulation.

simulation, parasitic elements were considered in the simulated circuit [see Fig. 13(a)]. What is more, the coil-cookware setup was modeled with a series of an inductor and a resistance, as reported in [42]. To perform a coupled electro-thermal simulation, two equivalent thermal networks were used to simulate the self-heating effect within the device as shown in Fig. 13(b). The time-constant values for the thermal networks were obtained from the DUT data-sheet [37]. A simple RC pair was also used as a mutual thermal impedance. It was calibrated following the approach reported in [43]. A TCAD electro-thermal simulation was performed with a given electrical power dissipation in the IGBT region. From the monitoring of the temperature increase in the diode region, it was possible to evaluate the time constant of the mutual impedance. A mutual thermal resistance of 2.15 mK/W was extracted from the steady-state temperature increase, resulting in a 3.6 J/K mutual thermal capacitance. Results of the electro-thermal simulation are shown in Fig. 14 (dashed lines) and it is clearly visible how the simulated waveforms replicate very accurately the experimental results. Simulation results also show the steady-state temperature of the IGBT and diode along the time.

The average device temperature over the ambient temperature ($T_0 =$ 300 K) is about 367.5 K and, therefore, it is in good accordance with the experimental data.

IV. Conclusion

A compact model of RC-IGBT with monolithically integrated body diode has been developed which reproduces the device behavior with good accuracy for the whole range of operating temperatures. This has been achieved by taking into account the physical phenomena involved into RC-IGBTs with a quasi-2-D modeling approach. The optimization of IGBT and p-i-n diode SPICE models has been deeply discussed. The obtained improvements guarantee an effective modeling of modern designs. Numerical simulations on 2-D TCAD structure have been used to correctly describe interaction between IGBT and diode regions inside the device. The resulting model is able to correctly describe the primary snapback phenomenon and the forward recovery effect. In order to have low complex model and to prevent convergence issues, empirical functions and fitting parameters are used, to reproduce the physical involved phenomena. Finally, the effectiveness of the model has been proved with an electro-thermal application. A quasi-resonant converter circuit has been realized and measurements are compared with simulation, showing an excellent agreement.

Acknowledgment

The authors would like to thank Prof. V. d'Alessandro and Prof. E. Napoli for many stimulating discussions.

References

[1] H. Takahashi, A. Yamamoto, S. Aono, and T. Minato, "1200V reverse conducting IGBT," in *Proc. IEEE 16th Int. Symp. Power Semicond. Devices ICs*, May 24–27, 2004, pp. 133–136.

[2] D. Kumar, M. Sweet, K. Vershinin, L. Ngwendson, and E. M. S. Narayanan, "RC-TCIGBT: A reverse conducting trench clustered," in *Proc. IEEE 19th Int. Symp. Power Semicond. Devices IC's*, May 27–31, 2007, pp. 161–164.

[3] B. Yi, Z. Lin, and X. Chen, "Snapback-free reverse-conducting IGBT with low turnoff loss," *Electron. Lett.*, vol. 50, no. 9, pp. 703–705, Apr. 2014.

[4] M. Gärtner, D. Vietzke, D. Reznik, M. Stoisiek, K. G. Oppermann, and W. Gerlach, "Bistability and hysteresis in the characteristics of segmented anode lateral IGBTs," *IEEE Trans. Electron Devices*, vol. 45, no. 7, pp. 1575–1579, Jul. 1998.

[5] H. Jiang *et al.*, "Low turnoff loss reverse-conducting IGBT with double n-p-n electron extraction paths," *Electron. Lett.*, vol. 48, no. 8, pp. 457–458, Apr. 2012.

[6] W. Chen, Z. Li, B. Zhang, M. Ren, Y. Liu, and Z. Li, "A snapback suppressed reverse-conducting IGBT with soft reverse recovery characteristic," *Superlattices Microstruct.*, vol. 61, no. 0749-6036, pp. 59–68, Sep. 2013.

[7] K. Takahashi *et al.*, "New reverse-conducting IGBT (1200V) with revolutionary compact package," in *Proc. IEEE 26th Int. Symp. Power Semicond. Devices IC's*, Jun. 15–19, 2014, pp. 131–134.

[8] M. Rahimo, A. Kopta, U. Schlapbach, J. Vobecky, R. Schnell, and S. Klaka, "The bi-mode insulated gate transistor (BIGT) a potential technology for higher power applications," in *Proc. IEEE 21st Int. Symp. Power Semicond. Devices IC's*, Jun. 14–18, 2009, pp. 283–286.

[9] L. Storasta, A. Kopta, and M. Rahimo, "A comparison of charge dynamics in the reverse-conducting RC IGBT and bi-mode insulated gate transistor BiGT," in *Proc. IEEE 22nd Int. Symp. Power Semicond. Devices IC's*, Jun. 6–10, 2010, pp. 391–394.

[10] U. Vemulapati, N. Kaminski, D. Silber, L. Storasta, and M. Rahimo, "Reverse conducting-IGBTs initial snapback phenomenon and its analytical modelling," *IET Circuits, Devices Syst.*, vol. 8, no. 3, pp. 168–175, May 2014.

[11] V. d'Alessandro *et al.*, "SPICE modeling and dynamic electrothermal simulation of SiC power MOSFETs," in *Proc. IEEE 26th Int. Symp. Power Semicond. Devices IC's*, Jun. 15–19, 2014, pp. 285–288.

[12] R. Kraus, P. Turkes, and J. Sigg, "Physics-based models of power semiconductor devices for the circuit simulator SPICE," in *Proc. IEEE 29th Annu. Power Electron. Spec. Conf.*, May 17–22, 1998, pp. 1726–1731, vol. 2.

[13] R. Azar *et al.*, "Advanced SPICE modeling of large power IGBT modules," *IEEE Trans. Ind. Appl.*, vol. 40, no. 3, pp. 710–716, May/Jun. 2004.

[14] D. Cavaiuolo *et al.*, "A robust electro-thermal IGBT SPICE model: Application to short-circuit protection circuit design," *Microelectron. Rel.*, vol. 55, nos. 9–10, pp. 1971–1975, Aug./Sep. 2015.

[15] A. G. M. Strollo, "A new SPICE model of power P-I-N diode based on asymptotic waveform evaluation," *IEEE Trans. Power Electron.*, vol. 12, no. 1, pp. 12–20, Jan. 1997.

[16] A. G. M. Strollo and E. Napoli, "Improved PIN diode circuit model with automatic parameter extraction technique," *IEE Proc.—Circuits, Devices Syst.*, vol. 144, no. 6, pp. 329–334, Dec. 1997.

[17] M. Antoniou, F. Udrea, F. Bauer, and I. Nistor, "A new way to alleviate the RC IGBT snapback phenomenon: The Super Junction solution," in *Proc. IEEE 22nd Int. Symp. Power Semicond. Devices IC's*, Jun. 6–10, 2010, pp. 153–156.

[18] M. Cotorogea, "Physics-based SPICE-model for IGBTs with transparent emitter," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2821–2832, Dec. 2009.

[19] A. R. Hefner and D. M. Diebolt, "An experimentally verified IGBT model implemented in the Saber circuit simulator," *IEEE Trans. Power Electron.*, vol. 9, no. 5, pp. 532–542, Sep. 1994.

[20] A. R. Hefner, "Modeling buffer layer IGBTs for circuit simulation," *IEEE Trans. Power Electron.*, vol. 10, no. 2, pp. 111–123, Mar. 1995.

[21] X. Kang, E. Santi, J. L. Hudgins, P. R. Palmer, and J. F. Donlon, "Parameter extraction for a physics-based circuit simulator IGBT model," in *Proc. IEEE 18th Annu. Appl. Power Electron. Conf. Expo.*, Feb. 9–13, 2003, pp. 946–952.

[22] D. Cavaiuolo *et al.*, "An effective parameters calibration technique for PSPICE IGBT models application," *Proc. Int. Symp. Power Electron., Elect. Drives, Autom. Motion*, 2014, pp. 133–138, doi: 10.1109/SPEEDAM.2014.6872055.

[23] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, 2007, ch. 4.

[24] M. Riccio, L. Maresca, A. Irace, G. Breglio, and Y. Iwahashi, "Impact of gate drive voltage on avalanche robustness of trench IGBTs," *Microelectron. Rel.*, vol. 54, nos. 9–10, pp. 1828–1832, Sep./Oct. 2014.

[25] D. A. Grant and J. Gowar, *Power MOSFETs: Theory and Applications*. Hoboken, NJ, USA: Wiley-Interscience, 1989.

[26] S. Pendharkar and K. Shenai, "A critique of the turn-on physics of power bipolar devices," in *Proc. Bipolar/BiCMOS Circuits Technol. Meeting*, Oct. 2–3, 1995, pp. 209–212.
[27] S. Pendharkar and K. Shenai, "Zero voltage switching behavior of punchthrough and nonpunchthrough insulated gate bipolar transistors (IGBT's)," *IEEE Trans. Electron Devices*, vol. 45, no. 8, pp. 1826–1835, Aug. 1998.
[28] A. G. M. Strollo, "A new IGBT circuit model for SPICE simulation," in *Proc. IEEE 28th Annu. Power Electron. Spec. Conf.*, Jun. 22–27, 1997, pp. 133–138.
[29] S. Pendharkar and K. Shenai, "Evaluation of turn-on performance of p-i-n rectifiers and IGBT's under zero voltage switching," *IEEE Trans. Electron Devices*, vol. 43, no. 4, pp. 647–654, Apr. 1996.
[30] A. G. M. Strollo and E. Napoli, "Power rectifier model including self-heating effects," *Microelectron. Rel.*, vol. 38, no. 12, pp. 1899–1906, Dec. 1998.
[31] C. M. Tan and K. J. Tseng, "Using power diode models for circuit simulations: A comprehensive review," *IEEE Trans. Ind. Electron.*, vol. 46, no. 3, pp. 637–645, Jun. 1999.
[32] N. Jankovic, T. Pesic, and P. Igic, "All injection level power PiN diode model including temperature dependence," *Solid-State Electron.*, vol. 51, no. 5, pp. 719–725, May 2007.
[33] E. Napoli, A. G. M. Strollo, and P. Spirito, "Numerical analysis of local lifetime control for high-speed low-loss p-i-n diode design," *IEEE Trans. Power Electron.*, vol. 14, no. 4, pp. 615–621, Jul. 1999.
[34] A. Kopta, M. Rahimo, and U. Schlapbach, "New plasma shaping technology for optimal high voltage diode performance," in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 2–5, 2007, pp. 1–10.
[35] S. Matthias, S. Geissmann, M. Bellini, A. Kopta, and M. Rahimo, "Inherently soft free-wheeling diode for high temperature operation," in *Proc. IEEE 25th Int. Symp. Power Semicond. Devices ICs*, May 26–30, 2013, pp. 335–338.
[36] M. T. Rahimo and N. Y. A. Shammas. "Freewheeling diode reverse-recovery failure modes in IGBT applications," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 661–670, Mar./Apr. 2001.
[37] Data sheet of reverse conducting IGBT with monolithic body diode IHW30N120R3. [Online]. Available: http://www.infineon.com/cms/en/product/, 2015
[38] A. G. M. Strollo, E. Napoli, L. Fratelli, and G. Giannini, "Automatic parameter extraction technique for a PiN diode circuit model," in *Proc. 21st Int. Conf. Microelectron.*, Sep. 14–17, 1997, pp. 269–272, vol. 1.
[39] *PSPICE: User's Manual. OrCAD 16.5*, Cadence, Portland, OR, USA, 2011.
[40] J. Acero, C. Carretero, I. Millán, Ó. Lucía, R. Alonso, and J. M. Burdío, "Analysis and modeling of planar concentric windings forming adaptable-diameter burners for induction heating appliances," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1546–1558, May 2011.
[41] Ó. Lucia, L. A. Barragan, J. M. Burdio, Ó. Jimenez, D. Navarro, and I. Urriza, "A versatile power electronics test-bench architecture applied to domestic induction heating," *IEEE Trans. Ind. Electron.*, vol. 58, no. 3, pp. 998–1007, Mar. 2011.
[42] I. Sheikhian, N. Kaminski, S. Voß, W. Scholz, and E. Herweg, "Optimisation of the reverse conducting IGBT for zero-voltage switching applications such as induction cookers," *IET Circuits, Devices Syst.*, vol. 8, no. 3, pp. 176–181, May 2014.
[43] F. Ferranti *et al.*, "Effective electrothermal analysis of electronic devices and systems with parameterized macromodeling," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 5, no. 6, pp. 788–796, Jun. 2015.

Michele Riccio received the B.Sc., M.S., and Ph.D. degrees in electronics engineering from the University of Naples Federico II, Naples, Italy, in 2004, 2007, and 2011, respectively.

He is a Research Fellow with the Department of Electric and Information Technology Engineering, University of Naples Federico II. His research interests include electro-thermal modeling and simulation of power devices; advanced experimental characterization of electrical and thermal behavior of solid-state electronic devices.

Giuseppe De Falco received the bachelor's and master's degrees in electronic engineering from the University of Naples Federico II, Naples, Italy, in 2008 and 2011, respectively, and also the Ph.D. degree, in 2015, in electronic engineering.

His research activities include the analysis of reliability of power semiconductor devices operating in avalanche as well as in short circuit conditions. In 2016, he joined Infineon Technologies, Austria, as an Application Engineer.

Paolo Mirone received the master's degree in electronic engineering from the University of Naples Federico II, Naples, Italy, in 2013. He is currently working toward the Ph.D. degree in information technology and electrical engineering, working on the modeling, design, and characterization of power semiconductor devices.

Luca Maresca received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Naples Federico II, Naples, Italy, in 2005, 2009, and 2013, respectively.

He is currently a Research Fellow with the Department of Electrical Engineering and Information Technologies, University of Naples Federico II. His research interests include modeling, simulation, design, and experimental characterization of semiconductor power devices (IGBTs and diodes) in the field of high reliability, up to harsh operating conditions.

Marianna Tedesco received the bachelor's degree (*cum laude*) in electronic engineering from the University of Naples Federico II, Naples, Italy, in 2015.

Her research interests include modeling, simulation, and characterization of power semiconductor devices with particular focus on reverse-conducting IGBTs and p-i-n diodes.

Giovanni Breglio received the bachelor's degree (*cum laude*) in electronic engineering and the Ph.D. degree in electronic engineering and computer science from the University of Naples Federico II, Naples, Italy, in 1990 and 1994, respectively.

He is currently an Associate Professor of Electronics at the University of Naples Federico II. His research interests include the electro-thermal modeling and characterization of semiconductor devices, the design of optoelectronic devices and the development of new fiber optical sensors. He has authored more than 50 peer-reviewed journal papers and more than 110 proceedings of international conferences.

Andrea Irace (M'98–SM'12) received the Laurea and Ph.D. degrees in electronic engineering from the University of Naples Federico II, Naples, Italy, in 1994 and 1998, respectively.

He is currently an Associate Professor of electronics. His interests include power semiconductor devices and optoelectronic devices.

Prof. Irace is a Member of the Technical Program Committee of the IEEE International Symposium on Power Semiconductor Devices and ICs and a regular Reviewer for International Journals and Conferences.