A Wide Load Range ZVS Push–Pull DC/DC Converter With Active Clamped

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***Abstract*—A new active-clamped zero-voltage switching (ZVS) push–pull converter is proposed in this paper. Compared with the conventional push–pull converter, one auxiliary switch Q_3 and a clamping capacitor C_a are added in the primary side of the transformer to recycle the energy stored in the leakage inductors and clamp the voltage spike. Owing to the proposed converter which maintains ZVS of all the three switches from full load to very light-load condition, switching losses are reduced significantly. The voltage across the switch can be clamped at the input voltage plus the clamping capacitor voltage, i.e., $V_{\rm in}+V_{Ca}$, are much less than those of a conventional push–pull converter that enabling the use of low-voltage, low-performance, and low-cost devices. In addition, the proposed topology can eliminate the problems of flux imbalance existing in the conventional one. Detailed operation, analysis, design, comparative study, and experimental results for the proposed converter are presented in this paper. An 800 W prototype was developed in the laboratory to evaluate and demonstrate the validity of the converter.**

***Index Terms*—Active clamped, push–pull converter, voltage spike, zero-voltage switching (ZVS).**

I. Introduction

CURRENTLY, most electrical equipments are designed with the focus on isolation, lightweight, small size, high power density, high reliability, low cost, and low electromagnetic interference (EMI) to meet high expectations of the consumer. The push–pull converters have attributes of simple circuitry, galvanic isolation, high-voltage conversion ratio, and better transformer utilization; also, they are widely used in low-input voltage applications such as uninterruptible power supply (UPS) [1], battery chargers [2], electric vehicles [3], fuel cell systems [4], and photovoltaic systems [5], etc. It is worth to mention that on one hand the conventional push–pull converter suffers from high turn-off voltage spike because of transformer leakage inductor; on the other hand, the hard-switched results in the amount of switching losses. Besides, the problem of EMI will be serious when the switching frequency is higher. As a consequence, the conventional push–pull converter is unable to meet aforesaid requirements because of high switch stress, high switching losses, and the problem of EMI. In order to fulfill the above said demand and overcome the aforementioned limitations, many zero-voltage switching (ZVS) and zero-current switching (ZCS) topologies have been proposed and developed in the past literature [6]–[10]. The soft-switching converter switches can be controlled to be at zero or near zero at the moment of switching. Such operation principle is usually achieved by making use of series resonance phenomenon, parallel resonance phenomenon, and series-parallel resonance phenomenon that occur between dedicated components or parasitic elements in the converter circuit itself.

Among these numerous circuits, a push–pull converter can be categorized as either current-fed or voltage-fed based on the switching scheme and placement of the filter inductor. Current-fed push–pull converters [11]–[20] employ the filter inductor in the primary-side of high frequency (HF) transformer and the switching scheme refrains from the occurrence of open circuit. The transformer leakage inductor can be utilized as part of the filter inductor. Compared with voltage-fed push–pull converters [21]–[31], current-fed push–pull converters usually have the lower input current ripple due to the existence of the input inductor and the lower rectifier diode voltage surge because of the capacitive output filter. However, the physical size of the input inductor existed in the current-fed converter is dramatically increased owing to a high input current demand (due to energy being proportional to current squared) in voltage step-up applications. So the current-fed appliance has a relatively large volume caused by the high input current in the low voltage side, which leading to it is not a good choice in some productions. On the contrary, the filter inductor of the voltage-fed push–pull converters is placed at the output side, which can be manufactured with a smaller volume. Moreover, the voltage-fed push–pull converter can utilize the leakage inductor for resonance action to realize ZVS or ZCS to minimize switching losses, and high efficiency can be realized with resonant switching [6]–[9]. The current-fed push–pull converters are mostly used in the new energy system [5], [16]–[20], while the voltage-fed push–pull converters are preferable in battery charges and electric vehicles applications [2], [21]–[24].

It is worth noticing that both current-fed and voltage-fed push–pull converters have a common problem that voltage spikes occur at the turn-off moment of power switches. These voltage spikes are caused by the abrupt switching and leakage inductor of the HF transformer. In view of this drawback, several kinds of passive snubbers [25]–[26] and active clamp circuits [17]–[20], [27]–[30] are presented to release the

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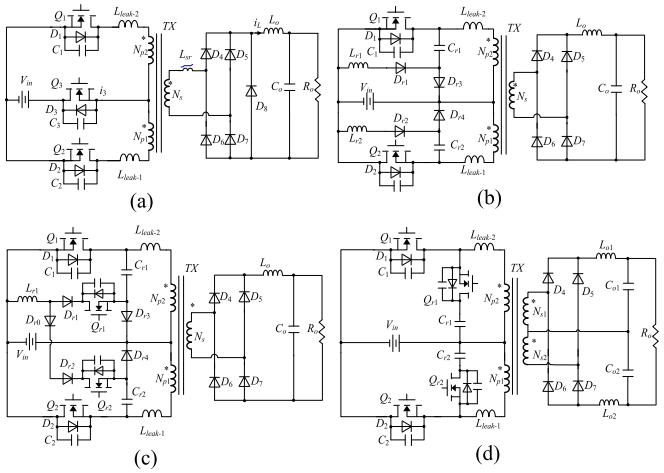

Fig. 1. (a) ZVS push–pull converter without voltage clamped in [24]. (b) Passive snubber circuit for push–pull converter in [26]. (c) Proposed active-clamped push–pull converter in [27]. (d) Presented ZVS push–pull converter with active clamped in [30].

energy stored in the leakage inductor. The passive snubber circuit in [26] [see Fig. 1(b)] has an unintentional current path when the clamping capacitor voltage is higher than the input voltage, and the duty cycle of power switch has to be fixed 50%. The converter proposed in [27] [see Fig. 1(c)] solves the discharge problem [26] of the clamping capacitor and can feedback energy of the clamping capacitor to output. However, this converter adds too many power devices. The active power switches of the converters in [17], [18], and [28] are located both on the primary and secondary sides of the high transformer and all of the active switches can achieve ZVS. However, the complicated driver circuits are needed and the cost is high. The three-phase push–pull converters with active-clamp [19], [20] circuits also increase the driving complexity and associated cost. The topology [29] adds two active clamping circuits to recycle leakage energy at the primary side of high transformer and the clamping switches can also realize ZVS. But the components stress imposed on the clamping switches are greater than twice the input voltage. A buck–boost type of active clamping circuits is proposed in [30], as shown in Fig. 1(d). Two auxiliary power switches are added and all four power switches can achieve ZVS. But the drawback is that the maximum duty cycle is limited by the clamping circuit and complicated drivers for the added active switches are needed. Recent work with an active energy recovery clamp (AERC) circuit topology has been discussed to address the voltage stress issue with the SiC devices [31]. AERC utilizes a switching converter to transfer power back to the input voltage source.

In this paper, a new push–pull converter with active clamped is proposed, as shown in Fig. 2. ZVS can be realized for all of the three switches under the wide load range condition. The voltage across the switch , i.e., $V_{\rm in}+V_{Ca}$, is much less than those of the conventional push–pull converter. This paper is organized as follows. Section II gives the topology structure and the detailed operation state of the proposed converter. In Section III, the features and design guidelines are analyzed deeply and followed by the topology comparative study in Section IV. Subsequently,

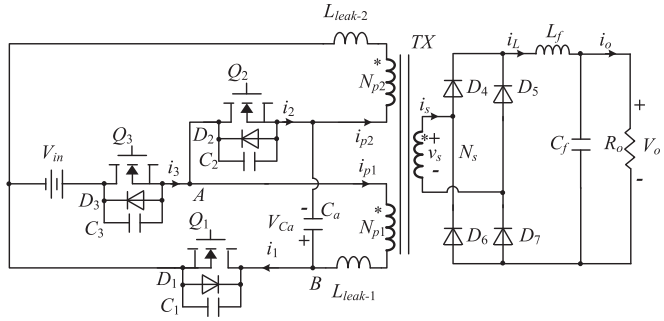

Fig. 2. Proposed ZVS push–pull converter with voltage clamped.

the experimental results are provided in Section V. Section VI presents the conclusion of this paper.

II. Operation and Analysis of the Proposed Converter

Fig. 2 shows the circuit configuration of the proposed push–pull converter. One switch Q_3 and a clamping capacitor C_a are added in the primary side of HF transformer compared with the conventional push–pull converter. Diodes $D_1 - D_3$ and capacitors $C_1 - C_3$ are the antiparallel body diodes and the parasitic capacitors of the switches $Q_1 - Q_3$, respectively. The HF transformer *TX* is utilized to achieve isolation and boost the low input voltage. The secondary side circuit is composed of diodes $D_4 - D_7$, filter inductor L_f, filter capacitor C_f, and load R_o. The inductors $L_{\rm leak-1}\,{\rm and}\,{\rm L}_{\rm leak-2}$ represent the leakage inductors of the HF transformer.

The principle operation of the proposed push–pull converter is explained using the idealized current and voltage waveforms of the key components in Fig. 3. The gate signals adopt the switching strategy presented in [24], where dividing the operating status of Q_1,Q_2 and Q_3 into four states, 101→110→011→110 (1 represents switch-on, while 0 represents switch-off). The last time of state 101 is same with state 011 ensuring the flux balance of HF transformer. Moreover, dead time is inserted between the gate signals for the switches $(Q_1$ and , $Q_3, Q_2\,{\rm and}\,Q_3)$ in practical applications to realize ZVS.

To simplify description of the operational principles, the following assumptions are given:

1) all the switching devices, MOSFETs and diodes are ideal with antiparallel body diodes and parasitic capacitors;
2) capacitance of C_a and C_f is large enough, and the voltage across them can be seen as constant, V_{ca} and V_o, respectively;
3) capacitance value of C_1 and that of C_2,C_3 are identical, and inductance $L_{\rm leak-1}$ and that of $L_{\rm leak-2}$ are identical;
4) the transformer consists of an ideal transformer with a turn ratio of $N_{\rm s} : N_{p1} = N_s : N_{p2} = n$. The magnetizing inductance is large enough and the magnetizing current can be ignored.

Based on the aforesaid assumptions, the detailed operation of one switching period of the proposed converter can be subdivided into 12 intervals. Fig. 4 shows the equivalent circuits of the proposed converter under different intervals. Since the former

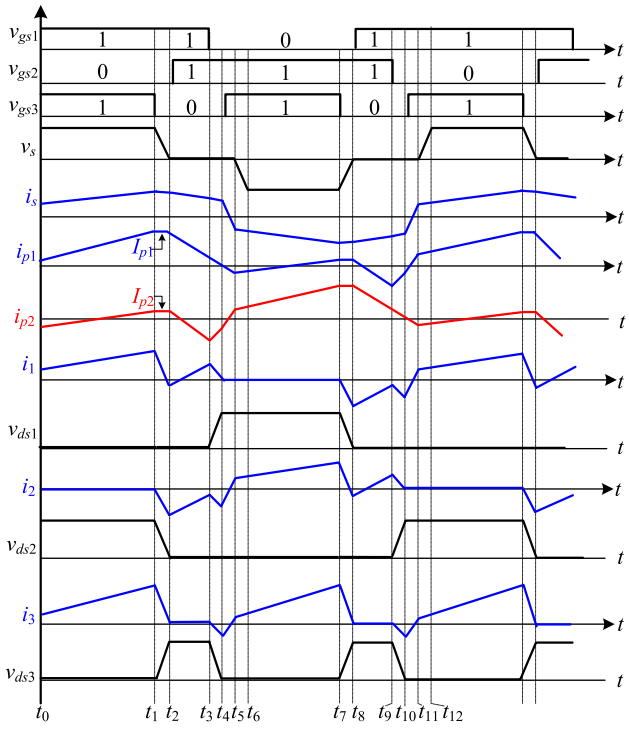

Fig. 3. Gate signals and the key waveforms of the proposed converter.

half-cycle is symmetrical to the latter half-cycle, the analysis of the working principle will focus on the former half-cycle only.

Interval 1[Fig. 4(a), $t_0 \le t < t_1$]: In the primary, both Q_1 and Q_3 are conducting, and Q_2 is reverse biased by $V_{\rm in}+V_{\rm ca}$. While in the secondary, diodes D_4 and D_7 are freewheeling. The power is transferred from the input to the load. Since the voltage $V_{\rm in}$ and $V_{\rm ca}$ are paralleled with the primary side winding N_{p1} and N_{p2}, respectively, primary currents $i_{p1}(t)$ and $i_{p2}(t)$ increase linearly, and can be expressed as follows:

$$i_{p1}(t) = i_{p1}(t_0) + \frac{V_{\rm in} - v_s/n}{L_{\rm leak}}(t - t_0) \tag{1}$$

$$i_{p2}(t) = i_{p2}(t_0) + \frac{(V_{Ca} - v_s/n)}{L_{\rm leak}}(t - t_0) \tag{2}$$

where v_s is the steady-state voltage of the secondary winding N_s.$i_{p1}(t_0)$, and $i_{p2}(t_0)$ are the initial values of $i_{p1}(t)$, and $i_{p2}(t)$ at time t_0.

In this interval, the currents through Q_3 and Q_1 are given by

$$i_3(t) = i_{p1}(t) \tag{3}$$

$$i_1(t) = i_{p1}(t) - i_{p2}(t). \tag{4}$$

Interval 2 [Fig. 4(b), $t_1 \le t < t_2$]: At t_1, Q_3 is turned off and it can achieve zero-voltage turn-off because of C_3. Primary current $i_{p1}(t)$ begins charging the parasitic capacitor C_3 of Q_3 and discharging the parasitic capacitor C_2 of Q_2. The v_{ds2} starts to decrease from $V_{\rm in}+V_{Ca}$ and the HF transformer voltage v_s decreases simultaneously. Since both of the magnetizing inductance and output filter inductor L_f are very large, $i_{p1}(t)$ and $i_{p2}(t)$ can be considered as two constant current sources I_{p1} and I_{p2}. Moreover, as the ideal voltage source, the voltage sources of $V_{\rm in}$ and $V_{\rm Ca}$ can be regarded as short circuit because of very small inner impedance in this very short time, so the capacitors C_1 and C_2 are in parallel with each other. The changing equations for this interval are

$$i_{p1}(t) = i_{p1}(t_1) = I_{p1} \tag{5}$$

$$i_{p2}(t) = i_{p2}(t_1) = I_{p2} \tag{6}$$

$$v_{ds3}(t) = I_{p1}(t - t_1)/2C \tag{7}$$

$$v_{ds2}(t) = V_{\rm in} + V_{Ca} - I_{p1}(t - t_1)/2C \tag{8}$$

where C is the effective drain-to-source MOSFET capacitance.

At t_2, the voltage v_{ds2} decays to zero and the current i_{p1} forces the body diode D_2 conducting which creates a ZVS condition for Q_2. In addition, the voltage of Q_3 increases to $V_{\rm in}+V_{\rm Ca}$ and will be clamped at that value. In this stage, the current i_3 decreases and i_2 reverse increases linearly to keep I_{p1} and I_{p2} constant. The secondary state is same with interval 1. This interval ends when the voltage v_s decreases to zero.

Interval 3 [Fig. 4(c), $t_2 \le t < t_3$]: This interval starts with v_{ds2} dropping to zero at t_2 and the driving signal v_{gs2} is applied to Q_2 to realize ZVS. Since the voltage of HF transformer v_s has been decreased to zero, the clamped-voltage V_{Ca} imposes on the primary leakage inductor $L_{\rm leak-1}$ and $L_{\rm leak-2}$ directly. Primary currents $i_{p1}(t)$ and $i_{p2}(t)$ decrease linearly, which can be expressed as

$$i_{p1}(t) = I_{p1} + \frac{-V_{Ca}}{L_{\rm leak}}(t - t_2) \tag{9}$$

$$i_{p2}(t) = I_{p2} + \frac{-V_{Ca}}{L_{\rm leak}}(t - t_2). \tag{10}$$

Meanwhile, currents i_1 and i_2 change linearly according to the variation of $i_{p1}(t)$ and $i_{p2}(t)$ during this interval. The energy stored in leakage inductors releases to the clamping capacitor. On the secondary side of HF transformer, voltage of L_f sustains $-V_o$ and i_{Lf} begins dropping linearly. Rectifier diodes D_4 and D_7 are still conducting, while D_5 and D_6 are reversely biased.

Interval 4 [Fig. 4(d), $t_3 \le t < t_4$]: At t_3,Q_1 is turned off. Q_1 can achieve ZVS feature due to the function of C_1. In this interval, leakage inductor $L_{\rm leak-2}$ resonates with C_1 and C_3, while leakage inductor $L_{\rm leak-1}$ is applied to the clamped voltage V_{Ca}. The capacitor C_1 is discharged down to zero, while capacitor C_3 is charged toward $V_{\rm in}+V_{Ca}$. The capacitors C_1 and C_3 can be viewed in parallel with each other in this short moment as discussed in interval 2. The current $i_{p2}(t)$ decreases because of resonance, and $i_{p1}(t)$ still decays linearly as interval 3. Therefore, the governing equations for this interval are

$$i_{p2}(t) = i_{p2}(t_3)\cos\omega_1(t - t_3) \tag{11}$$

$$v_{ds1}(t) = i_{p2}(t_3)\sqrt{L_{\rm leak}/(2C)}\sin\omega_1(t - t_3) \tag{12}$$

$$v_{ds3}(t) = V_{\rm in} + V_{Ca} - i_{p2}(t_3)\sqrt{L_{\rm leak}/(2C)}\sin\omega_1(t - t_3) \tag{13}$$

where

$$\omega_1 = 1/\sqrt{2L_{\rm leak}C}. \tag{14}$$

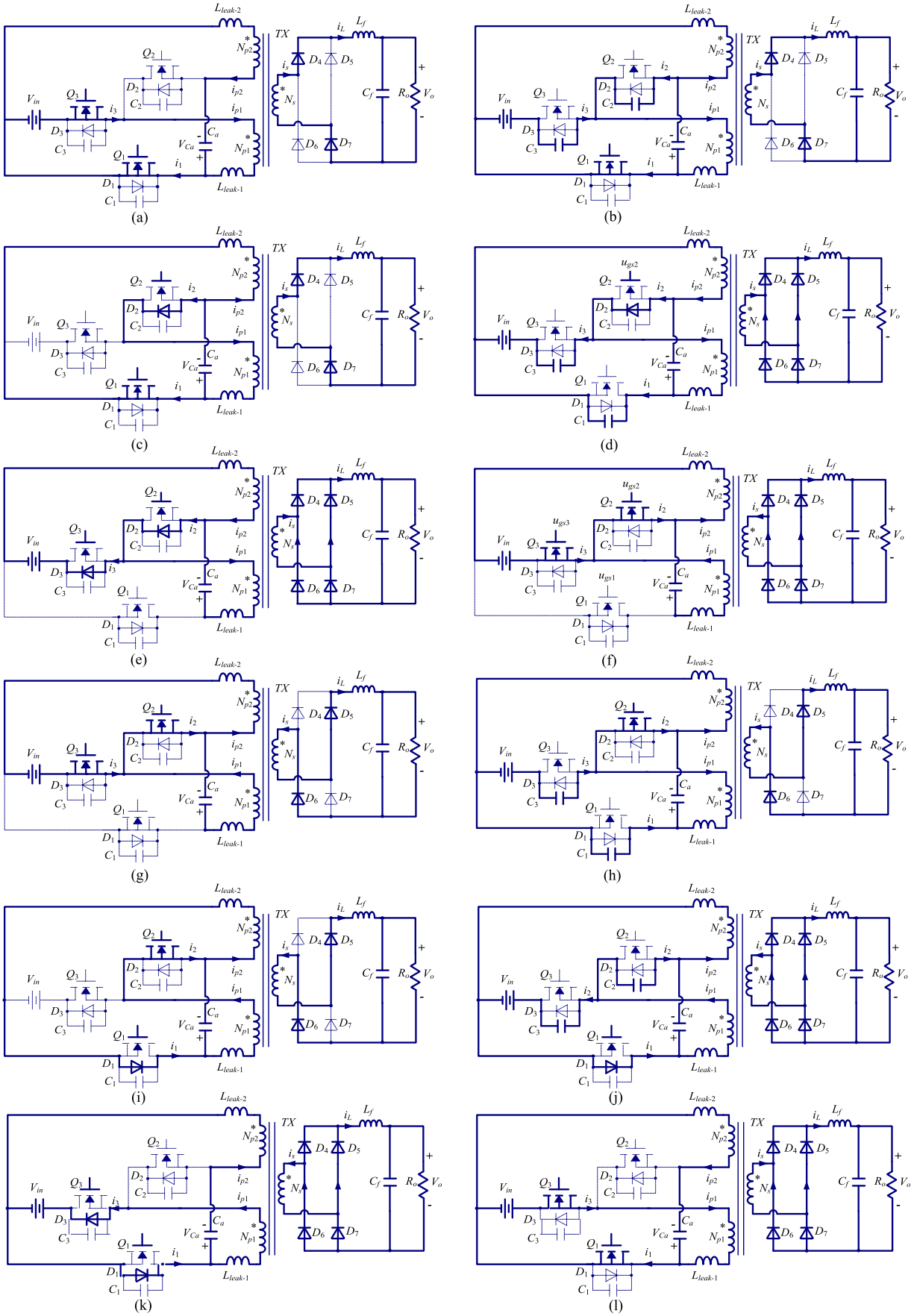

Fig. 4. Equivalent circuits for 12 operating intervals of the proposed ZVS push–pull converter with active clamped (a)–(f) intervals 1–6, (g)–(l) interval 7–12.

TABLE I.
SUMMARY OF CONDUCTING COMPONENTS AT DIFFERENT INTERVALS

Interval	Conducting components
Interval 1	Q_3, Q_1, D_4, D_7
Interval 2	Q_1, D_4, D_7
Interval 3	Q_1, D_2, D_4, D_7
Interval 4	D_2, D_4, D_5, D_6, D_7
Interval 5	$D_2, D_3, D_4, D_5, D_6, D_7$
Interval 6	$Q_2, Q_3, D_4, D_5, D_6, D_7$
Interval 7	Q_3, Q_2, D_5, D_6
Interval 8	Q_2, D_5, D_6
Interval 9	Q_2, D_1, D_5, D_6
Interval 10	D_1, D_4, D_5, D_6, D_7
Interval 11	$D_1, D_3, D_4, D_5, D_6, D_7$
Interval 12	$Q_1, Q_3, D_4, D_5, D_6, D_7$

During this interval, leakage inductor $L_{\mathrm{leak}-1}$ keeps to release its stored energy to the clamped capacitor C_a. On the secondary side, diodes $D_4 - D_7$ begin to freewheel simultaneously. This interval ends when the v_{ds3} decays to zero providing ZVS condition for Q_3.

Interval 5 [Fig. 4(e), $t_4 \leq t < t_5$]: At t_4, switch Q_3 can be turned on with ZVS when the antiparallel body diode D_3 conducts. After D_3 conducts, V_{in} is impressed on $L_{\mathrm{leak}-2}$. Thus, $i_{p2}(\mathrm{t})$ is forced to rise up more rapidly than previous state, while $i_{p1}(\mathrm{t})$ maintains the variation slope. These currents reflects into the secondary side and results in the commutation of four rectifier diodes quickly. The currents flowing through D_4 and D_7 increase quickly, synchronously that of D_5 and D_6 decrease. When currents of diodes D_4 and D_7 reach their peak reverse current at t_5, this interval finishes.

In this stage, the current $i_{p2}(\mathrm{t})$ can be expressed by

$$i_{p2}(t) = i_{p2}(t_4) + \frac{V_{\mathrm{in}}}{L_{\mathrm{leak}}}(t - t_4). \tag{15}$$

Interval 6 [Fig. 4(f), $t_5 \leq t < t_6$]: After t_5, diodes D_4 and D_7 start reverse recovery. The voltages across diodes D_4 and D_7 begin rising up, and the voltage of winding N_s rises from zero to V_{Ns} (V_{Ns} is the steady-state voltage of the secondary wingding.). As the currents of D_4 and D_7 reverse to zero at t_6, this interval ends.

From t_6, the latter half-cycle interval (Interval 7–12) begins working, and the equivalent circuits are shown in Fig. 4(g)–(l). The operation principle is exactly the same as that of the former half-cycle. Furthermore, the switching states of all power switches during different intervals are listed in Table I.

III. ANALYSIS AND DESIGN GUIDELINES

A. Clamped Voltage and Voltage Gain

When the proposed converter operates in steady state, the duration time of interval 2 and interval 4 are very short compared to one switching period. Therefore, these two stages can be neglected in analysis of clamped voltage and voltage gain. Fig. 5 shows the simplified waveforms. In Fig. 5, D represents the duty ratio of Q_3. T_s is the switching period of switch Q_3. It is noted that the inductance of $L_{\mathrm{leak}-1}$ or $L_{\mathrm{leak}-2}$ is less than that

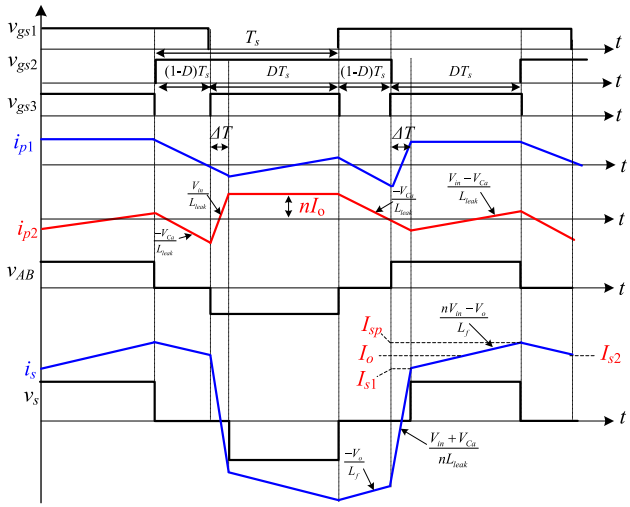

Fig. 5. Simplified key current and voltage waveforms of the proposed converter.

of the magnetizing inductance of the HF transformer. So, the voltage across $L_{\mathrm{leak}-1}$ or $L_{\mathrm{leak}-2}$ will not be considered, and the current i_{p1} and i_{p2} shown in Fig. 5 can be considered as constant current that are equal to nI_{o} [30] during interval 1 and interval 7, respectively. According to the volt–second balance principle of inductors, the voltage V_{Ca} can be derived as

$$V_{Ca} = \frac{D}{2 - D} V_{\mathrm{in}}. \tag{16}$$

The voltage gain of the proposed push–pull converter can be expressed as

$$\frac{V_o}{V_{\mathrm{in}}} = n(D - D_{\mathrm{loss}}) \tag{17}$$

where $D_{\mathrm{loss}} = \Delta T / T_s$, which is the loss duty cycle in the secondary voltage.

From Fig. 5, D_{loss} can be expressed as

$$D_{\mathrm{loss}} = \frac{I_{s1} + I_{s2}}{\frac{V_{\mathrm{in}} + V_{Ca}}{nL_{\mathrm{leak}}} T_s} \tag{18}$$

or

$$D_{\mathrm{loss}} = \frac{nL_{\mathrm{leak}}}{T_s(V_{\mathrm{in}} + V_{Ca})} \left(2I_o - \frac{V_o}{L_f}(1 - D)T_s \right). \tag{19}$$

When the term containing (1–D) T_s in (19) is small compared to $2I_o$, thus (19) can be simplified as

$$D_{\mathrm{loss}} = \frac{2I_o nL_{\mathrm{leak}}}{T_s(V_{\mathrm{in}} + V_{Ca})}. \tag{20}$$

By (16)–(19), it is observed that D_{loss} depends on the load for a given converter specification. Fig. 6 shows the relationship between the loss duty cycle D_{loss}, duty ratio D and load current I_o for the specification of $\mathrm{n} = 4, \mathrm{L_{leak}} = 5.5\mu\mathrm{H}$ and $\mathrm{V_o} = 200\ \mathrm{V}$ at the frequency of 88 kHz. It can be seen that D_{loss} is rising up with increase of I_o. This characteristic cannot be ignored in design of the converter.

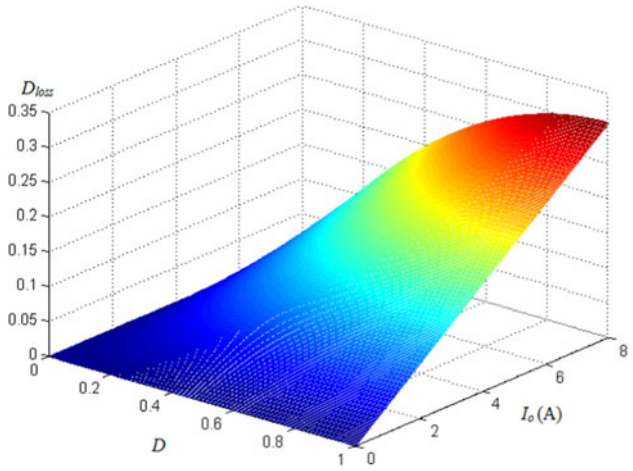

Fig. 6. Plots of the relationship between the loss duty cycle $D_{\rm loss}$, the duty ratio D and the load current I_o for $n = 4$, $L_{\rm leak} = 5.5\mu$H and $\rm V_o = 200$ V at the frequency of 88 kHz.

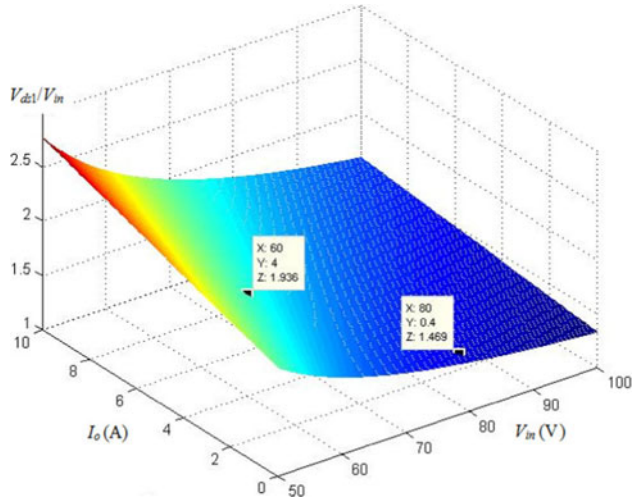

Fig. 7. Plots of the relationship between voltage stress $V_{ds1}/V_{\rm in}$, load current $I_{\rm o}$ and input voltage $V_{\rm in}$ for $n = 4$,$\rm L_{leak} = 5.5\,\mu H$ and $\rm V_o = 200$ V at the frequency of 88 kHz.

B. Stress of Power Switches

According to the foresaid operational intervals, the voltage stress of switches Q_1–Q_3 and rectifier diodes D_4–D_7 can be expressed as follows:

$$V_{ds1} = V_{ds2} = V_{ds3} = V_{\rm in} + V_{Ca} \tag{21}$$

$$V_{D4} = V_{D5} = V_{D6} = V_{D7} = nV_{\rm in}. \tag{22}$$

In the steady state, by using the ampere–second balance principle to the clamped capacitor C_a, the average current flowing through C_a can be considered as zero. Therefore, the average current passing through switches $Q_1 - Q_3$ and diodes $D_4 - D_7$ can be derived as follows:

$$I_3 = \frac{nI_o(D - D_{\rm loss})}{\eta} \tag{23}$$

$$I_1 = I_2 = \frac{nI_o(D - D_{\rm loss})}{2\eta} \tag{24}$$

$$I_{D4} = I_{D5} = I_{D6} = I_{D7} = I_o/2 \tag{25}$$

where η represents the converter efficiency.

From (16)–(21), the relationship between the voltage ratio $V_{ds1}/V_{\rm in}$, load current I_o, and input voltage $V_{\rm in}$ with the same specification shown in Fig. 6 can be drawn, as illustrated in Fig. 7. It can be seen that the voltage ratio $V_{ds1}/V_{\rm in}$ is ascending with increase of I_o, but decreasing with rising up of input voltage. Particularly, Fig. 7 implies that the component stresses $V_{ds1} - V_{ds3}$ are less than twice input voltage comparing to the conventional push–pull converter. Lower voltage stress means that the power switches with lower on-state resistor can be utilized. Furthermore, it is noted that the problem of voltage spike across the switch can be eliminated and the energy stored in leakage inductor can be recycled.

C. ZVS Conditions and ZVS Range

1) Conditions for Switches Q_1 and Q_2: When Q_3 is turned off, the primary current is reaching its peak value. The energy available to charge C_3 and discharge C_2 ($\rm C_1$) is the energy stored in $L_{\rm leak}$ plus that in the output filter inductor L_f. Because the energy stored in L_f is large compared to that required to charge C_3 from zero to $V_{\rm in}+\rm V_{Ca}$ and discharge C_2 (C_1) from $\rm V_{in}+V_{Ca}$ to zero. Therefore, the capacitor C_2 (C_1) can be considered discharged approximately at a linear rate with a constant current. The ZVS condition of switch Q_1 (Q_2) can be obtained from energy viewpoint and is given by

$$(L_{\rm leak} + L_f/n^2)I_{P1}^2 \geq 2C(V_{\rm in} + V_{Ca})^2. \tag{26}$$

The required dead time t_{d1} between Q_3 and Q_2 (Q_1) can be derived as

$$t_{d1} \geq \frac{V_{\rm in} + V_{Ca}}{2I_{p1}C}. \tag{27}$$

2) Condition for Switch Q_3: For switch Q_3, ZVS is provided by the resonance process between the primary leakage inductor $L_{\rm leak-2}$ ($\rm L_{leak-1}$), the parasitic capacitors C_1 (C_2) and C_3. When Q_1 (Q_2) is turned off, the available energy to charge C_1 (C_2) and discharge C_3 is just that in leakage inductor. According to the explanation in interval 4, the energy condition ZVS for Q_3 can be expressed as

$$L_{\rm Leak}(i_{p2}(t_3))^2 > 2C(V_{\rm in} + V_{Ca})^2. \tag{28}$$

Similarly, the needed dead time t_{d2} between Q_1 (Q_2) and Q_3 in this interval can be obtained by providing a sinusoidal voltage across the C_3 that arrives at a maximum at one fourth of the resonant period

$$t_{d2} \geq \frac{\sqrt{2}\pi}{2}\sqrt{L_{\rm leak}C}. \tag{29}$$

3) ZVS Load Range: The ZVS for Q_1 and Q_2 can be achieved easily because of the large energy of filter inductor. Therefore, the ZVS range is mainly determined by that of Q_3. However, Q_3 only realizes ZVS for a load current above a critical value $I_{\rm cirt}$, which can be calculated form (28):

$$I_{\rm crit} = \sqrt{2C(V_{\rm in} + V_{Ca})^2/L_{\rm Leak}}. \tag{30}$$

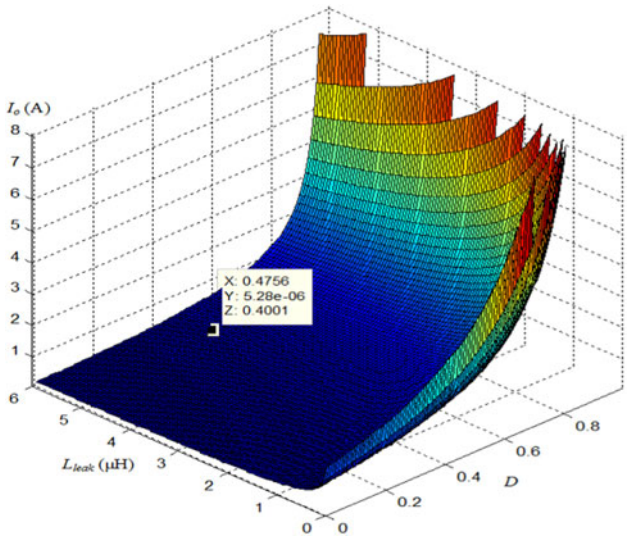

Fig. 8. Plots of the relationship between voltage stress I_o, duty ratio D and leakage inductor $L_{\rm leak}$.

From Fig. 5, the current through $L_{\rm leak}$ at t_3 can be calculated as

$$i_{p2}(t_3) = nI_o - \frac{V_{\rm in}}{L_{\rm leak}}\Delta T = nI_o(D-1). \tag{31}$$

In order to achieve ZVS of Q_3, the absolute value of $i_{p2}(t_3)$ has to satisfy

$$|i_{p2}(t_3)| > I_{\rm crit}. \tag{32}$$

Therefore, the ZVS load range can be obtained as

$$I_o > \frac{I_{\rm crit}}{n(1-D)}. \tag{33}$$

From (33) and (19), it can be seen that ZVS is realized over a greater load range with larger value of the leakage inductor $L_{\rm leak}$. However, the effective duty cycle in the secondary will decrease because of the larger $L_{\rm leak}$. So, the leakage inductor $L_{\rm leak}$ has to be selected with comprehensively considering.

According to (30) and (33), if the parasitic capacitor C and transformer turn ratio n are used as the following prototype parameters. To obtain the ZVS range, the relationship between the leakage inductor $L_{\rm leak}$, output current I_o, and duty cycle D can be plotted as shown in Fig. 8. Note here that the leakage inductor $L_{\rm leak}$ should be selected from the area above the curved surface for realizing the ZVS.

D. Solution of Flux Imbalance

There is a potential problem existed in conventional push–pull converter that is the flux imbalance resulting from the different duty ratios for the power switches. The proposed converter with the clamped function can solve this problem. For example, different duty ratios of switches $Q_1 - Q_3$ will result in different magnetizing and leakage inductor. Since the energy in leakage inductor can be recycled to the clamped capacitor C_a, thus, the relative larger inductor current because of the asymmetrical duty cycle will result in more charges stored in the clamped capacitor C_a. Then, the voltage V_{Ca} will increase. The increase of V_{Ca} will in turn induce from a larger product of voltage–second, which can be used to balance the excessive flux caused by a larger duty cycle. Therefore, the potential flux imbalance issue can be solved in this proposed converter.

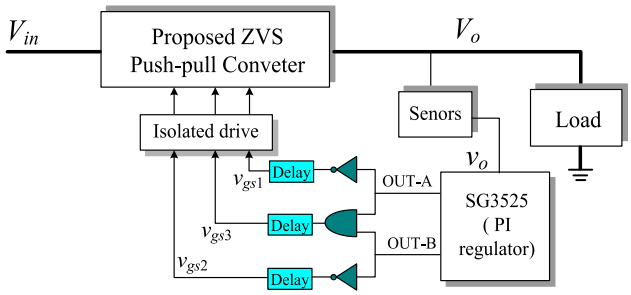

Fig. 9. Control block diagram.

E. Control Loop

The output voltage and power can be regulated by varying the duty cycle D of Q_3. According to the switching sequence, the control block can be given as shown in Fig. 9. The conventional voltage feedback loop can be used to regulate the specified output voltage. The signal v_o sampled by the sensor feeds back to the widely used IC SG3525. IC SG3525 and the connection of its peripheral circuit compose the PI regulator to generate the command value for pulse width modulation signals OUT-A and OUT-B. Signals OUT-A and OUT-B pass through simple logic and delay circuits to generate gate signals v_{gs1}, v_{gs2} and v_{gs3}. It is noted that three delay parts are inserted between the gate-signals to realize ZVS of the switches. Besides, the gate signals can also be implemented with digital signal processor.

F. Main Design Procedure

The equations presented in Section III-A–C are used to design the proposed converter. Specifications needed to begin the design are: input voltage $V_{\rm in}$, output voltage V_o, rated power P_o, and switching frequency f_s. The main design procedure is illustrated as follows.

1) Choosing the maximum duty cycle $D_{\max}$. The larger $D_{\max}$ means the smaller HF transformer ratio n and lower current stress. However, $D_{\max}$ is limited by the resetting time for the transformer magnetizing current. In this converter, $D_{\max}$ can be selected as large as possible because the clamping voltage V_{Ca} assists the transformer-reset operation.
2) From the specifications, choosing secondary transformer voltage v_s. v_s should be selected as low as possible to reduce the voltage stressed of secondary diodes. But v_s is relevant to transformer ratio n, effecting the value of $L_{\rm leak}$ and the loss duty cycle $D_{\rm loss}$. Therefore, for this reason, the initial value of v_s can be given by

$$v_s \geq V_o/D_{\max}. \tag{34}$$

3) Once v_s is selected, it is straightforward to calculate n.

TABLE II.
COMPARISON OF FIVE TOPOLOGIES

Comparison of primary side	Conventional PP converter	Basic phase-shift ZVS full-bridge converter	ZVS TTPP converter in [24]	ZVS active-clamped PP converter in [30]	Proposed ZVS active-clamped PP converter
Total components	Two power switches Q_1 and Q_2	Four power switches $Q_1 - Q_4$	Three power switches $Q_1 - Q_3$	Four power switches $Q_1 - Q4$ and 2 clamping capacitors C_{r1}, C_{r2}	Three power switches $Q_1 - Q_3$ and a clamping capacitor C_a
The maximum duty cycle	>0.5	>0.5	>0.5	<0.5	>0.5
Voltage stress	Q_1 and Q_2: $2V_{in}$	$Q_1 - Q_4$:V_{in}	Q_1 and Q_2: $2V_{in}$ Q_3:V_{in}	$Q_1 - Q_4$:V_{in} $+V_{Clamp} < 2V_{in}$	$Q_1 - Q_3$:$V_{in}+V_{Ca} < 2V_{in}$
Voltage-clamped	No	No	No	Yes	Yes
Switching features	Q_1 and Q_2 : Hardswitching	Leading-leg switches Q_1 and Q_2: ZVS turn-on in a wide load range Lagging-leg switches Q_3 and Q_4: ZVS turn-on hardly at light load	Q_1 and Q_2: ZVS turn-on in a wide load range Q_3: ZVS turn-on hardly at light load	$Q_1 - Q_4$: ZVS turn-on in a wide load range	$Q_1 - Q_3$: ZVS turn-on in a wide load range
Switching losses	High	Medium	Medium	Low	Low
Leakage inductor energy recovery	No	No	No	Yes	Yes

4) Select the ZVS range. From Fig. 8 and the minimum output current for realizing ZVS, the leakage inductor L_{leak} can be determined.
5) According to the specified input voltage and determined D, n, L_{leak}, similar with Fig. 7, verify if the voltage stresses of switches Q_1–Q_3 are below the rated voltage of the power devices. Otherwise, change the values of n and L_{leak}, and repeat steps 2–4.

IV. TOPOLOGIES COMPARISON

Since the proposed push–pull converter has soft-switching and voltage-clamped features, the conventional push–pull converter, the basic phase-shift ZVS full-bridge converter [32], the presented converter in [24] and [30] are selected for performance comparison because of the similarity in architectural structure, characteristics, and application. Table II summarizes the differences of these topologies, which have the same structure in the secondary side of the transformer.

By Table II, it is obvious that the proposed active-clamped ZVS push–pull converter has a good performance. Its maximum duty cycle is more than 0.5, which can increase the voltage gain and reduce the transformer ratio compared to the presented converter in [30]. Moreover, the voltage across the primary switches of the proposed topology is clamped at lower voltage only by adding a switch and a clamping capacitor. In addition, all of three switches can achieve ZVS in a wide load range and the leakage inductor energy can be recycled. Therefore, the efficiency of the proposed converter is higher than the previous similar converters.

V. EXPERIMENTAL VERIFICATION

In order to verify the effectiveness of the proposed ZVS push–pull converter, an 800 W experimental prototype was built and tested. Table III shows the specifications and key parameters. With the specifications and the main design procedure, the maximum duty cycle can be designed as 0.85, $v_s = 240$ V is determined from (34) and the HF transformer turns ratio $n = 4$ could be selected when $V_{in} = 60$ V. If the ZVS turn-on can be achieved for switch Q_3 with 10% load, the leakage inductance should be determined as 5.5 μH and it is noted in Fig. 8.

TABLE III.
KEY PARAMETERS AND COMPONENTS

Input voltage	60–80 V DC
Output voltage	200 V DC
Switching frequency (Q_3)	88 kHz
Output rated power	800 W
Primary switches: $Q_1 - Q_3$	IRPF260N, V_{DSS}= 200 V,I_D = 50 A,$R_{DS(on)}$= 0.04 Ω,C_{oss} = 370 pF
Secondary diodes: $D_4 - D_7$	MUR880E, V_R= 800 V,$I_{F(AV)}$ = 8.0A,I_{FM} = 16 A
HF transformer	ETD49/ N87 ($turnratio: N_{P1}:N_{P2}:N_s = 10:10:40$) Leakage inductance L_{leak-1} =L_{leak-2} = 5.5 μH
Clamping capacitor C_a	10 μF /200 V film capacitor
Output filter capacitor C_o	470 μF
Output filter inductor L_f	400 μH

It is noticed that the signals for switches $Q_1 - Q_3$ are generated by a *IC SG3525* with some analog circuits. The control loop adopts single PI voltage loop as shown in Fig. 9

The experimental prototype of the proposed converter was tested under various output power and input voltage conditions as shown in Figs. 10 and 11. Fig. 10 shows the results for $V_{in} = 60$ V, output rated power and Fig. 11 shows that for $V_{in} = 80$ V, 10% power conditions, respectively. It can be seen that experimental results match closely with theoretical waveforms as shown in Fig. 2.

Parts (a) of Figs. 10 and 11 show the switching sequence for primary power switches Q_1–Q_3 and the voltage across the secondary winding, and $v_s = 240$ V is the same with the design value. Parts (b) of Figs. 10 and 11 verify the relationship among clamping voltage V_{Ca}, input voltage and the duty cycle of Q_3 as shown in (16). We can clearly find that the voltage V_{Ca} has not a ring voltage and can keep a constant. The currents i_{p1}, i_{p2} in the primary side and i_s in the secondary side, depicted in parts (c) of Figs. 10 and 11, are also confirmed by the experimental results.

Parts (d) and (e) of Figs. 10 and 11 show the drain-to-source and gate-to-source waveforms across the primary switches,

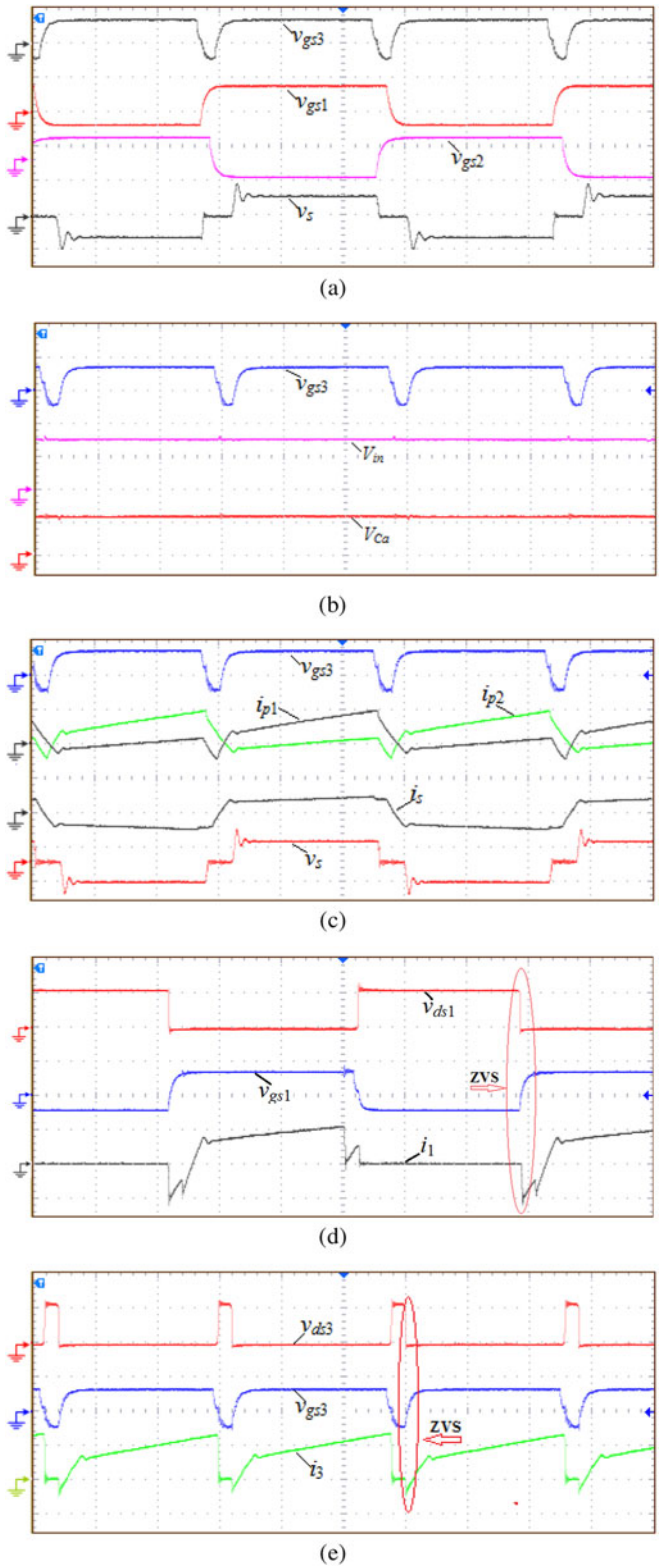

Fig. 10. Experimental waveforms at $V_{\rm in} = 60$ V and rated power (4 μs/div). (a) Primary switches voltages v_{gs1} (20 V/div), v_{gs2} (20 V/div),$v_{\rm gs3}$ (20 V/div) and secondary transformer voltage v_s (400 V/div). (b) Switch Q_3 voltage v_{gs3} (20 V/div), input voltage $V_{\rm in}$ (40 V/div) and clamping capacitor voltage V_{Ca} (40 V/div). (c) Switch Q_3 voltage v_{gs3} (20 V/div), primary current i_{p1}(20 A/div),$i_{\rm p2}$(20 A/div), secondary current i_s(10 A/div) and secondary transformer voltage v_s (400 V/div). (d) Switch Q_1 voltages v_{gs1} (20 V/div),$v_{\rm ds1}$ (100 V/div) and current i_1 (20 A/div). (e) Switch Q_3 voltages v_{gs3} (20 V/div),$v_{\rm ds3}$ (100 V/div) and current i_3 (20 A/div).

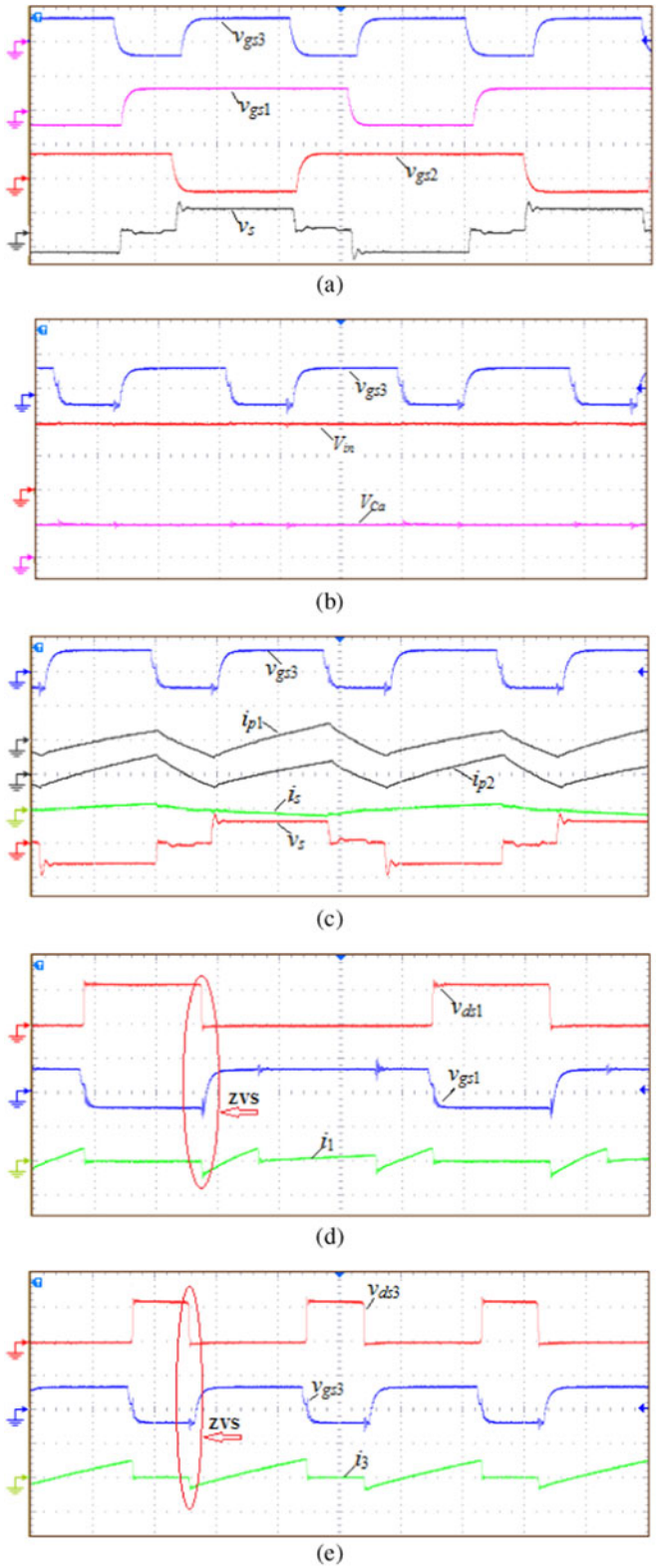

Fig. 11. Experimental waveforms at $V_{\rm in} = 80$ V and 10% rated power (4 μs/div). (a) Primary switches voltages v_{gs1} (20 Vn/div), v_{gs2} (20 V/div), v_{gs3} (20 V/div) and secondary transformer voltage v_s (400 V/div). (b) Switch Q_3 voltage v_{gs3} (20 V/div), input voltage $V_{\rm in}$ (40 V/div) and clamping capacitor voltage V_{Ca} (40 V/div). (c) Switch Q_3 voltage v_{gs3} (20 V/div), primary current i_{p1}(10 A/div), i_{p2} (10 A/div), secondary current i_s(5 A/div) and secondary transformer voltage v_s (400 V/div). (d) Switch Q_1 voltages v_{gs1} (20 V/div), v_{ds1} (100 V/div) and current i_1 (10 A/div). (e) Switch Q_3 voltages v_{gs3} (20 V/div), v_{ds3} (100 V/div) and current i_3 (10 A/div).

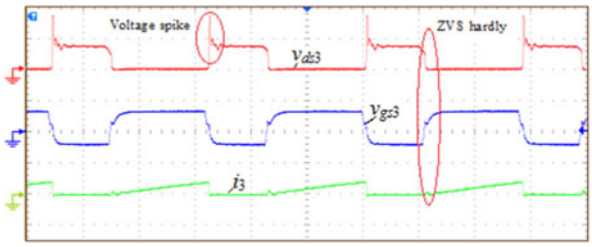

Fig. 12. Experimental waveforms of Q_3 from the converter in [24] under 80 W output power $(4\ \mu s/\mathrm{div})$:$\mathrm{v_{gs3}}$ $(20\ \mathrm{V/div})$, v_{ds3} $(100\ \mathrm{V/div})$ and current i_3 $(10\ \mathrm{A/div})$.

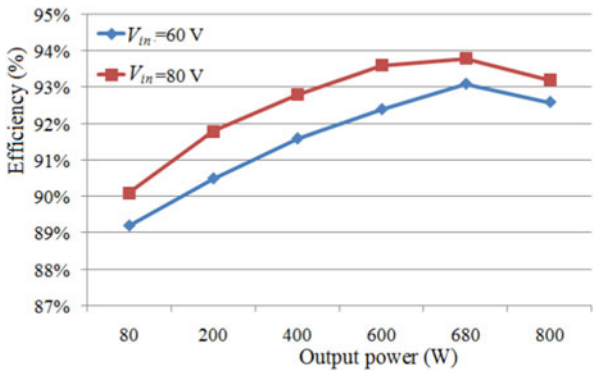

Fig. 13. Efficiency versus output power under different load condition of the proposed converter with $V_{\mathrm{in}} = 60\ \mathrm{V}$ and $\mathrm{V_{in}} = 80\ \mathrm{V}$.

and the currents waveform through devices $(Q_1$ and $Q_3)$. The switch Q_2 has the same situation with Q_1 as aforesaid. Obviously, switches Q_1 and Q_3 can achieve ZVS turn-on. Their body diodes conduct prior to switch conduction confirming ZVS conditions. Gate-driven signals $v_{gs1}\ (Q_1)\ v_{gs3}\ (Q_3)$ have been applied to switches when voltages across them v_{ds1} and $\mathrm{v_{ds3}}$, respectively, are zero already, either under the rated power or light power. In addition, parts (b), (d), and (e) of Figs. 10 and 11 illustrate that the voltage across switch $Q_1\ (Q_3)$ are clamped at near $V_{\mathrm{in}}+V_{\mathrm{ca}}$, low voltage stress and no spike at switch $Q_1\ (Q_3)$. Therefore, low on-state resistance can be adopted because of low clamped voltage across them, which result in lower conduction losses and higher frequency.

By comparison, the measured waveforms of Q_3 under light load from the converter in [24] without clamping circuit are presented in Fig. 12. When the body diode of Q_2 is conducting, the parasitic capacitor C_3 will continue to resonant with the two leakage inductors $L_{\mathrm{leak}-1}$ and $\mathrm{L_{leak-2}}$. This will lead to a relative high voltage spike across the switch Q_3, as shown in Fig. 12. Moreover, the switch Q_3 realizes ZVS hardly under light load due to lower energy stored in the leakage inductor. However, from parts (e) of Figs. 10 and 11, it can be observed that this voltage spike can be suppressed and the switch Q_3 can achieve ZVS easily with the proposed topology, which enabling the use of low-voltage, low-performance, and low-cost devices.

Fig. 13 shows the efficiency curves of the proposed converter with different output power at $V_{\mathrm{in}} = 60$ V and $V_{\mathrm{in}} = 80$ V. The efficiency can reach or exceed 93.1% for $V_{\mathrm{in}} = 60$ V and 93.8% for $V_{\mathrm{in}} = 80$ V.

Fig. 14 represents the comparative efficiency with respect to the proposed ZVS push–pull converter with active clamped and

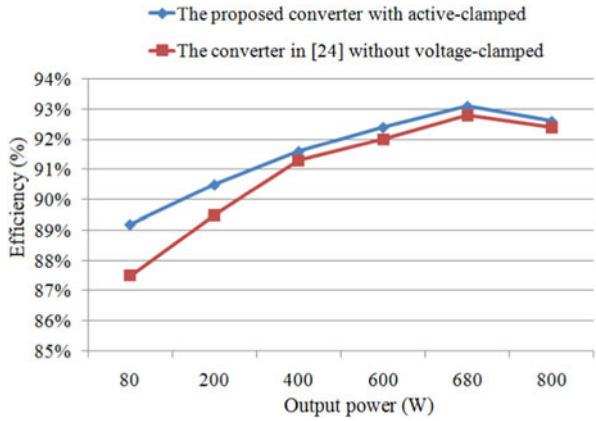

Fig. 14. Efficiency comparison with the converter in [24] and the proposed converter.

a similar converter in [24] without voltage clamped. It is shown that the converter efficiency using the active-clamped scheme in this paper under light load rises by more 1.5% than that in the converter in [24]. Moreover, the peak efficiency in [30] is just 91.3% because of the adding power losses caused by the clamped circuit.

VI. Summary and Conclusion

The conventional push–pull converter has a high switch-voltage stress and hard switching. To relieve this problem, a new ZVS push–pull converter with active clamped has been presented in this paper. One switch and a clamping capacitor are added on the primary side of HF transformer compared to the conventional push–pull converter. All of three switches can achieve ZVS turn-on in a wide load range, which is to reduce the switching losses and increase the transfer efficiency. The voltage across switch can be clamped at a lower level which is much less than those of a conventional push–pull converter that enabling the use of lower voltage, lower performance, and lower cost devices. Besides, the problems of flux imbalance existing in the conventional push–pull converter can be eliminated and the energy stored in the leakage inductor can be recycled. The operation modes and features of the proposed converter were discussed thoroughly in this paper. In addition, some previous topologies with similar characteristics have been listed to make a comparative study. Finally, the analysis and performance have also been validated on an 88 kHz, 800 W experimental prototype. As a result, the proposed converter has advantages of simple topology, high efficiency, high performance, and galvanic isolation. It can be used in the battery and supercapacitor source applications.

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