A Novel Nine-Level Inverter Employing One Voltage Source and Reduced Components as High-Frequency AC Power Source

Junfeng Liu, Jialei Wu, Jun Zeng, and Huafang Guo

***Abstract*—Increasing demands for power supplies have contributed to the population of high-frequency ac (HFAC) power distribution system (PDS), and in order to increase the power capacity, multilevel inverters (MLIs) frequently serving as the high-frequency (HF) source-stage have obtained a prominent development. Existing MLIs commonly use more than one voltage source or a great number of power devices to enlarge the level numbers, and HF modulation (HFM) methods are usually adopted to decrease the total harmonic distortion (THD). All of these have increased the complexity and decreased the efficiency for the conversion from dc to HF ac. In this paper, a nine-level inverter employing only one input source and fewer components is proposed for HFAC PDS. It makes full use of the conversion of series and parallel connections of one voltage source and two capacitors to realize nine output levels, thus lower THD can be obtained without HFM methods. The voltage stress on power devices is relatively relieved, which has broadened its range of applications as well. Moreover, the proposed nine-level inverter is equipped with the inherent self-voltage balancing ability, thus the modulation algorithm gets simplified. The circuit structure, modulation method, capacitor calculation, loss analysis, and performance comparisons are presented in this paper, and all the superior performances of the proposed nine-level inverter are verified by simulation and experimental prototypes with rated output power of 200 W. The accordance of theoretical analysis, simulation, and experimental results confirms the feasibility of proposed nine-level inverter.**

***Index Terms*—Nine-level inverter, one voltage source, self-voltage balancing, two capacitors.**

I. Introduction

With the increasing demands for power supplies in computer, telecom, electric vehicle, and other similar areas where low voltage and high current are needed, the traditional dc power distribution system (DC PDS) is gradually unable to meet the requirements due to its insufficiencies such as more conversion stages, low efficiency, and poor transient response. High-frequency ac power distribution system (HFAC PDS) proposed in [1] has become an alternative [2]–[5] because of its merits such as fewer conversion stages, higher efficiency, faster response, high power density, distributed heat profile, and potential for connector-less power transfer.

HFAC PDS is usually composed of two stages: a high-frequency (HF) multilevel inverter (MLI) or a resonant inverter as the source side and several ac/ac or ac/dc voltage-regulation modules as the load side. In order to raise the power capacity, one of the most popular methods of the source side is to connect multiple resonant inverters in series or in parallel [6], while the control for the HF synchronizations of both amplitudes and phases will become extremely complicated. In contrast, using a HF MLI as the power source is a preferable solution with larger power capacity and lower switch stress. In HFAC PDS as shown in Fig. 1, a HF MLI is employed to transform the dc voltage source from the batteries, fuel cells, or photovoltaic cells into a HF staircase output, and the more number of voltage levels is significant to decrease the total harmonic distortion (THD) and electromagnetic interference, thus simplifying the design of output filters. However, the level number is restricted by the complexity of the MLI. The output frequency of the HF inverter usually ranges from 400 Hz to 50 kHz [4], [7], [8]. As a result, the HF modulation (HFM) methods represented by multicarrier phase disposition [9] are no longer suitable, as the excessively high switching frequency and so-caused switching loss are unbearable for HF applications. In other words, the fundamental-frequency modulation (FFM) methods will have to be adopted in HF fields, and the further discussions are necessary to customize a HF MLI that can output sufficient number of voltage levels with a simplified structure to increase the efficiency and decrease the THD for HF applications.

Traditional MLIs include the neutral-point-clamped (NPC) inverter [10], flying capacitor (FC) inverter [11], and cascade H-bridge (CHB) inverter. The NPC and FC inverters, respectively, use diodes and capacitors to clamp the voltage levels, and more levels can be obtained by increasing the number of power devices. However, both the circuit configurations and their controls will become extremely complicated along with the increasing number of voltage levels. Additionally, the capacitors' imbalance is another problem needed to be solved. The CHB inverter increases the output voltage levels and simplifies the modulation by the combination of H-bridge cells.

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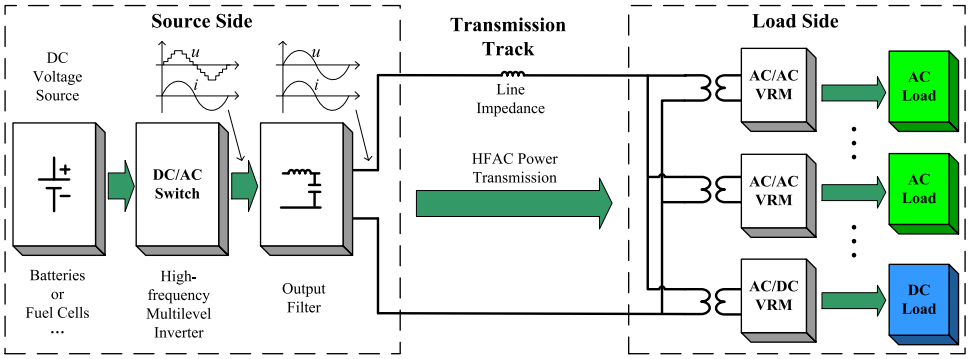

Fig. 1. Structure of HFAC PDS using a MLI as the source side.

However, the number of power devices and input dc sources multiplies when outputting more voltage levels. Several simplified topologies have been proposed in recent years to overcome the shortcomings of the traditional ones. However, they have the common disadvantage that symmetric or asymmetric dc inputs are needed [12]–[17]. A single phase grid-connected inverter was proposed in [18]. However, the limited five output levels will lead to more output harmonics. A seven-level pulse width modulation inverter was proposed in [19], in which three capacitors are connected in series and then paralleled with the dc source to obtain extra $\pm 1/3V_{\rm dc}$ and $\pm 2/3V_{\rm dc}$ voltage levels. However, the capacitor voltages are in unbalancing conditions, thus increasing the control complexity. Meanwhile, both topologies in [18] and [19] adopt the multicarrier modulation method to decrease the THD of the staircase outputs. The high switching frequency makes them unsuitable for HFAC PDS. A grid-connected converter topology was proposed with only one voltage source, a FC and eight switches [20]. It can output nine levels exactly when the HFM strategy keeps the capacitor voltage at a desired level such as $1/3V_{\rm dc}$, which is indeed difficult to be realized without any auxiliary charging circuit, and the literature [20] merely presents the experimental results from a seven-level prototype. Moreover, the HFM has limited the proposed topology to low-frequency (LF) occasions only. A series of step-up multilevel topologies was proposed based on switched-capacitor (SC) techniques [21]–[24]. They can be used as HF power sources. However, more dc sources or more components are required to accomplish higher number of output voltage levels. The power switches in the backend H-bridges bear the sharply cumulative voltage levels from the SC frontends, and the extremely high-voltage stress has limited their applicability to low-input occasions only.

In this paper, a nine-level inverter employing one voltage source and two capacitors is proposed for HFAC PDS. Compared with the aforementioned topologies, the proposed inverter has more voltage levels with fewer components. Lower THD of output voltage is obtained and the voltage stress on the power switches in the backstage is relatively relieved. More importantly, the inherent self-voltage balancing ability of the two capacitors has simplified the modulation algorithm. The rest of this paper is organized as follows. Detailed configurations and operational principles of the proposed nine-level inverter are presented in Section II. Section III gives the capacitor calculation and loss analysis, and Section IV demonstrates the comparisons with existing typical MLIs. The performance evaluations including simulation and experimental results are presented in Section V, followed by concluding remarks.

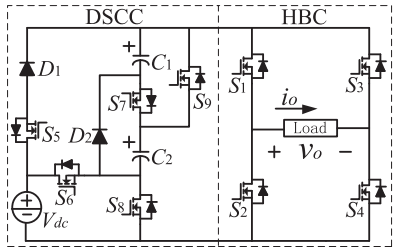

Fig. 2. Circuit of proposed nine-level inverter.

II. Proposed Nine-Level Inverter

A. Circuit Topology

Fig. 2 shows the proposed nine-level inverter, which consists of two stages. The circuit in the frontend is a developed SC circuit (DSCC), which is different from the basic SC cells in [21]–[24] in that it can output more voltage levels with relatively fewer components. An H-bridge circuit (HBC) is used in the backend to change the polarity of the frontend output. In ideal circumstance, the proposed inverter has nine output voltage levels: $\pm 2V_{\rm dc}$, $\pm 3V_{\rm dc}/2$, $\pm V_{\rm dc}$, $\pm V_{\rm dc}/2$ and 0, and to achieve this goal, only one dc voltage source, two capacitors, two diodes, and nine power switches are needed.

B. Description of Each Voltage Level

For the proposed nine-level inverter, switching patterns are listed in Table I, including the states of the diodes and capacitors, and to have a quick and better understanding, current paths in the positive half cycle are demonstrated in Fig. 3(a)–(e) for each case, respectively. Previously, assumptions have been given: all the power devices are ideal, whose on-state resistances and forward voltage drops are considered as zero; the two capacitors have the same capacitance that is large enough; the load is a pure resistor; the proposed inverter has already entered steady states.

TABLE I
SWITCHING PATTERNS AND STATES OF THE DIODES AND CAPACITORS AT EACH VOLTAGE LEVEL

	Switches in HBC				Switches in DSCC					Diodes		Capacitors	
Voltage levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	D_1	D_2	C_1	C_2
$2\,V_{\rm dc}$	1	0	0	1	1	1	1	0	0	0	0	D	D
$3\,V_{\rm dc}/2$	1	0	0	1	1	1	0	0	1	0	1	D	D
$V_{\rm dc}$	1	0	0	1	1	0	0	1	0	1	0	C	C
$V_{\rm dc}/2$	1	0	0	1	0	0	0	1	1	0	1	D	D
0	0	1	0	1	0	0	0	1	1	0	0	–	–
$-V_{\rm dc}/2$	0	1	1	0	0	0	0	1	1	0	1	D	D
$-V_{\rm dc}$	0	1	1	0	1	0	0	1	0	1	0	C	C
$-3V_{\rm dc}/2$	0	1	1	0	1	1	0	0	1	0	1	D	D
$-2V_{\rm dc}$	0	1	1	0	1	1	1	0	0	0	0	D	D

Here, symbols of 1 or 0 in the switches column indicate that the switches are turned ON or turned OFF; symbols of 1 or 0 in the diodes column indicate that the diodes are forward passed or reverse biased; symbols of C, D, or – in the capacitors column indicate that the capacitors are charged, discharged, or unchanged, respectively.

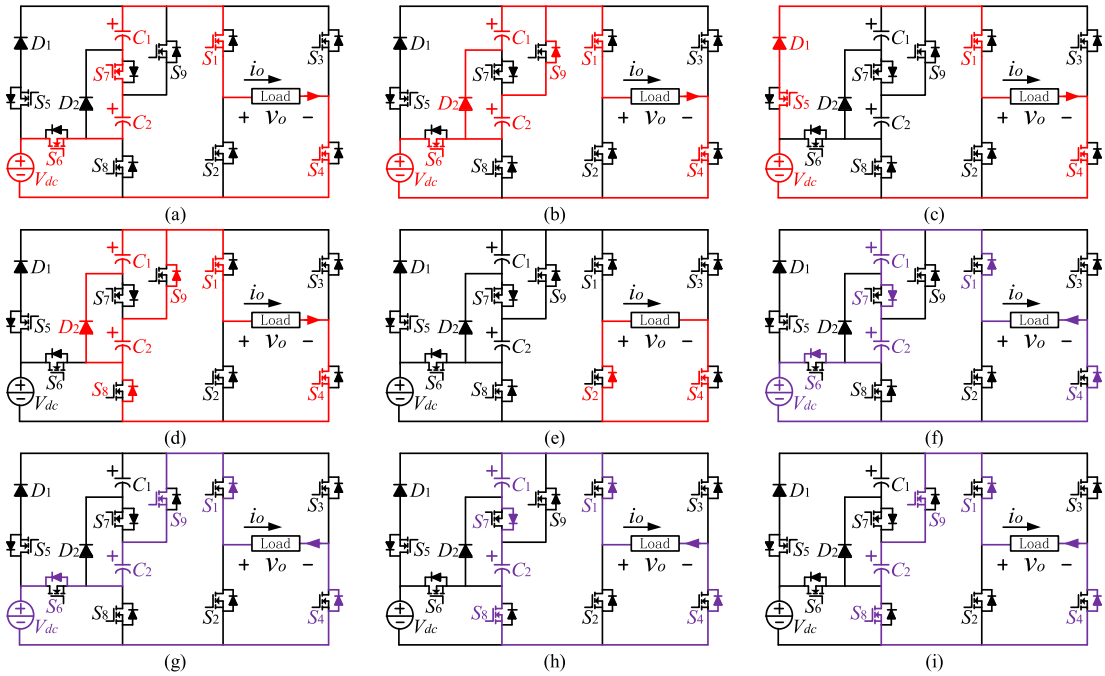

Fig. 3. Current paths for different output voltage levels. (a) Forward current path at level $2V_{\rm dc}$. (b) Forward current path at level $3V_{\rm dc}/2$. (c) Forward current path at level $V_{\rm dc}$. (d) Forward current path at level $V_{\rm dc}/2$. (e) Forward current path at level 0. (f) Reverse current path at level $2V_{\rm dc}$. (g) Reverse current path at level $3V_{\rm dc}/2$. (h) Reverse current path at level $V_{\rm dc}$. (i) Reverse current path at level $V_{\rm dc}/2$.

From Table I and Fig. 3(a)–(e), the two capacitors are charged and discharged in series at levels $\pm V_{\rm dc}$ and $\pm 2V_{\rm dc}$, respectively, and in these intervals, they share the same charging or discharging currents. At levels $\pm V_{\rm dc}/2$ and $\pm 3V_{\rm dc}/2$, the two capacitors are connected in parallel. As a result, the voltages on them get balanced. At level 0, the two capacitors' voltages remain unchanged. Overall, the proposed nine-level inverter is equipped with the self-voltage balancing ability, thus simplifying the driving circuits and modulation algorithms [25], [26]. When the load is inductive, the current will flow in the opposite direction, and Fig. 3(f)–(i) show the reverse current paths for each voltage level in the positive half cycle. It can be found that the output voltage levels remain the same regardless of the directions of the load current. In other words, the proposed topology can be used as an independent inverter.

C. Modulation Analysis

Fig. 4 shows the operational principles of proposed inverter. The nine-level staircase output can be synthesized by four quasi-square waves $v_{\rm oi}(i = 1, 2, 3, 4)$, whose amplitudes and conducting angles are $\pm V_{\rm dc}/2$ and θ_i, respectively. Obviously, the angles should satisfy

$$0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \theta_5 = 90^\circ. \tag{1}$$

The Fourier decomposition of each quasi-square waveform is

$$v_{\rm oi} = \frac{2V_{\rm dc}}{\pi} \sum_{k=1,3,\ldots}^{\infty} \frac{\cos(k\theta_i)}{k} \times \sin k\omega t \tag{2}$$

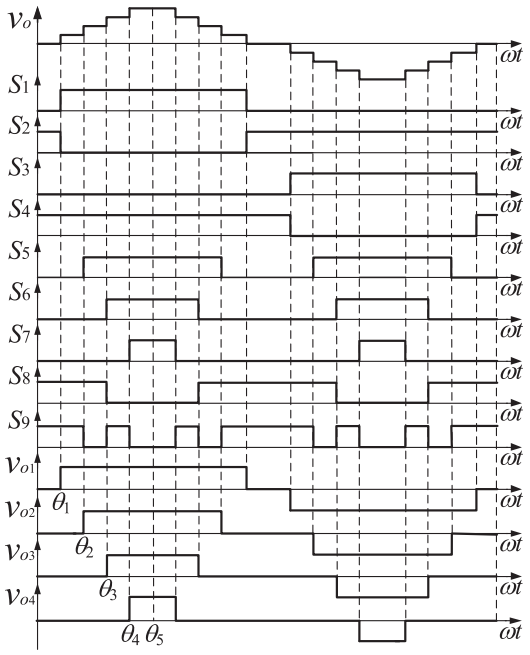

Fig. 4. Operational principles of proposed nine-level inverter.

where ω is the angular frequency of the staircase output. Thus, the Fourier decomposition of the output voltage is

$$v_o = \frac{2V_{\rm dc}}{\pi} \sum_{k=1,3\ldots}^{\infty} \sum_{i=1}^{4} \frac{\cos(k\theta_i)}{k} \times \sin k\omega t. \tag{3}$$

From (3), the fundamental component of the staircase output is

$$v_{\rm of} = \frac{2V_{\rm dc}}{\pi} \sum_{i=1}^{4} \cos(\theta_i) \times \sin \omega t. \tag{4}$$

Therefore, the amplitude modulation index of the fundamental waveform $M_{\rm of}$ and the THD of the proposed nine-level inverter can be expressed as

$$M_{\rm of} = \frac{1}{4} \sum_{i=1}^{4} \cos(\theta_i) \tag{5}$$

$$\mathrm{THD} = \frac{\sqrt{\sum_{k=3,5\ldots}^{\infty} \left[\sum_{i=1}^{4} \frac{\cos(k\theta_i)}{k}\right]^2}}{\sum_{k=1}^{4} \cos(\theta_k)} \times 100\%. \tag{6}$$

When the selected harmonic elimination method is adopted to modulate the proposed nine-level inverter, the 5th, 7th, and 11th harmonics can be selected to be eliminated. Thus, the conducting angles $\theta_{\rm i}$ ($i = 1, 2, 3, 4$) can be calculated by

$$\begin{cases} \cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) = 4M_{\rm of} \\ \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) = 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) = 0 \\ \cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) = 0 \end{cases}. \tag{7}$$

When the amplitude modulation index $M_{\rm of}$ is set to 0.8, the conducting angles θ_i can be then obtained as

$$\begin{cases} \theta_1 = 9.84^\circ & \theta_2 = 20.37^\circ \\ \theta_3 = 40.05^\circ & \theta_4 = 60.42^\circ \end{cases}. \tag{8}$$

Combining (8) with Fig. 4, the conducting angles of the driving signals for switches S_1–S_9 can further be determined, and according to (6) and (8), the theoretical THD of the proposed HF inverter can be obtained as 3.13%.

III. Capacitor Calculation and Loss Analysis

A. Capacitor Calculation and Ripple Loss Analysis

When the two capacitors in proposed nine-level inverter discharge to supply the load separately or in series with the voltage source, voltage ripples will appear on them, which should be limited to no more than 10% of the capacitors' own maximum voltages [22]. The range of the voltage fluctuation for a capacitor is determined by its capacitance and discharging period, and is also related to the load type. It can be found from Table I and Fig. 4 that both capacitors in the proposed MLI have the same maximum continuous discharging period in the interval from θ_3 to π-θ_3 in the positive half cycle when continuously outputting voltage levels $3V_{\rm dc}/2$ and $2V_{\rm dc}$, and the same largest discharging gap also occurs in the negative half cycle when generating voltage levels $-3V_{\rm dc}/2$ and $-2V_{\rm dc}$ continuously. From the connection relations of the two capacitors and the current paths shown in Fig. 3, the two capacitors have the same discharging currents, which are $i_o/2$ and $i_{\rm o}$ at levels $\pm 3V_{\rm dc}/2$ and $\pm 2V_{\rm dc}$, respectively. Thus, the continuous discharging amount of each capacitor during θ_3–π-θ_3 is

$$\Delta Q = \int_{\theta_3}^{\theta_4} \frac{i_o}{2\omega} d\omega t + \int_{\theta_4}^{\pi-\theta_4} \frac{i_o}{\omega} d\omega t + \int_{\pi-\theta_4}^{\pi-\theta_3} \frac{i_o}{2\omega} d\omega t. \tag{9}$$

Obviously, the largest discharging amount and the so-caused maximum voltage ripple for each capacitor are obtained under condition of pure resistive load, as the peak of the load current aligns with the midpoint of the discharging period, and once the capacitance is determined under pure resistive condition, voltage ripple on the capacitor will be smaller when supplying an inductive load. When the load is a pure resistor, the load current is also a staircase waveform. Thus, ΔQ can be further calculated by

$$\Delta Q = \frac{V_{\rm dc}}{4\pi f_o R_o} (4\pi - 3\theta_3 - 5\theta_4) \tag{10}$$

where f_o is the frequency of the staircase output and R_o is the load resistance. The voltage ripple on each capacitor can be then calculated by

$$\Delta V = \frac{V_{\rm dc}}{4\pi f_o R_o C} (4\pi - 3\theta_3 - 5\theta_4) \tag{11}$$

where C is the capacitance of each capacitor. Finally, taking the allowable voltage ripple $\Delta U_{\rm ripple}$ into consideration, the minimum capacitance should meet the following formula:

$$C_{\min} = \frac{V_{\rm dc}}{4\pi f_o R_o \Delta U_{\rm ripple}} (4\pi - 3\theta_3 - 5\theta_4). \tag{12}$$

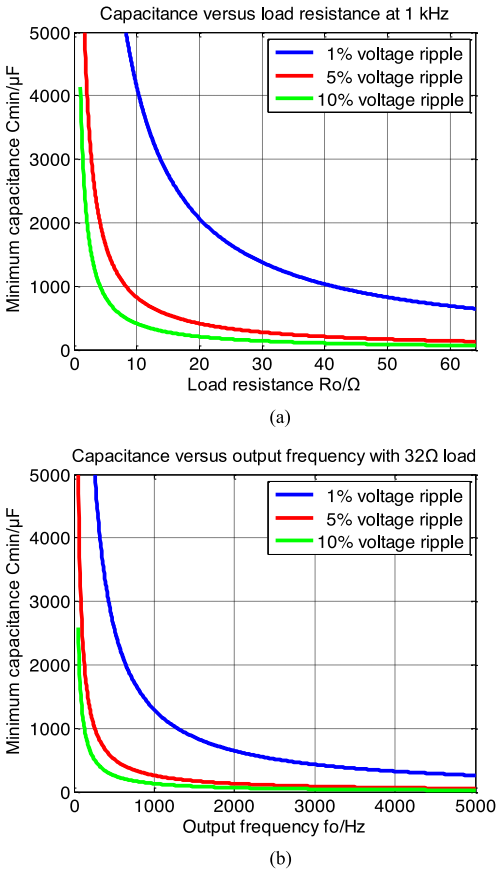

Fig. 5. Curves of minimum capacitance versus load resistance and output frequency. (a) Curves of minimum capacitance versus load resistance at frequency 1 kHz. (b) Curves of minimum capacitance versus output frequency with rated load resistance of 32 Ω.

Fig. 5 shows the curves of minimum capacitance versus the load resistance and output frequency. It can be found that the capacitance should be enlarged with the increasing of rated output power to keep the voltage ripple within an allowable range, and the higher frequency is capable of decreasing the capacitance.

Another smaller continuous discharging interval in half cycle is from $-\theta_2$ to θ_2 when continuously outputting voltage levels $\pm V_{\rm dc}/2$ and 0, and the discharging currents are $i_o/2$ and 0, respectively. Similarly, the smaller voltage ripple can be calculated by

$$\Delta V' = \frac{V_{\rm dc}}{2\pi f_o R_o C}\left(\theta_2 - \theta_1\right). \tag{13}$$

Consequently, the ripple loss can be expressed by

$$P_{\rm rip} = f_o C(\Delta V^2 + \Delta V'^2). \tag{14}$$

B. Conducting Loss Analysis

Conducting loss is caused by the parasitic parameters including the on-state resistances of switches and the forward voltage drops of diodes along the current loops in practical circuits. Fig. 6 shows the equivalent current path, where $V_{\rm eq}, V_{\rm Deq}, r_{\rm eq}$, and R_o are the output voltage, the equivalent voltage drop over diodes, the equivalent parasitic resistance, and the load resistance, respectively. For simplicity, all the diodes including the body diodes of switches are assumed to have the same voltage drop V_D and internal resistance r_D; all the switches are assumed to have the same on-state resistance r_S. Therefore, from the analysis in Section II, the equivalent parameters under pure resistive condition can be expressed as

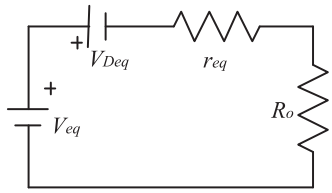

Fig. 6. Equivalent current path.

$$V_{\rm eq} = \begin{cases} 0 & i=0 \\ \frac{V_{\rm dc}}{2} & i=1 \\ V_{\rm dc} & i=2 \\ \frac{3V_{\rm dc}}{2} & i=3 \\ 2V_{\rm dc} & i=4 \end{cases} \tag{15}$$

$$V_{\rm Deq} = \begin{cases} V_D & i=0,2,3 \\ 2V_D & i=1 \\ 0 & i=4 \end{cases} \tag{16}$$

$$r_{\rm eq} = \begin{cases} r_D + r_S & i=0 \\ \frac{3r_D + {\rm ESR}c}{2} + 2r_S & i=1 \\ r_D + 3r_S & i=2 \\ \frac{r_D + {\rm ESR}c}{2} + 3r_S & i=3 \\ 2{\rm ESR}c + 4r_S & i=4 \end{cases} \tag{17}$$

where ESRc is equivalent series resistance of each capacitor, and the variable i can be obtained by

$$i = \left|\frac{2v_o}{V_{\rm dc}}\right|. \tag{18}$$

From Figs. 4 and 6, the average conducting loss can be calculated by

$$P_{\rm con} = \frac{2}{\pi}\sum_{i=1}^{4}\left\{\left(\frac{V_{\rm eq} - V_{\rm Deq}}{r_{\rm eq} + R_o}\right)^2 \times r_{\rm eq} \times (\theta_{i+1} - \theta_i)\right\}. \tag{19}$$

Considering the fact that the ESRc of an electrolytic capacitor is inversely proportional to its capacitance, increasing the capacitor's capacitance can not only decrease its voltage ripple and so-caused ripple loss, but also cut down the conducting loss by reducing the parasitic ESRc. However, compromises should always be made between the capacitance and its investment cost.

C. Switching Loss Analysis

Switching loss of a switch is caused by the overlaps of its voltage and current when it changes its states, and it can be estimated from the charging and discharging processes of the

TABLE II
DETAILED OPERATIONAL PARAMETERS OF EACH SWITCH

	Switches in HBC	Switches in DSCC				
Parameters	S_1–S_4	S_5	S_6	S_7	S_8	S_9
f_s	f_o	$2f_o$	$2f_o$	$2f_o$	$2f_o$	$6f_o$
V_b	$2V_{\rm dc}$	$V_{\rm dc}/2$	$V_{\rm dc}$	$V_{\rm dc}/2$	$V_{\rm dc}$	$V_{\rm dc}/2$

parasitic capacitance between the drain and the source [24] by

$$P_{\rm switch} = f_s C_{\rm ds} V_b^2 \tag{20}$$

where $f_s, C_{\rm ds}$, and V_b are the switching frequency, the parasitic capacitance, and the maximum block voltage of each switch, respectively. The values of these parameters in the proposed nine-level inverter are listed in Table II. Thus, the switching loss can be calculated by

$$P_{\rm switch} = \frac{45 f_0 C_{\rm ds} V_{\rm dc}^2}{2}. \tag{21}$$

Overall, the theoretical efficiency can be obtained by

$$\eta = \frac{P_o}{P_{\rm rip} + P_{\rm con} + P_{\rm sw} + P_o} \tag{22}$$

where $P_{\rm o}$ is the rate output power of proposed inverter.

IV. COMPARISONS WITH EXISTING TOPOLOGIES

A. Comparisons With LF Topologies Proposed in [18]–[20]

The LF inverters in [18]–[20] all use only one voltage source. However, the topology in [18] only has five output levels and the topology in [19] only has seven levels. The topology in [20] can output nine levels exactly when the redundant switch configurations are utilized to keep the voltage over the FC at a desired level, which is actually difficult to be realized, from the experimental results presented by [20]. The lowest THD of the three topologies can only reach 4% [18], although the multicarrier modulation is used to regulate the magnitudes and decrease the THD values of their outputs. More seriously, in multicarrier modulation, the operating frequencies of switching devices are close to the carrier frequency that is dozen times of the output frequency, making modulation methods of this kind inappropriate for HF applications. In this paper, the lower THD of 3.13% can be accomplished by the proposed nine-level inverter merely with a FFM method, thus the switching loss that is proportional to switching frequency is declined sharply. Additionally, the topologies in [18] and [19] need extra control algorithms to maintain the complete balance of series-connected capacitors, which is avoided by the inherent advantage of self-voltage balancing in the proposed MLI. Consequently, the proposed topology contributes to lower THD, higher efficiency, easier control than the topologies in [18]–[20] for HF applications.

B. Comparisons With SC Topologies Proposed in [21]–[24]

All the topologies in [21]–[24] are based on SC techniques and can output any voltage level with the increase of component numbers. However, compromises should always be made between the level numbers and investment costs, and a MLI with nine output levels is completely able to meet the requirements for industrial applications. Therefore, the proposed inverter is further compared with the topologies proposed in [21]–[24] in the number of power devices and their peak inverse voltages (PIVs) when all of them have the same staircase output of nine levels. The comparison results are listed in Table III.

TABLE III
PARAMETER COMPARISONS WITH THE TOPOLOGIES IN [21]–[24]

Parameters	Proposed inverter	Inverter in [21]	Inverter in [22]	Inverter in [23]	Inverter in [24]
$N_{\rm source}$	1	1	2	1	1
$N_{\rm cap}$	2	3	2	3	3
$N_{\rm switch}$	9	13	12	10	8
$N_{\rm diode}$	2	0	2	3	6
PIV	$2V_{\rm dc}$	$4V_{\rm dc}$	$2V_{\rm dc}$	$4V_{\rm dc}$	$4V_{\rm dc}$

Here, $N_{\rm source}, N_{\rm cap}, N_{\rm switch}$, and $\rm N_{diode}$ are the numbers of voltage sources, electrolytic capacitors, switches, and diodes, respectively.

TABLE IV
SIMULATION PARAMETERS OF PROPOSED NINE-LEVEL INVERTER

Modes	Names	Values
Component parameters	Froward voltage drop of diodes (V_D)	0.3 V
	On-state resistance of switches ($R_{\rm on}$)	4.8 mΩ
	Capacitance of capacitors	1000 uF
Circuit parameters	Input dc source ($V_{\rm dc}$)	60 V
	Output frequency (f_o)	1 kHz
	Load impedance (Z_L)	32 Ω

It can be observed from Table III that the proposed nine-level inverter needs only one voltage source and the fewest components, which means less installation space and higher conversion efficiency. The PIV of the proposed inverter is merely half of those in single-input-source topologies proposed in [21], [23] and [24], which has broadened its application range. It is notable that the topology in [24] is unable to supply inductive loads, although it needs eight switches only, and to address this deficiency, at least ten switches are needed. In other words, the proposed MLI also has the greatest advantage in terms of the switch number.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

Power simulation (PSIM) simulation is conducted to verify the performance of the proposed nine-level inverter, and the detailed simulation parameters are shown in Table IV. The output frequency is set to 1 kHz, which is the optimized frequency for HFAC micro-grids [4].

Fig. 7 demonstrates the simulation waveforms of driving signals, and Fig. 8 shows the simulation waveforms of output voltages and load currents when supplying different types of loads. In Fig. 8(a), the load is a 32 Ω pure resistor, thus the output voltage and current have the same phase, and their rms values are

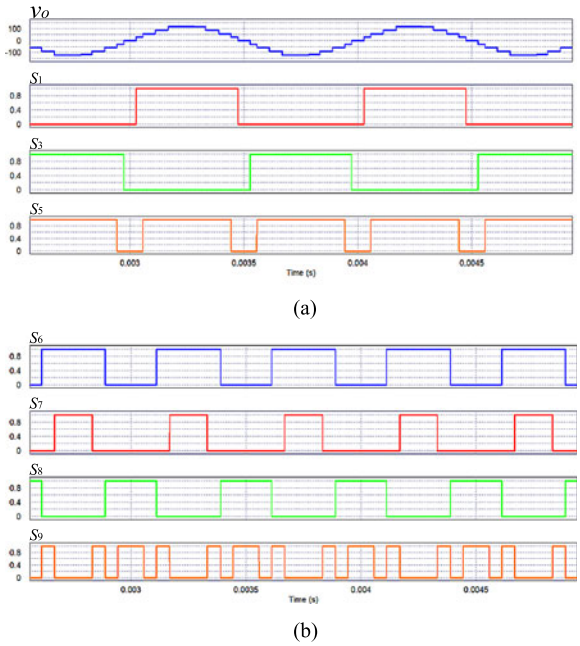

Fig. 7. Simulation waveforms of driving signals.

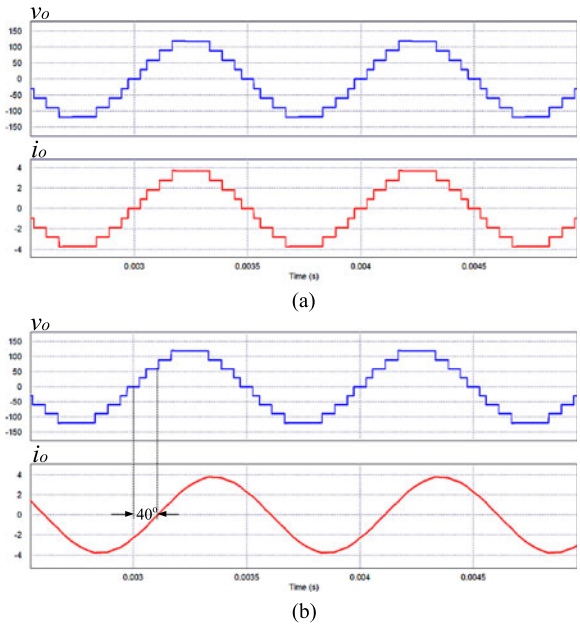

Fig. 8. Simulation waveforms of output voltages and currents under different load-types. (a) $R_o = 32\,\Omega$. (b) $Z_L = 24 + j20\,\Omega (R_o = 24\,\Omega, L_o = 3.2\,\text{mH}, |Z_L| = 31.2\,\Omega, \phi = 40°)$.

85.17 V and 2.66 A, respectively. Nevertheless, in Fig. 8(b), the load is a series-connected *RL* load ($R_o = 24\,\Omega, L_o = 3.2\,\text{mH}$), thus the current lags behind the voltage with an angle of 40°, which is the impedance angle of the inductive load.

Simulation waveforms of capacitors' voltages are shown in Fig. 9. The voltage on capacitor C_1 varies from 29.08 to 29.84 V, and it varies from 28.78 to 29.54 V on capacitor C_2. The difference can be neglected, thus the two capacitors are self-balanced without any complicated balancing circuit or algorithm. Lastly, the frequency spectrum of the staircase output voltage is demonstrated in Fig. 10. It can be observed that odd-order harmonics are decayed many times compared with the fundamental component, whose frequency is the same as the output voltage. In other words, the low THD is obtained by the proposed nine-level inverter with fewer components.

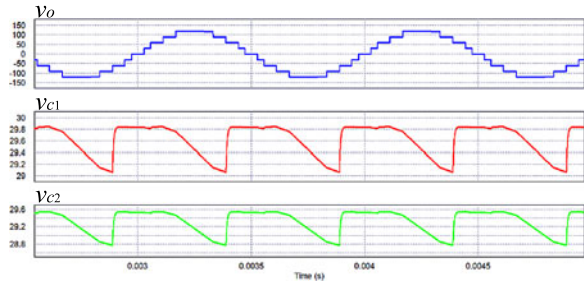

Fig. 9. Simulation waveforms of the staircase output and capacitors' voltages.

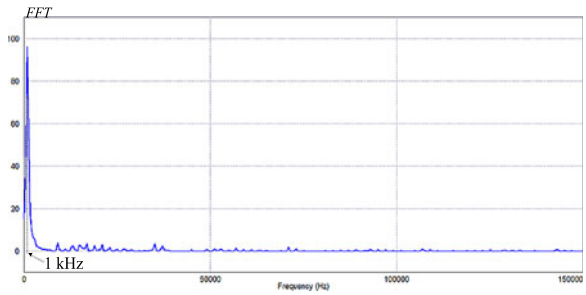

Fig. 10. Simulation waveform of frequency spectrum at fundamental frequency of 1 kHz.

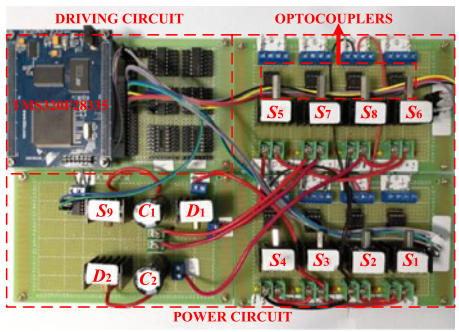

Fig. 11. Experimental prototype of proposed nine-level inverter.

B. Experimental Results

To further verify the feasibility of proposed HF inverter, an experimental prototype is implemented as shown in Fig. 11. The circuit parameters are set the same as those listed in Table IV and the specifications of the used devices are tabulated as Table V.

Fig. 12 shows the observed waveforms of the output voltage and load current under the pure resistive condition, and their rms values are 83.3 V and 2.63 A, respectively. Little difference exists when compared with the simulation results due to the parameter tolerance. Considering the digital displays on the input

TABLE V
COMPONENTS OF THE EXPERIMENTAL PROTOTYPE

Devices	Modes
Switches S_1–S_4	IRFP250
Switches S_5–S_9	IRFP4568
Capacitors C_1 and C_2	1000 μF/ 250 V
Diodes D_1 and D_2	MBR20200CTG
Controller	TMS320F28335
Optocouplers	A3140

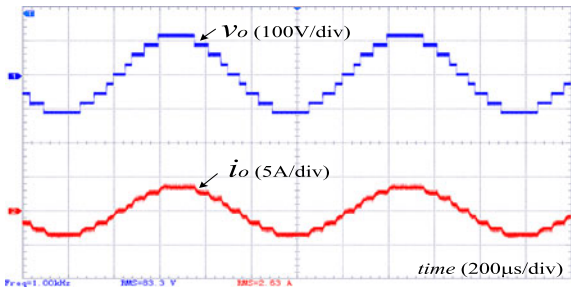

Fig. 12. Experimental results of the output voltage and load current with a pure resistor.

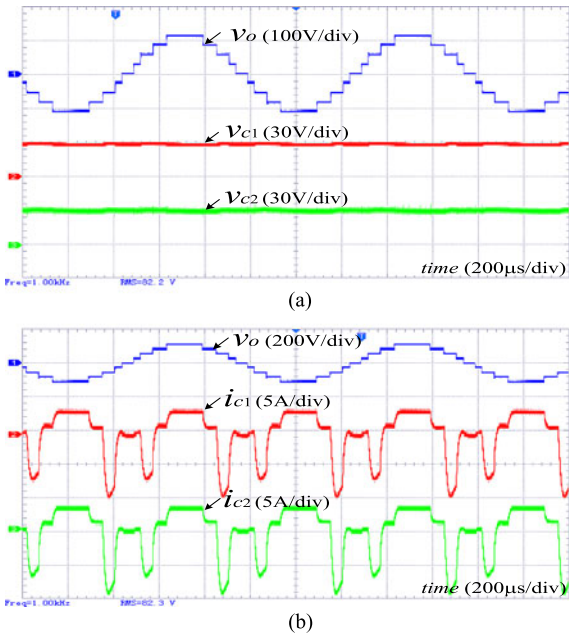

Fig. 13. Experimental results of the two capacitors' voltages and currents.

dc power supply, the transmission efficiency of the designed prototype is 94.18%, which is a little less than the theoretical efficiency 95.23% calculated by (22). Fig. 13 shows the experimental results of the two capacitors' voltages and currents. It can be found that the two capacitors have the same variation trajectories in both voltage and current. The accordance with the theoretical analysis in Section II-B and the simulation results in Fig. 9 proves the merit of self-voltage balancing in the proposed HF inverter once more. In Fig. 13(b), current spikes appear when the series-connected capacitors are paralleled with the voltage source to be charged. Their peak values are proportional to the

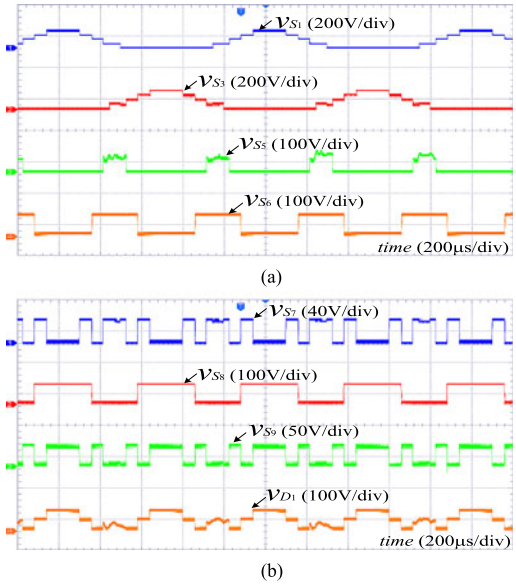

Fig. 14. Experimental results of the voltages on switches.

capacitors' voltage ripples, which can be reduced by increasing the capacitance or working frequency of the proposed inverter, as shown in Fig. 5.

Fig. 14 shows the experimental waveforms of the voltages over switches. The maximum PIV is approximately 120 V, which is twice the voltage of the input dc source. The less voltage stress indicates that the proposed inverter has larger application range than the topologies listed in Table III.

Overall, the proposed HF inverter can output nine levels using only one voltage source and fewer components. The staircase output has less harmonics, although FFM method is adopted, thus the switching loss is decreased greatly. Moreover, the proposed inverter with two capacitors is equipped with the self-voltage balancing ability, which simplifies the control algorithms. Consequently, the proposed nine-level inverter is a better choice of HFAC power source.

VI. CONCLUSION

In this paper, a novel nine-level inverter is proposed for HFAC PDS. Compared with the existing topologies, the proposed topology can achieve nine-level staircase output with only one voltage source, fewer power devices and relatively less voltage stress. All these have enlarged its application scopes. Voltage balance problem is avoided by the inherent self-voltage balancing ability, which has simplified the modulation circuits or algorithms, and the lower THD of 3.13% is realized without using HFM methods. As a result, the switching loss is significantly reduced. The capacitor calculation and power loss analysis are conducted in this paper, and the comparisons with existing topologies further testify the superiority of the proposed HF inverter. All the merits and the feasibility of the proposed topology are evaluated by a simulation model and an experimental prototype with rate power of 200 W, and their results illustrate that the proposed inverter is a preferable topology to implement HF power source for HFAC PDS.

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