A Family of Ripple Estimation–Cancellation Methods Based on Switched-Resistor Circuits and Their Application in Fast-Response PFC Preregulator

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***Abstract*—Power-factor-correction (PFC) preregulator commonly suffers from slow dynamic response due to the need to operate with small closed-loop bandwidth for realizing low total harmonic distortion of input current. Ripple cancellation is one of the widely adopted strategies to achieve high power factor and fast dynamic response simultaneously. The main idea is to eliminate the double-line frequency component in the sampled output voltage by means of subtracting a replica of the output voltage ripple from the sampled output voltage. In this paper, a systematic derivation and analysis of the main figures of merit of PFC preregulator incorporating ripple cancellation is presented. Based on the equations obtained, three variants of a family of ripple cancellation methods based on switched-resistor circuits are proposed. The performances of these methods are experimentally investigated and compared by implementing them in a 200-W average-current-mode-controlled boost PFC preregulator. By comparing the measured figures of merit, it is shown that near-perfect ripple cancellation is achievable when the amplitude and phase angle of the sampled output voltage ripple are estimated independently, whereas a more cost-effective solution is provided by another approach that tracks the ripple amplitude only at the expense of decreased power factor and increased total harmonic distortion.**

***Index Terms*—Fast response, low-frequency ripple, power factor correction (PFC), ripple estimation/cancellation, unity power factor.**

I. Introduction

POWER-FACTOR-CORRECTION (PFC) preregulators have been commonly used for converting ac power into dc power for mains-connected dc loads. They also serve the need to limit the level of harmonic current injected into the mains power line, as specified in international standards such as EN 61000-3-2 [1] and IEEE STD 519-1992 [2]. For medium-to-high power applications, boost PFC preregulator with average current mode (ACM) control is particularly attractive as it offers a direct control of PFC preregulator's input current and gives rise to low total harmonic distortion (THD) of input current and low conduction loss. The configuration of a boost PFC preregulator with ACM control is shown in Fig. 1. Generally, the bandwidth of the inner current control loop is configured to be large, which causes the inductor current to closely track the reference signal $i_{\text{ref}}(t)$ that results from the multiplication of the sampled rectified input voltage $K_m\,|v_{\text{in}}(t)|$ by the output signal of the voltage error amplifier $v_{\text{vea}}(t)$. For the outer voltage control loop, it is responsible for regulating the PFC preregulator's output voltage by comparing the sampled output voltage $\beta v_o(t)$ to the reference voltage V_{ref}, and the resulting error voltage is amplified by the voltage error amplifier. In practice, the bandwidth of voltage error amplifier is usually designed to be small in order to provide a sufficient attenuation of the double-line frequency component that is present in the output voltage of PFC preregulator [3], [4]. Although this configuration leads to unity power factor (PF) and input current with very low THD, the small bandwidth being employed also gives rise to poor dynamic response of PFC preregulator.

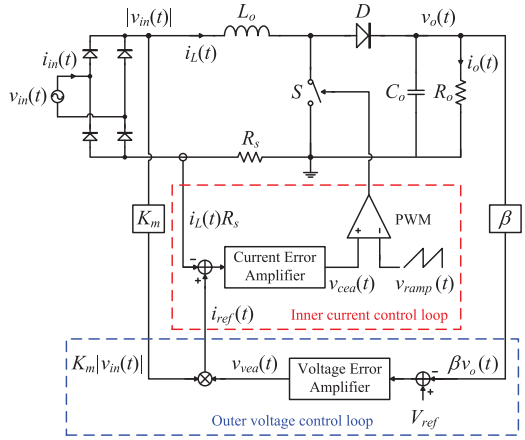

Fig. 1. Configuration of standard boost PFC preregulator with ACM control.

Researchers had proposed various strategies, in the form of both analog and digital implementation, to achieve near-unity PF without sacrificing the dynamic response of PFC preregulator. Two of these methods are load-current feedforward [3] and line-voltage feedforward [5]–[6] that provide fast compensation against load and line-voltage variations, respectively. However, as is true for all feedforward methods, selection of the optimum feedforward gain that will provide exact compensation requires accurate modeling of the PFC preregulator in question. Deviation from the optimum feedforward gain due to unmodeled circuit parameters will give rise to residual perturbation that must be compensated by the typical slow voltage feedback loop of conventional PFC preregulators, leading to slow recovery

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of the output voltage. Thus, although feedforward methods are effective in reducing voltage undershoot/overshoot during transient state, a fast voltage feedback loop is still desirable. Besides, since the optimum feedforward gain is a function of the operating point of PFC preregulator, it must be adaptively changed at different line voltage and load conditions for maintaining optimality, which complicates the controller design.

Two-stage solution that includes the cascading of a wide-bandwidth dc–dc converter provides a tight regulation of output voltage [7], [8]. However, the massive increase in component count and low efficiency make it unsuitable for low-power applications. To avoid these problems, various single-stage isolated PF corrector power supplies (S^2IP^2) were proposed [9]–[11]. Although switching loss is lowered by the reduction of switches, a high-voltage stress is imposed on the dc-link capacitor unless some additional control circuitry is implemented [12]. This, however, complicates the controller design.

Sliding-mode control is a nonlinear control method that is used to improve the dynamic response of PFC preregulator. In [13], overshoot and undershoot voltages during step-load changes are reduced by controlling the switching behavior according to a desired sliding function. However, despite the reduced overshoot and undershoot, the settling time of output voltage does not improve compared to the conventional design. Similar to sliding-mode control, boundary control is another nonlinear control method that is used to achieve both sinusoidal input current and fast dynamic response in PFC preregulator [14], [15]. The PFC preregulator's switch is controlled in such a way that the instantaneous values of the state variables (i.e., $\hat{i}_L$ and $\hat{v}_o$) are varying along the targeted operating trajectories. This method is attractive as PFC preregulator can reach its steady state within one to two switching cycles after step-load changes. However, a large amount of computational power is required for analyzing complex system equations, and some calibration processes are needed to compensate for the variances in converter's components' values.

Another approach to achieve both fast dynamic response and high PF simultaneously is to eliminate the sampled output voltage ripple before it is processed by voltage error amplifier. One way to implement this approach is by using a notch filter [16]–[19]. By inserting a notch filter that provides strong attenuation at the double-line frequency, the amplitude of the sampled output voltage ripple can be significantly reduced before it is processed by voltage error amplifier. As a result, the bandwidth of voltage error amplifier can be increased without distorting input current's waveform. Although the notch filter can be realized using analog devices [20], it can lead to performance degradation due to the presence of component tolerances. Digital implementation enables the realization of a high-quality notch filter [21], [22] due to greater stability, higher precision, and programmability. However, high implementation cost limits its use to specific high-end applications only.

An alternative solution based on ripple estimation/cancellation has been proposed to eliminate ripple component from error voltage by subtracting an estimated replica of the output voltage ripple from the sampled output voltage [23]–[25]. As a result, an undistorted and sinusoidal input current can be obtained even if the bandwidth of voltage error amplifier is increased considerably compared to conventional design. In the work of Spiazzi *et al*. [26], the authors proposed a ripple estimation circuit that consists of a bandpass filter, an amplifier with a fixed gain, and a 90° phase shifter. Ripple estimation is made according to an idealized equation of output voltage ripple derived by assuming that PFC preregulator's efficiency is known and output capacitor is very large. Despite its simplicity, it is prone to estimation error due to uncertainties in estimating the parameter values used in the equation, which can lead to distortion in the input current of PFC preregulator. To alleviate this problem, an adaptive ripple estimator was proposed in [27], where the amplitude of the estimated output voltage ripple is forced to track the amplitude of the sampled output voltage ripple. However, the drawback is the need for a phase locked loop and that the additional high-pass filters are required to be identical.

In view of the limitations of these methods, a precise ripple estimation/cancellation circuit consisting of an amplitude tuner and a phase shifter was proposed in [28]. The estimated output voltage ripple is made to track the sampled output voltage ripple accurately both in magnitude and in phase angle over a wide range of operating conditions. Although near-ideal ripple estimation/cancellation is achievable, the proposed ripple estimation network is very complex as it involves many switching circuitries. In this paper, two other ripple estimation methods are proposed. It can be shown that these methods and the method proposed in [28] can all be inferred from the figures of merit of PFC preregulator and constitute a family of switched-resistor-circuit-based ripple estimation methods. It will be shown that these methods can differ considerably in terms of complexity of hardware implementation and THD and PF performances. This paper aims to present a detailed study on their implementation and characterization of their performances.

This paper is organized as follows. The figures of merit of PFC preregulator are first derived in Section II. Based on an analysis of the equations obtained, three ripple estimation methods are proposed in Section III. Following this, the hardware implementation of these ripple estimation methods are discussed in Section IV along with a detailed explanation of their operating principles. In Section V, the performance of the three ripple estimation methods are investigated and compared by implementing them on a 200-W ACM-controlled boost PFC preregulator power stage. Through the performance comparisons under different operating conditions, suggestions are given to choose the preferred method based on user's PF and THD requirements. Finally, conclusion is given in Section VI.

II. Derivation of Main Figures of Merit

In this section, the main figures of merit of PFC preregulator with ripple cancellation are derived. Fig. 2 shows the basic configuration of a PFC preregulator's outer voltage control loop with ripple estimation/cancellation, where $\beta v_o(t)$ and $v_{\text{est}}(t)$ is the sampled output voltage and the estimated output voltage ripple, respectively. In this voltage control loop, the estimated output voltage ripple $v_{\text{est}}(t)$ is first subtracted from the sampled

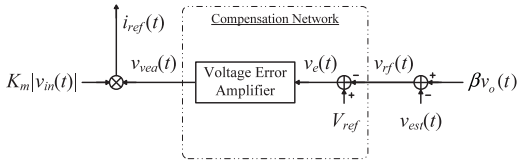


Fig. 2. Basic configuration of the PFC preregulator's outer voltage control loop including ripple estimation/cancellation.

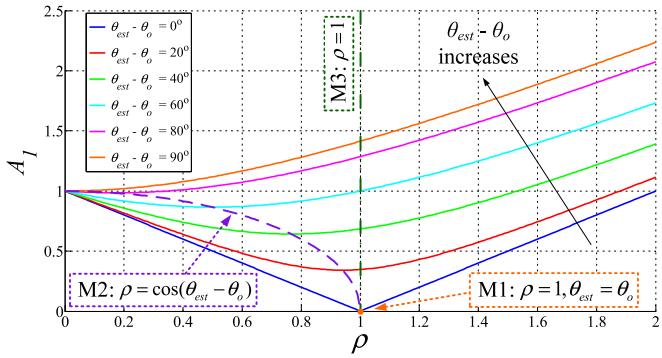


Fig. 3. Plot of A_1 versus ρ, where $\rho = V_{\text{est}}/\beta V_r$.

output voltage $\beta v_o(t)$ in order to produce an (ideally) ripple-free output voltage feedback signal $v_{\text{rf}}(t)$. Next, the error voltage, $v_e(t) = V_{\text{ref}} - v_{\text{rf}}(t)$, is amplified by the compensation network, and its output signal $v_{\text{vea}}(t)$ is subsequently multiplied by the rectified line voltage template $K_m\,|v_{\text{in}}(t)|$ to obtain the input current reference signal $i_{\text{ref}}(t)$ that determines the line current waveform.

Assume that the PFC preregulator is operating with unity PF and its output voltage contains a dc component and a double-line frequency component. According to [28], the output voltage of PFC preregulator has the general form described by (1), where ω_{line} is the angular line frequency and $\theta_o = \tan^{-1}(\omega_{\text{line}} R_o C_o)$ varies in the range of $0^{\text{o}} \le \theta_o \le 90^{\text{o}}$. The resulting sampled output voltage $\beta v_o(t)$ is given by (2)

$$\begin{aligned} v_o(t) &= V_o + \tilde{v}_o(t) \\ &= V_o - V_r \cos(2\omega_{\text{line}} t - \theta_o) \qquad (1) \\ \beta v_o(t) &= \beta\,(V_o + \tilde{v}_o(t)) \\ &= \beta V_o - \beta V_r \cos(2\omega_{\text{line}} t - \theta_o) \qquad (2) \end{aligned}$$

where V_o and V_r is the average output voltage of PFC preregulator and the amplitude of output voltage ripple, respectively.

Assume that the estimated output voltage ripple has an amplitude of V_{est} and a phase angle of θ_{est} (with respect to line voltage), it can be written mathematically as

$$v_{\text{est}}(t) = -V_{\text{est}} \cos(2\omega_{\text{line}} t - \theta_{\text{est}}) \qquad (3)$$

where $0^{\text{o}} \le \theta_{\text{est}} \le 90^{\text{o}}$.

By subtracting the estimated output voltage ripple $v_{\text{est}}(t)$ from the sampled output voltage $\beta v_o(t)$, the resultant signal, $v_{\text{rf}}(t) = V_{\text{rf}} + \tilde{v}_{\text{rf}}(t)$, which constitutes the input of the compensation network, is given by

$$\begin{aligned} v_{\text{rf}}(t) &= \beta v_o(t) - v_{\text{est}}(t) \\ &= [\beta V_o - \beta V_r \cos(2\omega_{\text{line}} t - \theta_o)] - [-V_{\text{est}} \cos(2\omega_{\text{line}} t - \theta_{\text{est}})] \\ &= \begin{cases} \beta V_o + A_1 \cdot \beta V_r \cdot \cos(2\omega_{\text{line}} t - \theta_{\text{rf}}), & \text{if } \rho > \dfrac{\cos\theta_o}{\cos\theta_{\text{est}}} \\ \beta V_o - A_1 \cdot \beta V_r \cdot \cos(2\omega_{\text{line}} t - \theta_{\text{rf}}), & \text{if } \rho \le \dfrac{\cos\theta_o}{\cos\theta_{\text{est}}} \end{cases} \end{aligned} \qquad (4)$$

where

$$\rho = \frac{V_{\text{est}}}{\beta V_r} \qquad (5)$$

$$A_1 = \sqrt{[\rho - \cos(\theta_{\text{est}} - \theta_o)]^2 + \sin^2(\theta_{\text{est}} - \theta_o)} \qquad (6)$$

$$\theta_{rf} = \tan^{-1}\left(\frac{\rho \sin\theta_{\text{est}} - \sin\theta_o}{\rho\cos\theta_{\text{est}} - \cos\theta_o}\right), \text{where } -90^{\text{o}} \le \theta_{\text{rf}} \le 90^{\text{o}}. \qquad (7)$$

Typically, θ_o tends to approach 90^{o} for most PFC preregulators with reasonably large output capacitor in order to provide a low impedance path for the flow of the double-line frequency component. In fact, this condition is assumed in all existing ripple estimation methods, and therefore, θ_{est} is typically fixed at 90^{o}. Based on this assumption, the value of ρ is always less than $\frac{\cos\theta_o}{\cos\theta_{\text{est}}}$ (since $\cos\theta_{\text{est}} = 0$), and hence, only the case of $\rho \le \frac{\cos\theta_o}{\cos\theta_{\text{est}}}$ is considered in the following analysis.

After subtraction, $v_{\text{rf}}(t)$ is further processed by the compensation network, which includes a reference voltage V_{ref} and a voltage error amplifier. Let $G_{2\omega_{\text{line}}}$ and $\theta_{2\omega_{\text{line}}}$ be the gain and the phase shift introduced by the compensation network at the double-line frequency, respectively; the output signal of the voltage error amplifier is given by

$$\begin{aligned} v_{\text{vea}}(t) &= V_{\text{vea}} + \tilde{v}_{\text{vea}}(t) \\ &= V_{\text{vea}} + G_{2\omega_{\text{line}}} \cdot A_1 \cdot \beta V_r \cdot \cos(2\omega_{\text{line}} t - \theta_{\text{rf}} + \theta_{2\omega_{\text{line}}}) \\ &= V_{\text{vea}}\left[1 + \frac{G_{2\omega_{\text{line}}} \cdot A_1 \cdot \beta V_r}{V_{\text{vea}}} \cos(2\omega_{\text{line}} t + (\theta_{2\omega_{\text{line}}} - \theta_{\text{rf}}))\right] \end{aligned} \qquad (8)$$

where V_{vea} is the average value of the voltage error amplifier's output signal.

Following that, $v_{\text{vea}}(t)$ is multiplied by the rectified line voltage template $K_m V_p\,|\sin(\omega_{\text{line}} t)|$ to obtain the input current reference waveform $i_{\text{ref}}(t)$, as given by (9), where K_m is the line-voltage-step-down ratio and V_p is the peak value of the line voltage

$$\begin{aligned} i_{\text{ref}}(t) &= K_m V_p\,|\sin(\omega_{\text{line}} t)|\, V_{\text{vea}} \\ &\quad \times \left[1 + \frac{G_{2\omega_{\text{line}}} \cdot A_1 \cdot \beta V_r}{V_{\text{vea}}} \cos(2\omega_{\text{line}} t + (\theta_{2\omega_{\text{line}}} - \theta_{\text{rf}}))\right]. \end{aligned} \qquad (9)$$

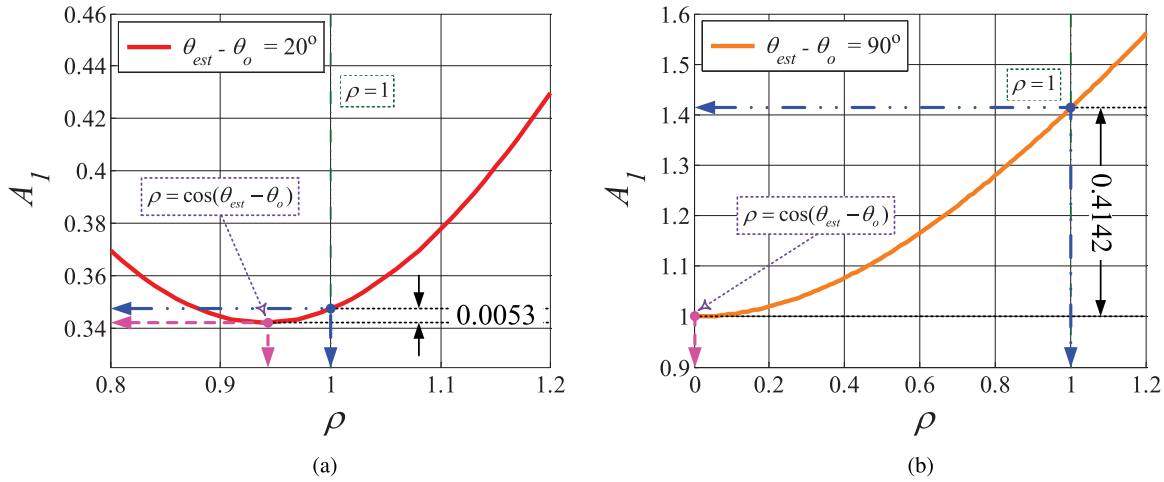


Fig. 4. Plot of A_1 versus ρ for different values of $(\theta_{\text{est}} - \theta_o)$, where $\rho = V_{\text{est}}/\beta V_r$.

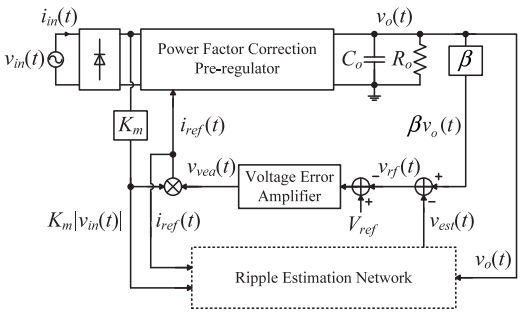


Fig. 5. PFC preregulator with ripple estimated network.

The input current reference waveform $i_{\text{ref}}(t)$ is then compared with the sensed inductor current $i_L(t)R_s$ through the inner current control loop, where $i_L(t)$ and R_s is the inductor current and inductor current sensing resistor, respectively. As the bandwidth of the inner current loop is typically large, the sensed inductor current is assumed to closely track the input current reference waveform, i.e., $i_L(t)R_s = i_{\text{ref}}(t)$. Hence, the switching-cycle-averaged inductor current is given by

$$i_L(t) = \frac{K_m V_p V_{\text{vea}}}{R_s} |\sin(\omega_{\text{line}} t)| \times \left[1 + \frac{G_{2\omega_{\text{line}}} \cdot A_1 \cdot \beta V_r}{V_{\text{vea}}} \cos(2\omega_{\text{line}} t + (\theta_{2\omega_{\text{line}}} - \theta_{\text{rf}}))\right]. \tag{10}$$

Since the inductor current is equal to the rectified input current of PFC preregulator, the input current waveform can be obtained as follows:

$$\begin{aligned} i_{\text{in}}(t) &= \frac{K_m V_p V_{\text{vea}}}{R_s} \sin(\omega_{\text{line}} t) \times \left[1 + \frac{G_{2\omega_{\text{line}}} \cdot A_1 \cdot \beta V_r}{V_{\text{vea}}} \cos(2\omega_{\text{line}} t + (\theta_{2\omega_{\text{line}}} - \theta_{\text{rf}}))\right] \\ &= i_{\text{in1}}(t) + i_{\text{in3}}(t) \end{aligned} \tag{11}$$

where

$$i_{\text{in1}}(t) = \frac{K_m V_p V_{\text{vea}}}{R_s} \sqrt{1 - (k_1 A_1)\cos(\theta_{2\omega_{\text{line}}} - \theta_{\text{rf}}) + \left(\frac{k_1 A_1}{2}\right)^2} \times \sin\left[\omega_{\text{line}} t - \tan^{-1}\left(\frac{k_1 A_1 \sin(\theta_{2\omega_{\text{line}}} - \theta_{\text{rf}})}{2 - k_1 A_1 \cos(\theta_{2\omega_{\text{line}}} - \theta_{\text{rf}})}\right)\right] \tag{12}$$

$$i_{\text{in3}}(t) = \frac{K_m V_p V_{\text{vea}}}{R_s} \left(\frac{k_1 A_1}{2}\right) \sin(3\omega_{\text{line}} t + (\theta_{2\omega_{\text{line}}} - \theta_{\text{rf}})) \tag{13}$$

and

$$k_1 = \frac{G_{2\omega_{\text{line}}} \beta V_r}{V_{\text{vea}}}. \tag{14}$$

By using (11)–(14), the THD of the input current and PF of the PFC preregulator can be derived as given by (15) and (16), respectively. It can be seen that both THD and PF are related to the values of k_1, A_1, $\theta_{2\omega_{\text{line}}}$, and θ_{rf}. They further show that when the product $k_1 A_1$ is small, low THD and high PF are obtained. Therefore, small values of the product $k_1 A_1$ are desirable for achieving high PF and low THD of PFC preregulator's input current

$$\text{THD} = \frac{k_1 A_1}{\sqrt{4 - 4(k_1 A_1)\cos(\theta_{2\omega_{\text{line}}} - \theta_{\text{rf}}) + (k_1 A_1)^2}} \tag{15}$$

$$\text{PF} = \frac{\sqrt{2}(1 - 0.5(k_1 A_1)\cos(\theta_{2\omega_{\text{line}}} - \theta_{\text{rf}}))}{\sqrt{2 + (k_1 A_1)^2 - 2(k_1 A_1)\cos(\theta_{2\omega_{\text{line}}} - \theta_{\text{rf}})}}. \tag{16}$$

III. Family of Three Ripple Estimation Methods

As discussed in the previous section, in order to achieve high PF, it is necessary to minimize the value of the product $k_1 A_1$. However, from (14), it can be observed that k_1 is directly proportional to $G_{2\omega_{\text{line}}}$, which is related to the unity-gain bandwidth of PFC preregulator. This implies that when the bandwidth of PFC preregulator is increased for improved dynamic response, k_1 will also be increased accordingly. In this case, A_1 should be

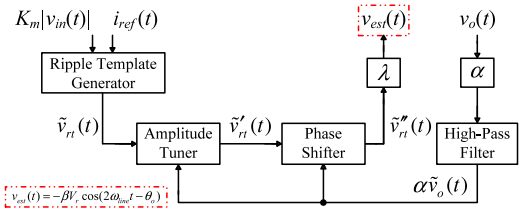


Fig. 6. Basic configurations of ripple estimation/cancellation network based on Method 1.

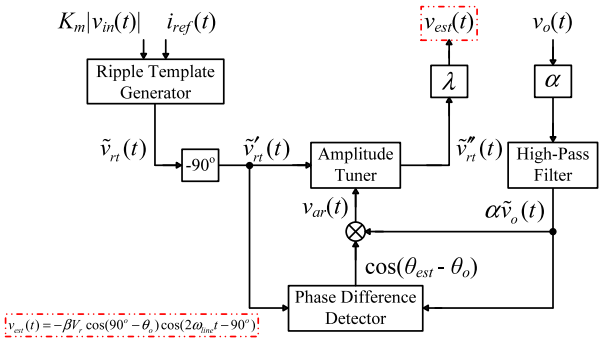


Fig. 7. Basic configuration of ripple estimation/cancellation network based on Method 2.

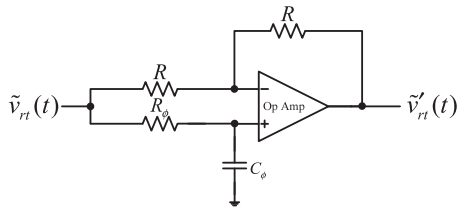


Fig. 8. Basic configuration of a standard all-pass filter.

minimized in order to reduce the value of the product $k_1 A_1$ as much as possible so that both fast dynamic response and high PF can be achieved simultaneously. In this section, three ripple estimation methods are discussed based on an analysis of the relationship between A_1 and ρ for different values of $(\theta_{\text{est}} - \theta_o)$.

A. Minimization of Global Cancellation Error

Recall that A_1 is a function of ρ and the phase difference between θ_{est} and θ_o as given by (17). A graphical representation of A_1 plotted against ρ for different values of $(\theta_{\text{est}} - \theta_o)$ is shown in Fig. 3. From the graph, it can be seen that when $\rho = 1$ and $\theta_{\text{est}} = \theta_o$, the value of A_1 is zero. Minimum global cancellation error occurs under this condition, which leads to zero THD of PFC preregulator's input current and unity PF despite the use of large unity-gain bandwidth for attaining fast dynamic response. In this paper, this ripple estimation method is defined as Method 1 (or M1) with $\rho = 1$ and $\theta_{\text{est}} = \theta_o$, where the estimated output voltage ripple $v_{\text{est}}(t)$ is described by (18)

$$A_1 = \sqrt{[\rho - \cos(\theta_{\text{est}} - \theta_o)]^2 + \sin^2(\theta_{\text{est}} - \theta_o)}$$

$$\text{Method 1}: \tag{17}$$

$$v_{\text{est}}(t) \xrightarrow[\theta_{\text{est}}=\theta_o]{V_{\text{est}}=\beta V_r} -(\beta V_r)\cos(2\omega_{\text{line}}t - \theta_o). \tag{18}$$

B. Minimization of Local Cancellation Error

When the condition $\theta_{\text{est}} = \theta_o$ cannot be attained, an alternative solution is sought to achieve minimum local cancellation error in the presence of phase estimation error $(\theta_{\text{est}} - \theta_o \neq 0)$. By differentiating A_1 with respect to ρ, as shown in (19), it can be solved that A_1 is at its local minimum value given by $A_1 = \sin(\theta_{\text{est}} - \theta_o)$ when $\rho = \cos(\theta_{\text{est}} - \theta_o)$

$$\frac{dA_1}{d\rho} = \frac{\rho - \cos(\theta_{\text{est}} - \theta_o)}{\sqrt{\rho^2 - 2\rho\cos(\theta_{\text{est}} - \theta_o) + 1}} = 0$$

$$\|A_1\| \xrightarrow{\rho=\cos(\theta_{\text{est}}-\theta_o)} |\sin(\theta_{\text{est}} - \theta_o)|. \tag{19}$$

Since $\rho = V_{\text{est}}/\beta V_r$, it can be deduced that, when $\theta_{\text{est}} \neq \theta_o$, the estimated output voltage ripple $v_{\text{est}}(t)$ should have an amplitude of $\beta V_r \cos(\theta_{\text{est}} - \theta_o)$ in order to achieve minimum A_1 associated with a given phase estimation error $(\theta_{\text{est}} - \theta_o)$. The overall estimated output voltage ripple that results in local minimum of A_1 is given by

$$\text{Method 2}:$$

$$v_{\text{est}}(t) \xrightarrow[\theta_{\text{est}}\neq\theta_o]{V_{\text{est}}=\beta V_r\cos(\theta_{\text{est}}-\theta_o)} -[\beta V_r\cos(\theta_{\text{est}} - \theta_o)] \times \cos(2\omega_{\text{line}}t - \theta_{\text{est}}). \tag{20}$$

Equation (20) serves as the basis for an alternative ripple estimation method that results in minimum local cancellation error when the phase estimation error is nonzero. In this paper, this ripple estimation method is defined as Method 2 (or M2) with $\rho = \cos(\theta_{\text{est}} - \theta_o)$ and $\theta_{\text{est}} \neq \theta_o$.

C. Equalization of Ripple Amplitude Only

Since A_1 is closely related to both the THD of input current and PF, as suggested by (15) and (16), the performance of PFC preregulator is expected to be similar if A_1 does not vary significantly. By plotting the graph of A_1 against ρ with $(\theta_{\text{est}} - \theta_o)$ as parameter, as shown in Fig. 4, it can be observed that the value of A_1 at $\rho = 1$ does not differ significantly from that at $\rho = \cos(\theta_{\text{est}} - \theta_o)$ [see Fig. 4(a)], except when $(\theta_{\text{est}} - \theta_o)$ is large [see Fig. 4(b)]. Based on this observation, an alternative ripple estimation method based on equalization of ripple amplitude only (i.e., $\rho = 1$) is proposed. This method is defined as Method 3 (M3) and the estimated output voltage ripple is given by

$$\text{Method 3}:$$

$$v_{est}(t) \xrightarrow[\theta_{\text{est}}\neq\theta_o V_{\text{est}}]{v_{\text{est}}(t)=\beta V_r} -(\beta V_r)\cos(2\omega_{\text{line}}t - \theta_{\text{est}}). \tag{21}$$

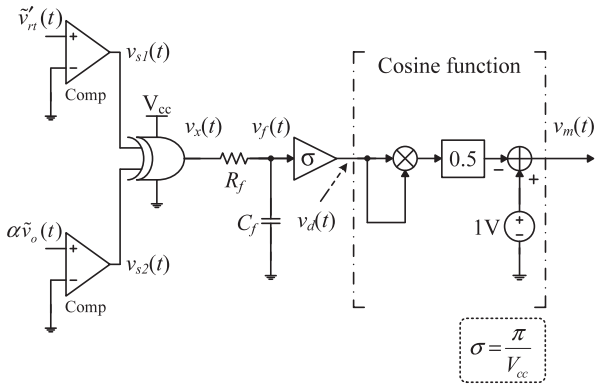


Fig. 9. Schematic diagram of the proposed phase difference detector.

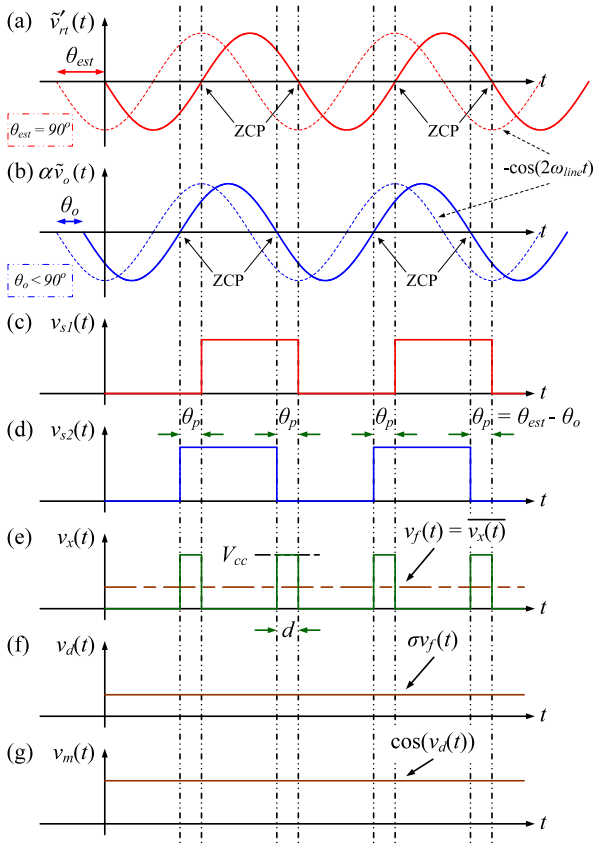


Fig. 10. Operating waveforms of the proposed phase difference detector.

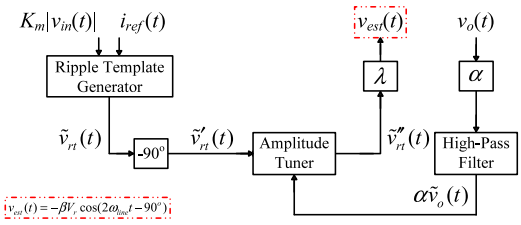


Fig. 11. Basic configuration of ripple estimation/cancellation network based on Method 3.

TABLE I
SPECIFICATIONS OF BOOST PFC PREREGULATOR PROTOTYPE

Description	Parameter	Value
Nominal input or line voltage (rms)	V_{in}	110 V_{rms}
Nominal input or line frequency	f_{line}	60 Hz
Nominal output voltage	V_o	400 V
Nominal output power	P_o	200 W
Nominal load resistance	R_o	800 Ω
Filter inductance	L_o	1 mH
Output capacitance	C_o	16 μF

From the above analysis, three ripple estimation methods have been proposed. They are (a) Method 1: $\rho = 1$ and $\theta_{\text{est}} = \theta_o$; (b) Method 2: $\rho = \cos(\theta_{\text{est}} - \theta_o)$ and $\theta_{\text{est}} \neq \theta_o$; (c) Method 3: $\rho = 1$ and $\theta_{\text{est}} \neq \theta_o$. A more detailed description of these ripple estimation methods and their methods of implementation are presented in the next section.

IV. HARDWARE IMPLEMENTATION

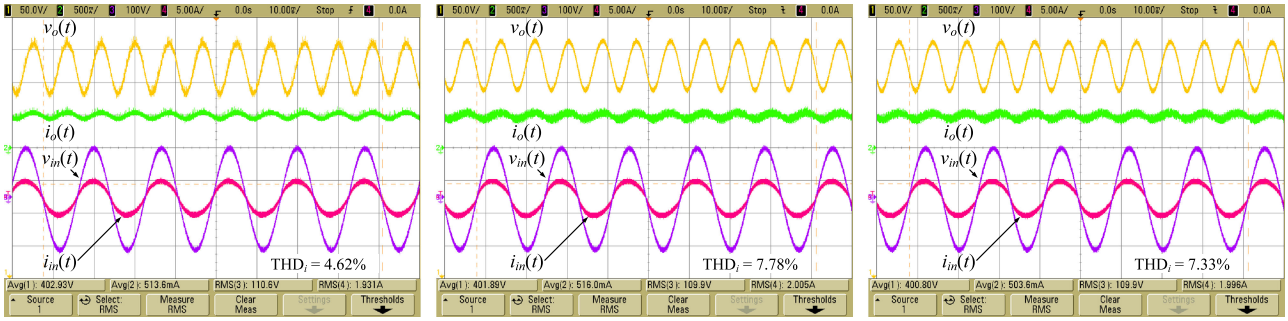
In this section, the methods of implementation of the three ripple estimation methods are discussed in detail. The block diagram of a PFC preregulator with ripple estimation network is depicted in Fig. 5. First, an unmodified ripple template $\tilde{v}_{\text{rt}}(t)$ is obtained by the ripple template generator proposed in [28], which multiplies the stepped-down rectified line voltage $K_m\,|v_{\text{in}}(t)|$ and the input current reference signal $i_{\text{ref}}(t)$, followed by high-pass filtering that removes the dc component. It can also be generated by multiplying $K_m\,|v_{\text{in}}(t)|$ to itself, i.e., $K_m^2\,|v_{\text{in}}(t)|^2$, and removing the dc component by high-pass filter. This method ensures that a sinusoidal ripple template is obtained even when the input current is distorted. For both approaches, the resulting ripple template $v_{\text{rt}}(t)$ is given by (22), where V_{rt} is the amplitude of the ripple template

$$\tilde{v}_{\text{rt}}(t) = -V_{\text{rt}} \cos(2\omega_{\text{line}} t)\,. \tag{22}$$

Subsequently, the amplitude and phase angle of the ripple template $\tilde{v}_{\text{rt}}(t)$ are modified through the ripple estimation network in accordance with the sampled output voltage ripple $\alpha v_o(t)$. The output of the ripple estimation network $v_{\text{est}}(t)$ is then subtracted from the sampled output voltage $\beta v_o(t)$ in order to produce an (ideally) ripple-free output voltage feedback signal $v_{\text{rf}}(t)$ for further processing by the voltage error amplifier.

A. Ripple Estimation Method Based on Minimum Global Cancellation Error

In order to achieve minimum global cancellation error (i.e., Method 1: $\rho = 1$ and $\theta_{\text{est}} = \theta_o$), the ripple template $\tilde{v}_{\text{rt}}(t)$ is modified in amplitude by an amplitude tuner, and subsequently in phase angle by a phase shifter. The block diagram of the ripple estimation network used to generate the estimated output voltage ripple based on Method 1 is shown in Fig. 6. The detailed description of the operating principle of the amplitude tuner and phase shifter are given in [28] and will not be repeated here. The sampled output voltage ripple $\alpha\tilde{v}_o(t)$, which is used as the reference signal for both the amplitude tuner and phase shifter, is obtained by scaling down the PFC preregulator's output voltage



(a) (b) (c)

Fig. 12. Input and output waveforms of boost PFC preregulator prototype with the ripple estimation/cancellation under nominal operating condition ($v_{\text{in}}(t)$: input or line voltage, $i_{\text{in}}(t)$: input or line current, $v_o(t)$: output voltage, $i_o(t)$: output current) [(a) Method 1; (b) Method 2; (c) Method 3].

by a factor of α, followed by high-pass filtering. In order to avoid the introduction of additional phase shift, the high-pass filter's cutoff frequency is configured to be approximately 1 Hz, i.e., two decades lower than the double-line frequency. During steady state, the output signal of the phase shifter $\tilde{v}''_{\text{rt}}(t)$ will be of the same amplitude and phase angle as the sampled output voltage ripple $\alpha\tilde{v}_o(t)$. Finally, in order to account for the difference between two sampling ratios (α and β), the estimated output voltage ripple $v_{\text{est}}(t)$ is obtained by stepping down the output signal of the phase shifter $\tilde{v}''_{\text{rt}}(t)$ by a factor of $\lambda = \beta/\alpha$ before it is subtracted from the sampled output voltage $\beta v_o(t)$ using a difference amplifier. Hence, the estimated output voltage ripple $v_{\text{est}}(t)$ is given by

$$\begin{aligned} v_{\text{est}}(t) &= \lambda \cdot \tilde{v}''_{\text{rt}}(t) \\ &= \lambda \cdot [-\alpha V_r \cos(2\omega_{\text{line}} t - \theta_o)] \\ &\xrightarrow{\lambda=\beta/\alpha} (\frac{\beta}{\alpha}) \cdot [-\alpha V_r \cos(2\omega_{\text{line}} t - \theta_o)] \\ &= -\beta V_r \cos(2\omega_{\text{line}} t - \theta_o) \\ &= \beta\tilde{v}_o(t). \end{aligned} \tag{23}$$

Recall that the sampled output voltage ripple $\beta\tilde{v}_o(t)$ is given by $-\beta V_r \cos(2\omega_{\text{line}} t - \theta_o)$. It can be deduced that the estimated output voltage ripple $v_{\text{est}}(t)$ are of the same amplitude and phase angle as the sampled output voltage ripple $\beta\tilde{v}_o(t)$, which fulfills the conditions required by Method 1, i.e., $\rho = 1$ and $\theta_{\text{est}} = \theta_o$. Under such a condition, the result of subtraction (i.e., $\beta v_o(t) - v_{\text{est}}(t)$) will produce a ripple-free signal for further processing by the voltage error amplifier.

B. Ripple Estimation Method Based on Minimum Local Cancellation Error

From the above analysis, a precise ripple estimation/cancellation method which incorporates an amplitude tuner and a phase shifter will give rise to minimum global cancellation error. Although the estimated output voltage ripple is an accurate replica of the actual one, the ripple estimation network is very complex as it involves many switching components and their associated gate drive circuitries. Alternatively, as discussed in Section III-B, the estimated output voltage ripple $v_{\text{est}}(t)$ should have an amplitude of $V_{\text{est}} = \beta V_r \cos(\theta_{\text{est}} - \theta_o)$ in the presence of phase estimation error in order to give rise to a minimum local cancellation error between the sampled output voltage ripple $\beta\tilde{v}_o(t)$ and the estimated output voltage ripple $v_{\text{est}}(t)$.

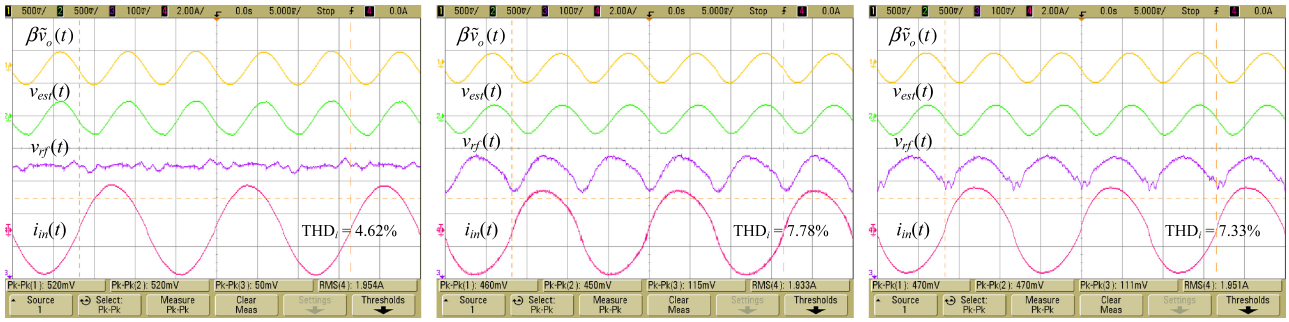
Fig. 7 shows the basic configuration of the ripple estimation/cancellation network based on Method 2 ($\rho = \cos(\theta_{\text{est}} - \theta_o)$ and $\theta_{\text{est}} \neq \theta_o$). As discussed earlier, the output voltage ripple of PFC preregulators has a typical phase shift that approaches 90° in the presence of reasonably large output capacitor, a condition that is generally met by PFC preregulators for achieving small output voltage ripple size. Hence, for Method 2, the ripple template $\tilde{v}_{\text{rt}}(t)$ is phase shifted by 90°, i.e., $\theta_{\text{est}} = 90°$, using a standard all-pass filter as shown in Fig. 8, which results in a phase-shifted ripple template $\tilde{v}'_{\text{rt}}(t)$ described by

$$\tilde{v}'_{\text{rt}}(t) = -V_{\text{rt}} \cos(2\omega_{\text{line}} t - 90°). \tag{24}$$

The phase-shifted ripple template $\tilde{v}'_{\text{rt}}(t)$ is then fed into an amplitude tuner, which will equalize the amplitude of the phase-shifted ripple template $\tilde{v}'_{\text{rt}}(t)$ with that of the reference signal $v_{\text{ar}}(t)$. According to (20), the amplitude of the estimated output voltage ripple should be made proportional to $\cos(\theta_{\text{est}} - \theta_o)$, which in turn is related to the phase difference between the estimated and the sampled output voltage ripple, i.e., $(\theta_{\text{est}} - \theta_o)$. To do this, the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ and the phase-shifted ripple template $\tilde{v}'_{\text{rt}}(t)$ are passed to a phase difference detector, which will generate the phase difference signal and the value of $\cos(\theta_{\text{est}} - \theta_o)$. The output of the phase difference detector, i.e., $\cos(\theta_{\text{est}} - \theta_o)$, is then multiplied by the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ to obtain the reference signal for the amplitude tuner $v_{\text{ar}}(t)$, as described by

$$\begin{aligned} v_{\text{ar}}(t) &= [\cos(\theta_{\text{est}} - \theta_o)] \cdot [\alpha\tilde{v}_o(t)] \\ &= [\cos(\theta_{\text{est}} - \theta_o)] \cdot [-\alpha V_r \cos(2\omega_{\text{line}} t - \theta_o)] \\ &= -\alpha V_r \cos(\theta_{\text{est}} - \theta_o) \cos(2\omega_{\text{line}} t - \theta_o). \end{aligned} \tag{25}$$

Under the action of the amplitude tuner, $\tilde{v}''_{\text{rt}}(t)$ will acquire the same amplitude as the reference signal $v_{\text{ar}}(t)$, i.e., $|\tilde{v}''_{\text{rt}}(t)| = \alpha V_r \cos(\theta_{\text{est}} - \theta_o)$. Considering that θ_{est} is set to 90°, the output signal of the amplitude tuner is therefore given by (26). Finally, the estimated output voltage ripple $v_{\text{est}}(t)$ is obtained by scaling the output signal of the amplitude tuner $\tilde{v}''_{\text{rt}}(t)$ by $\lambda = \beta/\alpha$ as



(a) (b) (c)

Fig. 13. Measured input and output waveforms of difference amplifier under nominal condition ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{\rm est}(t)$: estimated output voltage ripple, $v_{\rm rf}(t)$: output of difference amplifier, $i_{\rm in}(t)$: input or line current) under the actions of ripple estimation/cancellation method [(a) Method 1; (b) Method 2; (c) Method 3].

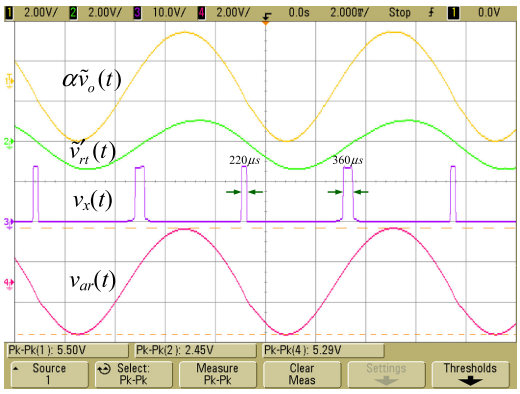


Fig. 14. Main operating waveforms of phase difference detector under the action of Method 2 ($\alpha\tilde{v}_o(t)$: sampled output voltage ripple, $\tilde{v}'_{\rm rt}(t)$: phase-shifted ripple template, $v_x(t)$: exclusive-or (XOR) gate's output signal, $v_{\rm ar}(t)$: reference signal for the amplitude tuner).

described by

$$\tilde{v}''_{\rm rt}(t) \xrightarrow{\theta_{\rm est}=90^{\rm o}} \alpha V_r \cos(90^{\rm o}-\theta_o) \times \cos(2\omega_{\rm line}t - 90^{\rm o}) \quad (26)$$

$$\begin{aligned} v_{\rm est}(t) &= \lambda \cdot \tilde{v}''_{\rm rt}(t) \\ &= \lambda \cdot [\alpha V_r \cos(90^{\rm o}-\theta_o)\cos(2\omega_{\rm line}t - 90^{\rm o})] \\ &= -\beta V_r \cos(90^{\rm o}-\theta_o)\cos(2\omega_{\rm line}t - 90^{\rm o}). \end{aligned} \quad (27)$$

1) Phase Difference Detector: The schematic diagram of the proposed phase difference detector is shown in Fig. 9. It is used to detect and generate a signal that represents the phase difference between the phase-shifted ripple template $\tilde{v}'_{\rm rt}(t)$ and the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ and subsequently approximates the cosine value of the phase difference. The key operating waveforms of the phase difference detector are depicted in Fig. 10.

The operation of the phase difference detector is described as follows. It takes the two input signals, $\tilde{v}'_{\rm rt}(t)$ and $\alpha\tilde{v}_o(t)$, and compares them individually with 0 V to detect the zero crossing points (ZCP) of each signal. By comparing the output signals of the two comparators, $v_{s1}(t)$ and $v_{s2}(t)$, through an exclusive-or (XOR) gate, the phase difference between $\tilde{v}'_{\rm rt}(t)$ and $\alpha\tilde{v}_o(t)$, i.e., $\theta_p = \theta_{\rm est} - \theta_o$, is reflected by the duty cycle of the XOR-gate's output signal $v_x(t)$. The sequence of actions described are shown in Fig. 10(c)–(e). Since its operation is based on the detection of ZCP, the proposed phase difference detector may suffer a degradation in accuracy when the input signals are distorted. However, in the proposed application, the line current is not expected to be severely distorted, hence the distortions of the input signals are expected to be small and should not have a significant impact on the measurement accuracy.

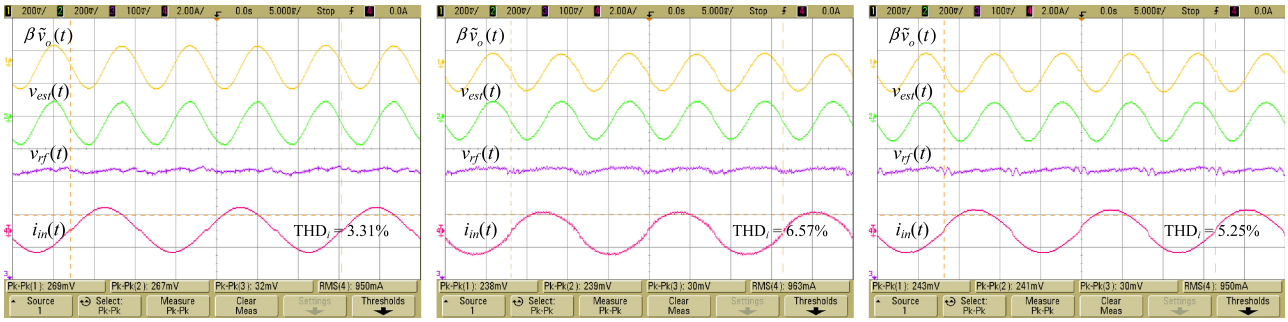
Recall that the objective of the phase difference detector is to calculate the cosine value of the phase difference between the input signals, i.e., $\tilde{v}'_{\rm rt}(t)$ and $\alpha\tilde{v}_o(t)$. This is achieved by adding a low-pass filter (R_f–C_f) and a gain stage of σ to convert the phase difference information from duty cycle to radian, and subsequently use the result to approximate its cosine value, i.e., $v_m(t) = \cos(v_d(t))$, where $v_m(t)$ is the output signal of the phase difference detector. Considering that $(\theta_{\rm est} - \theta_o)$ is usually small, as $\theta_o \to 90^{\rm o}$ for reasonably large output capacitor, the cosine function can be realized using small-angle approximation, as given by (28), where ϕ is in radian, in order to realize it using analog circuit.

$$\cos(\phi) \approx 1 - \frac{\phi^2}{2} \quad (28)$$

Finally, the output signal of the phase difference detector $v_m(t)$ is multiplied by the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ to produce the reference signal for the amplitude tuner $v_{\rm ar}(t)$, as described by

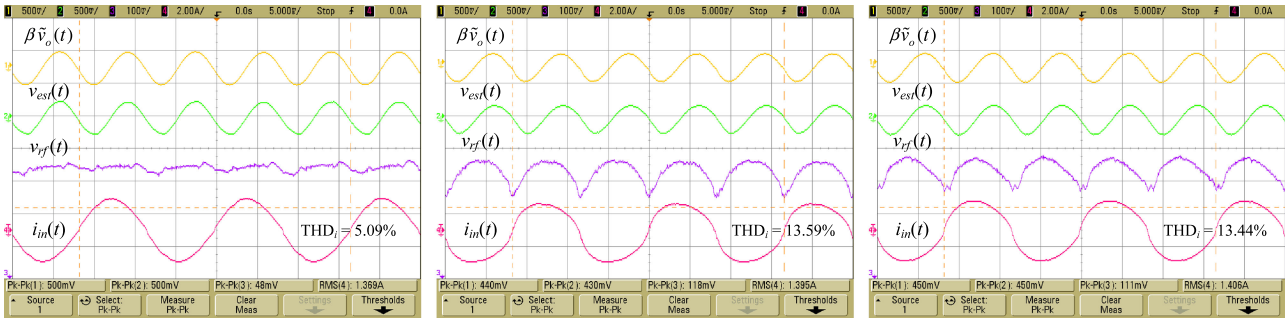
$$\begin{aligned} v_{\rm ar}(t) &= v_m(t)\cdot\alpha\tilde{v}_o(t) \\ &= [\cos(\theta_{\rm est}-\theta_o)]\cdot[-\alpha V_r\cos(2\omega_{\rm line}t-\theta_o)] \\ &= -\alpha V_r\cos(\theta_{\rm est}-\theta_o)\cos(2\omega_{\rm line}t-\theta_o) \\ &\xrightarrow{\theta_{\rm est}=90^{\rm o}} -\alpha V_r\cos(90^{\rm o}-\theta_o)\cos(2\omega_{\rm line}t-\theta_o). \end{aligned} \quad (29)$$

By using the ripple estimation circuit discussed above, the estimated output voltage ripple $v_{\rm est}(t)$ will operate with an amplitude that is proportional to the phase difference between the sampled output voltage ripple and the phase-shifted ripple template, i.e., $V_{\rm est} = \beta V_r \cos(\theta_{\rm est} - \theta_o)$, in order to achieve



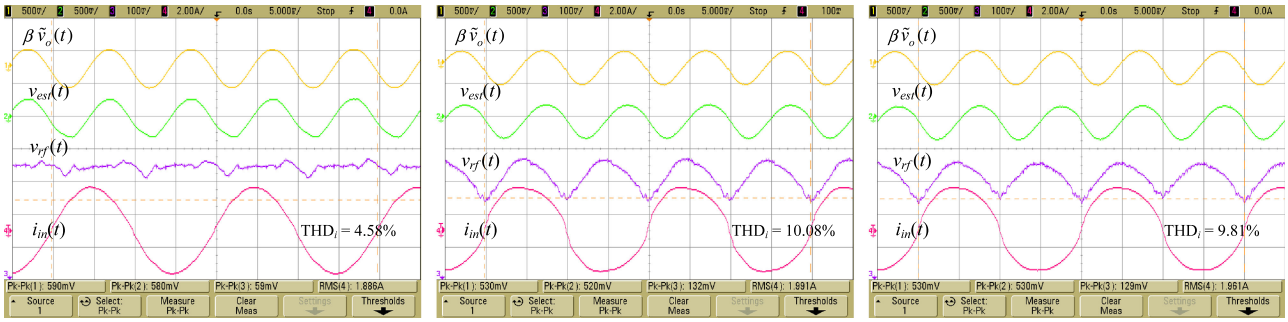
(a) (b) (c)

Fig. 15. Measured input and output waveforms of difference amplifier under half-load condition ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{\rm est}(t)$: estimated output voltage ripple, $v_{\rm rf}(t)$: output of difference amplifier, $i_{\rm in}(t)$: input or line current) under the actions of ripple estimation/cancellation method [(a) Method 1; (b) Method 2; (c) Method 3].



(a) (b) (c)

Fig. 16. Measured input and output waveforms of difference amplifier at $V_{\rm in} = 150\ {\rm V_{rms}}$ ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{\rm est}(t)$: estimated output voltage ripple, $v_{\rm rf}(t)$: output of difference amplifier, $i_{\rm in}(t)$: input or line current) under the actions of ripple estimation/cancellation method [(a) Method 1; (b) Method 2; (c) Method 3].



(a) (b) (c)

Fig. 17. Measured input and output waveforms of difference amplifier at $f_{\rm line} = 50$ Hz ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{\rm est}(t)$: estimated output voltage ripple, $v_{\rm rf}(t)$: output of difference amplifier, $i_{in}(t)$: input or line current) under the actions of ripple estimation/cancellation method [(a) Method 1; (b) Method 2; (c) Method 3].

minimum local cancellation error associated with a given phase estimation error. Although the design of the phase-shifting circuit is simplified, the complexity of the overall ripple estimation circuit is not reduced significantly due to the need for a phase difference detector.

C. Ripple Estimation Method Based on Equalization of Ripple Amplitude Only

With Method 1, the estimated output voltage ripple $v_{\rm est}(t)$ and the sampled output voltage ripple $\beta\tilde{v}_o(t)$ are configured to have the same amplitude and phase angle, which leads to perfect ripple estimation/cancellation. However, high complexity is the major drawback of this method. With Method 2, the adaptive phase shifter used in Method 1 is replaced by a constant phase shifter of $90^{\rm o}$ in order to produce a ripple estimation circuit having a simpler structure. Under the condition of nonzero phase estimation error, the amplitude of the estimated output voltage ripple $v_{\rm est}(t)$ is configured to closely track the optimum amplitude given by the function $\beta V_r \cos(\theta_{\rm est} - \theta_o)$. Although minimum local cancellation error can be realized with Method 2,

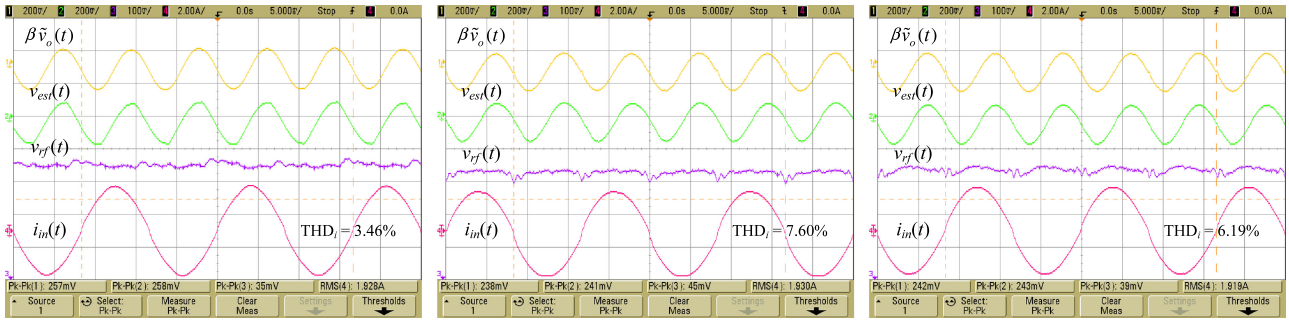


Fig. 18. Measured input and output waveforms of difference amplifier at $C_o = 32\ \mu$F ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{\rm est}(t)$: estimated output voltage ripple, $v_{\rm rf}(t)$: output of difference amplifier, $i_{\rm in}(t)$: input or line current) under the actions of ripple estimation/cancellation method [(a) Method 1; (b) Method 2; (c) Method 3].

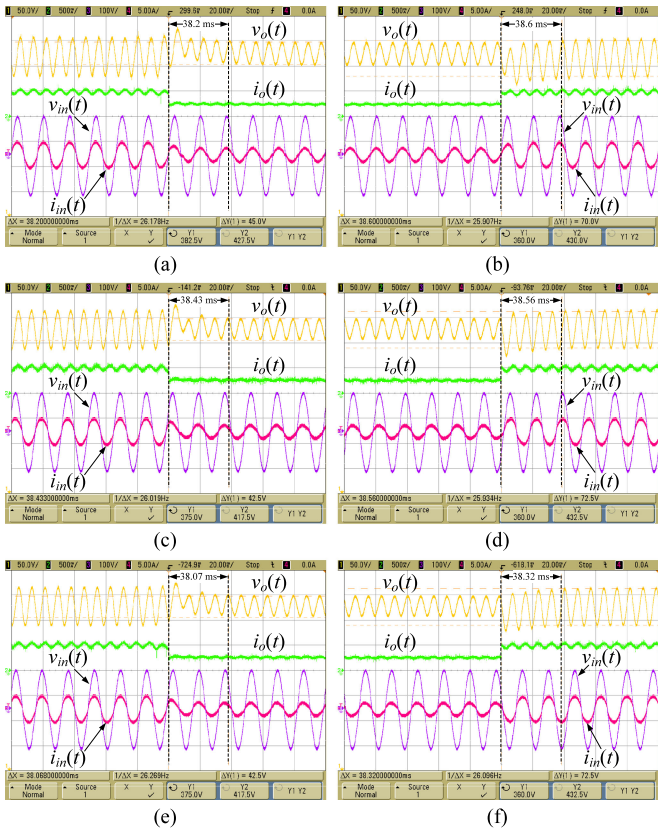


Fig. 19. Measured input and output waveforms of boost PFC preregulator under step decrease [(a), (c), and (e)] and increase [(b), (d), and (f)] in load ([(a) and (b)] Method 1; [(c) and (d)] Method 2; [(e) and (f)] Method 3).

the overall ripple estimation circuit, including the phase difference measurement, is not significantly reduced compared to Method 1.

Alternatively, as discussed in Section III-C, there is a very small difference in the performance of PFC preregulator when the amplitude of the estimated output voltage ripple is configured to be $V_{\rm est} = \beta V_r \cos(\theta_{\rm est} - \theta_o)$ or $V_{\rm est} = \beta V_r$, except when $(\theta_{\rm est} - \theta_o)$ is large. As θ_o does not deviate significantly from 90° for most PFC preregulators, the phase estimation error $(\theta_{\rm est} - \theta_o)$ is usually small when $\theta_{\rm est}$ is set to 90°. This enables a simpler ripple estimation network based on Method 3 which is depicted in Fig. 11. The ripple template is phase shifted by 90° and its amplitude is tuned by using the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ as the reference signal. As a result, the estimated output voltage ripple $v_{\rm est}(t)$ is equal in amplitude to the sampled output voltage ripple $\beta\tilde{v}_o(t)$ and is described by

$$v_{\rm est}(t) \xrightarrow[\theta_{\rm est}=90^{\rm o}]{V_{\rm est}=\beta V_r} -(\beta V_r)\cos(2\omega_{\rm line}t - 90^{\rm o}). \qquad (30)$$

With Method 3 ($\rho = 1$ and $\theta_{\rm est} \neq \theta_o$), the complexity of ripple estimation circuit can be significantly reduced by eliminating the need for a phase shifter or phase difference detector. Among these three ripple estimation methods, Method 3 provides the simplest solution as it essentially consists of an amplitude tuner only.

V. Experimental Verification

In this section, the three ripple estimation/cancellation methods are implemented and tested experimentally with a 200-W boost PFC preregulator having a unity-gain bandwidth of 60 Hz, which is significantly larger than conventional design ($\leq$ 10 Hz) for achieving fast dynamic response. The specifications of the PFC preregulator prototype are listed in Table I. By using this experimental setup, the THD and PF performances of the PFC preregulator under the actions of the three ripple estimation/cancellation methods will be investigated individually. The dynamic response of the PFC preregulator in the presence of the proposed ripple estimation/cancellation circuits will also be studied by subjecting it to step load changes.

Fig. 12(a) shows the steady-state input and output waveforms of the boost PFC preregulator prototype under nominal conditions when the estimated output voltage ripple is produced by Method 1, while Fig. 12(b) and (c) shows the same waveforms when Method 2 and Method 3 are used, respectively. The measured average output voltage and current of PFC preregulator in all three cases are approximately 400 V and 500 mA, respectively, and its efficiency is 90%. Under the action of Method 1, which involves an amplitude tuner and a phase shifter, the estimated output voltage ripple $v_{\rm est}(t)$ has approximately the same

TABLE II
MEASURED PEAK-TO-PEAK RIPPLE AMPLITUDES AND INPUT CURRENT'S PF AND THD UNDER THE ACTIONS OF THREE RIPPLE ESTIMATION/CANCELLATION METHODS

		$\lvert\beta\tilde{v}_o(t)\rvert$	$\lvert v_{\text{est}}(t)\rvert$	$\lvert v_{\text{rf}}(t)\rvert$	PF	THD_i
			Nominal condition			
Method 1	$\rho = 1$ $\theta_{\text{est}} = \theta_o$	520 mV_{pp}	520 mV_{pp}	50 mV_{pp}	0.999	4.62%
Method 2	$\rho = \cos(\theta_{\text{est}} - \theta_o)$ $\theta_{\text{est}} \neq \theta_o$	460 mV_{pp}	450 mV_{pp}	115 mV_{pp}	0.995	7.78%
Method 3	$\rho = 1$ $\theta_{\text{est}} \neq \theta_o$	470 mV_{pp}	470 mV_{pp}	111 mV_{pp}	0.995	7.33%
			Half load			
Method 1	$\rho = 1$ $\theta_{\text{est}} = \theta_o$	269 mV_{pp}	267 mV_{pp}	32 mV_{pp}	0.999	3.31%
Method 2	$\rho = \cos(\theta_{\text{est}} - \theta_o)$ $\theta_{\text{est}} \neq \theta_o$	238 mV_{pp}	239 mV_{pp}	30 mV_{pp}	0.997	6.57%
Method 3	$\rho = 1$ $\theta_{\text{est}} \neq \theta_o$	243 mV_{pp}	241 mV_{pp}	30 mV_{pp}	0.998	5.25%
			$V_{\text{in}} = 150\ \text{V}_{\text{rms}}$			
Method 1	$\rho = 1$ $\theta_{\text{est}} = \theta_o$	500 mV_{pp}	500 mV_{pp}	48 mV_{pp}	0.998	5.09%
Method 2	$\rho = \cos(\theta_{\text{est}} - \theta_o)$ $\theta_{\text{est}} \neq \theta_o$	440 mV_{pp}	430 mV_{pp}	118 mV_{pp}	0.990	13.59%
Method 3	$\rho = 1$ $\theta_{\text{est}} \neq \theta_o$	450 mV_{pp}	450 mV_{pp}	111 mV_{pp}	0.991	13.44%
			$f_{\text{line}} = 50$ Hz			
Method 1	$\rho = 1$ $\theta_{\text{est}} = \theta_o$	590 mV_{pp}	580 mV_{pp}	59 mV_{pp}	0.999	4.58%
Method 2	$\rho = \cos(\theta_{\text{est}} - \theta_o)$ $\theta_{\text{est}} \neq \theta_o$	530 mV_{pp}	520 mV_{pp}	132 mV_{pp}	0.992	10.08%
Method 3	$\rho = 1$ $\theta_{\text{est}} \neq \theta_o$	530 mV_{pp}	530 mV_{pp}	129 mV_{pp}	0.993	9.81%
			$C_o = 32\ \mu\text{F}$			
Method 1	$\rho = 1$ $\theta_{\text{est}} = \theta_o$	257 mV_{pp}	258 mV_{pp}	35 mV_{pp}	0.999	3.46%
Method 2	$\rho = \cos(\theta_{\text{est}} - \theta_o)$ $\theta_{\text{est}} \neq \theta_o$	238 mV_{pp}	241 mV_{pp}	45 mV_{pp}	0.995	7.60%
Method 3	$\rho = 1$ $\theta_{\text{est}} \neq \theta_o$	242 mV_{pp}	243 mV_{pp}	39 mV_{pp}	0.997	6.19%

amplitude and phase angle as the sampled output voltage ripple $\beta\tilde{v}_o(t)$, i.e., $\rho = 1$ and $\theta_{\text{est}} = \theta_o$, as depicted in Fig. 13(a). Since the estimated output voltage ripple $v_{\text{est}}(t)$ is almost identical to the sampled output voltage ripple $\beta\tilde{v}_o(t)$, difference amplifier's output signal $v_{\text{rf}}(t)$ [$= \beta v_o(t) - v_{\text{est}}(t)$] is near ripple-free (with a peak-to-peak voltage of 50 mV), which gives rise to near-ideal sinusoidal input current $i_{\text{in}}(t)$ with a PF of 0.999 and a very low THD of 4.62%. On the other hand, when the estimated output voltage ripple $v_{\text{est}}(t)$ is produced by Method 2 and 3, as shown in Fig. 13(b) and (c), respectively, the average phase difference between the phase-shifted ripple template $\tilde{v}'_{\text{rf}}(t)$ and the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ is approximately 13^{o}, i.e., $\theta_{\text{est}} - \theta_o = 13^{\text{o}}$, which is calculated by measuring the high-level time interval of the exclusive-or (XOR) gate's output signal $v_x(t)$ shown in Fig. 14. Since the phase estimation error is nonzero, the peak-to-peak voltage of the difference amplifier's output signal $v_{\text{rf}}(t)$ increases (compared to Method 1), which leads to a slight increment in the THD of the PFC preregulator's input current (7.78% for Method 2 and 7.33% for Method 3). Moreover, it can be observed that both Method 2 and 3 produce difference amplifier's output signals that are similar in amplitude; hence, both methods result in input current waveforms with similar PF and THD.

Fig. 15(a)–(c) shows the main operating waveforms under 50% load (i.e., $P_o = 200\,\text{W} \rightarrow 100\,\text{W}$) when Methods 1–3 is used, respectively. As usual, Method 1 generates an accurate replica of the sampled output voltage ripple, which causes the peak-to-peak voltage of the double-line frequency component at the input of the voltage error amplifier to reduce from 269 to 32 mV_{pp}. When Methods 2 and 3 are used, it can be seen that the estimated output voltage ripple $v_{\text{est}}(t)$ in both cases are of the same amplitude as the sampled output voltage ripple $\beta\tilde{v}_o(t)$. This can be explained by referring to (31). When the load is halved, the phase angle of the output voltage ripple θ_o, as suggested by (1) and (2), will tend to approach more closely to 90^{o}. Recall that θ_{est} is made constant and equal to 90^{o} for

TABLE III
SIMULATED PEAK-TO-PEAK RIPPLE AMPLITUDES AND INPUT CURRENT'S PF AND THD UNDER THE ACTIONS OF THREE RIPPLE ESTIMATION/CANCELLATION METHODS

		$\lvert\beta\tilde{v}_o(t)\rvert$	$\lvert v_{\text{est}}(t)\rvert$	$\lvert v_{\text{rf}}(t)\rvert$	PF	THD_i
			Nominal condition			
Method 1	$\rho = 1$, $\theta_{\text{est}} = \theta_o$	520 mV_{pp}	510 mV_{pp}	45 mV_{pp}	0.993	1.39 %
Method 2	$\rho = \cos(\theta_{\text{est}} - \theta_o)$, $\theta_{\text{est}} \neq \theta_o$	485 mV_{pp}	470 mV_{pp}	135 mV_{pp}	0.990	6.13 %
Method 3	$\rho = 1$, $\theta_{\text{est}} \neq \theta_o$	485 mV_{pp}	486 mV_{pp}	125 mV_{pp}	0.990	6.05 %
			Half load			
Method 1	$\rho = 1$, $\theta_{\text{est}} = \theta_o$	273 mV_{pp}	271 mV_{pp}	22 mV_{pp}	0.993	1.42%
Method 2	$\rho = \cos(\theta_{\text{est}} - \theta_o)$, $\theta_{\text{est}} \neq \theta_o$	250 mV_{pp}	248 mV_{pp}	48 mV_{pp}	0.991	4.13%
Method 3	$\rho = 1$, $\theta_{est} \neq \theta_o$	250 mV_{pp}	250 mV_{pp}	50 mV_{pp}	0.991	3.99%
			$V_{\text{in}} = 150\ \text{V}_{\text{rms}}$			
Method 1	$\rho = 1$, $\theta_{\text{est}} = \theta_o$	520 mV_{pp}	515 mV_{pp}	46 mV_{pp}	0.993	1.99%
Method 2	$\rho = \cos(\theta_{\text{est}} - \theta_o)$, $\theta_{\text{est}} \neq \theta_o$	460 mV_{pp}	435 mV_{pp}	125 mV_{pp}	0.978	10.69%
Method 3	$\rho = 1$, $\theta_{\text{est}} \neq \theta_o$	460 mV_{pp}	460 mV_{pp}	120 mV_{pp}	0.978	10.46%
			$f_{\text{line}} = 50$ Hz			
Method 1	$\rho = 1$, $\theta_{\text{est}} = \theta_o$	630 mV_{pp}	630 mV_{pp}	65 mV_{pp}	0.993	2.68%
Method 2	$\rho = \cos(\theta_{\text{est}} - \theta_o)$, $\theta_{\text{est}} \neq \theta_o$	578 mV_{pp}	545 mV_{pp}	153 mV_{pp}	0.985	9.22%
Method 3	$\rho = 1$, $\theta_{\text{est}} \neq \theta_o$	575 mV_{pp}	575 mV_{pp}	145 mV_{pp}	0.985	9.38%
			$C_o = 32\ \mu\text{F}$			
Method 1	$\rho = 1$, $\theta_{\text{est}} = \theta_o$	263 mV_{pp}	260 mV_{pp}	32 mV_{pp}	0.993	1.29%
Method 2	$\rho = \cos(\theta_{\text{est}} - \theta_o)$, $\theta_{\text{est}} \neq \theta_o$	256 mV_{pp}	250 mV_{pp}	50 mV_{pp}	0.993	2.05%
Method 3	$\rho = 1$, $\theta_{\text{est}} \neq \theta_o$	250 mV_{pp}	250 mV_{pp}	45 mV_{pp}	0.993	2.00%

both Method 2 and 3. Hence, according to (21), the estimated output voltage ripple $v_{\text{est}}(t)$ should have the same amplitude as the sampled output voltage ripple $\beta\tilde{v}_o(t)$. It can be observed that the estimated output voltage ripple $v_{\text{est}}(t)$ produced by all three methods are able to track the sampled output voltage ripple $\beta\tilde{v}_o(t)$ closely. As a result, the peak-to-peak voltages of the difference amplifier's output signals in all three cases are small ($\sim$30 mV_{pp}), which resulted in input current waveforms with very low THD (compared to the case of full-load condition) and near-unity PF.

$$\begin{aligned} |v_{\text{est}}(t)| &= \beta V_r \cos(\theta_{\text{est}} - \theta_o) \\ &\xrightarrow{\theta_{\text{est}} = \theta_o = 90^{\text{o}}} \beta V_r \cos(90^{\text{o}} - 90^{\text{o}}) \\ &= \beta V_r \cos(0^{\text{o}}) \\ &= \beta V_r \end{aligned} \tag{31}$$

Next, the performances of the three ripple estimation/cancellation methods are investigated under increased line voltage and decreased line frequency. Fig. 16 shows the key waveforms of the difference amplifier at $V_{\text{in}} = 150\ \text{V}_{\text{rms}}$, while Fig. 17 shows the same waveforms at $f_{\text{line}} = 50$ Hz. It can be seen that the ripple estimation/cancellation circuit based on Method 1 always produces estimated output voltage ripple $v_{\text{est}}(t)$ that is equal in amplitude and phase angle to the sampled output voltage ripple $\beta\tilde{v}_o(t)$; hence, the difference amplifier's output signal $v_{\text{rf}}(t)$ is approximately ripple-free in both cases. This is confirmed by the measured low THD of input current, amounting to 5.09% and 4.58% at $V_{\text{in}} = 150\ \text{V}_{\text{rms}}$ and $f_{\text{line}} = 50$ Hz, respectively. However, when the estimated output voltage ripple $v_{\text{est}}(t)$ is produced by Method 2, a ripple component (of 118 mV_{pp} at $V_{\text{in}} = 150\ \text{V}_{\text{rms}}$ and 132 mV_{pp} at $f_{\text{line}} = 50$ Hz) exists in the difference amplifier's output signal $v_{\text{rf}}(t)$, and caused the THD of input current to increase from 5.09% to 13.59% at $V_{\text{in}} = 150\ \text{V}_{\text{rms}}$ and from 4.58% to 10.08% at $f_{\text{line}} = 50$ Hz. Similar results were obtained when the estimated output voltage ripple $v_{\text{est}}(t)$ is produced by Method 3. Figs. 16(c) and 17(c) show that the difference amplifier's output signal $v_{\text{rf}}(t)$ under the action of

Method 3 is not ripple-free but has an amplitude of 111 $\mathrm{mV_{pp}}$ at $V_{\text{in}} = 150\ \mathrm{V_{rms}}$ and 129 $\mathrm{mV_{pp}}$ at $f_{\text{line}} = 50$ Hz, which are similar to those obtained with Method 2. The imperfect cancellation is predominantly caused by the phase estimation error between θ_{est} and θ_o.

Finally, the proposed ripple estimation/cancellation methods are examined under increased output capacitance of PFC preregulator, i.e., $C_o = 16\,\mu\text{F} \rightarrow 32\,\mu\text{F}$, which leads to reduction in the amplitude of the sampled output voltage ripple and causes its phase angle θ_o to approach more closely to 90^{o}. Under increased output capacitance, the behaviour of the sampled output voltage ripple is similar to that under half-load condition. From the measured input current, as depicted in Fig. 18, it was found that the THD of input current with Method 1 is 3.46%, while with Method 2 and 3 it increased to 7.60% and 6.19%, respectively. The reason for having achieved low THD of input current and near-unity PF for all three cases is due to the fact that the estimated output voltage ripple $v_{\text{est}}(t)$ should have the same magnitude as the sampled output voltage ripple $\beta\tilde{v}_o(t)$ as the phase difference $(\theta_{\text{est}} - \theta_o)$ approaches zero. As a result, the ripple cancellation error is small and the output signal of the voltage error amplifier is approximately ripple-free, and hence, an undistorted sinusoidal input current is obtained.

Table II summarizes the measured amplitudes of the input and output signals of difference amplifier and the measured PF and THD of input current under the aforementioned operating conditions for all three ripple estimation methods. The corresponding simulation results obtained from PSIM are given in Table III. It can be seen that, when the amplitude and phase angle of the sampled output voltage ripple are estimated individually, the PF of PFC preregulator is consistently unity and the THD of input current is very low under various operating conditions. However, if the estimated phase angle θ_{est} is fixed at 90^{o}, the THD of input current increases and PF is slightly degraded, and the degradation in performance is similar for both Methods 2 and 3. By comparing the measurement results obtained for Method 2 and 3, the peak-to-peak voltages of the difference amplifier's output signals and the THD of input currents resulting from both methods are generally similar. Therefore, it can be concluded that when unity PF and extremely low THD of input current are required, Method 1 provides an ideal solution. Otherwise, Method 3 should be adopted given the simplicity of its hardware implementation and acceptable level of performance in terms of PF and THD of input current.

Finally, the dynamic response of the boost PFC preregulator implemented with the three ripple estimation/cancellation methods was investigated by subjecting it to step load decrease and increase. The results are shown in Fig. 19. The time taken for the PFC preregulator to reach steady state after step load change is about 38 ms for all three methods since the PFC preregulator's unity-gain-bandwidth remains unchanged in all cases. From the above steady-state and the dynamic tests, it can be concluded that all three ripple estimation/cancellation methods are effective solutions to achieve near-unity PF and fast dynamic response simultaneously.

VI. Conclusion

In this paper, the main figures of merit of PFC preregulator were first derived. Deducing from the mathematical analysis, a family of three ripple estimation methods were proposed and their hardware implementation was discussed. The three methods include: 1) Method 1: $\rho = 1$ and $\theta_{\text{est}} = \theta_o$; 2) Method 2: $\rho = \cos(\theta_{\text{est}} - \theta_o)$ and $\theta_{\text{est}} \neq \theta_o$; and 3) Method 3: $\rho = 1$ and $\theta_{\text{est}} \neq \theta_o$, where $\rho = V_{\text{est}}/\beta V_r$ and θ_o is the phase angle of sampled output voltage ripple. It was shown that the complexity of the ripple estimation circuit based on Method 1 is the highest, albeit precise ripple estimation/cancellation and minimum global cancellation error are achieved, which gives rise to unity PF and zero THD of PFC preregulator's input current. When there exists phase estimation error, Method 2 provides a minimum local cancellation error. Although the design of phase shifter is greatly simplified, the complexity of the overall ripple estimation circuit, however, is not reduced significantly due to the need for a phase difference detector. Finally, it was shown that the configuration of Method 3 is the simplest since it essentially consists of an amplitude tuner only. The proposed three ripple estimation methods were tested experimentally under different operating conditions with a 200-W boost PFC preregulator as power stage having a large unity-gain bandwidth. By comparison of the experimentally measured figures of merit, it was found that Method 1, which consists of separate amplitude tuner and phase shifter, provides the most accurate ripple estimation/cancellation under a wide range of operating conditions, and results in near-unity PF and input current with very low THD. Although phase estimation errors are inherent with Methods 2 and 3, they do not cause a significant degradation in PF and distortion of input current waveform. From the operating waveforms of difference amplifier and the measured input current waveforms, it was demonstrated that the overall performances of Methods 2 and 3 are largely similar. Hence, it can be concluded that Method 1 is an ideal solution when unity PF and input current with extremely low THD are required. Otherwise, Method 3 should be adopted since it provides a simple and cost-effective solution for achieving high (but not unity) PF and fast dynamic response.

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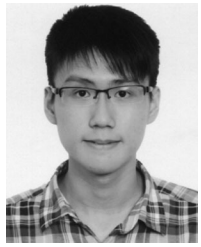

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