A Family of High-Frequency Single-Switch DC–DC Converters With Low Switch Voltage Stress Based on Impedance Networks

Kyung-Hwan Lee, *Student Member, IEEE*, Euihoon Chung, *Student Member, IEEE*, Yongsu Han, *Student Member, IEEE*, and Jung-Ik Ha, *Senior Member, IEEE*

***Abstract*—This paper presents a novel family of single-switch resonant dc–dc converters with low switch voltage stress. The single-switch resonant converter which has a ground-referenced switch is advantageous for implementing the gate drive circuit and operating at several-MHz switching frequency. However, the conventional ones mostly have high voltage stress on the switch, roughly 4–5 times the input voltage. In this paper, we propose the single-switch converter topologies derived from the drain-source impedance networks consisting of two inductors and two capacitors. The switch voltage of the proposed converters is shaped into a near trapezoid by designing the resonant networks to have the desired drain-source impedance. Furthermore, a simple and specific design scheme is presented here so that the peak switch voltage is lowered to 2.2–2.5 times the input voltage while zero voltage switching is achieved. Experimental results from a 20-W GaN-based prototype operating at 10 MHz demonstrate the feasibility of the proposed converter topologies and the design method.**

***Index Terms*—High frequency, resonant converter, single switch, switch peak voltage, zero voltage switching (ZVS).**

I. Introduction

THERE has been an increasing demand for high power density in power converters. One effective way to enhance the power density is increasing the switching frequency as in [1]–[5]. Since the required energy storage and magnetic flux linkage are scaled down, high switching frequency can reduce the size of passive elements that generally occupy most of the converter volume. In particular, the recent developments in wide bandgap switching devices such as the gallium nitride high electron mobility transistor (GaN HEMT) have spurred efforts to increase the switching frequency and achieve the high power density [6]. Despite such merits, the increase in the switching frequency causes the deterioration of the switching losses and the undesirable oscillations attributed to the parasitic inductance and capacitance.

To address these problems, various resonant switching techniques have been proposed, e.g., zero voltage switching (ZVS) quasiresonant converter (QRC) and multiresonant converter (MRC) [7]–[9]. Among many ZVS converters, the single-switch ZVS converter with the ground-referenced switch, which is also called the single-ended converter, is known to be more suitable for operating at high switching frequency of several MHz than a bride-type converter. This is because there exist many practical challenges in implementing a high-side gate driver, controlling dead time to a few nanosecond, and synchronizing the gate drive signals of the low- and high-side switches [10], [11]. In other words, the single-ended converter topology has the great advantage of simpler gate drive circuit especially when it comes to the MHz-range switching frequency. Nonetheless, its major drawback is relatively high voltage stress on the switch. For example, the single-ended ZVS-QRC suffers from high voltage stress, 5–10 times the input voltage, so it is confined to the low-voltage application [9]. In addition, the class E converter as well as ZVS-MRC also has the problem of high switch voltage stress. The peak switch voltage of the class E converter reaches to 3.6–4.4 times the input voltage considering the nonlinearity of the device capacitance [12, Ch. 12], [13].

Various methods have been studied in order to alleviate the switch voltage stress of the single-ended resonant converters. One common solution is simply clamping the peak switch voltage by using a snubber circuit, e.g., RCD clamp circuit [14], a Zener diode [15], and a lossless passive snubber [16]. Another solution is adding a harmonic-tuned circuit [17]–[24]. The flat-top class E converter proposed in [18] decreases the peak switch voltage to three times the input voltage by adding the parallel *LC* circuit of which the resonant frequency is tuned to the second harmonic to the output load network. In addition, the class F converter topology [19], which is derived from the class E converter, further reduces the switch voltage stress to about twice the input voltage. With the harmonic-tuned circuit connected in series to the load network, it is designed to have high impedance to odd harmonics, and thus its switch-voltage waveform is shaped to a near-square wave. Similarly, in the class EF_2 [20], [21], the class Φ_2 [22], [23], and the class Φ_2-derived boost converter [24], the series *LC* circuit tuned to the second-harmonic frequency is connected in parallel with the switch. The switch-voltage waveforms are similar to the trapezoidal wave primarily containing odd harmonics, and the voltage stresses are lowered to 2.2–2.5 times the input voltage. However, the aforementioned conventional solutions use more passive elements, thereby increasing the circuit complexity. Moreover, the addition of the harmonic-tuned circuit increases the number of the resonant *L* and *C* elements, so the design procedures of such converters are difficult or not specific.

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The authors are with the Department of Electrical and Computer Engineering, Seoul National University, Seoul 151-744, Korea (e-mail: kyugahsal@snu.ac.kr; ystar55@snu.ac.kr; hysjj0617@snu.ac.kr; jungikha@snu.ac.kr).

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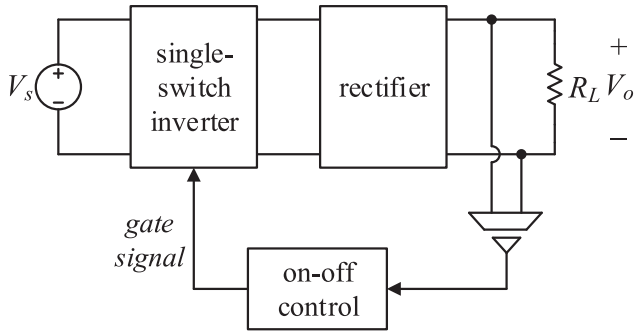

Fig. 1. Configuration of the proposed single-switch resonant dc–dc converter.

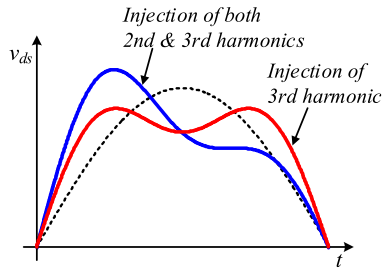

Fig. 2. Waveforms of the drain-source voltage $v_{\rm ds}$ with the injection of the second-harmonic or third-harmonic voltage.

This paper proposes a new family of the single-switch resonant converters based on the analysis of the *LC* impedance network. Utilizing two inductors and two capacitors, we make the *LC* resonant networks have the desired impedance, i.e., high impedance to the fundamental and third-harmonic components and low impedance to the second-harmonic one. Then the switch voltage is shaped to the near trapezoidal wave of which the peak value is almost twice the input voltage as in the class F, $\rm EF_2$, or Φ_2 topology. Nonetheless, the major difference with the conventional converters is the number of the resonant elements; the family of the proposed single-ended ZVS converters employs four passive elements, which is the minimum number for achieving the same purpose. On the other hand, the conventional counterparts require two or three more *L* and *C* elements because they are derived from the existing converter by adding the harmonic-tuned circuit. Besides, a relatively simple and specific design scheme is elaborated in this paper. A part of the proposed converter topology was presented in [25], but in this work, we find all possible *LC* impedance networks and organize the family of the single-ended resonant converters with low voltage stress.

The rest of the paper is organized as follows: In Section II, the analysis of the drain-source impedance and the design principles based on this are presented. Then the family of the proposed single-switch resonant converters is derived from the impedance networks. In Section III, we elaborate on the design procedure, and a design example is presented with simulation results. In Section IV, the experimental results of the 10-MHz, 20-W prototype validate the operation and performance of the proposed converters, and Section V concludes the paper.

II. Proposed Single-Switch Resonant DC–DC Converters

A. System Configuration

Fig. 1 shows the configuration of the proposed single-switch resonant dc–dc converter. It consists of an inverter and a rectifier. The inverter stage converts the input dc voltage V_s into the high-frequency ac voltage by the resonant operation. In this paper, it contains one switch which is referenced to the ground, and the resonant inductors and capacitors. Also, the rectifier changes the ac voltage to the output dc voltage V_o and delivers dc power to the load R_L. A half-wave rectifier, a full-bridge rectifier, and a center-tapped rectifier, which are classified as the current-driven class D rectifier in [12, Ch. 2], are generally used for the ac–dc rectification. Between the inverter and the rectifier, a transformation stage can be added to provide the isolation or the desired voltage gain of the converter.

In this work, we consider the applications where the output voltage of the converter is regulated by an on–off control as seen in Fig. 1. The on–off controller modulates the fraction of the turn-on time of the converter in order to make the output controlled to the desired output voltage reference. Recently, the on–off control is applied to many high-frequency converters as demonstrated in [23]–[31]. Particularly, the class E and the class Φ_2 converters are designed for a specific switching frequency, so their optimum operations are ensured within narrow frequency range. Accordingly, such converters have difficulty in using frequency modulation across a wide load range. On the other hand, the main advantage of the on–off control is that the design and operational characteristics of the power stage are not affected by the controller; hence, the optimum operation including ZVS is maintained across a wide load range with the fixed switching frequency of the power stage.

This work focuses on the inverter stage and thus proposes the novel single-switch resonant converters where the resonant inductors and capacitors in the inverter stage are designed to reduce the voltage stress on the switch. As in the class Φ_2 converter, the proposed converter topologies exhibit high performance under the on–off control as explained below.

B. Analysis of the Drain-Source Impedance $Z_{\rm ds}$

Before the topology derivation, we first analyze the drain-source impedance $Z_{\rm ds}$ that is the impedance seen from the drain-source terminal of the switch and describe its design principles to relieve the switch voltage stress.

In this paper, the waveform of the drain-source voltage $v_{\rm ds}$ is shaped to a near-square wave by injecting harmonic content as in the class F, $\rm EF_2$, and Φ_2 converters. If the third-harmonic voltage is injected, $v_{\rm ds}$ has the lowered peak value and becomes a near trapezoid as shown in Fig. 2. On the contrary, if both the second-harmonic and third-harmonic contents are injected, the peak of $v_{\rm ds}$ is rather increased and its waveform exhibits skewed one. That is, the third-harmonic voltage is helpful in reducing the peak switch voltage, but the second-harmonic one should be attenuated as much as possible.

As described in [19], [22], and [23], the steady-state waveform of $v_{\rm ds}$ is changed with respect to the characteristics of

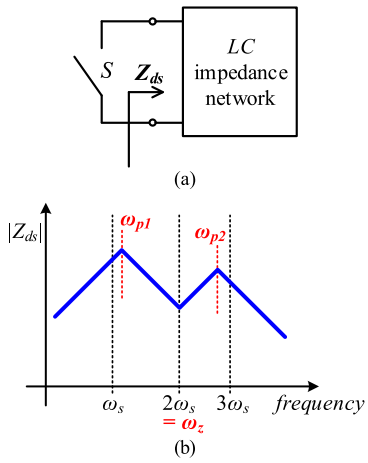

Fig. 3. (a) Drain-source impedance $Z_{\rm ds}$ when the switch S is OFF. (b) Desired shape of $|Z_{\rm ds}|$ to achieve ZVS and lower the peak switch voltage.

the drain-source impedance $Z_{\rm ds}$. When the switch S turns OFF, $v_{\rm ds}$ is determined by the resonance of all inductors and capacitors constituting the impedance network of $Z_{\rm ds}$ as drawn in Fig. 3(a). Thus, pole frequencies of $Z_{\rm ds}$ correspond to the solutions of the characteristic equation of the resonant network, and they are related to the frequency contents that noticeably appear in $v_{\rm ds}$. On the other hand, a zero of $Z_{\rm ds}$ results in low magnitude of the impedance around the zero frequency, which indicates the suppression of this zero-frequency content in $v_{\rm ds}$. Therefore, to inject the third-harmonic content and sufficiently attenuate the second-harmonic one as noted above, the following constraints on $Z_{\rm ds}$ should be fulfilled: 1) Two poles of $Z_{\rm ds}$ denoted by ω_{p1} and ω_{p2} should be located near the switching frequency ω_s and the third-harmonic frequency $3\omega_s$, respectively; 2) One zero of $Z_{\rm ds}$ represented by ω_z should be placed at $2\omega_s$ so that $|Z_{\rm ds}(j2\omega_s)|$ is low enough to suppress the second-harmonic component. Fig. 3(b) shows the magnitude of $Z_{\rm ds}$ satisfying the above two requirements.

Besides the waveform shaping, there are two more design constraints on the positions of ω_{p1} and ω_{p2}: achieving ZVS and reducing the peak switch voltage within 2.2–2.5 times the input voltage. Let us assume that ω_{p1} is the low-frequency pole and ω_{p2} is the high-frequency one. Because $Z_{\rm ds}(j\omega_s)$ is required to be inductive for ZVS, ω_{p1} is selected to be higher than ω_s as shown in Fig. 3(b). In addition, ω_{p2} is chosen to be lower than $3\omega_s$ because $Z_{\rm ds}(j3\omega_s)$ should be capacitive so that the injected third-harmonic voltage is almost in phase with the fundamental one and thereby the peak switch voltage is lowered. This is also depicted in Fig. 3(b). The more detailed explanation for choosing the pole locations is presented in the next section.

C. Topology Derivation

To derive the family of the proposed single-ended resonant converter topologies, first we construct all possible impedance networks that have the same impedance shape of $|Z_{\rm ds}|$ as in Fig. 3(b). For two poles and one zero of $Z_{\rm ds}$, at least two inductors and two capacitors are needed. Hence, by combining the minimum number of L and C elements, we construct four LC

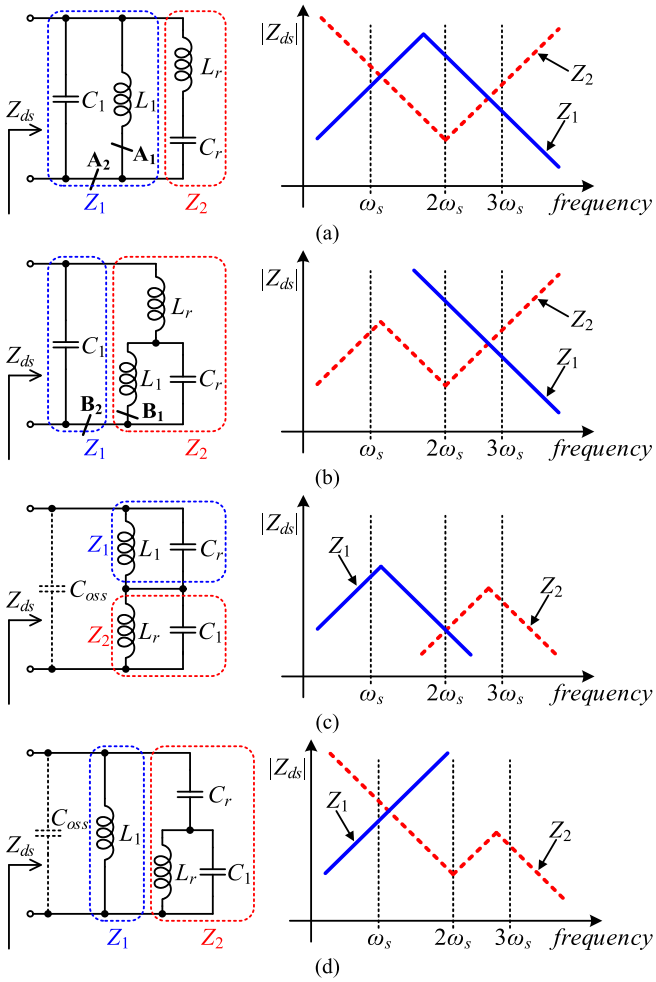

Fig. 4. Possible combinations of two inductors and two capacitors to make $|Z_{\rm ds}|$ have the desired shape as in Fig. 3(b). (a)–(d) Schematics of the LC impedance networks A–D and the asymptotic impedance Bode plots.

impedance networks as illustrated in Fig. 4(a)–(d), and they are named as the network A–D respectively. Here, two inductors are denoted by L_1 and L_r, and two capacitors are labeled as C_1 and C_r.

As shown in Fig. 4, the respective impedance network is divided into two parts: Z_1 and Z_2 which are connected in parallel or connected in series. If Z_1 and Z_2 are connected in parallel, the magnitude of the resultant impedance $Z_{\rm ds}$ $(= Z_1||Z_2)$ approximately follows the smaller one between Z_1 and Z_2. In contrast, if Z_1 and Z_2 are connected in series, the magnitude of $Z_{\rm ds}$ $(= Z_1 + Z_2)$ is approximated to the larger one. Accordingly, in the case of the impedance network A, the parallel resonant circuit Z_1 and the series resonant circuit Z_2 are connected in parallel as seen in Fig. 4(a); hence, $Z_{\rm ds}$ has a zero at the resonant frequency of Z_2, i.e., the resonant frequency of L_r and C_r. Also, the poles of $Z_{\rm ds}$ are placed around the points where the impedance diagrams of Z_1 and Z_2 intersect. Thus, to make $|Z_{\rm ds}|$ of the network A have the same shape as in Fig. 3(b), Z_2 consisting of L_r and C_r should be tuned to the second harmonic $2\omega_s$. In addition to the zero, the resonant frequency of Z_1 should be adjusted so that the positions of the

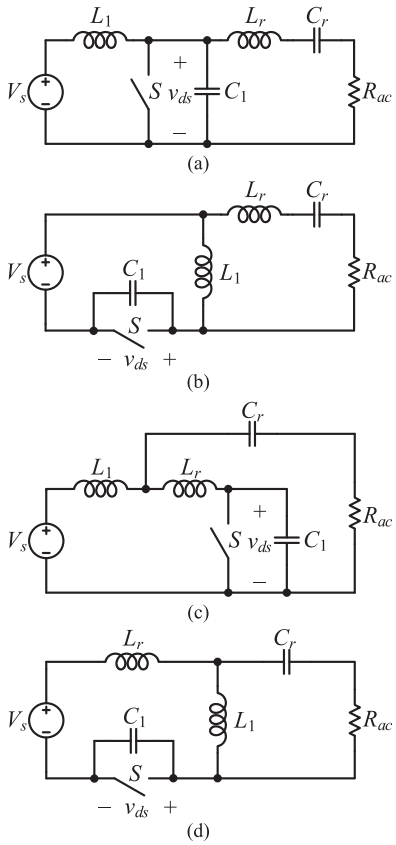

Fig. 5. Family of the proposed single-switch resonant dc-dc converters. Here, Rac represents the rectifier stage: (a) Topology A-I. (b) Topology A-II are derived from the network A. (c) Topology B-I. (d) Topology B-II originate from the network B.

two poles meet the requirements which are explained in the previous section. Likewise, the asymptotic impedance Bode plots of the networks B–D can be drawn as in Fig. 4(b)–(d). In all cases, $Z_{\rm ds}$ has two poles and one zero. This implies that the networks can also have the same shape of $|Z_{\rm ds}|$ as in Fig. 3(b) by designing L_1, L_r, C_1, C_r, and properly placing the diagrams of Z_1 and Z_2.

However, unlike the impedance networks A and B, the networks C and D require the additional assumption that the output capacitance of the switch, $C_{\rm oss}$, is far smaller than the other capacitances. Otherwise, the desired waveform of the switch voltage is not achievable. In fact, when the switching frequency is a few tens of MHz, C_1 and C_r are typically designed to be several hundreds of pF and $C_{\rm oss}$ is comparable to them. Thus, the design of the converter derived from the networks C or D is restricted to a certain frequency limit. In this paper, the networks C and D are excluded from the topology derivation due to this practical problem in the high-frequency design, and we here focus on the networks A and B.

Fig. 5 shows the family of the proposed single-switch resonant dc–dc converters derived from the impedance networks A and B. There are four converter topologies which are respectively named as Topology A-I, A-II, B-I, and B-II according to the position of the input dc voltage source V_s. Since the voltage source is considered as a short circuit at high frequencies, it can be added at the point $\rm A_1$, $\rm A_2$, $\rm B_1$, and $\rm B_2$ marked in Fig. 4(a) and (b) without harming the impedance $Z_{\rm ds}$. Here, the series connection of the voltage source and the capacitor is avoided when the connection points $\rm A_1-B_2$ are chosen. Then Topology A-I and A-II are derived from the network A of Fig. 4(a), and Topology B-I and B-II originate from the network B of Fig. 4(b). Also, the ac equivalent resistance $R_{\rm ac}$ is regarded as the rectifier because it is generally designed to seem resistive at the fundamental frequency. In the proposed converters, $R_{\rm ac}$ is connected in series with C_r, thereby eliminating the necessity of the additional dc blocking capacitor. Also, it should be noted that the current flowing through $R_{\rm ac}$ contains harmonic components since the output networks ($L_r-C_r-R_{\rm ac}$ branch for Topology A-I and A-II; $C_r-R_{\rm ac}$ branch for Topology B-I and B-II) have low impedance at the second-harmonic and third-harmonic frequencies as shown in the impedance plots of Fig. 5(a) and (b).

The common features of the proposed converter topologies are as follows: 1) the device output capacitance $C_{\rm oss}$ is absorbed into C_1, so its detrimental effects on the design and operation of the converter are removed; 2) the rectifier modeled as $R_{\rm ac}$ is connected in series to C_r. Hence, C_r plays a role in blocking the dc voltage as well as participating in the resonance, and thus an extra capacitor for dc-blocking is not required; 3) the converters contain no bulky energy-storage passive element. This property offers a benefit to the converter employing the on–off control: short settling time and fast transient response at the instant that the converter is activated and inactivated. Besides, the lower values of L_1 and L_r, which are typically in the order of a few hundred nH at the switching frequencies of several tens of MHz, allow the use of air-core inductors with a few turns of the windings. Then the losses associated with magnetic cores can be eliminated, and this is advantageous especially when the converter is operated in MHz-frequency ranges.

D. Comparison With the Conventional Converters

The switch-voltage waveforms of the proposed converters in Fig. 5 are shaped to almost square wave like those of the conventional ones, e.g., the class F and the class Φ_2 converters as noted above. In this section, we clarify the difference between the proposed converters and the conventional ones, even though their switch-voltage waveforms are almost identical.

Figs. 6 and 7 show the schematics and the drain-source impedance $Z_{\rm ds}$ of the class F and Φ_2 converters, respectively. First, as seen in Fig. 6(a), the class F converter uses the parallel *LC* circuit $L_{s3}-C_{s3}$ which is tuned to the third harmonic $3\omega_s$ so that the output load network has high impedance to the third-harmonic content [19]. Besides, the resonant frequency of L_{s1} and C_{s1} is set to the switching frequency. As shown in Fig. 6(b), $Z_{\rm ds}$ of the class F converter is comprised of seven passive elements. Here, $L_{\rm dc}$ and $C_{\rm dc}$ act as a dc current source and a dc blocking capacitor, respectively, so their values are much larger than other elements and thus $Z_{\rm ds}$ is not affected by $L_{\rm dc}$ and $C_{\rm dc}$. Similarly, in the class Φ_2 converter of Fig. 7(a), the series *LC* circuit L_m–C_m which is tuned to the second harmonic $2\omega_s$ is connected in parallel with the switch *S*. Then its impedance network includes six passive elements as

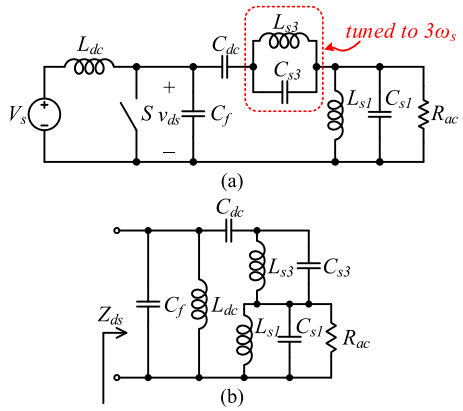

Fig. 6. (a) Schematic of the class F converter. (b) Drain-source impedance $Z_{\rm ds}$ of the class F converter.

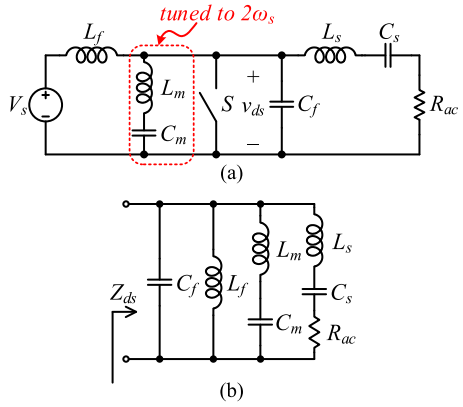

Fig. 7. (a) Schematic of the class Φ_2 converter. (b) Drain-source impedance $Z_{\rm ds}$ of the class Φ_2 converter.

TABLE I
COMPARISONS OF THE NUMBER OF PASSIVE ELEMENTS WITH THE CONVENTIONAL COUNTERPARTS

	Class F	Class Φ_2	Proposed
Passive elements consisting of $Z_{\rm ds}$	7	6	4
Bulky energy-storage elements	2($L_{\rm dc}, C_{\rm dc}$)	0	0

illustrated in Fig. 7(b). Though the class Φ_2 converter employs no bulky passive element such as $L_{\rm dc}$ and $C_{\rm dc}$, the output load network $L_s - C_s - R_{\rm ac}$ as well as L_f and C_f should be considered in designing $|Z_{\rm ds}|$ to have the same shape as in Fig. 3(b) and shaping the waveform of $v_{\rm ds}$ [22], [23].

Table I summarizes the comparisons of the number of the passive elements and the bulky elements constituting $Z_{\rm ds}$. As seen in the table, the class F and Φ_2 converters exploit two or three more elements than the proposed one. In other words, the proposed converter uses the reduced number of the passive elements, although it has the same switch-voltage waveform and switch voltage stress with the conventional counterparts. Furthermore, unlike the class E or F converter, the proposed converters do not contain the bulky energy-storage element. Utilizing only small-value inductors results in higher switch current stress compared to the class E converter having a large input inductor. However, removing the bulky passive element allows the advantage of the fast transient performance at the expense of the increased current stress. Therefore, the proposed converters are beneficial to the applications where the output is regulated by the on–off control and fast response is required as mentioned above.

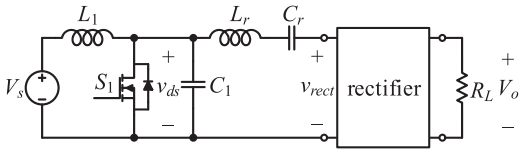

Fig. 8. Practical implementation of Topology A-I.

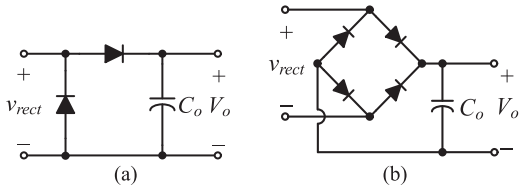

Fig. 9. Current-driven rectifier circuits: (a) a half-wave rectifier and (b) a full-bridge rectifier.

III. DESIGN OF PROPOSED CONVERTER TOPOLOGIES

In this section, we elaborate on the design procedure of the Topology A-I among the family of the proposed converters. The same design scheme can be applied to the Topologies A-II, B-I, and B-II owing to the topological similarities. In the proposed converters, it is too difficult to derive analytic equations for the design because four resonant inductors and capacitors produce a fourth-order state space and there exist multiple frequency contents due to the harmonics. This makes the resultant analytic solutions too complex and not intuitive. Hence, in this paper, a simple design scheme is presented based on some approximations and the above analysis of $Z_{\rm ds}$.

A. Design Equations

Fig. 8 shows the practical implementation of the Topology A-I by replacing $R_{\rm ac}$ in Fig. 5(a) with the rectifier circuit and the load resistor R_L. Though numerous types of the rectifier stage are possible, the current-driven class D rectifier is considered in this paper as seen in Fig. 9: a half-wave rectifier of Fig. 9(a) and a full-bridge rectifier of Fig. 9(b). From the approximation that the fundamental component is dominant, the half-wave rectifier and the full-bridge one are modeled into $R_{\rm ac} = 2R_L/\pi^2$ and $R_{\rm ac} = 8R_L/\pi^2$ respectively, as explained in [12, Ch. 2]. Then we proceed to design $L_1, C_1, L_r,$ and C_r, using the simplified circuit without the rectifier stage as in Fig. 5(a). This circuit can be easily transformed into one with the rectifier stage of Fig. 9(a) or (b) by applying the relationship between $R_{\rm ac}$ and R_L.

1) *Design of L_1 and C_1:* The drain-source impedance $Z_{\rm ds}$ of the Topology A-I is represented equivalently as in Fig. 4(a) assuming that the quality factor of the $L_r - C_r - R_{\rm ac}$ network is high enough to neglect $R_{\rm ac}$. Then, $Z_{\rm ds}(s)$ can

be expressed as

$$Z_{\rm ds}(s) \cong \frac{sL_1\left(s^2 L_r C_r + 1\right)}{s^4\left(L_1 C_1 L_r C_r\right) + s^2\left(L_1 C_1 + L_r C_r + L_1 C_r\right) + 1}. \tag{1}$$

As shown in the denominator of (1), the positions of two poles of $Z_{\rm ds}$ are dependent on all inductors and capacitors. On the other hand, the zero is determined by the resonant frequency of the $L_r - C_r$ circuit. Thus, to sufficiently attenuate the second-harmonic content in switch voltage, the $L_r - C_r$ circuit is tuned to $2\omega_s$ as depicted in the impedance plots of the network A [see Fig. 4(a)]. Also, L_r and C_r are designed to fulfill the desired output power and this will be described in detail below. Then the pole locations are manipulated by only L_1 and C_1. If ω_{p1} and ω_{p2} are denoted by $k_1 \cdot \omega_s$ and $k_2 \cdot \omega_s$, we can derive the expressions of L_1 and C_1 in terms of k_1 and k_2 by solving the equation that the denominator of (1) equals to zero

$$L_1 = \frac{4\left({k_1}^2 + {k_2}^2\right) - {k_1}^2 {k_2}^2 - 16}{4{k_1}^2 {k_2}^2 {\omega_s}^2 C_r} \tag{2}$$

$$C_1 = \frac{4}{{k_1}^2 {k_2}^2 {\omega_s}^2 L_1}. \tag{3}$$

As explained in Section II-B, two poles should be located around ω_s and $3\omega_s$ to make the switch-voltage waveform shaped to a near trapezoidal wave. Moreover, for ZVS and the reduced peak switch voltage, the following conditions should be satisfied: $\omega_{p1} > \omega_s$ and $\omega_{p2} < 3\omega_s$. First, the reason why ω_{p1} is placed at higher than ω_s is to achieve ZVS. For ZVS, $Z_{\rm ds}(j\omega_s)$ should be inductive because the zero crossing point of the switch voltage occurs prior to that of the switch current. Accordingly, ω_{p1} is higher than ω_s to make $Z_{\rm ds}(j\omega_s)$ inductive. In addition, the location of ω_{p2} influences the ratio of the third-harmonic voltage to the fundamental one, and it is proportional to $|Z_{\rm ds}(j3\omega_s)|$. Too large $|Z_{\rm ds}(j3\omega_s)|$ causes too high third-harmonic voltage, and the peak switch voltage is rather increased. Thus, $|Z_{\rm ds}(j3\omega_s)|$ has to be lower than $|Z_{\rm ds}(j\omega_s)|$ to reduce the switch voltage stress as intended. Also, considering that $Z_{\rm ds}(j\omega_s)$ is inductive, $Z_{\rm ds}(j3\omega_s)$ is required to be capacitive since the third-harmonic content should be almost in phase with the fundamental one as seen in Fig. 2. Therefore, ω_{p2} is selected below $3\omega_s$. Consequently, k_1 should be higher than 1, and k_2 should be lower than 3. Once k_1 and k_2 are chosen, L_1 and C_1 are designed by using (2) and (3). The effects of k_1 and k_2 on the switch-voltage waveform are observed in more detail below.

2) *Design of L_r and C_r:* The resonant frequency of the output network $L_r - C_r - R_{\rm ac}$ is set to $2\omega_s$ in order to locate the zero of $Z_{\rm ds}$ at the second harmonic as mentioned above. In addition, its quality factor is chosen for the desired output power. Then, L_r and C_r are obtained as

$$L_r = \frac{R_{\rm ac} Q_r}{\omega_r},\ C_r = \frac{1}{\omega_r R_{\rm ac} Q_r} \tag{4}$$

where ω_r and Q_r are the resonant frequency and quality factor of the $L_r - C_r$ circuit, respectively, which are represented by

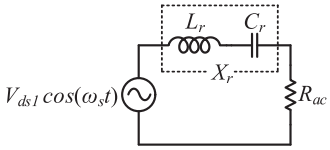

Fig. 10. Equivalent model of the output load network around the drive frequency.

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} = 2\omega_s \tag{5}$$

$$Q_r = \frac{1}{R_{\rm ac}}\sqrt{\frac{L_r}{C_r}}. \tag{6}$$

As shown in Fig. 10, $R_{\rm ac}$ and the reactance X_r consisting of L_r and C_r form a voltage divider, so the power delivered to $R_{\rm ac}$ is changed with the ratio between $R_{\rm ac}$ and X_r. By using (5) and (6), the reactance X_r at a certain frequency ω can be written as

$$X_r(\omega) = \omega L_r - \frac{1}{\omega C_r} = R_{\rm ac} Q_r \left(\frac{\omega^2 - {\omega_r}^2}{\omega_r \omega}\right). \tag{7}$$

Also, the ac voltage source, $V_{\rm ds1}\cos(\omega_s t)$, represents the fundamental component of the drain-source voltage $v_{\rm ds}$. The output power of the converter, P_o, is equal to the power transferred to $R_{\rm ac}$ if the loss of the rectifier is neglected. Then, considering that the peak value of the fundamental voltage, $V_{\rm ds1}$, is mainly contributed to the power, we can approximate P_o as

$$P_o = \frac{{V_{\rm ds1}}^2 R_{\rm ac}}{2\left[\left\{X_r(\omega_s)\right\}^2 + {R_{\rm ac}}^2\right]}. \tag{8}$$

In the proposed converters, $v_{\rm ds}$ is shaped into a near-square wave as explained above. To simply calculate $V_{\rm ds1}, v_{\rm ds}$ is further approximated to the square wave oscillating from 0 to $2V_s$ with 50% duty cycle, so $V_{\rm ds1}$ is calculated as $4V_s/\pi$. Then substituting the $V_{\rm ds1}$ value and (7) into (8) yields the following:

$$P_{\rm oN} = \frac{1}{\left(3Q_r/2\right)^2 + 1} \tag{9}$$

where $P_{\rm oN}$ denotes the normalized output power defined as

$$P_{\rm oN} \equiv \frac{P_o}{8{V_s}^2/\left(\pi^2 R_{\rm ac}\right)}. \tag{10}$$

Here, $P_{\rm oN}$ becomes unity when $X_r = 0$.

Fig. 11 plots the relationship between $P_{\rm oN}$ and Q_r from (9), showing that the output power of the converter is lower as Q_r increases. In order to verify the validity of the approximations applied to derive (9), we conducted the simulations where L_r and C_r were designed by (4) with various values of Q_r, and $k_1 = 1.1$, $k_2 = 2.9$ in (2) and (3) for determining L_1 and C_1. The simulation results are marked as the red triangles in Fig. 11. Although there are some errors in the low Q_r range, the calculated $P_{\rm oN}$ from (9) agrees well with the simulated one in the high Q_r range. The error is mainly attributed to the harmonic currents in $L_r - C_r - R_{\rm ac}$ network partially providing the power

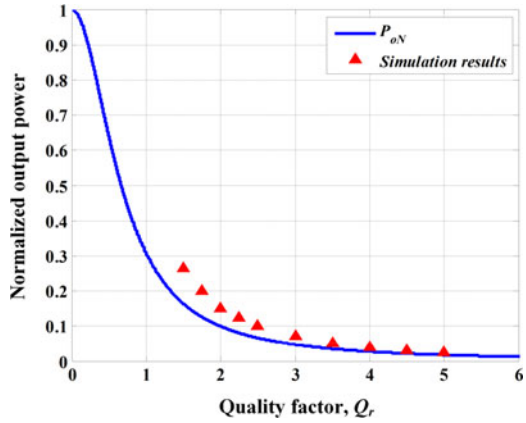

Fig. 11. Normalized output power $P_{\rm oN}$ with respect to quality factor Q_r. Also, the simulation results are marked as the red triangles.

and this becomes larger as Q_r decreases. In addition to this, too low Q_r leads to skewed waveform of $v_{\rm ds}$ since the second-harmonic voltage is not suppressed sufficiently, and this also makes an error in approximating $V_{\rm ds1}$. Nonetheless, the error is small enough in the reasonable range of Q_r, and in practice, (9) gives good starting values for choosing Q_r and designing L_r and C_r considering the design margin of the power. Consequently, if the desired output power of the converter is given, the required quality factor Q_r is determined as follows:

$$Q_r = \frac{2}{3}\sqrt{\frac{1}{P_{\rm oN}} - 1}. \tag{11}$$

B. Effects of the Pole Locations

The positions of ω_{p1} and ω_{p2} are related to the ZVS condition and the switch voltage stress respectively as explained above. To examine the effects of the pole locations on the drain-source voltage, the simulations are repeatedly executed when either k_1 $(=\omega_{p1}/\omega_s)$ or $k_2(=\omega_{p2}/\omega_s)$ is varied. As shown in Fig. 12(a), ZVS occurs when k_1 becomes higher than 1, whereas ZVS does not occur when k_1 is 1 or less. To achieve ZVS, k_1 is increased from 1 so that the phase angle of $Z_{\rm ds}(j\omega_s)$ is 30°–60° inductive as noted in [22], [23]. However, too high ω_{p1} causes the circulating energy for ZVS to be increased, leading to poor efficiency. In addition, the effect of k_2 can be observed in Fig. 12(b). As k_2 decreases from 3.2 to 2.8, the peak switch voltage is continuously reduced. Nevertheless, the duty cycle for the ZVS condition is also decreased with a smaller value of k_2 owing to the extended rising and falling time. In the proposed converters, k_2 is typically in the range of 2.8–3 to lower the voltage stress within 2.2–2.5 times the input voltage. Then the duty cycle is set to roughly 0.37–0.4, less than 0.5.

C. Impedance Transformation

It is so important in converter performance to properly determine Q_r. If $R_{\rm ac}$ is fixed, a lower value of Q_r leads to larger C_r as shown in (4), and thus (2) yields smaller L_1. Because too small L_1 increases circulating energy and conduction loss, too

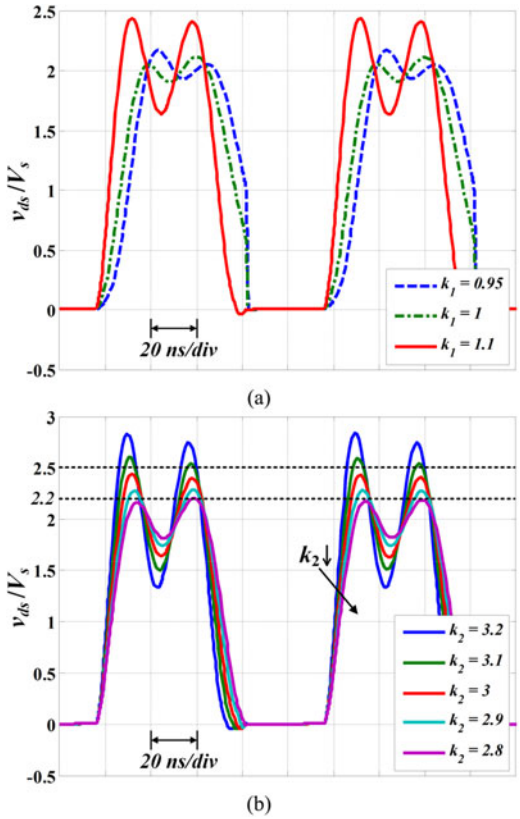

Fig. 12. Simulated waveforms of the drain-source voltage $v_{\rm ds}$ when either k_1 or k_2 is varied. (a) k_1 is changed from 0.95 to 1.1 with k_2 being fixed to 3. (b) k_2 is changed from 2.8 to 3.2 while k_1 is fixed to 1.1.

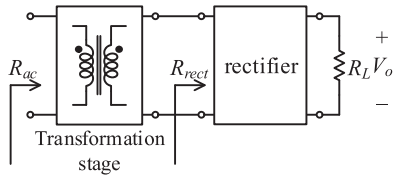

Fig. 13. Impedance transformation performed by the transformation stage.

low Q_r should be avoided. Besides, the drain-source voltage waveform is significantly deviated from the square wave due to low Q_r as mentioned above. On the other hand, higher Q_r results in lower $P_{\rm oN}$ as seen in Fig. 11, so the output power capability is decreased for the given V_s and $R_{\rm ac}$. Also, high Q_r implies relatively large resonant energy of the $L_r - C_r$ resonant tank compared to the power delivered to $R_{\rm ac}$. Therefore, as Q_r becomes higher, the ratio of the conduction loss in the $L_r - C_r$ circuit to the output power is increased, and it degrades the converter efficiency. Consequently, Q_r is typically selected in the range of 2–4 considering the tradeoff.

If Q_r calculated by (11) is too high or too low, a transformation stage can be utilized as in Fig. 13 to make Q_r within the reasonable range. The equivalent resistance of the rectifier circuit $R_{\rm rect}$ is changed to $R_{\rm ac}$ by the impedance transformation. Using (9), we can derive the dc voltage gain M_v of the converter

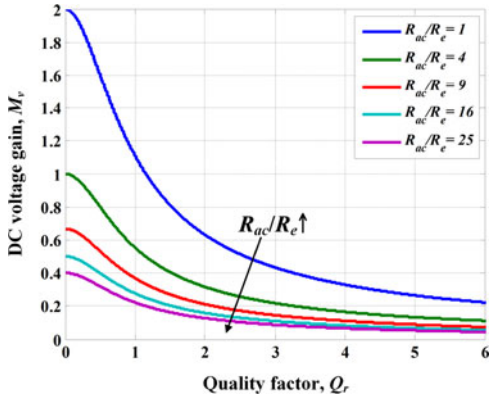

Fig. 14. DC voltage gain M_v with respect to Q_r for various $R_{\rm ac}/R_e$. Here R_e is defined as $2R_L/\pi^2$.

as

$$M_v \equiv \frac{V_o}{V_s} = 2\sqrt{\frac{1}{(3Q_r/2)^2+1}\cdot\left(\frac{1}{R_{\rm ac}/R_{\rm rect}}\right)\cdot\left(\frac{1}{R_{\rm rect}/R_e}\right)} \tag{12}$$

where R_e is $2R_L/\pi^2$, which corresponds to the equivalent resistance of the half-wave rectifier. Fig. 14 shows M_v with respect to Q_r for various $R_{\rm ac}/R_e$. If $R_{\rm ac}/R_e$ is fixed, M_v becomes lower as Q_r increases. On the other hand, Q_r is decreased with the increasing value of $R_{\rm ac}/R_e$ for a fixed M_v. This is also shown in (12). The value of Q_r required to provide a desired M_v becomes lower as $R_{\rm ac}/R_{\rm rect}$ or $R_{\rm rect}/R_e$ increases. If a transformer is used as the transformation stage, $R_{\rm ac}/R_{\rm rect}$ is proportional to the square of the turn ratio of the transformer. When the transformer has unity turn ratio, $R_{\rm ac}$ equals to $R_{\rm rect}$ as in the case that the transformation stage is not used. In fact, $R_{\rm rect}/R_e$ also affects Q_r, and it is dependent on the type of the rectifier such as the half-wave rectifier and the full-bridge rectifier as noted above. Hence, for the given M_v and R_L, the suitable value of Q_r can be obtained by modifying the gain of the transformation stage, e.g., the turn ratio of the transformer, or selecting the proper rectifier type.

D. Design Example and Simulation Results

A design example of the Topology A-I is presented in this section, and its specification is as follows. The input voltage V_s is 48 V and the output voltage V_o is 19 V. The output power P_o is 20 W, and the load R_L is 18.05 Ω. Also, the switching frequency is set to 10 MHz. Here, the half-wave rectifier of Fig. 9(a) is used without the transformation stage, so $R_{\rm ac} = 3.66\ \Omega$. Then, the following design procedures determine L_r, C_r, L_1, and C_1 of Fig. 8.

(Step I) Design L_r and C_r: First, the quality factor of L_r and C_r is calculated to fulfill the output power as explained in Section III-A. From (10), the normalized output power $P_{\rm oN}$ is 0.0392 for the given specification. Then, we obtain the quality factor as $Q_r = 3.3$ by using (11). Accordingly, substituting this into (4) yields $L_r = 96$ nH and $C_r = 660$ pF.

(Step II) Design L_1 and C_1: The next step is to design L_1 and C_1 by the pole locations of $Z_{\rm ds}$. Choosing k_1 and k_2 as 1.07 and 2.85, respectively, as discussed in Section III-B, we determine their values as $L_1 = 122$ nH and $C_1 = 896$ pF from (2) and (3).

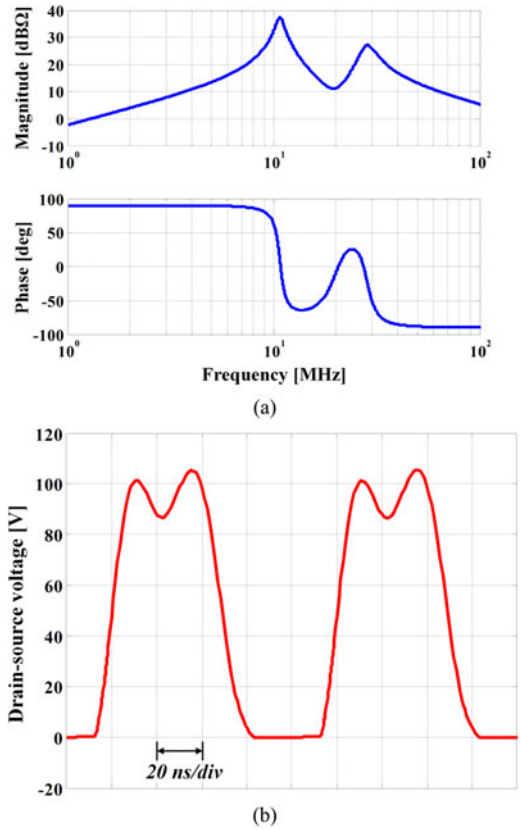

Fig. 15. (a) Magnitude and phase angle of $Z_{\rm ds}$. Here, $L_1 = 122$ nH, $C_1 = 896$ pF (including the device capacitance), $L_r = 96$ nH, $C_r = 660$ pF, and $R_{\rm ac} = 3.66\ \Omega$. (b) Simulated drain-source voltage waveform of Fig. 8 where the rectifier stage is a half-wave rectifier of Fig. 9(a) without transformation stage.

(Step III) Verify the Bode Plot of $Z_{\rm ds}$ and Simulation Results: Fig. 15(a) shows the magnitude and the phase angle of $Z_{\rm ds}$, and Fig. 15(b) displays the SPICE simulation of Fig. 8 with the nonlinearity of the device capacitance reflected. For the designed L and C values, $Z_{\rm ds}$ is 62° inductive at 10 MHz, leading to ZVS as seen in the simulation waveform. Also, the resultant magnitude of $Z_{\rm ds}$ is similar to Fig. 3(b): It is high at 10 MHz and 30 MHz and is low at 20 MHz. In addition, $Z_{\rm ds}$ is capacitive at 30 MHz, and $|Z_{\rm ds}(f_s = 30\ \text{MHz})|$ is much lower than $|Z_{\rm ds}(f_s = 10\ \text{MHz})|$. Thus, the drain-source voltage of Fig. 15(b) exhibits a near trapezoidal waveform as expected, and when V_s is 48 V, the peak switch voltage is 105.8 V, which is roughly 2.2 times higher than V_s.

IV. Experimental Results

A. Implementation

To verify the feasibility of the proposed converters, the Topology A-I is implemented and tested. The specification is the same as in the design example of Section III-D. Fig. 16 shows the implementation of the Topology A-I with the half-wave rectifier, and the components are listed in Table II. Here, the enhancement-mode GaN HEMT utilized as the switch S_1

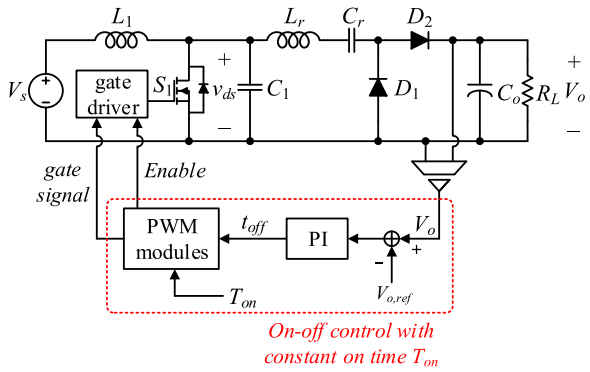

Fig. 16. Implementation of the Topology A-I and its on–off controller.

TABLE II
LIST OF COMPONENTS OF THE 10-MHZ 20-W TOPOLOGY A-I

Parameter	Value
L_1	117 nH
S_1	EPC2010C (GaN HEMT from EPC)
C_1	590 pF (externally connected in parallel with S_1)
L_r	90 nH
C_r	660 pF
D_1, D_2	DB24417
C_o	32 μF

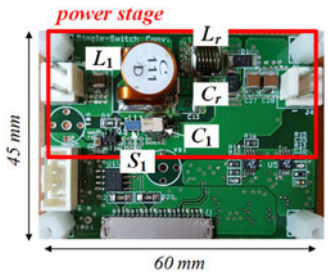

Fig. 17. 10-MHz laboratory prototype of the Topology A-I.

especially has the advantages of less gate charge and zero reverse recovery loss. Thus, it is more beneficial to switching at high frequency than Si-based MOSFETs. Together with its output capacitance, the capacitors are externally connected in parallel to augment the C_1 value. Also, L_1 and L_r are implemented with the air-core inductors to eliminate the effect of the core loss at high frequency. A photograph of the 10-MHz, 20-W laboratory prototype is shown in Fig. 17.

As noted in Section II-A, the on–off control is employed to regulate the output voltage of the proposed converters. While the converter is turned ON, the resonance of the L and C elements is not affected by the load variation because the output voltage is regarded as a constant dc voltage during the on–off control. Therefore, the drain-source voltage waveform as well as the ZVS operation is maintained, although the load R_L is changed. Consequently, the on–off control permits the fixed switching frequency and duty cycle of the power stage over a wide load range. Also, this implies that it is sufficient to design the converter for the full load.

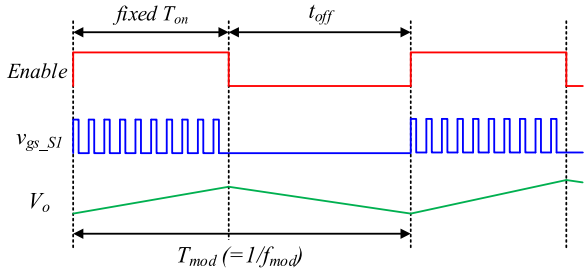

Fig. 18. Operation of the on–off control with the constant turn-on time $T_{\rm on}$.

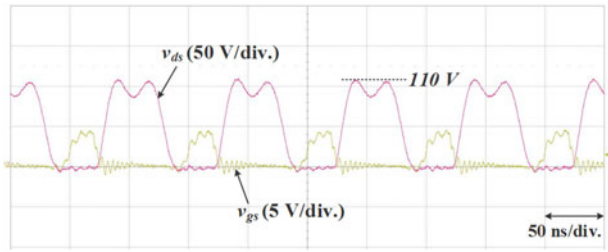

Fig. 19. Experimental waveforms of gate-source and drain-source voltages of Topology A-I when $V_s = 48$ V and load = 100%.

Among various types of the on–off control, a constant-on-time on–off control is applied as seen in Fig. 16. Its operation is illustrated in Fig. 18: While the turn-on time $T_{\rm on}$ is fixed, the turn-off time $t_{\rm off}$ is modulated depending on the output voltage error. Then the output power is decreased as the ratio of $t_{\rm off}$ to $T_{\rm on}(= t_{\rm off}/T_{\rm on})$ increases. In other words, if the load current decreases, $t_{\rm off}$ increases and the on–off modulation frequency $f_{\rm mod}$ decreases. Besides, the on–off control inherently causes the output voltage ripple of which the frequency is $f_{\rm mod}$ as shown in Fig. 18. Thus, the output capacitor C_o is properly sized to attenuate the ripple attributed to the on–off control. The size of C_o can be reduced by selecting $T_{\rm on}$ as short as possible since the smaller value of $T_{\rm on}$ lowers the voltage ripple for the same capacitance. However, too short $T_{\rm on}$ leads to too high $f_{\rm mod}$, and the efficiency deteriorates since the losses in the turn-on and turn-off transient periods significantly degrade the efficiency at high $f_{\rm mod}$. Considering this, $T_{\rm on}$ is set to 5 μs, and C_o is designed as 32 μF in this paper.

B. Experimental Results

Fig. 19 shows the experimental waveforms of the proposed converter when $V_{\rm s}$ is 48 V and the load is 100%. The gate-source voltage, $v_{\rm gs}$, and the drain-source voltage, $v_{\rm ds}$, demonstrate that ZVS occurs. Also, the waveform of $v_{\rm ds}$ is close to the trapezoid and includes the third-harmonic content as designed. The maximum value of $v_{\rm ds}$ is measured as 110 V, so the peak switch voltage of the converter is about 2.29 times the input voltage.

Figs. 20 and 21 exhibit the operation of the proposed converter under 80% load and 40% load, respectively. Compared to Fig. 19, the steady-state waveforms of $v_{\rm ds}$ in Figs. 20(a) and 21(a) are the same with that of the 100%-load condition, which is due to the on–off control as explained above. Consequently, the peak switch voltage remains at 110 V, roughly 2.29 times the input voltage. In addition to the near trapezoidal shape of $v_{\rm ds}$,

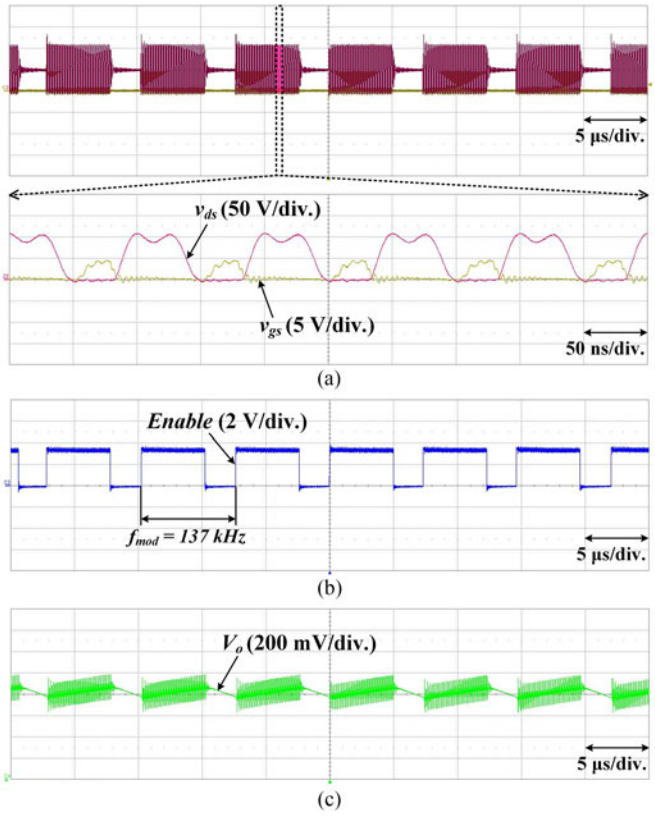

Fig. 20. Experimental waveforms during the on–off control when $V_s = 48$ V and load $= 80\%$. (a) $v_{\rm gs}$ and $v_{\rm ds}$. (b) Enable signal. (c) V_o with –19 V offset.

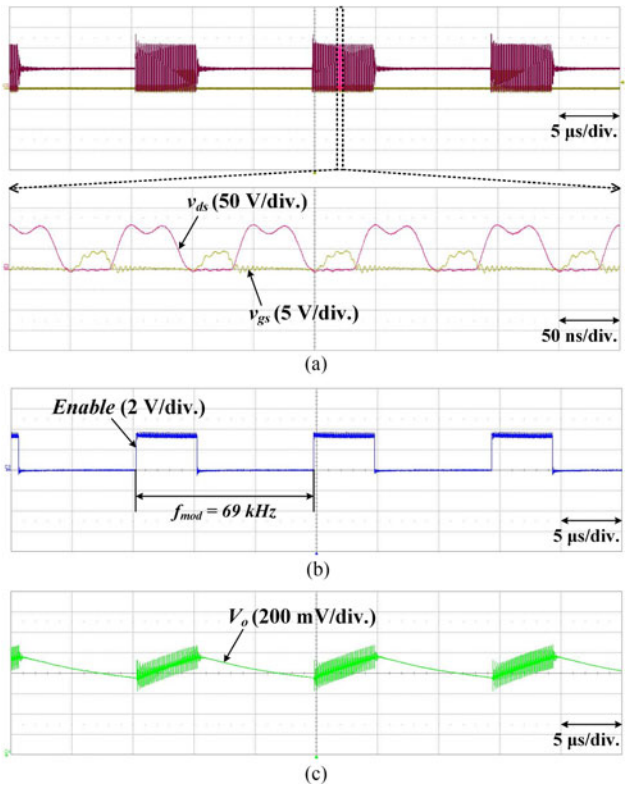

Fig. 21. Experimental waveforms during the on–off control when $V_s = 48$ V and load $= 40\%$. (a) $v_{\rm gs}$ and $v_{\rm ds}$. (b) Enable signal. (c) V_o with –19 V offset.

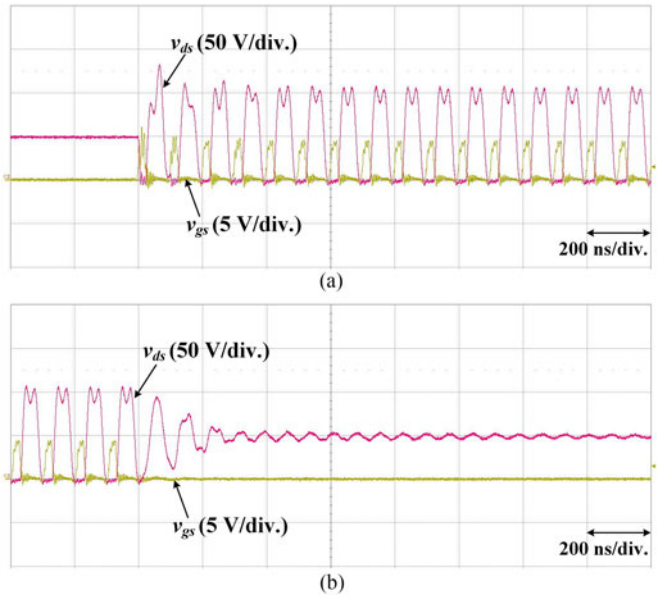

Fig. 22. (a) Turn-on transient response and (b) turn-off transient response of the converter. $V_s = 48$ V.

ZVS still occurs, although the load becomes lighter. As a result, it is verified that the proposed converter achieves both ZVS and the low switch voltage stress across the given load range. Besides, the turn-off time of the converter becomes longer when the load is changed from 80% to 40% as shown in Figs. 20(b) and 21(b). Accordingly, $f_{\rm mod}$ is decreased from 137 to 69 kHz. In this prototype, $f_{\rm mod}$ varies from 34 to 175 kHz when the load is changed from 20 to 100%. Figs. 20(c) and 21(c) display the output voltage ripple while the output voltage is controlled to 19 V. As the load decreases, the low-frequency ripple caused by the on–off control is slightly increased, but its peak-to-peak value is kept within 500 mV for the entire load range.

The waveforms in Fig. 22 show the turn-on and turn-off transient responses when $V_s = 48$ V. The converter reaches the steady state within a few switching periods after it is turned ON or turned OFF. The short settling time is thanks to the absence of the bulky inductor in the converter, and thereby this makes the proposed converter suited to the on–off control, as discussed above.

Fig. 23 plots the measured efficiency and calculated efficiency of the proposed converter when V_s is 48 V and V_o is 19 V. To calculate the efficiency as in [12, Ch. 12], the following factors are considered: the conduction losses due to the equivalent series resistances of the inductors and the capacitors; the conduction loss and turn-off switching loss of the switch; the conduction losses in two diodes of the half-wave rectifier. As a result, the calculated efficiency is 78% at full load, and the conduction losses in the inductors dominate the other loss components. For the ideal operation of the on–off control, the efficiency is calculated at the constant value regardless of the load current. However, in practice, the loss attributed to the turn-on and turn-off transient operations of the converter affects the efficiency. Because the amount of this additional loss is fixed irrespective of the load, the efficiency is gradually decreased as the load decreases.

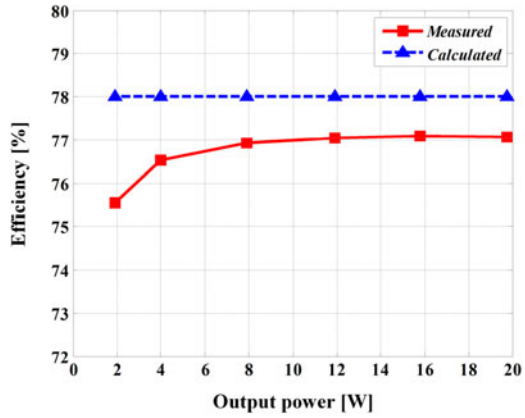

Fig. 23. Efficiency of the proposed converter. $V_s = 48$ V, and $V_o = 19$ V.

As demonstrated in Fig. 23, the efficiency of the prototype is measured as 77% at the full load and is slightly decreased for the lighter load. Nevertheless, the converter maintains similar efficiency across the output power range, and the efficiency is kept above 75% even under light loads, which is another benefit of the on–off control.

V. Conclusion

A family of the single-switch resonant converters proposed here has advantages for operating at a few MHz, and it features low switch voltage stress. The converters named as Topology A-I, A-II, B-I, and B-II are derived from the impedance networks by combining two inductors and two capacitors to offer the desired magnitude of the drain-source impedance $Z_{\rm ds}$. Then the drain-source voltage of the proposed converters is shaped toward a trapezoidal wave. Although the class F, $\rm EF_2$, and Φ_2 topologies have the similar shape of the drain-source voltage, the proposed converters utilize the reduced number of passive elements without the addition of harmonic-tuned circuit. This allows a compact design of the converter. Furthermore, this paper presents a relatively simple and specific design scheme based on the analysis of $Z_{\rm ds}$. By properly placing two poles and one zero of $Z_{\rm ds}$ associated with the four resonant elements, the proposed converters achieve the reduced switch voltage stress as well as ZVS operation. Among the family of the proposed single-switch converters, Topology A-I is designed and implemented. The 20-W GaN-based prototype experimentally validates the design scheme and operation of the proposed converter at 10-MHz switching frequency. The prototype has the peak switch voltage of about 2.29 times the input voltage and the efficiency of 77% at the full load. Also, thanks to the on–off control, it maintains the low voltage stress and ZVS property even for light loads.

References

[1] A. Knott *et al.*, "Evolution of very high frequency power supplies," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 3, pp. 386–394, Sep. 2014.

[2] W. Liang, J. Glaser, and J. Rivas, "13.56 MHz high power density DC-DC converter with PCB inductors," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4291–4301, Aug. 2015.

[3] D. J. Perreault *et al.*, "Opportunities and challenges in very high frequency power conversion," in *Proc. Appl. Power Electron. Conf. Expo.*, 2009, pp. 1–14.

[4] M. P. Madsen, A. Knott, and M. A. E. Andersen, "Very high frequency resonant DC/DC converters for LED lighting," in *Proc. Appl. Power Electron. Conf. Expo.*, 2013, pp. 835–839.

[5] W. Liang, L. Raymond, L. Gu, and J. Rivas, "27.12 MHz GaN resonant power converter with PCB embedded resonant air core inductors and capacitors," in *Proc. Energy Convers. Cong. Expo.*, 2015, pp. 4251–4256.

[6] D. Reusch and J. Strydom, "Evaluation of gallium nitride transistors in high frequency resonant and soft-switching DC-DC converters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5151–5158, Sep. 2015.

[7] K.-H. Liu and F. C. Lee, "Zero-voltage switching technique in DC-DC converters," *IEEE Trans. Power Electron.*, vol. 5, no. 3, pp. 293–304, Jul. 1990.

[8] W. A. Tabisz and F. C. Lee, "Zero-voltage-switching multi-resonant technique–a novel approach to improve performance of high frequency quasi-resonant converters," in *Proc. Power Electron. Spec. Conf.*, Apr. 1988, pp. 9–17.

[9] M. M. Jovanovic, "Merits and limitations of resonant and soft-switched converters," *in Proc. Telecommun. Energy Conf.*, 1992, pp. 51–58.

[10] W. Zhang, X. Huang, F. C. Lee, and Q. Li, "Gate drive design considerations for high voltage cascode GaN HEMT," in *Proc. Appl. Power Electron. Conf. Expo.*, 2014, pp. 1484–1489.

[11] I. D. de Vries, J. H. van Nierop, and J. R. Greene, "Solid state class DE RF power source," in *Proc. IEEE Symp. Ind. Electron.*, 1998, pp. 524–529.

[12] M. K. Kazimierczuk and D. Czarkowski, *Resonant Power Converters*, 2nd ed. New York, NY, USA: Wiley, 2011.

[13] M. J. Chudobiak, "The use of parasitic nonlinear capacitors in class E amplifiers," *IEEE Trans. Circuits Syst. I*, vol. 41, no. 12, pp. 941–944, Dec. 1994.

[14] G.-B. Koo, "Design guidelines for RCD snubber of flyback converters," Fairchild Application Note AN-4147, 2006.

[15] T. Suetsugu and M. K. Kazimierczuk, "Voltage clamped class-E amplifier with Zener diode," *IEEE Trans. Circuits Syst. I*, vol. 50, no. 10, pp. 1347–1349, Oct. 2003.

[16] T. Suetsugu and M. K. Kazimierczuk, "Design procedure for lossless voltage-clamped class E amplifier with a transformer and a diode," *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 56–64, Jan. 2005.

[17] Y.-J. Woo, S.-K. Kim, and G.-H. Cho, "Voltage-clamped class-E inverter with harmonic tuning network for magnetron drive," *IEEE Trans. Circuits Syst. II*, vol. 53, no. 12, pp. 1456–1460, Dec. 2006.

[18] A. Mediano and N. O. Sokal, "A class-E RF power amplifier with a flat-top transistor-voltage waveform," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5215–5221, Nov. 2013.

[19] F. H. Raab, "Class-E, class-C, and class-F power amplifiers based upon a finite number of harmonics," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 8, pp. 1462–1468, Aug. 2001.

[20] S. Aldhaher, D. C. Yates, and P. D. Mitcheson, "Modeling and analysis of class EF and class E/F inverters with series-tuned resonant networks," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3415–3430, May 2016.

[21] Z. Kaczmarczyk, "High-efficiency class E, EF2, and E/F3 inverters," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1584–1593, Oct. 2006.

[22] J. M. Rivas, Y. Han, O. Leitermann, A. D. Sagneri, and D. J. Perreault, "A high-frequency resonant inverter topology with low-voltage stress," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1759–1771, Jul. 2008.

[23] J. M. Rivas, O. Leitermann, Y. Han, and D. J. Perreault, "A very high-frequency DC-DC converter based on a class $\Phi 2$ resonant inverter," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2980–2992, Oct. 2011.

[24] R. C. N. Pilawa-Podgurski, A. D. Sagneri, J. M. Rivas, D. I. Anderson, and D. J. Perreault, "Very-high-frequency resonant boost converters," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1654–1665, Jun. 2009.

[25] K.-H. Lee, E. Chung, Y. Han, and J.-I. Ha, "Design and control of 10-MHz class E DC-DC converter with reduced switch voltage stress," in *Proc. Energy Convers. Cong. Expo.*, 2015, pp. 4257–4263.

[26] E. Chung, K.-H. Lee, Y. Han, and J.-I. Ha, "Design of single switch DC-DC converter with parasitic parameters," in *Proc. Energy Convers. Cong. Expo.*, 2015, pp. 1455–1460.

[27] J. M. Rivas, R. S. Wahby, J. S. Shafran, and D. J. Perreault, "New architectures for radio-frequency DC-DC power conversion," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 380–393, Mar. 2006.

[28] J. Hu, A. D. Sagneri, J. M. Rivas, Y. Han, S. M. Davis, and D. J. Perreault, "High-frequency resonant SEPIC converter with wide input and output voltage ranges," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 189–200, Jan. 2012.

[29] M. Kovacevic, A. Knott, and M. A. E. Andersen, "A VHF interleaved self-oscillating resonant SEPIC converter with phase-shift burst-mode control," in *Proc. Appl. Power Electron. Conf. Expo.*, 2014, pp. 1402–1408.
[30] Z. Zhang, J. Lin, Y. Zhou, and X. Ren, "Analysis and decoupling design of a 30 MHz resonant SEPIC converter," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4536–4548, Jun. 2016.
[31] Y. Zhou, Z. Zhang, X.-W. Zou, Z. Dong, and X. Ren, "A 10-MHz isolated class-Φ_2 synchronous resonant dc-dc converter," in *Proc. Appl. Power Electron. Conf. Expo.*, 2016, pp. 73–78.

Kyung-Hwan Lee (S'13) received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 2013, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include design and control of dc–dc converters, and high-frequency power conversion.

Euihoon Chung (S'14) received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 2014, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include design of dc–dc converters and high-frequency power conversion.

Yongsu Han (S'12) was born in Korea, in 1988. He received the B.S. degree in electrical engineering, in 2011, from Seoul National University, Seoul, Korea, where he is currently working toward the Ph.D. degree.

His current research interests include electric machine drives, control of dc–dc converters, and renewable energy conversion system.

Jung-Ik Ha (S'97–M'01–SM'12) was born in Korea, in 1971. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1995, 1997, and 2001, respectively.

From 2001 to 2002, he was a Researcher in Yaskawa Electric Co., Japan. From 2003 to 2008, he worked for Samsung Electronics Co., Korea as a Senior and Principal Engineer. From 2009 to 2010, he was a Chief Technology Officer, LS Mechapion Co., Korea. Since 2010, he has been with the Department of Electrical and Computer Engineering, Seoul National University, Seoul, Korea, where he is currently an Associate Professor. His research interests include circuits and control in high efficiency, and integrated electric energy conversions for various industrial fields.