A 1 MHz Half-Bridge Resonant DC/DC Converter Based on GaN FETs and Planar Magnetics

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***Abstract*—A 1 MHz half-bridge resonant dc/dc converter based on GaN FETs and planar magnetics is proposed in this paper, which improves the system efficiency and power density. The resonant network can achieve satisfactory soft-switching characteristics based on a small impedance angle, which greatly reduces the losses of switches and diodes. The losses characteristics during the turn-on and turn-off transitions are analyzed in detail. The calculation results show that the GaN FETs with low output capacitance and on resistance can achieve fast switching speed and low losses in high-frequency conditions. To reduce the profile and increase the power density of the system, planar magnetics are used in this paper. The response surface methodology (RSM) and modular layer model (MLM) are adopted to help design the planar inductor and transformer, respectively. Both of the methods offer clearer and more effective ways to design the planar magnetics. A 25-W prototype is built to verify the feasibility of the proposed high-frequency converter.**

***Index Terms*—GaN FETs, high frequency, planar magnetics, resonant converter.**

I. Introduction

OVER the past several years, with the fast development of electronic power conversion technology, the feature of high power density is extremely expected in many fields, such as LED drivers, chargers, and consumer electronics [1]–[3]. The small size and lightweight can make the power electronic systems more portable and space-saving, which are important qualities to attract consumers. To achieve the aforementioned goals, the operating frequency of the switch-mode power supplies (SMPS) must be increased. By a higher operating frequency, the value and volume of passive elements can be greatly decreased [4]–[6].

However, a higher operating frequency will lead to greater system losses, which are mainly composed of semiconductor devices' switching losses and magnetic elements' losses. These losses are proportional to the system operating frequency and limit the system efficiency at high operating frequency. At the same time, many standards have put forward more stringent requirements to system efficiency. To deal with the aforementioned contradiction between efficiency and operating frequency, proper methods must be applied to improve the efficiency characteristics at high operating frequency. Researchers mainly focus on the following three points: the first is the research on resonant topologies, the second is the research on new material semiconductor device applications, and the third is the research on materials and structures of magnetics.

Resonant topologies with soft-switching characteristics, such as series resonant converter, parallel resonant converter, and other high-order resonant converters, have been widely used to improve the system efficiency [7]–[11]. Both the zero-voltage switching (ZVS) characteristics and the zero-current switching (ZCS) characteristics can achieve almost no losses during the turn-on or turn-off instant of semiconductor devices. In [12], a high-frequency *LCL* resonant converter with dual-tank is proposed, which can achieve ZVS turn-on for both of the switches and can be applied in small-scale wind energy conversion systems. In [13], a 500 kHz *LLC* resonant converter with high power density is analyzed and designed. It has been successfully verified that the volumes of passive components (transformer and output capacitor) can be greatly reduced at high frequency. The output voltage ripple also decreases at higher operating frequency. Meanwhile, the ZVS feature of switches and ZCS feature of diodes are also maintained. However, most of the resonant converters only focus on the ZVS turn-on characteristics of switches, the switch turn-off current is still high. So in high-operating-frequency conditions, the turn-off losses severely reduce the system efficiency.

Meanwhile, many power ICs have been developed whose operating frequencies are several megahertz, such as the EP53F8QI, EN23F0QI from Altera's Enpirion and LTM8042 from Linear Technology. However, most of the state-of-the-art ICs are based on nonisolated topologies such as synchronous buck and boost circuits, etc., which cannot be applied in isolating conditions. Besides that, some very high frequency (VHF) converters whose working frequencies are in the range 30–300 MHz, have been proposed, such as the resonant Boost converter, the resonant Sepic converter [14]–[16].

As the increasing of operating frequencies, the losses of inductors and transformers also increase correspondingly. So many factors must be taken into consideration carefully, such as core materials, core structures, and winding structures. The

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values of the inductors and transformers are reduced at high operating frequency, which helps to use a smaller size core. At the same time, the magnetics take the maximum vertical space in systems, so planar magnetics with low profile are more and more widely adopted in high-frequency converters to reduce the height and volume of converters [17]–[21]. For planar magnetics, a great surface area can help to improve the heat dissipation capability. At the same time, with greater magnetic cross-section area, fewer turns are needed to reach the designed inductance. The copper tracks on printed circuit board (PCB) are mostly adopted as the windings of the planar magnetics instead of the litz wires. In summary, planar magnetics have many merits compared with the traditional type cores, such as low profile, good reproductive feature, and so on.

However, some challenges need to be solved about the design of planar magnetics as mentioned earlier, the turns and structure of windings on PCB cannot be changed flexibly once the PCB is manufactured, so the planar magnetics should be modeled as accurate as possible in the design process. For resonant converters operating in high operating frequency conditions, a small deviation of resonant parameters will greatly affect the circuit operating situations. There are many factors affecting the parameters and parasitic parameters of the magnetics, at the same time, some factors are coupled. By some complex and time consumption three-dimensional (3-D) simulations, the parameters of planar magnetics can be obtained; however, clear design concepts and models are not available. So to achieve a clearer and more effective design process, some proper methods should be adopted to help design the planar magnetics, such as response surface methodology (RSM) [22]–[26] and modular layer model (MLM) [27].

Another part of the system losses is corresponding to characteristics of the device itself, such as the on losses and parasitic capacitor losses. With the fast development of semiconductor devices, the performance of the silicon (Si) devices has almost reached the theoretical limits, especially the on-resistance and parasitic parameters [28]. New type material devices, such as Gallium nitride (GaN) and silicon carbide (SiC), have wider band gap and higher electron mobility than Si devices, which can guarantee much lower on-resistance comparing with the traditional devices at the same voltage level. By the increasingly sophisticated production techniques, the GaN devices show their perfect performances in high-frequency situations and have been used in some applications. In [29] and [30], GaN FETs are adopted in hard-switching-mode converters in the field of point of load (POL), though in the hard-switching mode, the system efficiencies still increase. Wu *et al.* [31] build a power factor correction circuit based on GaN FETs. In [32] and [33], after using GaN FETs, the properties of these resonant converters are greatly improved. Reusch and Strydom [34] propose a 1.2 MHz full-bridge resonant circuit with electrical isolation property. Based on GaN FETs, the system achieves a 25% decrease in device power losses comparing with the one using Si MOSFETs. The characteristics of low output charge losses and low gate charge losses are described in detail. These aforementioned characteristics suggest that GaN FETs are good replacements of Si MOSFETs.

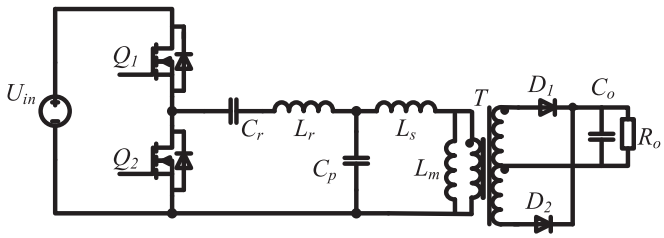

Fig. 1. Circuit of the half-bridge CLCL converter.

Wang *et al*. [35] propose a CLCL resonant topology; with the satisfactory soft-switching characteristics, it is more suitable for operating at higher frequency. Based on the CLCL circuit, further studies are conducted and high-frequency implementation solution is proposed in this paper. The CLCL converter can be applied in many dc/dc transferring fields, such as intermediate bus converters, automotive, and photovoltaic systems. In the proposed 1 MHz CLCL converter, the GaN FETs and planar magnetics are adopted. Section II introduces the working principles of the CLCL topology. Meanwhile, the switch losses during the turn-on and turn-off transitions are analyzed, which helps to design the impedance angle and system parameters. The analysis and design of planar inductors and transformers are described in Section III. RSM is introduced to design planar inductors, which can help to establish the linear and nonlinear relationships between corresponding factors. MLM is adopted to design planar transformers, which can help to choose the best winding layout to achieve smallest leakage inductances and other parasitic parameters. In Section IV, a 25 W prototype aimed for secondary power supply is built, which the input voltage is 80 V and the output voltage is 15 V. Meanwhile, a comparison between the presented solution and the other state-of-the-art solutions is given. The conclusion is provided in section V.

II. Working Principle and Analysis of the CLCL Converter

Fig. 1 shows the circuit of the half-bridge CLCL converter. Q_1 and Q_2 represent the switches, and four passive components: C_r, L_r, L_s, and C_p form the resonant tank. T represents the transformer, D_1 and D_2 are the rectifier diodes in the secondary side. C_o is the filter capacitor, R_o is the output load. The pulse frequency modulation (PFM) control strategy is adopted in the CLCL converter, and the duty cycle of each switch is 50% neglecting the dead time.

A. Analysis of the CLCL Converter

For the CLCL resonant converter, the operating process in one working period can be separated into ten different modes. Half of the ten working modes are shown in Fig. 2 and described in detail as follows. The voltage and current waveforms are shown in Fig. 3.

Mode 1 ($t_0 - t_1$): At t_0, the driving signal level of Q_2 becomes zero and it turns off. The current i_{cr} increases, capacitor C_{ds2} is charged, and capacitor C_{ds1} is discharged. The rectifier

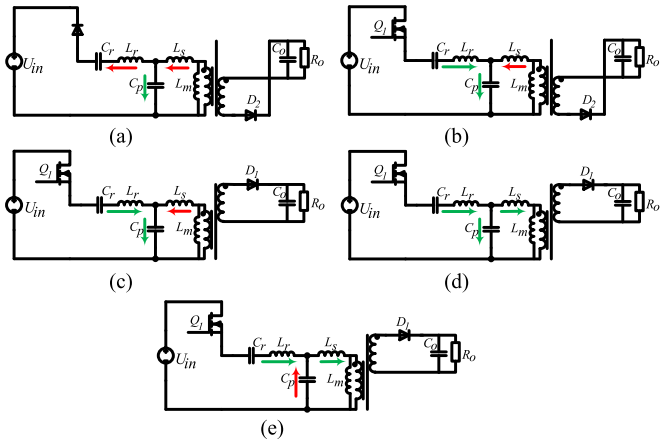

Fig. 2. Working modes of the CLCL converter. (a) Mode 1 $[t_0 - t_1]$, (b) Mode 2 $[t_1 - t_2]$, (c) Mode 3 $[t_2 - t_3]$, (d) Mode 4 $[t_3 - t_4]$, (e) Mode 5 $[t_4 - t_5]$.

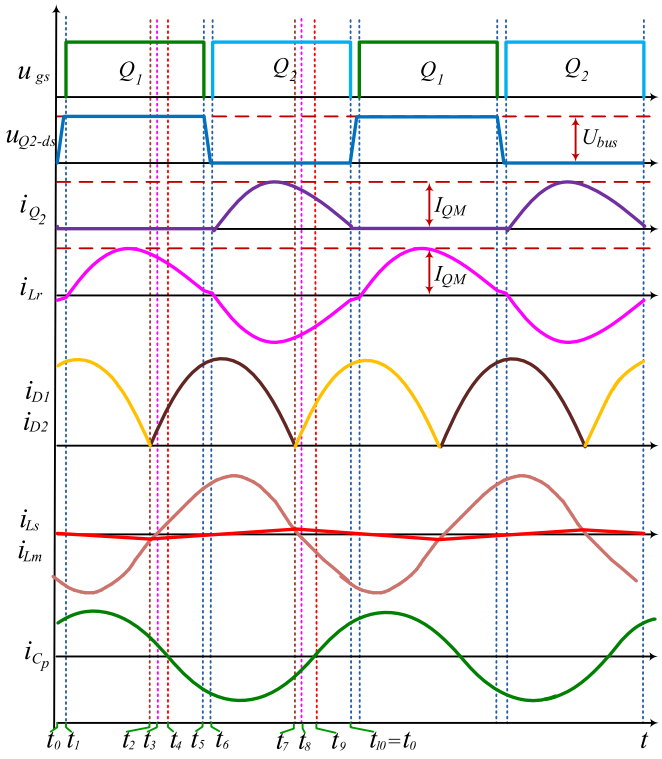

Fig. 3. Main current and voltage waveforms of the CLCL converter.

diode D_2 is still on, so the voltage of L_m is clamped by the output voltage to be -nV_o. This mode ends at t_1.

Mode 2 ($t_1 - t_2$): At t_1, the driving signal of Q_1 is applied and the drain-source voltage of Q_1 has already been zero. The current i_{cr} is zero and then increases. The rectifier diode D_2 is still on, and U_{Lm} is $-nVo$. Therefore, the current i_{Lm} decreases linearly. When i_{Lm} equals i_{Ls}, the current transferred to the secondary side is zero, and D_2 turns off in the ZCS mode naturally. At this time, i_{Lm} reaches its minimum value and this mode ends.

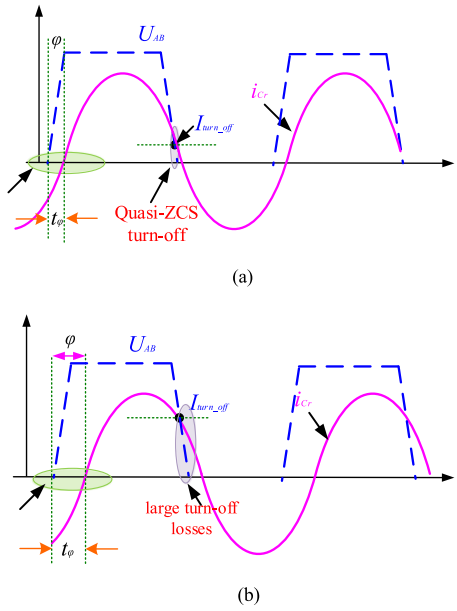

Fig. 4. Waveforms comparison between the CLCL resonant tank and *LLC* resonant tank. (a) The input voltage and current of CLCL resonant tank. (b) The input voltage and current of *LLC* resonant tank.

Mode 3 ($t_2 - t_3$): At t_2, this mode begins. The current of L_s continues to increase towards zero, and the current transferred to the secondary side reverses. Therefore, diode D_1 turns on and then U_{Lm} begins to be clamped at nVo. The current i_{Lm} starts to increase, and C_p continues to be charged. At t_3, the current i_{Ls} resonates to zero, and this mode ends.

Mode 4 ($t_3 - t_4$): In this mode, the current i_{Ls} begins to increase above zero, the current i_{Lm} continues to increase linearly, and the resonant current i_{cp} decreases. At time t_4, the current i_{cp} resonates to zero, so the voltage U_{cp} reaches its peak value in the positive direction. This mode ends at t_4.

Mode 5 ($t_4 - t_5$): In this mode, C_p begins to discharge, the resonant current of L_s keeps increasing, and the resonant current i_{cr} decreases. Until t_5, the driving signal level of Q_1 becomes zero and the current i_{cr} resonates to almost zero. Therefore, the turn-off losses are quiet low. The next five working modes are similar to the former ones, and then a new period begins.

As shown in Fig. 3, one of the main advantages of the CLCL converter is that the voltage and current are in same phase ideally, so the switch Q_1 and Q_2 can achieve ZVS characteristics at turn-on instant and ZCS characteristics at turn-off instant, which can be seen in Fig. 4(a). In the ideal condition, there are no losses during the switching transition. However, for the traditional *LLC* circuit, when the circuit works at the resonant frequency, the impedance of the resonant tank is inductive, which means that the resonant current has to fall behind the voltage at large phase angle. As can be seen in Fig. 4(b), in this condition, though the switch can achieve ZVS, the turn-off current is high, which cause large turn-off losses.

To further analyze the properties of CLCL resonant tank, the equivalent resonant tank circuit is shown in Fig. 5, where the

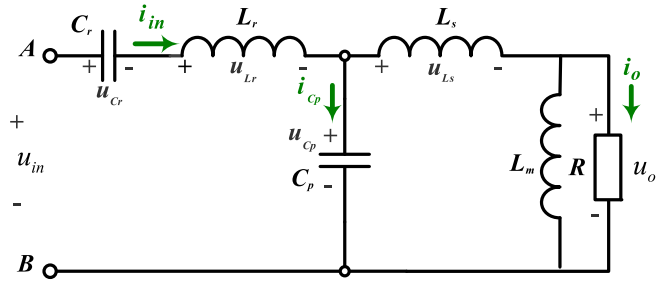

Fig. 5. Equivalent circuit of the proposed resonant converter.

load is transferred to the primary side based on fundamental waveform principle.

Based on Fig. 5, the voltage gain expression can be obtained by

$$M_V(s) = \left| \frac{\frac{2\sqrt{2}nU_o}{\pi}}{\frac{\sqrt{2}}{\pi}U_{in}} \right| = \left| \frac{s^2 L_m C_r R}{as^5 + bs^4 + cs^3 + ds^2 + L_m s + R} \right| \tag{1}$$

where

$$a = L_r L_s C_r C_p L_m, c = L_r C_r L_m + L_m L_s C_r + L_m L_s C_p,$$
$$b = RL_r C_r C_p (L_m + L_r),$$

and $d = L_r C_r R + (L_m + L_r) RC_p + (L_m + L_r) RC_r$.

At the same time, two approximate resonant frequencies can be calculated. Equation (2) shows the low part resonant frequency f_{rL} when the capacitor C_p can be seen as open. Equation (3) shows the high part resonant frequency f_r when the capacitor C_r can be seen as short

$$f_{rL} \approx \frac{1}{2\pi\sqrt{(L_r + L_s)C_r}} = \frac{\omega_{rL}}{2\pi} \tag{2}$$

$$f_r \approx 1/2\pi\sqrt{C_p\left(\frac{L_r L_s}{L_r + L_s}\right)} = \frac{\omega_r}{2\pi}. \tag{3}$$

Based on (1) and (3), the voltage gain curves with different values of quality factor Q can be obtained. Here, the quality factor is defined to be $Q = \sqrt{\frac{L_s L_r}{L_s + L_r}/C_p}/R$.

As can be seen from Fig. 6, there are two resonant points existing in each curve. With the increase of Q, the value of the voltage gain decreases at the same frequency. Meanwhile, at the resonant frequency f_r, the voltage gain keeps at a constant value independent of load R, which can be obtained as shown

$$|M_V|_{@f_r} \approx \left| \frac{\frac{R}{L_r + L_s}}{\frac{L_r L_s C_p}{L_r + L_s}s^3 + \frac{L_r C_p R}{L_r + L_s}s^2 + s + \frac{R}{L_r + L_s}} \right| = \frac{L_s}{L_r}. \tag{4}$$

At the same time, through the equivalent circuit, the impedance angle φ can also be obtained as shown

$$\varphi = \arctan\left(\frac{\alpha\gamma - \beta\chi}{\alpha\chi + \beta\gamma}\right) \tag{5}$$

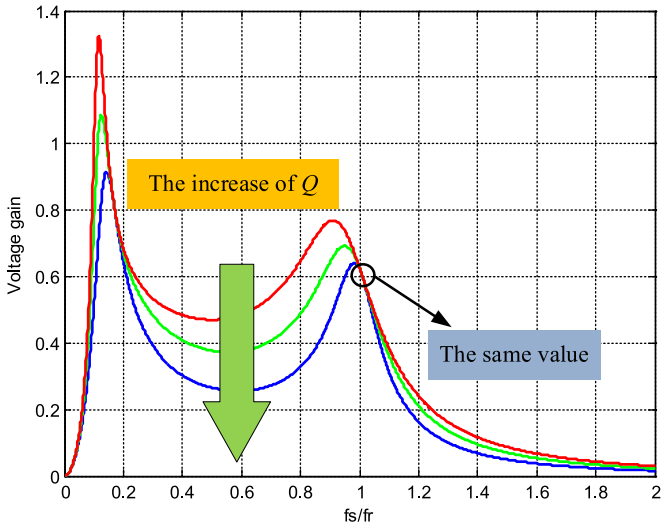

Fig. 6. Voltage gain curves with different values of quality factor Q.

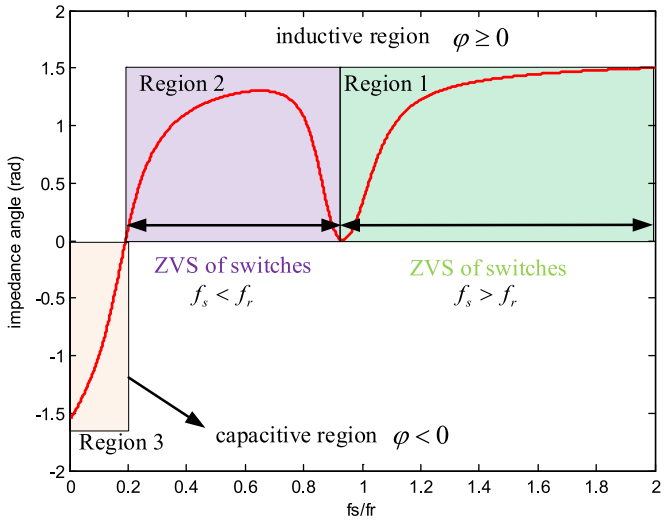

Fig. 7. Input impedance angle curve of the CLCL converter.

where

$$\alpha = L_m L_s C_r C_p \omega^4 - L_r L_m \omega^2, \beta = C_r R\omega - C_r C_p R (L_m + L_s) \omega^3,$$
$$\gamma = L_m L_s C_r C_p L_r \omega^5 - (L_m L_s (C_p + C_r) + L_m C_r L_r) \omega^3 + L_m \omega,$$

and $\chi = (C_p C_r L_r (L_m + L_s) R\omega^4 - ((L_m + L_s)(C_p + C_r) R + L_r C_r R)\omega^2 + R)$.

Fig. 7 shows the curve of the input impedance, as can be seen, around the resonant frequency f_r, the impedance angle φ is about zero, which is the ideal operating condition, and the voltage and current are in the same phase. Meanwhile, according to Fig. 7, the operating conditions of the CLCL converter can be divided into three regions. In region 1 and region 2, the angle φ is above zero, so the switches work in ZVS mode. In the capacitive region 3, the ZVS feature is lost.

In ideal condition, the input impedance angle can be zero, however, in actual situation, the switches cannot turn on or turn

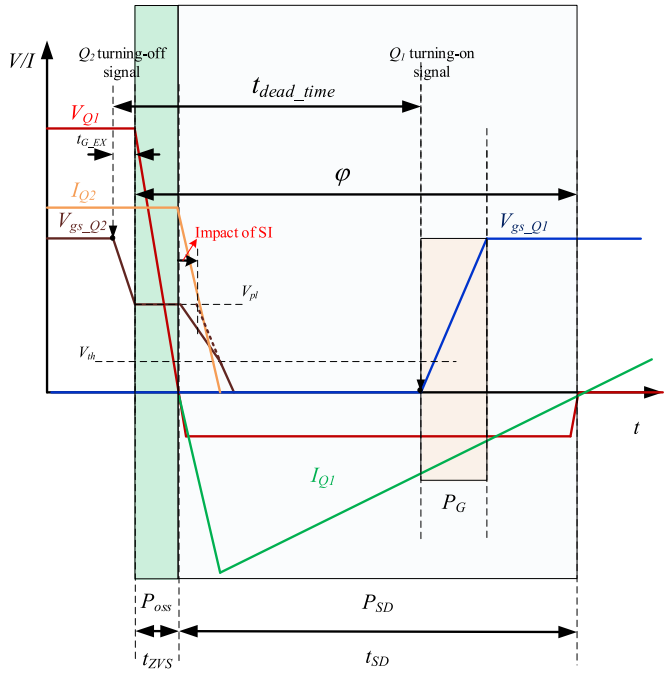

Fig. 8. Voltage and current waveforms in ZVS condition during the turn-on transition.

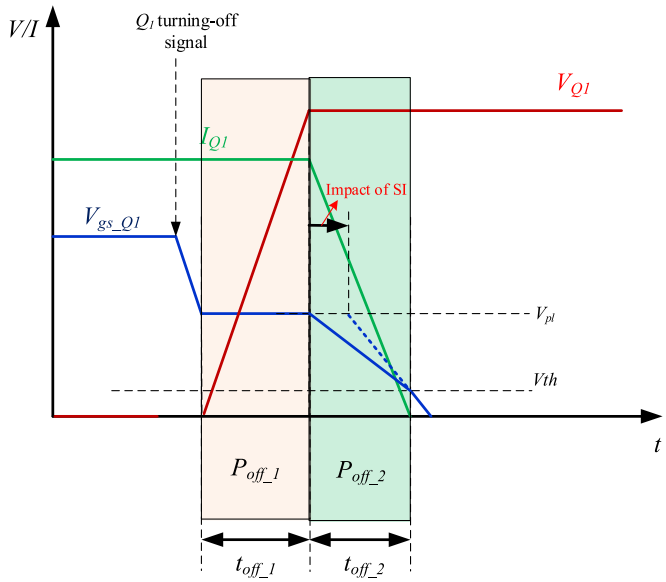

Fig. 9. Voltage and current waveforms during turn-off transition.

off immediately. So the dead time is necessary and a small phase difference must be existing between the voltage and current. Meanwhile, in ZVS condition, the reverse conduction time is closely relevant to the turn-off current. A small turn-off current will increase the time to charge the output capacitor, which results in a long turn-off transition. In high-frequency condition, the impedance angle, turn-off current and dead time should all be taken into consideration.

B. Analysis of the Turn-On or Turn-Off Transitions

Fig. 8 shows the detailed voltage and current waveforms during the turn-on transition, the structure of Q_1 and Q_2 is the same as in Fig. 1. Meanwhile, the source inductors in practical circuits are also taken into consideration in the high-frequency condition. Here, only the losses of Q_1 are analyzed and the total switch losses are twice of the calculated value.

Once the turn-off signal of Q_2 comes, there is a time delay t_{G_EX} before the G-S voltage decreases to gate plateau voltage V_{pl}. Then the output capacitance $C_{\rm oss}$ of Q_1 begins to be discharged and the output capacitance $C_{\rm oss}$ of Q_2 begins to be charged. So the voltage V_{ds} of Q_1 decreases. For the demand of ZVS turn-on characteristics, before the driving signal of Q_1 reaching high level, the voltage V_{ds} of Q_1 must already be zero. So the time period $t_{\rm ZVS}$ can be calculated by

$$t_{\rm ZVS} = \frac{Q_{\rm OSS\_Q1} + Q_{\rm OSS\_Q2}}{I_{\rm turn\_off}}. \tag{6}$$

Here, $Q_{\rm OSS\_Q1}$ and $Q_{\rm OSS\_Q2}$ are the output charge, which can be calculated according to (7) where the output capacitance $C_{\rm OSS}$ forms a nonlinear relationship with the drain-source voltage $v_{\rm DS}$, which can be obtained from the device datasheet

$$Q_{\rm OSS} = \int_0^{V_{\rm in}} C_{\rm OSS}(v_{\rm DS}) \cdot {\rm d}v_{\rm DS}. \tag{7}$$

In (8), the turn-off current $I_{\rm turn\_off}$ can be calculated as follows, which forms a proportional relationship with the input impedance angle φ, where $|Z_{\rm eq}|$ is the impedance amplitude of the resonant tank

$$I_{\rm turn\_off} = \frac{2U_{\rm in}}{\pi\,|Z_{\rm eq}|}\sin\varphi. \tag{8}$$

Within this period $t_{\rm ZVS}$, the output capacitance losses $P_{\rm oss}$ can be calculated as follows:

$$P_{\rm OSS} = f_{SW} \times \int_0^{V\,\rm bus} v_{\rm DS} \cdot C_{\rm OSS}(v_{\rm DS}) \cdot dv_{\rm DS}. \tag{9}$$

After this period, the drain current and gate voltage of Q_2 begin to decrease until zero, and the transition is lengthened for the existing of source inductance, which is detailed analyzed in the follows turn-off part as Fig. 9 shown. Meanwhile, the current will flow through Q_1 in the reverse direction with a constant voltage drop $V_{\rm SD}$, until the reverse conduction current reaches zero, this mode ends. The reverse conduction time $t_{\rm SD}$ can be calculated by

$$t_{\rm SD} = t_{\varphi} - t_{\rm ZVS} = \frac{\varphi}{2\pi f_{SW}} - \frac{Q_{\rm OSS\_Q1} + Q_{\rm OSS\_Q2}}{I_{\rm turn\_off}}. \tag{10}$$

Assuming the reverse conduction current varies linearly, the reverse conduction losses $P_{\rm SD}$ within the period $t_{\rm SD}$ can be calculated by

$$\begin{aligned} P_{\rm SD} &= f_{SW} \times \int_0^{t_{\rm SD}} V_{\rm SD} \cdot i_{\rm SD} \cdot {\rm d}t_{\rm SD} \\ &= V_{\rm SD} \cdot \frac{I_{\rm turn\_off}}{2} \cdot t_{\rm SD} \cdot f_{SW}. \end{aligned} \tag{11}$$

TABLE I
PARAMETERS OF THE GAN FET EPC2010C

Parameter	Test Conditions	Typical	Max	Unit
$C_{\rm ISS}$	Input capacitance	380	540	pF
$C_{\rm OSS}$	Output capacitance	240	320	pF
$C_{\rm RSS}$	Reverse transfer capacitance	1.8	2.7	pF
Q_G	Total gate charge ($V_{\rm GS}$ = 5V)	3.7	5.3	nC
$Q_{\rm GD}$	Gate-to-drain charge	0.7	1.3	nC
$Q_{\rm GS}$	Gate-to-source charge	1.3	Not Available	nC
$Q_{\rm OSS}$	Output charge	40	52	nC

At the same time, to achieve the ZVS characteristics, the driving signal of Q_1 must be applied before the end of the reverse conduction period. In Fig. 8, it can be seen that in the ZVS condition, the Miller plateau does not exist, so the actual gate charge is the difference between the total gate charge Q_G and Miller charge Q_{GD}. So the gate charge losses P_G in ZVS condition can be calculated by

$$P_G = (Q_G - Q_{GD}) \cdot V_{DR} \cdot f_{SW}. \tag{12}$$

During the turn-off transition, the voltage and current waveforms are shown in Fig. 9. The turn-off losses can be divided into two parts: $P_{\rm off\_1}$ and $P_{\rm off\_2}$. During period $t_{\rm off\_1}$, the current is constant and the voltage changes linearly; on the other hand, within $t_{\rm off\_2}$, the voltage is constant and current varies linearly. So the turn-off losses can be calculated by

$$P_{\rm off} = \frac{V_{\rm in} \cdot I_{\rm turn\_off} \cdot f_{SW}}{2}(t_{\rm off\_1} + t_{\rm off\_2}) = \frac{V_{\rm in} \cdot I_{\rm turn\_off} \cdot f_{SW}}{2} \left(\frac{Q_{GD} \cdot R_{G\rm off}}{V_{pl}} + \frac{Q_{GS2} \cdot (R_{G\rm off} + R_{SI})}{((V_{pl} + V_{th})/2)}\right) \tag{13}$$

where V_{th} is the gate threshold voltage and Q_{GS2} represents the corresponding charge during $t_{\rm off\_2}$, which can be calculated according to the transfer characteristic figure of devices, $R_{G\rm off}$ is the gate loop resistance during turn-off period, R_{SI} is the equivalent source inductance resistance, which is detailed calculated in the Appendix. From (13) and Fig. 9, it can be seen that the source inductor lengthens the turn-off transition. However, in the ZVS soft-switching condition as shown in Fig. 8, the turn-on transition is not affected by source inductance.

Based on (9) to (13), the total switching losses during the ZVS turn-on and turn-off transitions can be calculated as shown in (14), which are mainly composed of output capacitance losses $P_{\rm oss}$, gate charge losses P_G, reverse conduction losses $P_{\rm SD}$, and turn-off losses $P_{\rm off}$

$$P_{\rm Total} = P_{\rm OSS} + P_{\rm SD} + P_G + P_{\rm off}. \tag{14}$$

Here, takes GaN FETs EPC2010C manufactured by Efficient Power Conversion for example to calculate the corresponding losses of the CLCL converter in ZVS condition. The parameters of EPC2010C are shown in Table I.

According to Fig. 10, it can be seen that both reverse conduction losses $P_{\rm SD}$ and turn-off losses $P_{\rm off}$ are proportional to the impedance angle φ. Meanwhile, output capacitance losses $P_{\rm oss}$ and gate charge losses P_G both keep a constant value with

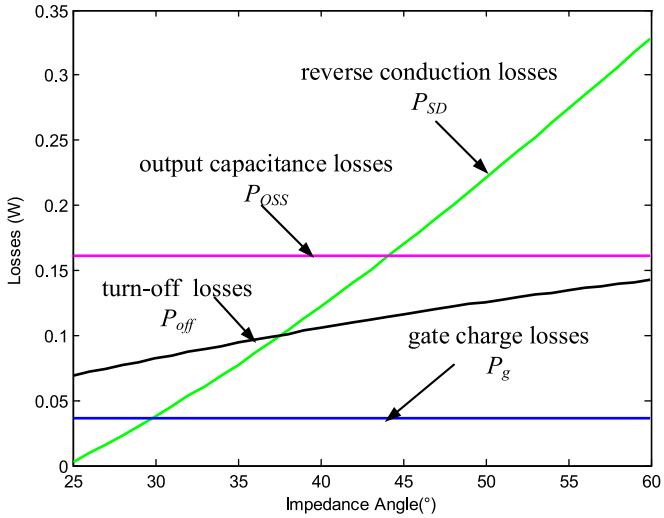

Fig. 10. Curves of losses VS impedance angle.

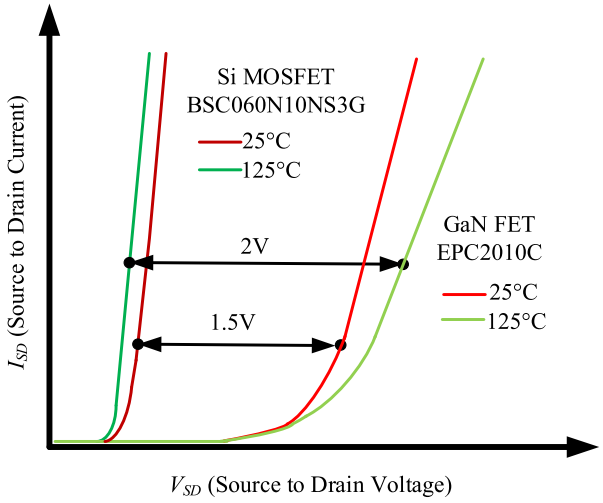

Fig. 11. Curves of $V_{\rm SD}$ VS $I_{\rm SD}$ in different conditions.

the variation of φ. So it can be concluded that the total losses increase with the growth of impedance angle φ.

At the same time, it can be seen that the reverse conduction losses take a great part of the total losses. Actually, it is because that the reverse conduction voltage of GaN FETs is higher than Si MOSFETs. To be exact, there is not a body diode in GaN FETs. However, a special mechanism to conduct reverse current exists, which allows GaN FETs operate similarly as Si MOSFETs when the device is off. Fig. 11 shows the curves of source to drain current $I_{\rm SD}$ against source to drain voltage $V_{\rm SD}$ in different situations. As can be seen from the figure, the voltage drop of GaN FETs is 1.5 V higher than common Si MOSFETs in 25 °C condition. At a higher temperature, voltage difference will be as high as 2 V. This high voltage drop can be reduced by paralleling a low-conduction voltage Schottky diode between the drain and source ends of GaN FETs. However, this method will introduce additional inductors, such as the parasitic inductors of the diode and the inductors between the pins of GaN

TABLE II
PARAMETERS OF THE SI MOSFET BSC060N10NS3G

Parameter	Test Conditions	Typical	Max	Unit
$C_{\rm ISS}$	Input capacitance	3700	4900	pF
$C_{\rm OSS}$	Output capacitance	650	860	pF
$C_{\rm RSS}$	Reverse transfer capacitance	25	Not Available	pF
Q_G	Total gate charge ($V_{\rm GS}$ = 5V)	51	68	nC
$Q_{\rm GD}$	Gate-to-drain charge	9	Not Available	nC
$Q_{\rm GS}$	Gate-to-source charge	15	Not Available	nC
$Q_{\rm OSS}$	Output charge	68	91	nC

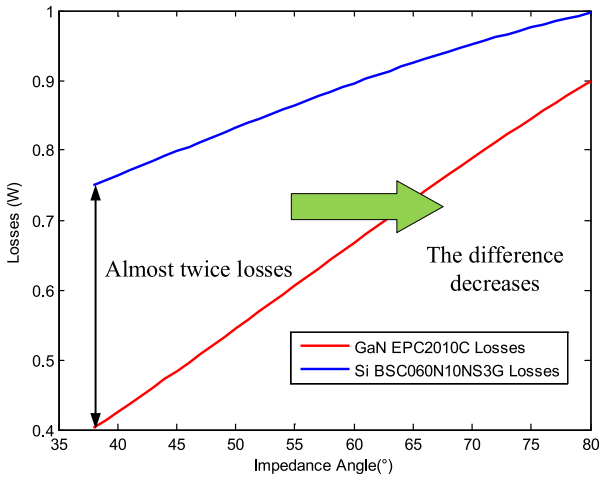

Fig. 12. Losses curves comparing different material switches.

FETs and the diodes. These additional inductances greatly affect the switching characteristics, such as voltage overshooting etc. On the other hand, an addition diode increases the output capacitance losses for an extra output capacitance.

Though the reverse conduction voltage of GaN FETs is higher, the low output capacitance feature is more important in high-frequency condition. Here, the parameter list of BSC060N10NS3G is shown in Table II. The output charge is almost twice of that in EPC2010C. With two same switches, the time needed to achieve ZVS can be calculated as follows:

$$t_{\rm ZVS} = \frac{Q_{\rm OSS\_Q1} + Q_{\rm OSS\_Q2}}{I_{\rm turn\_off}} = \frac{2Q_{\rm OSS}}{I_{\rm turn\_off}}. \tag{15}$$

At the same turn-off current value, $t_{\rm ZVS}$ for BSC060N10NS3G is almost twice of that in EPC2010C, a long transition time will greatly limit the improvement of operating frequency.

Meanwhile, substituting the corresponding parameters into (14). The total losses curves of EPC2010C and BSC060N10NS3G are shown in Fig. 12, respectively. It is indicated that though the reverse conduction voltage is high, the total losses of EPC2010C are still much lower than the losses of BSC060N10NS3G. In large impedance angle condition, the reverse conduction losses of EPC2010C increase much faster, so the difference between the two losses decreases.

III. DESIGN OF THE PLANAR MAGNETICS

In high-frequency condition, the magnetics losses and size limit the efficiency and power density of the converter. For material, 3F35 ferrite material has been selected in this paper for its low magnetic power losses. Meanwhile, planar cores are adopted to reduce the profile and size of the magnetics. However, for the design of planar magnetics, many coupled factors greatly affect the properties of the inductors and transformers, such as copper track structure and winding layout. Though simulations can help to guide the design process, there is not a clear explanation that how these factors affect the magnetics properties. Some more effective ways should be adopted to help the planar magnetics design.

A. Design of Planar Inductor Based on RSM

At the beginning, we start to design the planar inductors, which are easier and less complex than the transformers. For the copper tracks are often adopted as the windings of the planar inductors, copper thickness, track width, and track turns, all affect the inductance and resistance of the inductor. At the same time, these factors are coupled and might form a nonlinear relationship. So some proper methods should be adopted to obtain an easy and effective parameter estimation of the planar inductors.

RSM has been applied to deal with the complex and nonlinear problems, so in this paper, the RSM is adopted to design planar inductors. The basic idea of RSM is to extract parameter models through regression analysis of the results obtained from several experiments and simulations. The basic equation of the method is shown

$$F(Y) = a_0 + \sum_{i=1}^{n} a_i x_i + \sum_{i=1}^{n}\sum_{j=1}^{n} b_{ij} x_i x_j. \tag{16}$$

In (16), *Y* represents the measured results through experiments or simulations. *F* is the transforming function of the measured results *Y*. a_0 denotes the average value of the measurements, and a_i and b_{ij} represent the linear and quadratic regression coefficients, respectively. *n* represents the total number of the relevant factors x_i and x_j.

At the same time, to avoid excessive complex calculating procedure, a two-level factorial design method is adopted in the paper. There are 5 levels and corresponding values in this method: very low represents by -2, low represents by -1, midpoint represents by 0, high represents by $+1$, very high represents by $+2$. By this way, the quadratic model can be obtained to help the planar inductor design.

As mentioned earlier, the inductance and resistance of a planar inductor closely tie with many factors, such as core material, core type, air gap length, copper thickness, track width and track turns etc. In the following, a detailed design process of the planar inductor is illustrated, in which the core is chosen to be EQ/PLT 30 with 3F35 material manufactured by Ferroxcube. Four main factors affecting the properties of the planar inductor are listed in Table III, which also contains the code and corresponding levels of the factors.

TABLE III
DEFINITION OF LEVELS FOR DIFFERENT PARAMETERS

Factor	Coded	−2	−1	0	1	2	Units
Copper thickness	A	1	1.5	2	2.5	3	oz/ft^2
Air gap length	B	0	0.25	0.5	0.75	1	mm
Track width	C	0.3	0.4	0.5	0.6	0.7	mm
Turns	D	3	4	5	6	7	

For copper thickness, the range from 1 to 3 oz is chosen within the manufacturable level. Air gap length range is 0–1 mm, which is a general choice. The five levels are arranged arithmetically. Considering the chosen core size, with a constant 0.2 mm clearances, the track width and turns can be decided to achieve maximum utilization of core space. After setting these parameters, it is important to ensure the intended inductance within the design factors range. It is well known that the inductance is mainly depended on the air gap length and turns, which is inversely proportional to the air gap length and directly proportional to the turns. The two quasi-extreme conditions: 1) $B = -1$ and $D = +1$; 2) $B = +1$ and $D = -1$ should be first tested. If the intended inductance is not covered, then the turns and corresponding track width must be reselected.

After setting the parameters, different conditions are listed in Table IV. To simplify the process, the very high and very low conditions are only combined with the midpoint levels. Each condition is simulated by MAXWELL software, which can also be done by experiments. Through these simulations, the value of inductances and resistances can be obtained and the results are also listed in Table IV. The intended inductance value in the example is 20–30 μH, which is calculated in Section IV. It can be seen from Table IV that the intended inductances can be covered.

After obtaining results of the 25 conditions, by the regression algorithm, the expressions of the inductance and resistance can be obtained as shown

$$L \approx 15.01 - 12.3B + 5.76D - 6.51BD + 4.51B^2 + 0.48D^2 \tag{17}$$

$$R \approx 246 - 84.8A - 53.1C + 63.74D - 2.2AC + 23.7A^2 + 14.1C^2 + 4.02D^2. \tag{18}$$

To further validate the model accuracy, fifteen different conditions within the range are tested. The model formulas match the results with adjusted R^2 values of 0.989 and 0.983, respectively.

Once the equations are obtained, the windings and the core air gap properties can be designed to achieve the desired inductance value, at the same time, the smallest value of resistance is expected to decrease the losses of the windings. Some trends can also be seen from the earlier equations, the inductance mainly depends on the air gap length and turns as analyzed. Also, the resistance is inversely proportional to the width and thickness of the tracks. So with the help of the equations based on RSM, the planar inductor with expected inductance and resistance can be designed more effectively within the acceptable error range.

B. Design of Planar Transformer Based on MLM

For planar magnetics, besides inductors, planar transformers are also very important, especially in the resonant converters such as *LLC* circuit and CLCL circuit, which play the role of high-ratio voltage transferring and isolating. Comparing with planar inductors, the structure of planar transformers is more complicated. For example, the turns in primary side and in secondary side have to be located in different PCB layers, which causes many different layout choices, so it is hard to still use RSM to design transformers in different structure conditions.

Because there are many layers in the planar transformers and some relationships between them are formed, an MLM based on lumped circuit is adopted in [27]. In the design process, many factors affect the properties of planar transformers, such as winding layout, insulation materials, thickness of insulation layers, copper thickness and so on. At the same time, an optimized planar transformer design should guarantee smaller leakage inductances and resistances in the primary and secondary side. Based on MLM, all the factors mentioned earlier can be taken into account to achieve small leakage inductances and parasitic resistances.

Here, a planar transformer with center tapped in the secondary side is designed based on MLM in this paper for the CLCL resonant converter. A PCB with six layers is used, primary winding and two secondary windings take two layers, respectively. The turn ratio of the transformer is set to be 2. The modeling procedure based on MLM is depicted as follows.

1) Model of Each Conductor Layer: According to MLM, though different layers exist in the designed transformer, the fundamental equations for each layer are the same as shown in (19) with $1 \le i \le 6$

$$\begin{cases} d_i E_{Ti} = w_i H_{Ti} \dfrac{d_i}{w_i} \dfrac{\Psi_i \left(1 - e^{-\Psi_i h_i}\right)}{\sigma_i \left(1 + e^{-\Psi_i h_i}\right)} \\ \qquad\qquad + w_i K_1 \dfrac{d_i}{w_i} \dfrac{2\Psi_i e^{-\Psi_i h_i}}{\sigma_i \left(1 - e^{-2\Psi_i h_i}\right)} \\ d_i E_{Bi} = w_i K_i \dfrac{d_i}{w_i} \dfrac{2\Psi_i e^{-\Psi_i h_i}}{\sigma_i \left(1 - e^{-2\Psi_i h_i}\right)} \\ \qquad\qquad - w_i H_{Bi} \dfrac{d_i}{w_i} \dfrac{\Psi_i \left(1 - e^{-\Psi_i h_i}\right)}{\sigma_i \left(1 + e^{-\Psi_i h_i}\right)} \\ H_{Ti} - H_{Bi} = K_i \\ w_i K_i = I_i m_i \end{cases}. \tag{19}$$

In the *i*th layer, E_{Ti} and E_{Bi} denote the electric field strength on top and bottom surface, respectively; H_{Ti} and H_{Bi} represent the magnetic field strength on top and bottom surface, respectively; and d_i, h_i, and w_i represent the length, thickness, and width of one turn, respectively. I_i and K_i represent the current and the current per width. m_i denotes the number of turns. Also the parameter $\Psi_i = (1 + j)\sqrt{\omega \mu_i \sigma_i}/\sqrt{2}$, where ω is the angular frequency, μ_i is the permeability, and σ_i is the electric conductivity. Based on (19), each conductor layer can be modeled as a three-terminal impedance network as Fig. 13 shown, where $Z_{ai} = \left(\Psi_i \left(1 - e^{-\Psi_i h_i}\right)\right) / \left(\sigma_i \left(1 + e^{-\Psi_i h_i}\right)\right)$ and $Z_{bi} = 2\Psi_i e^{-\Psi_i h_i} / \left(\sigma_i \left(1 - e^{-2\Psi_i h_i}\right)\right)$.

TABLE IV
RESULTS OF DIFFERENT PARAMETER CONDITIONS

A	B	C	D	R (mΩ)	L (μH)	A	B	C	D	R (mΩ)	L (μH)
−1	−1	−1	−1	316.556	16.7802	+1	−1	−1	+1	312.178	38.0919
+1	+1	−1	−1	189.934	6.6951	−1	+1	−1	+1	520.297	15.3156
+1	−1	+1	−1	132.011	16.8788	−1	−1	+1	+1	367.07	38.2662
−1	+1	+1	−1	220.018	6.74669	+1	+1	+1	+1	220.242	15.4876
+1	−1	−1	−1	189.934	16.7802	−1	−1	−1	+1	520.297	38.0919
−1	+1	−1	−1	316.556	6.6951	+1	+1	−1	+1	312.178	15.3156
−1	−1	+1	−1	220.018	16.8788	+1	−1	+1	+1	220.242	38.2662
+1	+1	+1	−1	132.011	6.74669	−1	+1	+1	+1	367.07	15.3156
−2	0	0	0	510.194	14.9254	0	0	+2	0	191.233	15.0241
+2	0	0	0	170.065	14.9408	0	0	−2	0	404.117	14.8088
0	+2	0	0	255.097	8.30034	0	0	0	+2	392.496	29.6263
0	−2	0	0	255.097	52.7954	0	0	0	−2	137.904	5.31205
0	0	0	0	255.097	14.9404						

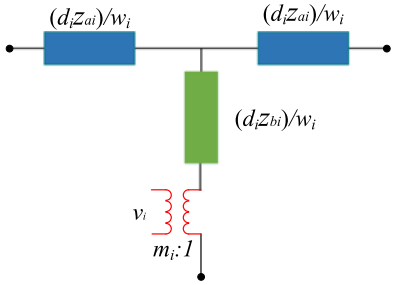

Fig. 13. Three-terminal model of single conductor layer.

2) Effect of Layer Spacing and Magnetic Core: The relationship between the two adjacent layers i and j can be calculated by

$$\begin{cases} j\omega\Phi_{Bi} = V_1 - dE_{Bi} \\ j\omega\Phi_{Tj} = V_2 - dE_{Tj} \\ \Phi_{Bi} + \Phi_{Sij} = \Phi_{Tj} \\ H_{Sij} = \Phi_{Sij}/\mu_0 a_{ij} d \end{cases} \tag{20}$$

where $j = I + 1$; Φ represents the magnetic flux; and μ_0 and a_{ij} denote the permeability and thickness of the insulator space, respectively. V_i and V_j are the external voltages at the two layer ports. Based on (20), the interconnect impedance between adjacent layers can be represented as $Z_{si} = j\omega\mu_i a_{ij}$. At the same time, the top layer and bottom layer form certain relationship with magnetic core and gaps, which can be included by adding impedances $Z_T = j\omega/Z_{\text{reluc\_}T}$, $Z_B = j\omega/Z_{\text{reluc\_}B}$ in the front and end of the model network. $Z_{\text{reluc\_}T}$ and $Z_{\text{reluc\_}B}$ are reluctances at top and bottom of magnetic core.

3) Final MLM Including Different Layers Connections: Based on the aforementioned analysis, the impedance network of transformer can be established, which is shown in Fig. 14. Under the one-dimensional (1-D) assumption, all layers own the same parameters d and w approximately. Meanwhile, in the transformer, the primary winding is formed by series connecting layers 3 and 4, secondary side 1 is formed by series connecting layers 1 and 2, and the secondary side 2 is similarly formed by layers 5 and 6, as shown in Fig. 14. The idea connecting method ignores the small effect caused by cross-layer capacitances and interconnect impedances. Besides calculating the formulas manually, the software named M2Spice can help us to establish the network of MLM.

4) Parameters Extraction of T-Type Model Based on MLM: To evaluate the transformer parameters more easily, the T-type model can be built based on MLM. Because the two secondary windings are symmetric and do not work simultaneously, take the primary winding and the secondary winding 1 for example to obtain the T model. In the four-port network of Fig. 14, voltages and currents satisfy (21) where the matrix terms can be calculated through open-circuit tests at both windings in MLM

$$\begin{bmatrix} V_p \\ V_{s1} \end{bmatrix} = \begin{bmatrix} R_{11} + j\omega L_{11} & R_{12} + j\omega L_{12} \\ R_{21} + j\omega L_{21} & R_{22} + j\omega L_{22} \end{bmatrix} \begin{bmatrix} I_p \\ I_{s1} \end{bmatrix}. \tag{21}$$

Based on the obtained matrix terms R_{ij} and L_{ij} in (21), the T model can be built as Fig. 15 shows, where L_1 and L_3 denote the leakage inductors and L_2 represents the magnetizing inductor. R_1, R_2, and R_3 are corresponding resistors. These six parameters can be calculated as shown in (22) and then the transformer characteristics can be compared

$$\begin{cases} R_1 = R_{11} - \dfrac{n_1}{n_2} \times R_{12}; \qquad L_1 = L_{11} - \dfrac{n_1}{n_2} \times L_{12} \\ R_2 = \dfrac{n_1}{n_2} \times R_{12}; \quad L_2 = \dfrac{n_1}{n_2} \times L_{12} \\ R_3 = \dfrac{n_1^2}{n_2^2}\left(R_{22} - \dfrac{n_2}{n_1} \times R_{12}\right); \quad L_3 = \dfrac{n_1^2}{n_2^2}\left(L_{22} - \dfrac{n_2}{n_1} \times L_{12}\right) \end{cases}. \tag{22}$$

IV. SYSTEM DESIGN AND EXPERIMENTAL RESULTS

In this paper, a 1 MHz CLCL resonant converter is designed and built in the laboratory. The input voltage is 80 V, and the output voltage is 15 V. The output power is 25 W. According to (14) and Fig. 12, GaN FETs are chosen as the switch to reduce the switching losses. The transformer turns ratio is set to be 2, and the resonant frequency is set to be a little bit higher than the operating frequency as follows:

$$f_r \approx 1/2\pi\sqrt{C_p\left(\frac{L_r L_s}{L_r + L_s}\right)} = 1.05 f_s. \tag{23}$$

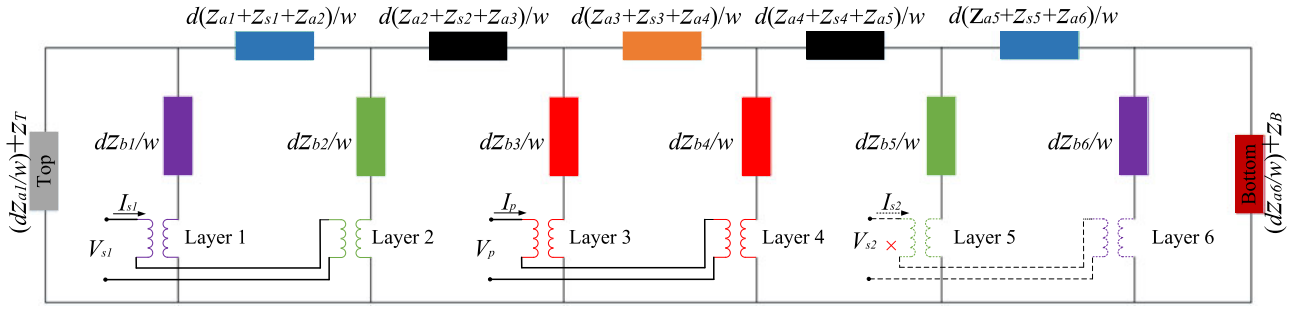

Fig. 14. Final impedance network based on MLM.

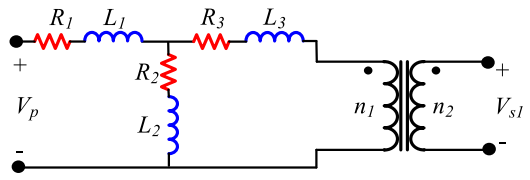

Fig. 15. Lumped circuit of final transformer model based on MLM.

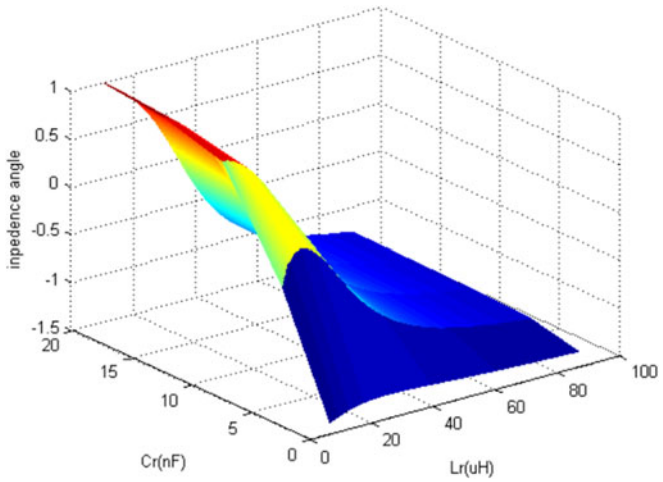

Fig. 16. Impedance curves at different C_r and L_r values.

According to (1) and (4), (24) can be obtained

$$|M_V|_{@f_r} \approx \left|\frac{2nU_o}{U_{in}}\right| = \frac{L_s}{L_r} = 0.7. \tag{24}$$

Substituting the parameters into (23) and (24), the capacitor C_p can be calculated as shown

$$C_p = \frac{1.7}{0.7L_r}\left(\frac{1}{2\pi \times 1.05 f_s}\right)^2. \tag{25}$$

Then to design the impedance angle to the expected condition, the curves of the impedance angles can be obtained based on (5) as shown in Fig. 16.

From Fig. 16, it can be seen that when the inductor L_r changes between 23 and 32 μH, C_r changes between 12 and 20 nF and the impedance angles at the operating frequency are around zero, which can achieve soft-switching characteristics and low switching losses, as analyzed in Section II-B.

Meanwhile, the overall losses of the converter are mainly consisted of four parts: switching losses, switches conduction losses, diodes conduction losses, and magnetics losses. According to (11), (13), and Fig. 10, the small impedance angle can help to reduce the switching losses. At the same time, in a given operating condition, the switches conduction losses, diodes conduction losses, and magnetics losses are almost unchanged with constant current rms values. So the overall efficiency can be optimized and improved by the small impedance angle.

In the calculation process, all the equations are based on fundamental waveform analysis, which assumes all the system energy is transferred by the fundamental current and voltage. However, actually high-order harmonics also effect the properties of the CLCL circuit. Also some simplifications are used. So these parameters obtained earlier have to be tuned by the simulation. Here, the PSIM software is adopted to simulate the circuit.

Based on the simulations, a proper group of parameters can be obtained, where $C_r = 15$ nF, $L_r = 30$ μH, $C_p = 1.8$ nF, and $L_s = 20$ μH. The simulation results are shown in Fig. 17 where the switches turn on in ZVS mode and turn off at a low current value, and the diodes in secondary side turn off in ZCS mode.

Here, EQ/PLT 30 with 3F35 material is chosen as the core. For material, 3F35 is recommended by Ferroxcube to operate around 1 MHz with low core losses. For core type, the planar cores are chosen to achieve a low profile, such as planar E cores, planar EQ cores, and planar ER cores. Considering the calculated inductance value, with a certain margin, the EQ/PLT 30 core is chosen. This core type can guarantee reasonable track turns, which can be realized in PCB windings.

For the planar inductor L_r, based on (17) and (18), the copper thickness is 3 oz, the number of turns is 5, the track width is 5 mm, and the air gap length is 0.23 mm. For L_s, these factors are the same as L_r except the air gap length is 0.45 mm. The values of L_r and L_s are measured by impedance analyzer Agilent 4396B, and the results are shown in Fig. 18.

For the planar transformer, many models based on different parameter combinations are established through the earlier analysis. After comparing the values of leakage inductors and corresponding resistors, the optimal structure is shown in Fig. 19.

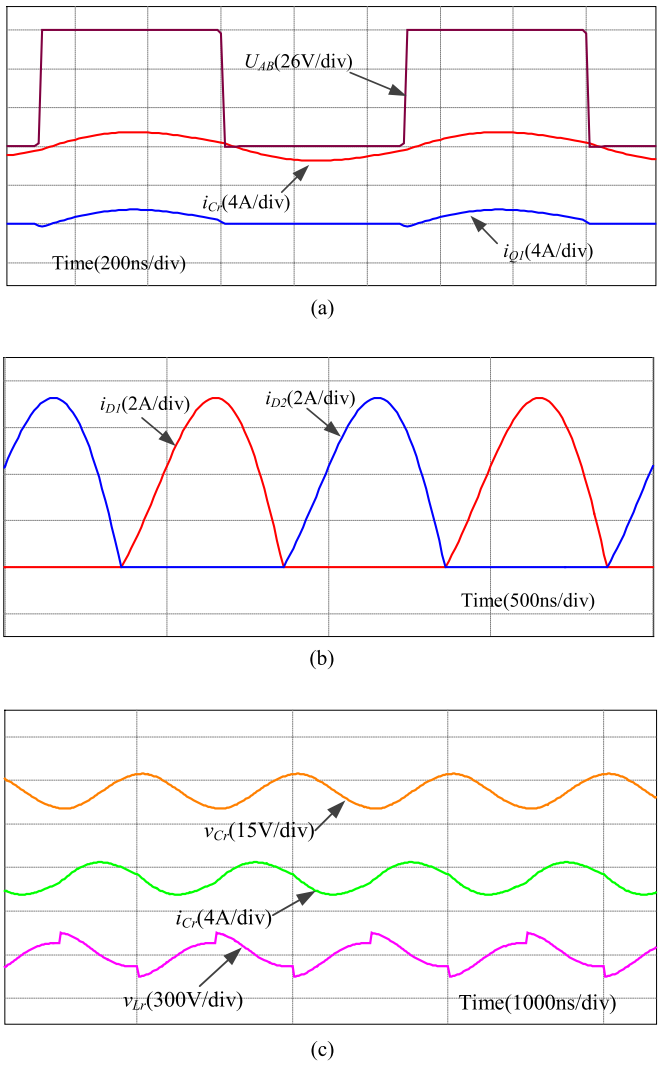

Fig. 17. Simulation results by the tuned parameters. (a) The resonant tank input voltage and current of C_r and Q_1. (b) The current of output diodes. (c) The voltage of C_r and L_r also the current of C_r.

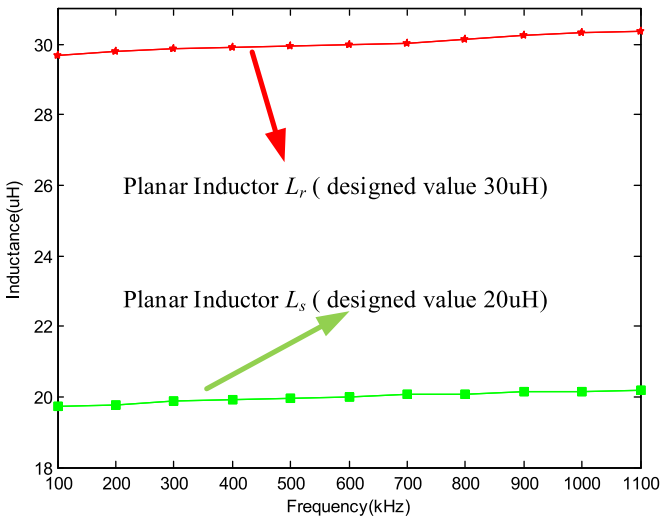

Fig. 18. Measurement results of the planar inductors.

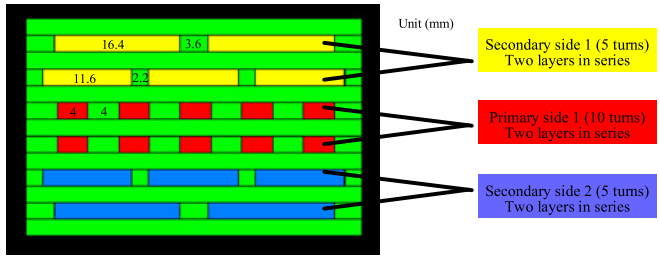

Fig. 19. Optimal structure of the transformer with center tapped in secondary side.

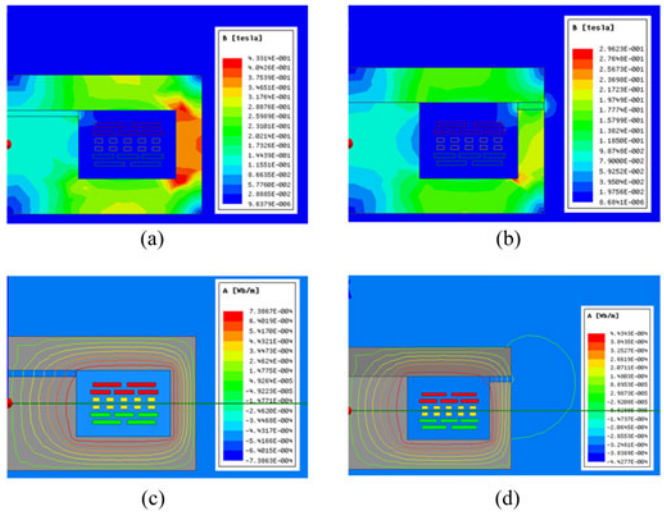

Fig. 20. Distributions of flux and flux density in different conditions. (a) flux density distribution of optimal structure with center leg air gap, (b) flux density distribution of optimal structure with outer leg air gap, (c) magnetic flux distribution of optimal structure with center leg air gap, (d) magnetic flux distribution of optimal structure with outer leg air gap.

To better determine the gap location, it is difficult and computational to obtain distribution of magnetic flux and flux density based on MLM. Fig. 20 shows magnetic flux and flux density distributions of optimal structure at different gap location conditions simulated by MAXWELL software, where the windings are exaggerated to show more clearly. From Fig. 20(a) and (b), it can be seen that the flux densities are both below the saturation flux density of 3F35 at 1 MHz, which is about 500 mT. As seen in Fig. 20(c) and (d), the outer leg air gap causes serious magnetic fringing effects, so in the prototype, the center leg air gap way is adopted.

In this condition, the leakage inductance and the resistance are the smallest. The leakage inductor L_1 and L_3 are 0.6 and 0.31 μH, the corresponding resistor R_1 and R_2 are 178 and 83 mΩ, and the resistor in series with the magnetizing inductor is 723 mΩ, the magnetizing inductance is 60 μH.

The whole system circuit is shown in Fig. 21, and the main parameters and device types are listed in Table V. Here, the resonant capacitors rated for 200 V are adopted indeed, in order to avoid the capacitance change with the operating voltage. Meanwhile, because the loop inductance can result in voltage waveforms' oscillations, the 200 V GaN devices EPC 2010C are selected to guarantee enough voltage margin. The

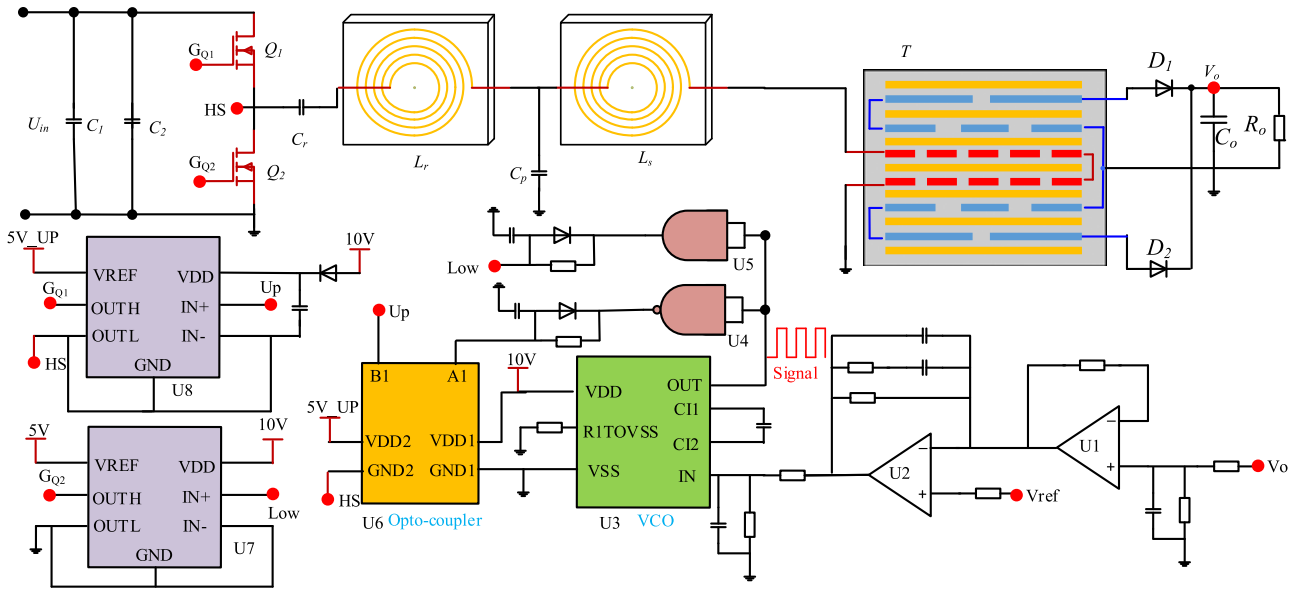

Fig. 21. Whole system circuit of the CLCL prototype.

TABLE V
MAIN PARAMETERS AND DEVICE TYPES OF THE SYSTEM

Device Label	Value/Type	Device Label	Value/Type
C_1, C_2	0.1 μF/250 V	C_o	330 μF/PCJ1C331
Q_1, Q_2	EPC2010C	U_1, U_2	Op Amp/LM8261
D_1, D_2	MBRS540T3G	U_3	VCO/CD4046
L_r	30 μH (EQ/PLT 30)	U_4	NAND GATE/NC7SZ00L6X
L_s	20 μH (EQ/PLT 30)	U_5	AND GATE/NC7SZ08L6X
C_r	15 nF/200 V	U_6	Opto-couple/Si8610BC
C_p	1.8 nF/200 V	U_7, U_8	Gate driver/UCC27611
Transformer	$L_m = 60\ \mu H, n = 2, n_p = 10$		

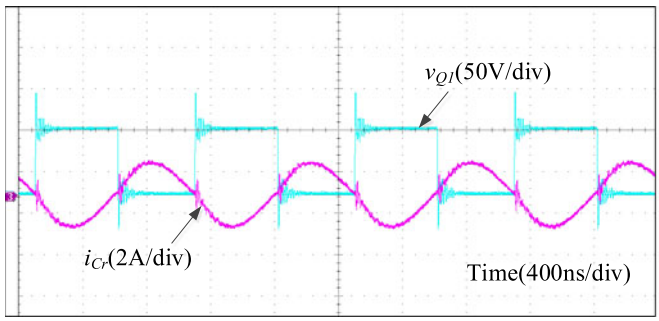

Fig. 22. Waveforms of input voltage v_{Q1} and resonant current i_{Cr} (full-load condition).

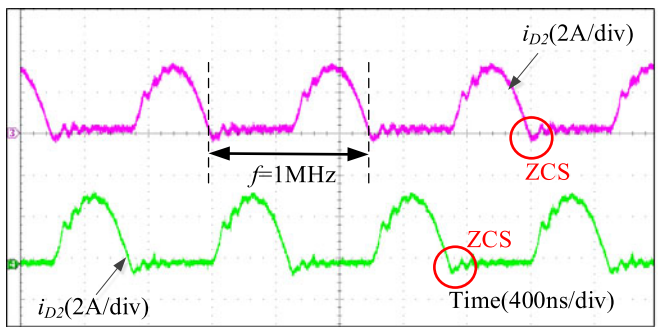

Fig. 23. Current waveforms of D_1 and D_2 (full-load condition).

output voltage is sampled and adjusted in the sampling and compensating stage based on amplifiers. Then the signal comes into the voltage control oscillator (VCO) where the frequency of the output signal can be adjusted. The frequency-variation signal is separated into two channels with 180° phase difference by AND gate and NAND gate. Then the driving signal of low switch Q_2 is generated directly by the driving chip UCC27611. For the up switch Q_1, before the signal coming into the driving chip, it should be isolated by the optocoupler.

Based on the prototype, in full-load condition, the waveforms of input voltage v_{Q1} and resonant current i_{Cr} are shown in Fig. 22. Some oscillations appear because of loop inductances. It can be seen that the input voltage and current of the resonant circuit are almost in the same phase. The switches turn on in ZVS condition and turn off at a very low current. Fig. 23 shows the currents of diodes D_1 and D_2, the operating frequency is 1 MHz, and both of the diodes turn off in ZCS condition. Some current oscillations can be observed in Figs. 23 and 26 follows. Actually, it is mainly caused by transformer parasitic capacitance between the primary side and secondary side. Reducing copper tracks facing area can decrease the parasitic capacitance; however, it will cause large leakage inductance. Fig. 24 shows the waveforms of the output voltage and current, which are consistent with design.

According to the voltage gain curves and the impedance angle curves, when the system load decreases, the output voltage can maintain constant at a lower operating frequency. For the 50% load condition, the waveforms of input voltage v_{Q1} and resonant

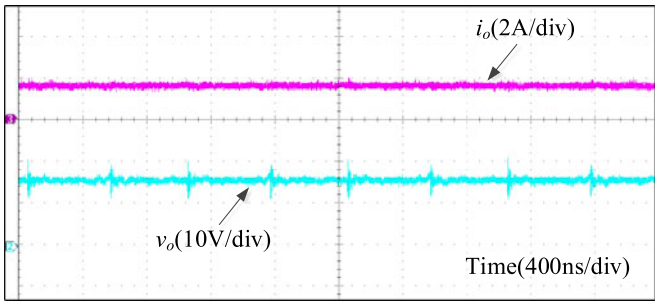

Fig. 24. Waveforms of output voltage and output current (full-load condition).

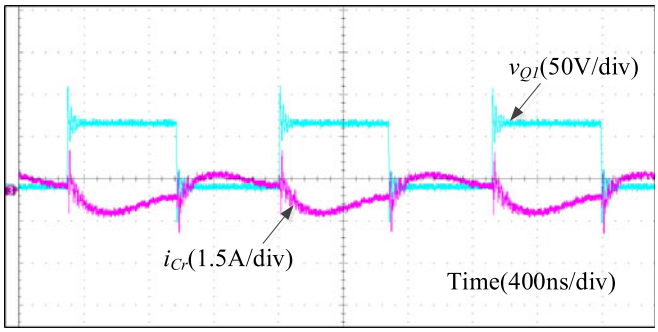

Fig. 25. Waveforms of input voltage v_{Q1} and resonant current i_{Cr} (50% load condition).

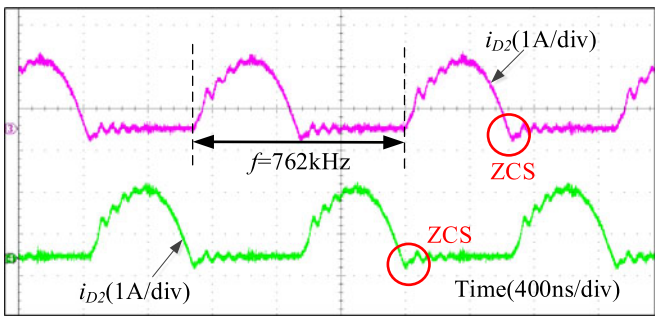

Fig. 26. Current waveforms of D_1 and D_2 (50% load condition).

current i_{Cr} are shown in Fig. 25. It can be seen that the switches still turn on in ZVS condition and the impedance angle is a little bit larger than that in full-load condition. The turn-off current still keeps at a low level.

Fig. 26 shows the currents of output diodes D_1 and D_2, the operating frequency is 762 kHz. At this working frequency, both of the diodes still operate in ZCS condition.

The efficiency curve of the system is shown in Fig. 27 where the full load is 25 W. When the output power changes from 50% to 100%, the efficiency keeps above 80% and the efficiency is 88.7% at rated output power. Fig. 28 shows the calculated and measured power losses curves at rated point. From the result, it can be seen that the values of different parts are almost the same, which proves that the proposed methodology is correct.

Table VI shows the properties' comparisons of different topologies in high-frequency conditions [36]–[45]. Observing

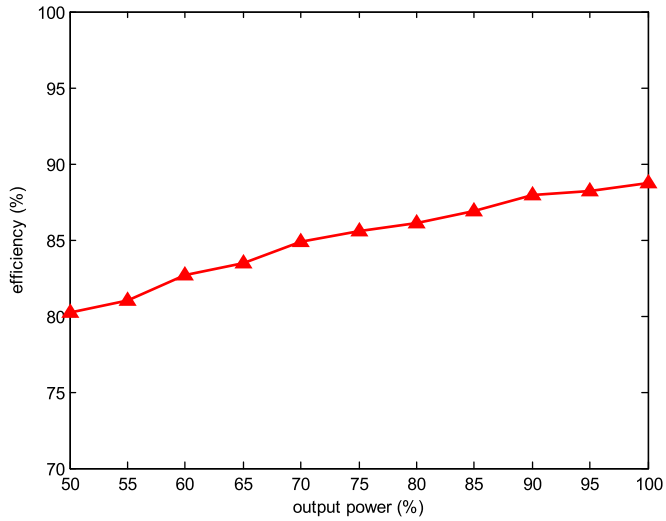

Fig. 27. System efficiency in different load conditions.

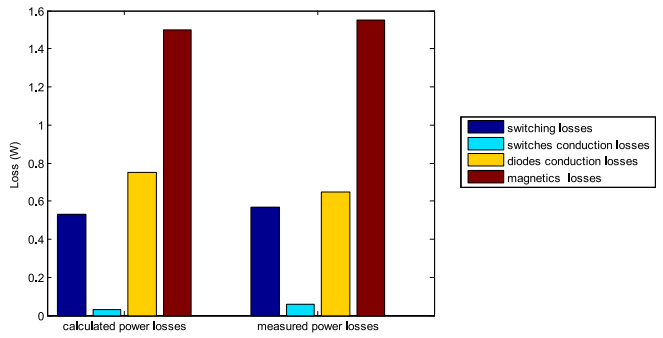

Fig. 28. Calculated power losses and measured power losses.

switching states of power semiconductors (switches and diodes) in Table VI, it can be seen that the proposed CLCL converter owns the best soft-switching characteristics among whole operating range; thus, it can decrease the switching losses, which is the main part of the total loss in ultra-high-frequency converters. In general, from Table VI, the topologies with isolation functions suffer more losses caused by transformers. Also, it is clear that the efficiency always forms a proportional relationship with the output power.

Based on the available data from these papers, the area of *LLC* converter in [39] is about $13\ \text{cm} \times 14\ \text{cm}$ and the area of *LLC* converter in [41] is about $8.2\ \text{cm} \times 7.5\ \text{cm}$. The PCB area of the proposed prototype is $8.2\ \text{cm} \times 7.1\ \text{cm}$, which is little than the earlier two *LLC* prototypes. The volume of prototype is $8.2\ \text{cm} \times 7.1\ \text{cm} \times 1.3\ \text{cm}$, including the control and driving circuit, the power density is 0.33 W/cm^3, which is not high because the desired out power is only 25 W.

In the future work, a 1000-W prototype will be built to use as intermediate bus converters based on the proposed CLCL converter. Through simulations with unideal components (switches, diodes, inductors, and transformers), the efficiency of 1000 W prototype of CLCL converter can be improved and the power

TABLE VI
PROPERTIES COMPARISONS BETWEEN DIFFERENT TOPOLOGIES IN HIGH-FREQUENCY CONDITIONS

Topology	f_s	Input Voltage	Output Voltage	Output Power	Isolation	Efficiency	Switch State		Diode State	
							Turn-on	Turn-off	Rated Power	Light Power
Proposed	1 MHz	80 V	15 V	25 W	Yes	88.7%	ZVS	ZCS	ZCS	ZCS
AHB [36]	1 MHz	28 V	3.3 V	50 W	Yes	91%	ZVS	Hard	Hard (synchronous rectifiers)	
Boost [37]	500 kHz	8 V	16.7 V	16.7 W	No	84.7%	N.A.	N.A.	N.A.	
Synchronous Buck [38]	1 MHz	12 V	1.8 V	27 W	No	84%	Hard	Hard	N.A.	
LLC [39]	1 MHz	300 V	12 V	120 W	Yes	90%	ZVS	Hard	ZCS	Hard
Buck [40]	800 kHz	15–60 V	10 V	480 W	No	93.9%	Hard	Hard	Hard (synchronous rectifiers)	
LLC [41]	1 MHz	360 V	40 V	1000 W	Yes	96.5%	ZVS	Hard	ZCS	Hard
Buck–Boost [42]	1 MHz	6–45 V	10 V	70 W	No	92.35%	Hard	Hard	Hard (synchronous rectifiers)	
Switched-Capacitor [43]	1.2 MHz	25 V	100 V	185 W	No	90%	ZCS	ZCS	Hard (synchronous rectifiers)	
Boost [44]	1 MHz	50 V	100 V	130 W	No	91.8%	ZVS	Hard	Hard	
Buck–Boost [45]	2 MHz	24–80 V	48 V	60 W	No	90.4%	ZVS	Hard	ZVS (synchronous rectifiers)	

density is 13.2 W/cm^3. Besides, magnetic integration technology can be used to further improve the power density.

V. CONCLUSION

This paper proposes and investigates a high-frequency resonant converter topology. Among the operating range, the switches can turn on in ZVS mode and turn off at a low current value. Meanwhile, the secondary diodes always turn off in ZCS mode. These satisfactory soft-switching characteristics guarantee a high efficiency of the system. The system losses are further reduced by adopting a small phase angle and GaN FETs according to the thorough analysis of switch losses. At the same time, based on the planar magnetics, the system profile is reduced and the system power density is improved. The RSM and MLM provide clearer and more effective ways to design the planar inductor and transformer. The 1 MHz prototype validates the feasibility of the proposed converter and design methods. The system efficiency is 88.7% in the rated 25 W output power condition.

APPENDIX

The circuit during the turn-off transition is shown in Fig. A1, where R_{Goff} is the gate resistance and L_{SI} is the source inductance.

During the calculation procedure, some simplifying assumptions are made as follows:

1) the voltage induced across the source inductance can be regarded as a voltage source in phase with the gate voltage;
2) the external drain current I_D is constant during the transition;

Based on KVL, the voltage relationship in the gate circuit can be obtained as follows:

$$V_{GS} = V_{RG\mathrm{off}} + V_{\mathrm{LSI}}. \tag{A1}$$

Substituting drain current I_D into (A1), the following equation can be obtained:

$$V_{GS} = I_G \cdot R_{G\mathrm{off}} + \frac{L_{SI} \cdot I_D}{t_{\mathrm{off\_2}}}. \tag{A2}$$

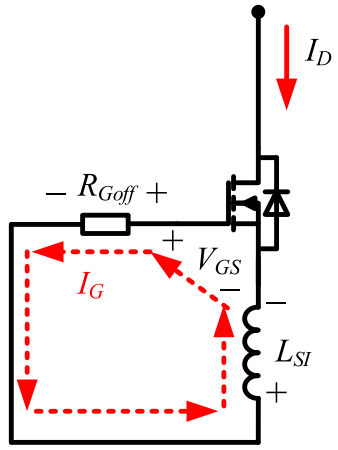

Fig. A1. Equivalent circuit during turn-off transition.

The driving current is given by (A3), where g_m is the transconductance of the transistor

$$I_G = \frac{Q_{GS2}}{t_{\mathrm{off\_2}}} = \frac{C_{GS} \cdot I_D}{t_{\mathrm{off\_2}} \cdot g_m}. \tag{A3}$$

Based on (A2) and (A3), it can be calculated that

$$t_{\mathrm{off\_2}} = \frac{I_D}{V_{GS}} \frac{C_{GS}}{g_m} \left(\frac{L_{SI} \cdot g_m}{C_{GS}} + R_{G\mathrm{off}} \right). \tag{A4}$$

It means the effect of the source inductance can be seen as an extra gate resistance, so the equivalent source inductance resistance (R_{SI}) can be represented as

$$R_{SI} = \frac{L_{SI} \cdot g_m}{C_{GS}}. \tag{A5}$$

For example, 10 pH of source inductance in EPC2010 circuit with C_{GS} of 400 pF, and $g_m = 60$ S results in 1.5 Ω equivalent resistance. Thus, the equivalent resistance R_{SI} is added into the approximate losses formula (13).

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